

NC State University
Department of Electrical and Computer Engineering
ECE 463/563 (Prof. Rotenberg)
Project #3: Dynamic Instruction Scheduling
REPORT TEMPLATE (Version 1.0)

by

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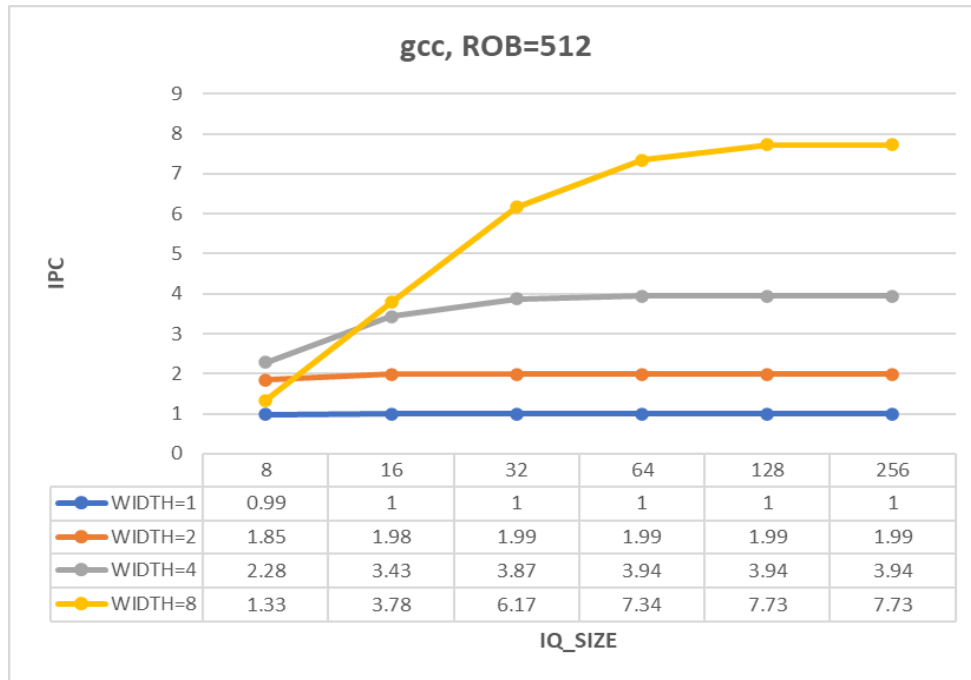
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Student's electronic signature: GAGANA SINDHU SABBAVARAPU
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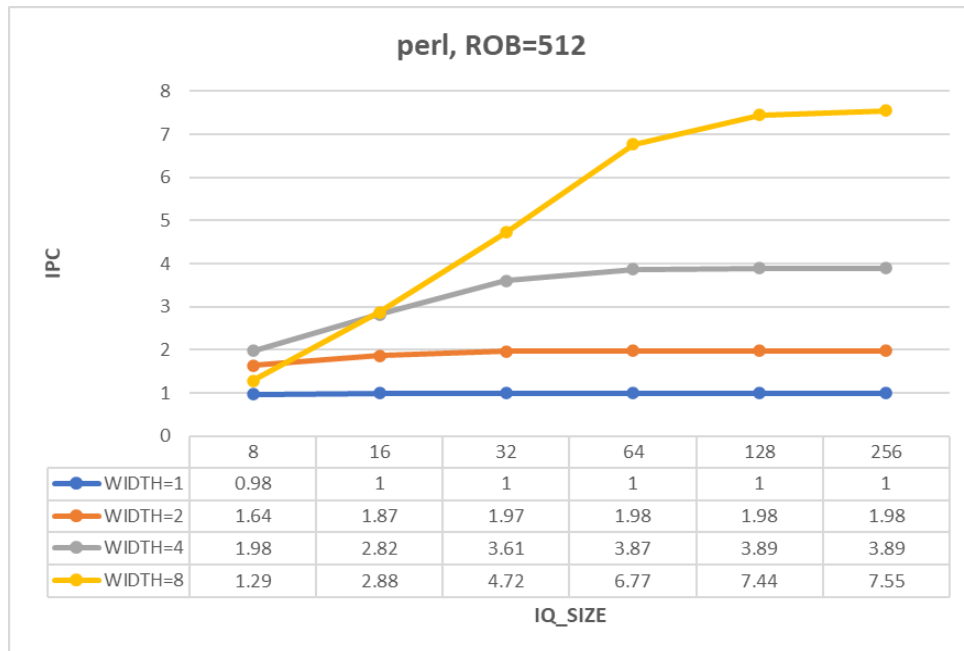
Course number: 563

A. Large ROB, effect of IQ_SIZE

GRAPH “gcc, ROB=512”



GRAPH “perl, ROB=512”



1. Graph Analysis:

	“Optimized IQ_SIZE per WIDTH” Minimum IQ_SIZE that still achieves within 5% of the IPC of the largest IQ_SIZE	
	gcc	perl
WIDTH = 1	8	8
WIDTH = 2	16	32
WIDTH = 4	32	64
WIDTH = 8	128	128

2. Discussion:

- The goal of a superscalar processor is to achieve an IPC that is close to WIDTH, which is the peak theoretical IPC of the processor. As we increase WIDTH, we observe that a **larger** IQ is needed to achieve this goal. This is because, with greater WIDTH, the IQ needs to look **farther** in the dynamic instruction stream to find **more** independent instructions that can issue in parallel to WIDTH execution lanes, each cycle.
- For WIDTH=8, perl’s “optimized IQ_SIZE” is **equal to** gcc’s “optimized IQ_SIZE”.

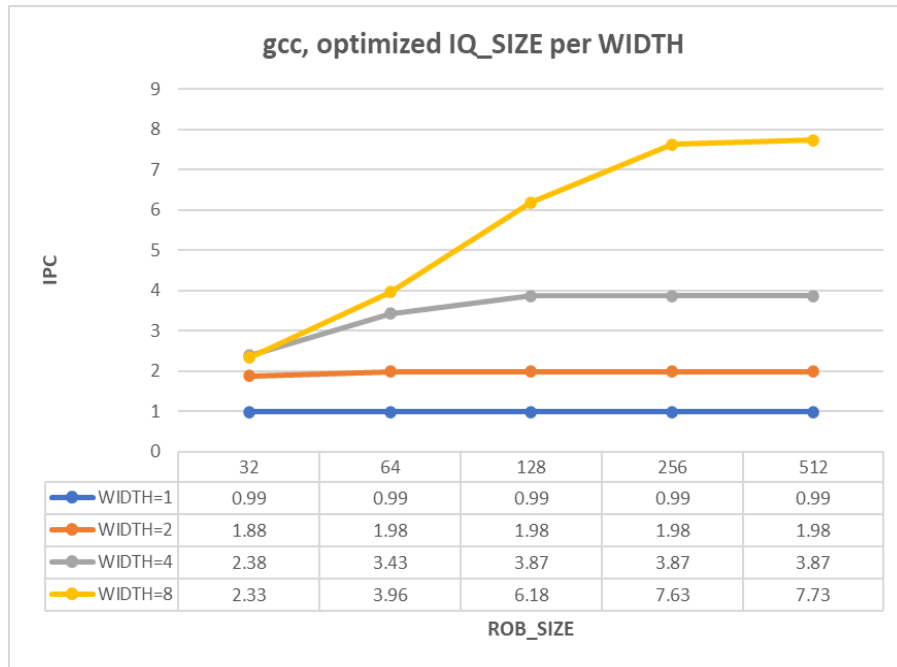
Why might this be the case?

- a. Perhaps perl has **a similar number of** data-dependent instructions within a fixed window of instructions, such that it **may look the same distance** in the dynamic instruction stream to get the same number of independent instructions as gcc.
- b. Perhaps perl has **a similar number of** long-latency instructions within a fixed window of instructions as compared to gcc.
- c. All of the above: both a and b are plausible explanations.

Answer: **<c>**

B. Effect of ROB_SIZE

GRAPH “gcc, optimized IQ_SIZE per WIDTH”



GRAPH “perl, optimized IQ_SIZE per WIDTH”

