```
; 32bitAdder.asm
; Created: 29/08/2017 08:59:21 p.m.
; Author : Gabriel Aguilar Lemus
.org 0
            XH, 0x01
    ldi
            XL, 0x04
    ldi
            YH, 0x01
    ldi
    ldi
            YL, 0x08
    ldi
            ZH, 0x01
    ldi
            ZL, 0x0c
    ldi
            r18, 4
ciclo_suma:
    1d
            r16, -X
    1d
            r17, -Y
    add
            r16, r17
    st
            -Z, r16
    brcs
            hay_carry
cont:
    dec
            r18
    breq
            fin
            ciclo_suma
    rjmp
hay_carry:
    dec
            XL
    1d
            r16, X
    inc
            r16
            X, r16
    st
            \mathsf{XL}
    inc
    rjmp cont
fin:
    nop
    rjmp
            fin
```