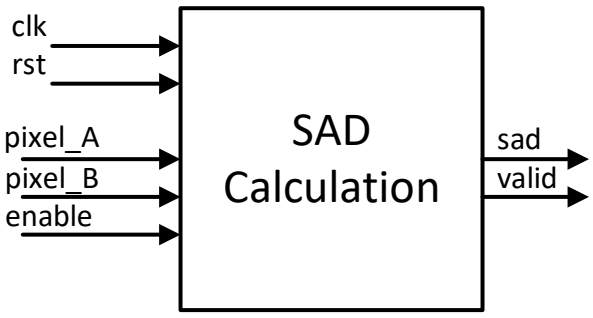
SAD Calculation Between Two Images

The Sum of Absolute Differences (SAD) may be used for a variety of purposes, such as object recognition, the generation of disparity maps for stereo images, and motion estimation for video compression. It is defined as the sum of the absolute difference between two monochromatic images, pixels by pixels. It is required to design a digital circuit for implementing such operation for images of NxN 8-bit pixels (N is a VHDL generic and is a power of 2 for simplicity). The interface of the circuit to be designed is as follows:



Pixels are provided externally, one per cycle for each image. The output must be wide enough to represent the information correctly. The output valid signal must be set when all the images have been processed (it depends on N). If *enable* = 0, the circuit keeps its state regardless of the value of the input signals.

You are requested to deal with the various possible error situations, documenting the choices made. In particular, it is necessary to take into consideration:

- Possible overflows during calculation
- Elaboration of more than one couple of images (more than NxN pixels)

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions