CS2074 : Computer Organization Laboratory

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Dataflow Modeling

- Dataflow modeling style is mainly used to describe combinational circuits.
- The basic mechanism used is the continuous assignment.
- In a continuous assignment, a value is assigned to a data type called net.
- The syntax of a continuous assignment is

  assign [delay] LHS_net = RHS_expression;

- LHS_net is a destination net of one or more bit, and RHS_expression is an expression consisting of various operators.
- The statement is evaluated at any time any of the source operand value changes and the result is assigned to the destination net after the delay unit.
- Dataflow modeling describes the design in terms of expressions instead of primitive gates. *expressions, operators, and operands* form the basis of dataflow modeling

Examples

```
// perform and function on in1 and in2 and assign the result to out1
    assign out1 = in1 & in2;

// perform not function on in1 and assign the result to out2
    assign out2 = not in1;

// perform the desired function and assign the result after 2 units
    assign #2 z[0] = ~(ABAR & BBAR & EN);

wire COUNT, CIN;            // scalar net declaration
wire [3:0] SUM, A, B;       // vector nets declaration
// A and B vectors are added with CIN and the result is assigned to a
concatenated vector of a scalar and vector nets
```

- assign {COUNT,SUM} = A + B + CIN;

Implicit Continuous Assignment

Regular continuous assignmnet

Same effect is achieved by an implicit continuous assignment

Example

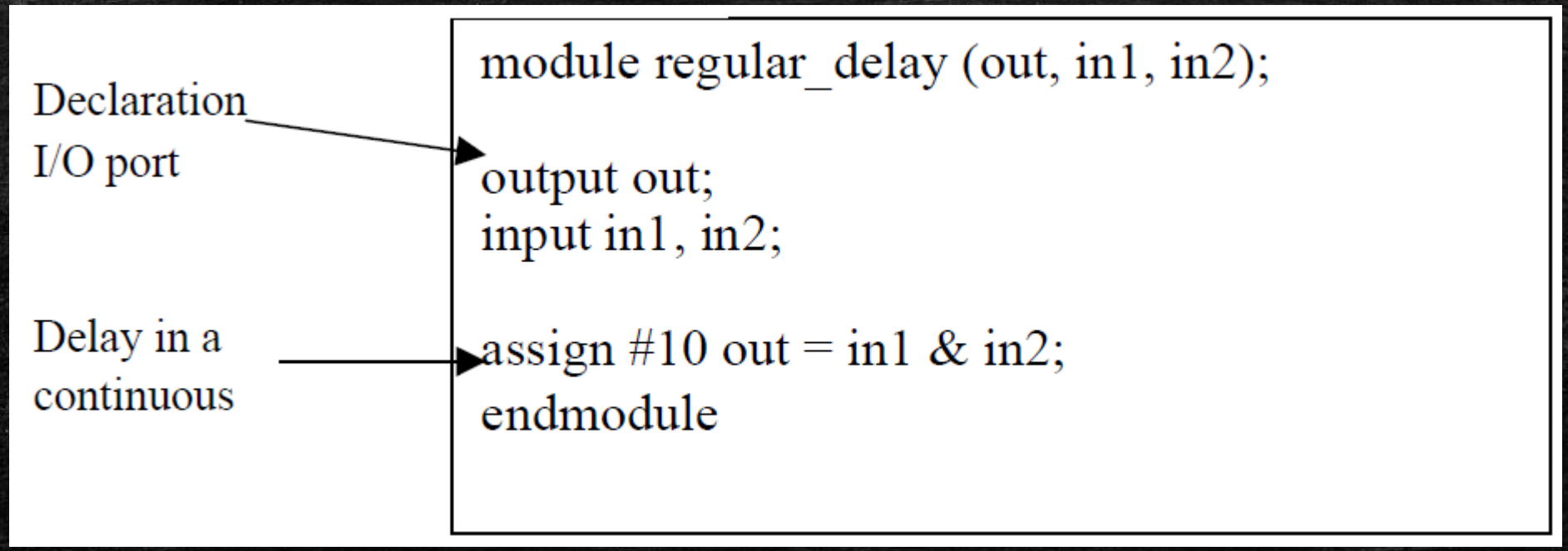
```
wire out ;
assign   out = in1 & in2 ;

wire     out = in1 & in2 ;
```

Delays

- Delay value control the time between the change in a right-hand-side operand and when the new value is assigned to the left-hand-side.

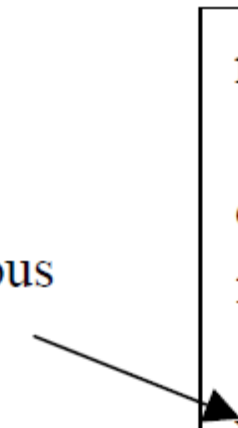
1. Regular Assignment Delays

- The delay value is specified after the keyword assign..



2. Implicit Continuous Assignment Delay

Delay in a continuous assign



```
module implicit_delay (out, in1, in2);

output out;
input in1, in2;

wire #10 out = in1 & in2;

endmodule
```

3. Net Declaration Delay

- A delay can be specified on a net when it is declared without putting a continuous assignment on the net.
- If a delay is specified on a net out, then any value change applied to the net out is delayed accordingly.

No delay in a continuous assignment

```
module net_declare (out, in1, in2);

output out;
input in1, in2;

assign out = in1 & in2;

endmodule
```

Test Stimulus Code

Declare the delay on the net.

Input test value

Show the result

Call net_declare module

```
module stimulus;

wire #10 OUT;
reg IN1, IN2;

initial
begin
    IN1 = 0; IN2= 0;
    #20 IN1=1; IN2= 1;
    #40 IN1 = 0;
    #40 IN1 = 1;
    #5 IN1 = 0;
    #150 $stop;
end

initial
    $monitor("out", OUT, "in1", IN1, "in2",
IN2);

net_declare rd1(OUT, IN1, IN2);

endmodule
```

Thank You.