National Institute of Technology, Rourkela

CS2074: Computer Organization Laboratory

SPRING 2021-2022

Assignment 1: Gate Level Design: Logic Gates and Circuits

Due: February 05, 2022, 09:00 a.m.

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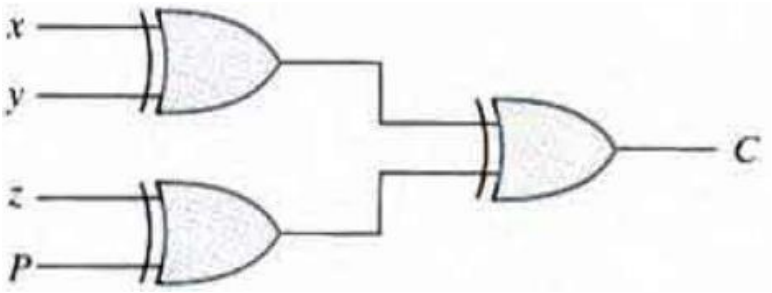
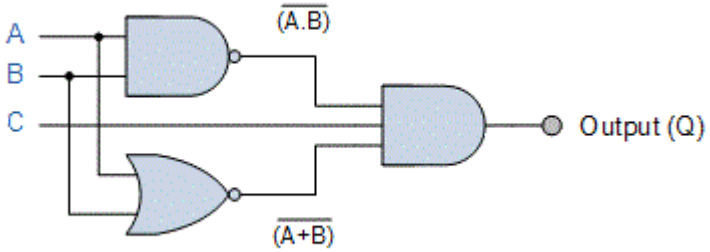
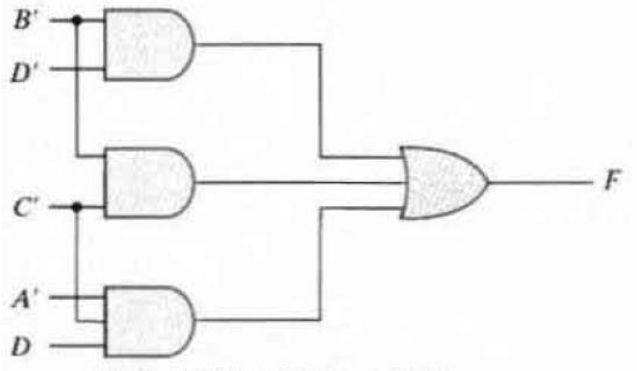
1. Realize the following circuit and generate truth table using Verilog.



2. Realize the following circuit and generate truth table using Verilog.

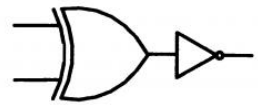


3. Realize the following circuit and generate truth table using Verilog.

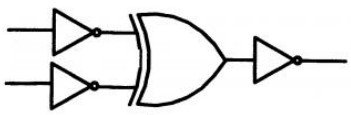


4. Realize the following circuit and generate truth table using Verilog.

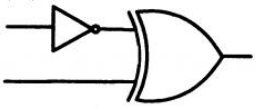
(A)



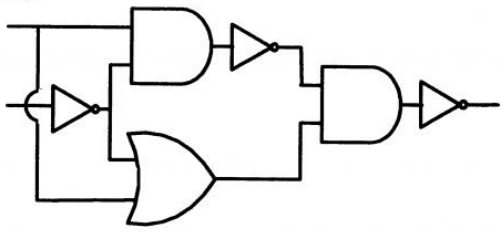
(B)



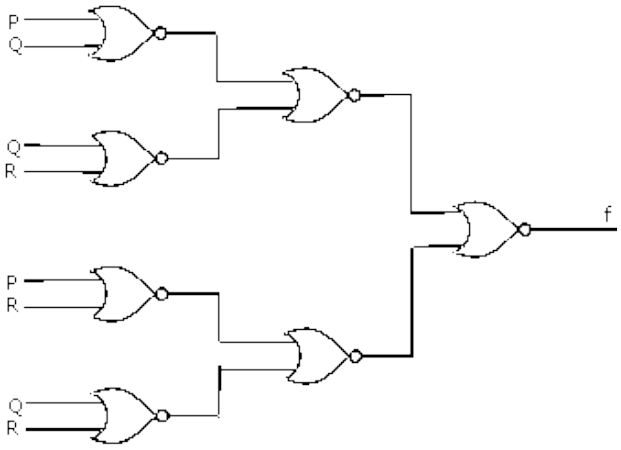
(C)



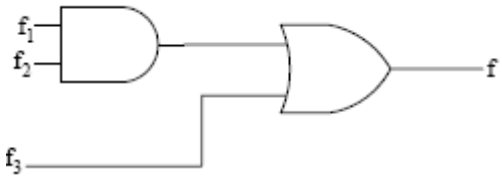
(D)



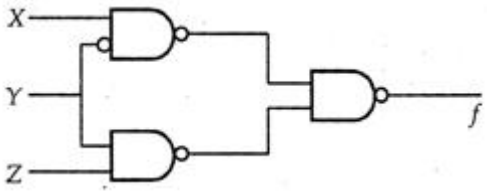
5. Realize the following circuit and generate truth table using Verilog.



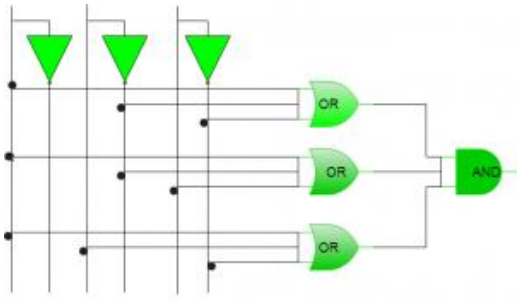
6. Realize the following circuit and generate truth table using Verilog.



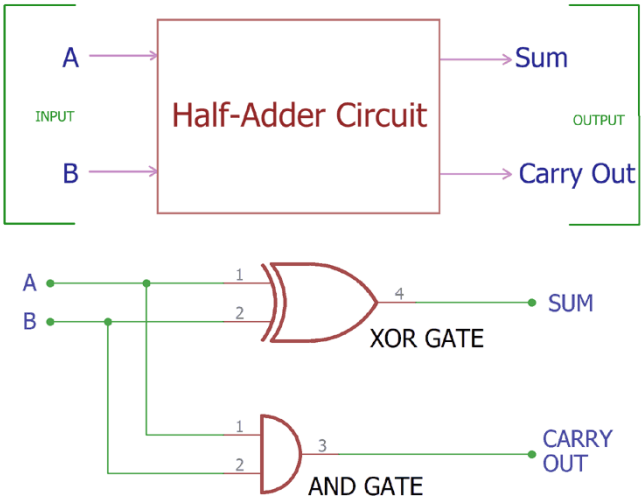
7. Realize the following circuit and generate truth table using Verilog.



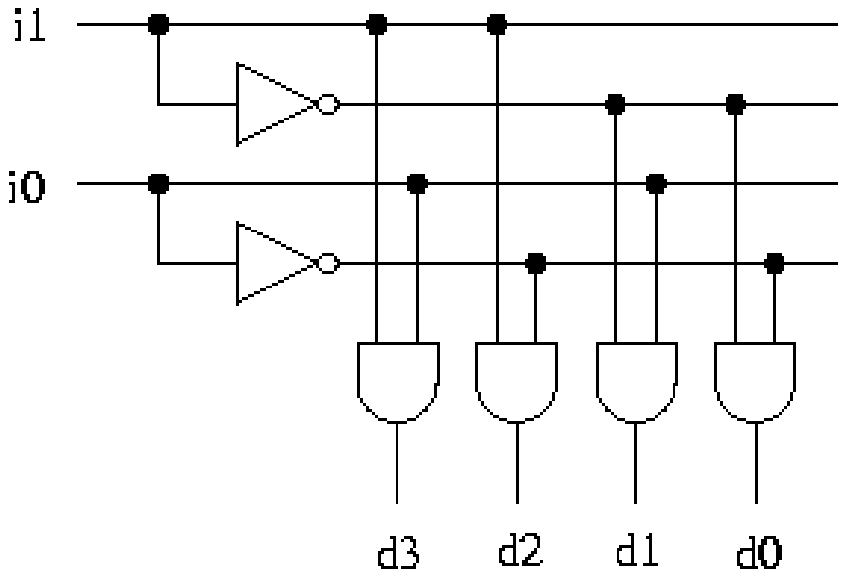
8. Realize the following circuit and generate truth table using Verilog.



9. Design a 2-bit Half adder shown in figure and test it by giving proper input using Verilog.



10. Design a 2 to 4 binary line decoder shown in figure and test it by giving proper input using Verilog.



11. Design a 4:1 Channel Multiplexer and test it by giving proper input using Verilog.