National Institute of Technology, Rourkela

CS2074: Computer Organization Laboratory

SPRING 2021-2022

Assignment 3: Gate Level Design: Logic Gates and Circuits

Due: February 11, 2022, 03:30 p.m.

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1. Design a 1-bit Full adder as discussed in COA theory class which generates carry and pro-gate logic.

2. Design 4 bit CLA adder (Carry Look-Ahead Adder) using 1-bit Full adder developed in Question 1.