National Institute of Technology, Rourkela

CS2074: Computer Organization Laboratory

SPRING 2021-2022

Assignment 5: Behavioural Modelling

Due: March 10, 2022, 23:59 hours

---

1. Use a behavioural model to design a 1-bit 4-to-1 mux using the if-else-if statement. Develop a test bench to verify the design.

2. Design a gray code generator using the case statement. The design will take a 4-bit BCD input and will output the corresponding gray code value, provided that the enable input on is TRUE. If the enable input is FALSE or the input is not BCD, then display error message.

3. Using behavioural data modelling implement Booth's algorithm.

4. Design a following Flip – Flops using behavioural modelling:
    a. R-S
    b. J-K
    c. T
    d. D
    e. Master-slave

5. Design 4-bit Parallel-In and Parallel-Out (PIPO) Shift Register using behavioural modelling.

6. Design synchronous counter with help of J-K Flip Flop using behavioural modelling.

7. Design a counter which counts in the sequence mentioned below. The counter should use behavioural modelling and a case statement. Develop a test bench to test it. The test bench should display the counter output in the simulator console output. Also provide waveform output for the same. Simulate using the clock period of 10 units for 200 ns. 000, 001, 011, 101, 111, 010, (repeat 000). The counter will have an enable signal, a reset signal, and a clock signal.