National Institute of Technology, Rourkela

CS2074: Computer Organization Laboratory

SPRING 2021-2022

Assignment 4: Dataflow Modelling

Due: March 03, 2022, 23:59 hours

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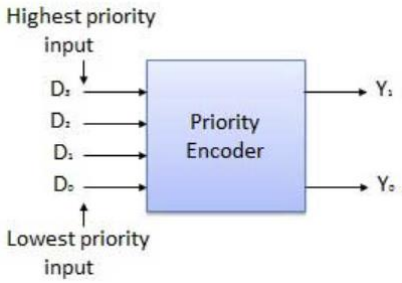
1. Design 4 bit CLA adder (Carry Look-Ahead Adder) using 1-bit Full adder. (Use Dataflow Modelling).
2. Design 4 bit CLA adder using High-order logic covered in theory class. (Use Dataflow Modelling).
3. Design a 3- bit Full Subtractor using Dataflow Modelling.
4. Design a priority encoder where priority is given to the input lines. If two or more input line are 1 at the same time, then the input line with highest priority will be considered. There are four input D0, D1, D2, D3 and two output Y0, Y1. Out of the four input D3 has the highest priority and D0 has the lowest priority. That means if D3 = 1 then Y1 Y1 = 11 irrespective of the other inputs. Similarly, if D3 = 0 and D2 = 1 then Y1 Y0 = 10 irrespective of the other inputs. (Use Dataflow Modelling).



5. Design a 2 to 4 binary line decoder using Dataflow Modelling.
6. Design a 4:1 Channel Multiplexer using Dataflow Modelling.
7. The truth table for the output Y in terms of 3 inputs A, B and C are given below. Realize the circuit and simulated using Verilog using dataflow modelling.

A	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1
Y	1	1	1	0	1	0	0	0