National Institute of Technology, Rourkela

CS2074: Computer Organization Laboratory

SPRING 2021-2022

Assignment 2: Gate Level Design: Logic Gates and Circuits

Due: February 04, 2022, 04:00 p.m.

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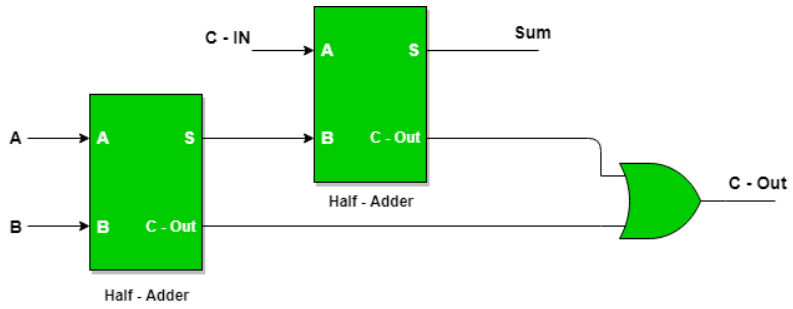
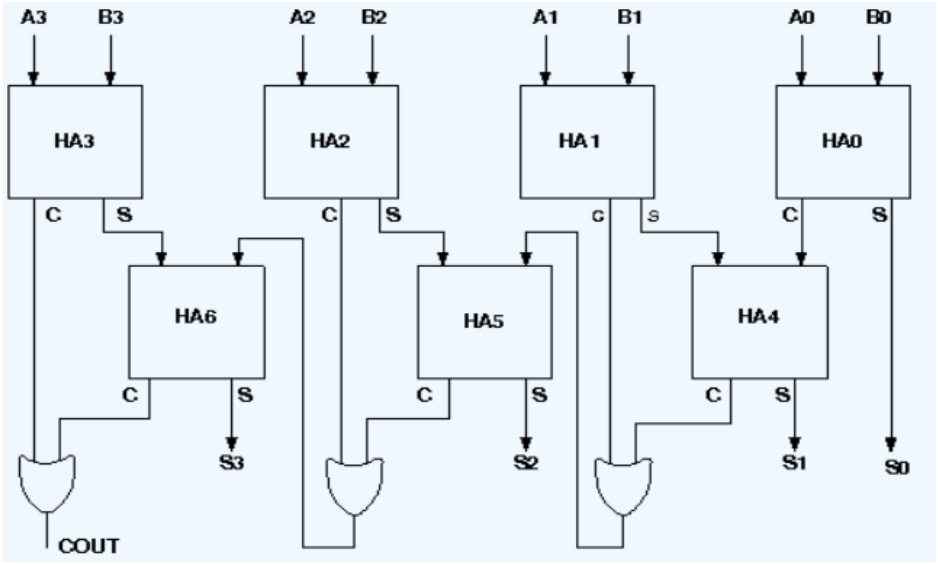
1. Design a Full adder shown in figure and test it by giving proper input using Verilog, **(use code reusability)**.



2. Sumanto was trying to design a circuit while reading lecture notes of COA subject. He came up with the circuit shown in the figure below. However, he could not figure it out what circuit he had created. He sought help from Saketh. Even though Saketh knows the answer, he didn't tell anything to Sumanto.



I. Help Sumanto by identifying the circuit.

II. Design the identified circuit and test with proper input using Verilog. **(use code reusability)**

3. Design 4:1 multiplexer using minimum number of 2:1 multiplexer and test with proper input using Verilog. **(use code reusability)**