PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

STARS – Digital logic – System Verilog

Project 7: 16-bit Carry Look Ahead Adder

Design 16-bit carry look ahead adder using System Verilog. What is a carry look ahead adder? Recall that a ripple adder is a series of full adder blocks where each full adder block (bit) is dependent on the carry bit from the previous full adder block (bit). Therefore, the results must be calculated bit by bit in series and the time to complete the full addition depends not only on the speed of the circuits, but the number of bits in the largest of the two operands. The carry look ahead adder gets around this limitation by adding combinational logic to calculate the carry for each bit all at the same time based on only the first carry-in bit and the values of the operands. The result is the fastest adder circuit at the cost of much more combinational logic.

Here is a website that gives a good overview of how this circuit works.
https://technobyte.org/carry-look-ahead-adder-working-circuit-truth-table/

So, you are to design a 16-bit carry look ahead adder and implement in System Verilog so that you can simulate and run on the FPGA boards. As in Project 6, create successive iterations of static values in the top module instantiation and then display your results on the 7-segment displays. You may display your results in decimal using BCD or by displaying the hexadecimal result values as 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.

Test it thoroughly to make sure it always indicates the correct sum.