PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

STARS – Introduction to System Verilog

Digital Logic Project 4
Design a Sensor Error Detector with the following specifications:

The Sensor Detector that you are designing monitors four (4) sensors and reports the existence of an error condition when at least two (2) independent low priority sensor events occur simultaneously or there is an event from the high priority sensor. However, the sensors on the third (3rd) and fourth (4th) inputs are a paired set and the triggering of either one or both only counts as one distinct low priority sensor event. The high priority sensor is attached to the first (1st) input and a low priority sensor is attached to the second (2nd) input.

A sensor error detector like this might be used in a manufacturing process to detect when a significant enough error occurs that requires the production line to halt. Sensor events correspond to a logic '1' and a logic '0' corresponds to no event from that sensor. Consider two examples (MSB to LSB where input 1 is the LSB): "1100" indicates that both redundant sensors have had events while the other two haven't and thus the output should be a logic '0'. However, "0001" indicates that the high priority sensor had an event and thus the output should be a logic '1'.

Write system Verilog code for your circuit using behavioral and structural modelling and use the keypad buttons as inputs and display both the inputs and output on the LEDs.