PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

STARS – Digital logic – System Verilog

Project 9: Electronic Combinational Locks

In this project you will be building some electronic combinational locks by expanding on the pattern detectors from Experiment 8.

Task 1:

A. Design an electronic combinational lock with digits 0 and 1 so that it unlocks every time the input is 101011. In addition to the binary combination input, the lock will have a reset button (input).

B. Before you start coding in System Verilog you must draw a state diagram and any necessary next state combinational logic and then show and explain your design to a TA.

C. Implement your design in System Verilog and then simulate. Use different input streams to ensure that it works properly.

Task 2:

A. Redesign Task 1 so that instead of a 6-digit binary combination, the electronic lock uses a 3-digit decimal combination. The inputs will be a string of natural BCD digits. Ensure that you do not have any unreachable or undefined states.

B. Before you start coding in System Verilog you must draw a state diagram and any necessary next state combinational logic and then show and explain your design to a TA.

C. Implement your design in System Verilog and then simulate. Use different input streams to ensure that it works properly.

Task 3:

A. Redesign Task 1 to allow the user to set and save their own combination. The user will need to input the current combination first, and then (with an additional input) be allowed to enter and save their own 6-digit binary combination.

B. Before you start coding in System Verilog you must draw a state diagram and any necessary next state combinational logic and then show and explain your design to a TA.

C. Implement your design in System Verilog and then simulate. Use different input streams to ensure that it works properly.