PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

STARS – Digital logic – System Verilog

Project 8: Clock Frequency Divider

In this project you will be building clock frequency divider circuits. In Lesson 6 we discussed using flip-flops as clock frequency dividers where with simple flip-flops you can divide by powers of two.

Task 1:

A. Design a clock divider circuit that divides the 100 Hz FPGA clock by 8. Blink an LED at your output frequency.

B. Before you start coding in System Verilog you must draw a state diagram and any necessary next state combinational logic and then show and explain your design to a TA.

C. Implement your design in System Verilog and then simulate.

D. Verify on the actual FPGA board and measure the output frequency.

Task 2:

Repeat Task 1 but divide the clock frequency by 10. You will need additional next state logic to accomplish this.

Task 2:

Repeat Task 1 but divide the clock frequency by 25. You will need additional next state logic to accomplish this.