PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

STARS – Digital logic – System Verilog

Project 5: 4-bit ALU

Design a 4-bit ALU with the following specifications:

Signal	Bit length	Port	Description
En	1-bit	input	Enable signal. The circuit works when En=1
Ctrl	3-bit	input	Control signal operation – see operation table
C_{in}	1-bit	input	Carry in
A	4-bit	input	4-bit - operand 1
B	4-bit	input	4-bit - operand 2
M	4-bit	output	4-bit output result
S	1-bit	output	Sign bit
O	1-bit	output	Overflow bit
C_{out}	1-bit	output	Carry out

Operations:

Ctrl	Operation	Result in M
000	Addition	A + B + C_{in}
001	Subtraction	A + ~B + 1
010	Bitwise NOT A	~A
011	Bitwise AND	A & B
100	Bitwise OR	A | B
101	Bitwise XOR	A ^ B
110	Shift A left (pad 0)	A multiplied by 2*
111	Shift A right (pad 0)	A divided by 2

* move the MSB of A into C_{out}

Consider when you need to set the S (sign status) and O (overflow status) bits.