PURDUE UNIVERSITY | Elmore Family School of Electrical and Computer Engineering

STARS – Digital logic – System Verilog

Project 6: Four-Digit (16-bit) BCD Adder

Construct a four-digit (16-bit) BCD adder. The module should have two 16-bit input ports named a and b, and a single-bit input named ci (carry-in). It should have a 16-bit output port named s (sum) and a single bit output port named co (carry-out). It's rather difficult to test something like this by pressing buttons. Instead, create successive iterations of static values in the top module instantiation. For instance, you can instantiate and test this module with the following:

```
logic co;
logic [15:0] s;
bcdadd4 ba1(.a(16'h1234), .b(16'h1111), .ci(0), .co(red), .s(s));
ssdec s0(.in(s[3:0]),   .out(ss0[6:0]), .enable(1));
ssdec s1(.in(s[7:4]),   .out(ss1[6:0]), .enable(1));
ssdec s2(.in(s[11:8]),  .out(ss2[6:0]), .enable(1));
ssdec s3(.in(s[15:12]), .out(ss3[6:0]), .enable(1));
```

You should see the result 2345 on the seven-segment displays. If you change the inputs to 16'h9876 and 16'h3333, the output should show 3209, and the red LED will be illuminated to indicate carry-out. Be sure to try cases with the ci input port set to 1.

Test it thoroughly to make sure it always indicates the decimal sum.