BSc. (Hons) in Information Technology
Specialized in
Computer Systems and Network Engineering

Year 02 - Semester 01

IE2010 – Digital Electronics

Assignment

Controlled 2-Digit BCD Up-Counter with Target Stop Logic

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Introduction to BCD counters and target stop logic.

A Binary Coded Decimal (BCD) counter is a digital device that represents each decimal digit using a 4-bit binary format. It sequentially counts from 0000 (decimal 0) up to 1001 (decimal 9), then resets to 0000. By cascading two such counters, a 2-digit BCD counter can be formed, enabling counting from 00 to 99 using valid BCD representations for each digit.

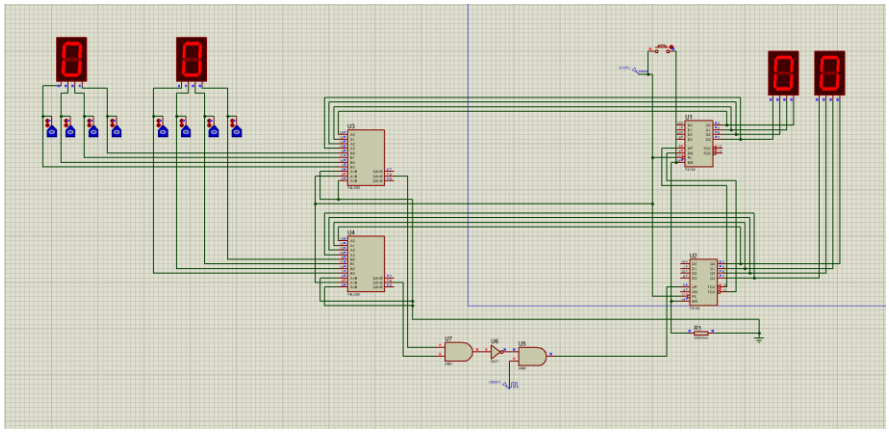
The objective of this project is to design and simulate a 2-digit BCD up-counter that automatically stops counting upon reaching a user-defined target value. This target is manually preset using toggle switches before the counter begins. As the system increments with each clock pulse, a comparator circuit continuously evaluates the counter output against the preset target.

Once the current count matches the target value, a control logic circuit disables the clock signal, thereby halting the counter. This intelligent stopping mechanism is particularly useful in applications such as digital timers, production line counters, and automation systems where reaching a specific count is critical.

The Proteus-based simulation integrates the following key components:

- A function generator to provide clock pulses.
- Two cascaded BCD counter ICs for tens and units' digits.
- Toggle switches for target value input.
- Two 4-bit comparator ICs for real-time value comparison.
- Logic gates (AND, NOT) to implement stop logic.
- A reset mechanism to restart the counting process after a stop.

Circuit Explanation and Diagrams



BCD Counter Logic (74192 ICs)

Two 74192 BCD up/down counters are cascaded to form a 2-digit counter (00 to 99).

- U1 handles the units digit.
- U2 increments by 1 whenever U1 overflows from 9 to 0, representing the tens digit.
- Both outputs are sent to 7-segment displays through BCD-to-7SEG converters for visualization.

Target Value Input

- Logic switches (Logic State) are used to input a 2-digit BCD target value.
- Left group (4 switches) sets the tens digit.
- Right group sets the units digit.
- These BCD values are continuously compared with the current count.

Comparator Circuit (74LS85)

- Two 74LS85 magnitude comparators compare the current counter value with the target.
- The first comparator checks the units digit, and the second checks the tens digit.
- Both comparators must assert equality for a complete match.

Stop Logic and Clock Control

- The equality outputs from both comparators are fed into an AND gate.
- If both are high (A=B), the output of the AND gate disables the clock signal.
- This halts further counting, effectively stopping the system at the desired value.

Reset and Enable

- A push-button reset is used to restart the counter.
- Clock pulses are generated using a function generator or simulated clock (ADC1031 in Proteus).

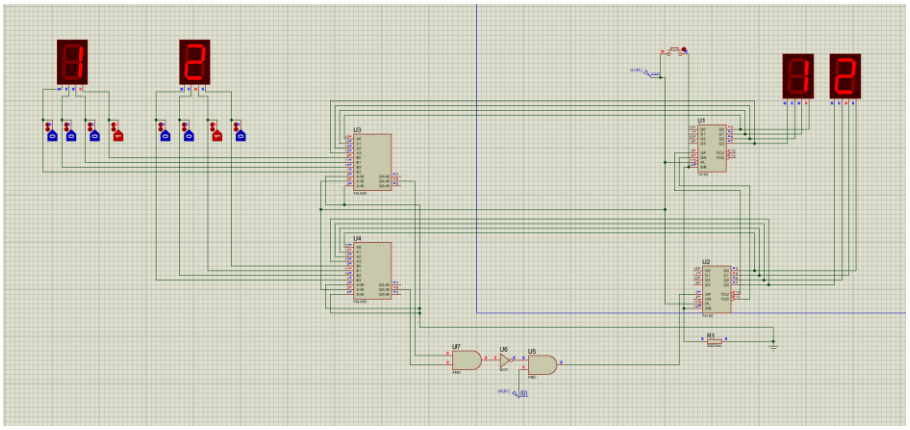
Test Results and Screenshots

Test 1

Target Value : 12

Stopped At : 12

Status : Success

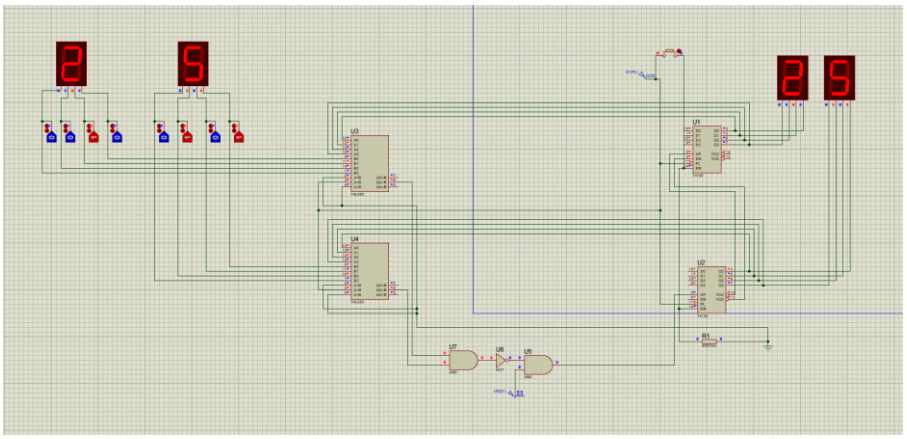


Test 2

Target Value : 25

Stopped At : 25

Status : Success

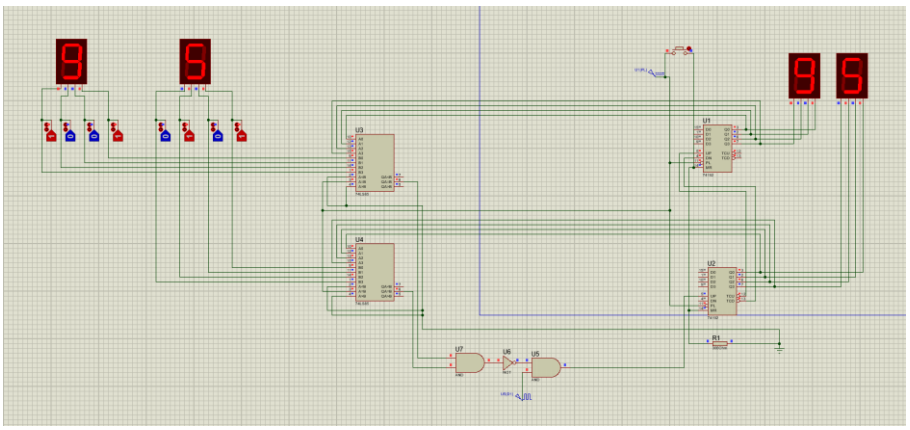


Test 3

Target Value : 95

Stopped At : 95

Status : Success



Observations and Possible Enhancements

Observations

- The circuit operates reliably in the Proteus simulator, accurately counting from 00 upward using two cascaded 74192 BCD counters.
- The target value, set using two sets of logic state switches, is correctly read and passed into the comparator inputs.
- The comparator logic using 74LS85 ICs successfully detects when the current count equals the target BCD value.
- Upon reaching the target, the AND-NOT gate control logic effectively disables the clock signal, halting the counter exactly at the desired value.
- The counter halts precisely and consistently, confirming the reliability and timing accuracy of the logic design.
- The reset mechanism, triggered by a push button, works properly and resets both counters to 00.
- The 7-segment displays provide clear, real-time visual output of the current count, updating accurately with each clock pulse.

Possible Enhancements

- Add buzzer or LED alert:
  Trigger a visual or audio indicator when the target value is reached to notify the user immediately.
- Display the target value:
  Include a second pair of 7-segment displays to show the preset target value alongside the live counter output.
- Integrate a 4×4 keypad:
  Replace toggle switches with a keypad for more user-friendly and precise target value input.
- Add pause/resume functionality:
  Introduce a pause button to temporarily halt the counter without resetting the entire system.
- Auto-reset with delay:
  Use a timer circuit to automatically reset the system a few seconds after reaching the target for cyclic or repeated operations.

Challenges faced and how they were resolved

Comparator Didn't Stop the Counter

The counter reached the target value, but the system didn't stop as expected.

Solution - I carefully rechecked the wiring and ensured that the counter outputs and target inputs were correctly mapped to the corresponding 74LS85 comparator inputs. After fixing the connections, the comparator successfully detected the match, and the stop logic worked.

Reset Button Didn't Work Properly

Pressing the reset button didn't reset the counter to 00.

Solution - I connected the CLR pins of both counters to a single reset button. After this correction, pressing the button successfully reset both counters to 00.

Incorrect Output on 7-Segment Displays

The 7-segment displays showed incorrect numbers, even though the counter outputs were accurate

Solution - I reviewed and corrected the connections between the BCD counter outputs and the 7SEG-BCD decoder. After fixing this, the display correctly showed the real-time counting values.

Conclusion

This project successfully demonstrated the design and simulation of a 2-digit BCD up-counter with an automatic stop mechanism. By using two cascaded 74192 counters and 74LS85 comparator ICs, the system accurately counted from 00 up to a user-defined target and halted as expected. The implementation of control logic using basic gates ensured proper clock disabling upon reaching the target value.

Through this task, I gained valuable experience in combining sequential and combinational digital circuits. The ability to simulate and test various target values in Proteus also enhanced my understanding of circuit behavior and timing. Overall, the project helped reinforce key digital electronics concepts such as BCD encoding, comparator-based logic, and system control using discrete components.

The system design is reliable and can be expanded in future applications like digital timers, counters, and industrial automation systems that require precision and conditional stopping.