

Design Rules Verification Report

Filename : C:\Users\Maxime\OneDrive - Université Laval\Github\design3\Électronique\Laser Power Meter\4 Layers Motherboard.PcbD
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Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.2mm) (Max=0.5mm) (Preferred=0.3mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.13mm) (All)	0
Hole Size Constraint (Min=0.15mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.5mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.05mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.05mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.15mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (Disabled)(InNet('DGND'))	0
Length Constraint (Min=0mm) (Max=2540mm) (All)	0
Matched Lengths(Tolerance=25.4mm) (InDifferentialPair('D'))	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	0