UDP/IP Integration HDL Testbench Instructions

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Dependencies

1. Xilinx Vivado v2016.4
2. File comparison tool (diff, cmp, fc, WinDiff, etc.)
3. `integration_tester.xpr.zip`

For the duration of this document, let the path `integration_tester/integration_tester.sim` equal `SIM`.

Test Inputs

Filename	Description	Test
`SIM/rx/behav/rx_integration_test.txt`	Simple tests for functionality	24
`SIM/rx/behav/rx_integration_test.out.chk.txt`	Expected output for the above test inputs	24
`SIM/rx/behav/rx_throughput_test.txt`	Larger packets (near 1500 bytes) to demonstrate throughput	24, 26
`SIM/rx/behav/rx_throughput_test.out.chk.txt`	Expected output for the above test inputs	24, 26
`SIM/rx/synth/timing/rx_integration_test.txt`	Simple tests for functionality	24
`SIM/rx/synth/timing/rx_integration_test.out.chk.txt`	Expected output for the above test inputs	24
`SIM/rx/synth/timing/rx_throughput_test.txt`	Larger packets (near 1500 bytes) to demonstrate throughput	24, 26
`SIM/rx/synth/timing/rx_throughput_test.out.chk.txt`	Expected output for the above test inputs	24, 26
`SIM/tx/behav/tx_integration_test.txt`	Simple tests for functionality	25
`SIM/tx/behav/tx_integration_test.out.chk.txt`	Expected output for the above test inputs	25
`SIM/tx/behav/tx_throughput_test.txt`	Larger packets (near 1500 bytes) to demonstrate throughput	25, 27
`SIM/tx/behav/tx_throughput_test.out.chk.txt`	Expected output for the above test inputs	25, 27
`SIM/tx/synth/timing/tx_integration_test.txt`	Simple tests for functionality	25
`SIM/tx/synth/timing/tx_integration_test.out.chk.txt`	Expected output for the above test inputs	25
`SIM/tx/synth/timing/tx_throughput_test.txt`	Larger packets (near 1500 bytes) to demonstrate throughput	25, 27
`SIM/tx/synth/timing/tx_throughput_test.out.chk.txt`	Expected output for the above test inputs	25, 27

Test Outputs

Filename	Description	Test
SIM/rx/behav/rx_integration_test.out.txt	Behavioral simulation output data in hex, in ascending order	24
SIM/rx/behav/rx_throughput_test.out.txt	Behavioral simulation output data in hex, in ascending order	24, 26
SIM/rx/synth/timing/rx_integration_test.out.txt	Post-synthesis timing simulation output data in hex, in ascending order	24
SIM/rx/synth/timing/rx_throughput_test.out.txt	Post-synthesis timing simulation output data in hex, in ascending order	24, 26
SIM/tx/behav/tx_integration_test.out.txt	Behavioral simulation output data in hex, in ascending order	25
SIM/tx/behav/tx_throughput_test.out.txt	Behavioral simulation output data in hex, in ascending order	25, 27
SIM/tx/synth/timing/tx_integration_test.out.txt	Post-synthesis timing simulation output data in hex, in ascending order	25
SIM/tx/synth/timing/tx_throughput_test.out.txt	Post-synthesis timing simulation output data in hex, in ascending order	25, 27

Procedure

1. Extract `integration_tester.xpr.zip`.
2. Open `integration_tester/integration_tester.xpr` in Vivado.
3. Receiver integration tests
   (a) In the `Sources` pane, right-click `Simulation Sources > tx` and select `Make Active`, if it is not grayed out.
   (b) Under `Simulation` in the `Flow Navigator`, click `Run Simulation > Run Behavioral Simulation`.
   (c) Run the file comparison tool on the outputs against the known good outputs, ignoring whitespace changes, for example:
   ```
   cd SIM/rx/behav
   diff -w rx_integration_test.out.chk.txt rx_integration_test.out.txt
   diff -w rx_throughput_test.out.chk.txt rx_throughput_test.out.txt
   ```
   There should be no differences, aside from whitespace.
   (d) Under `Simulation` in the `Flow Navigator`, click `Run Simulation > Run Post-Synthesis Timing Simulation`. There may be a warning about a blackbox, but it does not affect the simulation.
   (e) Run the file comparison tool again, ignoring whitespace changes, for example:
   ```
   cd SIM/rx/synth/timing
   diff -w rx_integration_test.out.chk.txt rx_integration_test.out.txt
   diff -w rx_throughput_test.out.chk.txt rx_throughput_test.out.txt
   ```
   There should be no differences, aside from whitespace.
4. Transmitter integration tests
   (a) In the `Sources` pane, right-click `Simulation Sources > tx` and select `Make Active`.
   (b) Under `Simulation` in the `Flow Navigator`, click `Run Simulation > Run Behavioral Simulation`.

(c) Run the file comparison tool on the outputs against the known good outputs, ignoring whitespace changes, for example:
`cd SIM/tx/behav`
`diff -w tx_integration_test.out.chk.txt tx_integration_test.out.txt`
`diff -w tx_throughput_test.out.chk.txt tx_throughput_test.out.txt`
There should be no differences, aside from whitespace.

(d) Under `Simulation` in the `Flow Navigator`, click `Run Simulation > Run Post-Synthesis Timing Simulation`.

(e) Run the file comparison tool again, ignoring whitespace changes, for example:
`cd SIM/tx/synth/timing`
`diff -w tx_integration_test.out.chk.txt tx_integration_test.out.txt`
`diff -w tx_throughput_test.out.chk.txt tx_throughput_test.out.txt`
There should be no differences, aside from whitespace.

Notes

- Large blocks of zeroes in the test input data are to create delays between input data. This is a workaround for a lack of pushback in certain modules.

A External Software Links

- Xilinx Vivado Design Suite
- Cygwin (can provide tools like `diff` and `cmp`)