



MIDDLE EAST TECHNICAL UNIVERSITY

## **EE464 - Static Power Conversion II Term Project**

**Implementing an Isolated DC-DC Converter  
Final Report**

**by uGAN Powertronics**

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## 1. Introduction

Isolated DC/DC converters have several benefits over non-isolated converters. The main reason for the isolation is safety. Chosen topology of Flyback converter is one of the isolated DC/DC converter topologies. In this report the term project of the EE464 course is explained in detail. The required task to complete is implementing an isolated boost converter. System requirements are given as in below table.

<b>Input Voltage Range (min,max)</b>	(12 V,18 V)
<b>Output Voltage (%3 Ripple Allowed)</b>	48 Volt
<b>Output Power</b>	48 Watt
<b>Line and Load Regulation</b>	%3

Other necessary requirements can be listed below as well.

- Closed Loop Control
- Isolated Input and Output
- Exhibition of final design on a PCB.
- Efficiency over %80

In the following pages of this report there will be explanations about the topology, design choices about the main components, snubber components, magnetic items and controller. Then there will be a loss and thermal analysis, the non-ideal simulation results, PCB design explanations and a critical subtopic in which we try to understand why we can't make it work properly. Finally this report will end with a conclusion.

## 2. Topology Selection

The chosen topology is a flyback converter in this project. Flyback Topology is chosen by considering the below specifications.

- It requires less component
- It is an isolated topology we analyzed most
- Less number of winding (Other topologies requires more than two winding)
- Tons of design guides, resources and references online about the flyback.
- Best to use in low to medium power (1W-100W)
- Simple to implement and control
- Since it has no limitations on the Duty Cycle as other topologies it has a wider range of variation of output voltage.

We attempted to achieve DCM (Discontinuous Conduction Mode) since in low power DCM can provide higher efficiency at light load conditions compared to CCM. Staying around the boundary region is the most efficient way to operate, so we tried to operate around the boundary region (mode will change when load is high).

### 3. Analytical Calculations

Flyback converter has the following gain relation.

$$V_o = \frac{D}{1-D} * \frac{N_s}{N_p} * V_{in}$$

According to the gain relation of the converter, and by inserting  $V_{in} = 12\text{ V} - 18\text{ V}$  and  $V_{out} = 48\text{ V}$  the below formulation can be obtained.

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} * \frac{N_s}{N_p} \quad \rightarrow \quad 4 \geq \frac{D}{1-D} * \frac{N_s}{N_p} \geq 2.67$$

Moreover, according to most of the guidelines and design references the duty cycle is advised to be less than or equal to 0.5. Thus, turn ratio of the transformer is

chosen as  $n = \frac{N_s}{N_p} = 4$  to achieve 48 V when input is 12V and max duty cycle is 0.5

and the switching frequency of the converter is arbitrarily designed as, personal design choice, 50 kHz.

Given turn ratio and frequency, the following parameters can be computed as follows.

$$V_{DS,max} = V_{in,max} + V_{Reflected} + V_{DS,max} * 0.3 \text{ (Safety Margin due to leakage ringing)}$$

$$0.7V_{DS,max} = 18 + (48 + 0.7) * 1/4 \text{ So } V_{DS,max} \approx 45\text{ V}$$

$$D_{max} = \frac{V_R}{V_R + V_{in,min}} = 0.505 \text{ therefore max D=0.5 can be achieved nearly.}$$

$$P_{in,max} = \frac{P_{out,max}}{\text{eff}} \text{ (assuming \%85 efficiency)} = 48/0.85 \approx 56.5\text{ W}$$

$$I_{Pri,Max} = \frac{2*P_{in,max}}{V_{in,min}*D_{max}} = \frac{2*56.5}{12*0.505} \approx 18.65\text{ A}$$

$$L_{pri,max} = \frac{V_{in,min}*D_{max}}{I_p*f_{sw}} = \frac{12*0.505}{18.65*50000} = 6.5 * 10^{-6}\text{ H} = 6.5\text{ }\mu\text{H}$$

The above  $L_{pri,max}$  is the maximum value of the mutual inductance to achieve DCM operation in all cases.

Around these frequencies and power ratings ferrite cores are advised to use with flyback converters, according to the design guidelines and papers  $B_{sat}$  values can be in the range of 0.2 - 0.34 Tesla. Again to stay in the safe region  $B_{sat}$  is selected as 0.24 T. A core with  $125\text{ mm}^2 A_e$  is found ( more details on magnetic design will be given in the respective section).

Therefore to not saturate the magnetic core it is necessary to find the minimum number of primary turns. With the values above it can be calculated with the below equation.

$$N_p = \frac{L_{p,max} * I_p}{B_{Sat} * A_e} = \frac{6.5 * 10^{-6} * 18.65}{0.24 * 0.000125} \approx 4 \text{ Turns}$$

So there should be a minimum four turns at the primary to achieve maximum flux density of 0.24 T. Again more information about the core can be found in the magnetic design section.

Then to choose the correct cable and wiring options RMS values of the currents should be calculated.

$$\text{For primary side } I_{p,rms} = I_{p,peak} * \sqrt{D_{max}/3} = 18.65 * \sqrt{0.505/3} = 7.65 \text{ A}$$

$$\text{For secondary side } I_{s,peak} = I_p * 1/4 = 4.67 \text{ A} , I_{s,rms} = 4.67 * \sqrt{\frac{1-0.505}{3}} = 1.9 \text{ A}$$

As it stated previously our switching frequency is designed as 50 kHz therefore to avoid skin effect and AC resistance the cable selection should be done wisely.

As it can be seen from the AWG (American Wire Gauge) system table below, AWG 23 type cable can be selected, realizing that as thin as the cables get their current transmission abilities decreases. So if one uses the thinnest cable either it should have lots of paralleling or it will burn as the high current passes through.

Since in this project the AWG 23 type is selected it can be seen that it has 0.729 A maximum current capacity therefore according to the previously calculated current values it should be wired as parallel as well

For the primary side, wire should contain at least 11 cables to satisfy current condition. This means there will be 44 AWG23 cable at the window for primary. For Secondary only 3 parallel cables are needed for secondary wire, thus there will be 48 cables. So in total 92 cables in the window and since each cable has 0.258 mm<sup>2</sup> area this makes a total of 24 mm<sup>2</sup> winding area. And it is wise to give this value a large error margin since cables will be wired as parallel and hand winding is not the tightest winding. Finally, the total area is assumed to be 50 mm<sup>2</sup>. Therefore the winding area of the core should be at least 50 mm<sup>2</sup> more analysis will be made in the magnetic design section.

AWG gauge	Conductor Diameter Inches	Conductor Diameter mm	Conductor cross section in mm <sup>2</sup>	Ohms per 1000 ft.	Ohms per km	Maximum amps for chassis wiring	Maximum amps for power transmission	Maximum frequency for 100% skin depth for solid conductor copper	Breaking force Soft Annealed Cu 37000 PSI
21	0.0285	0.7239	0.412	12.8	41.984	9	1.2	33 kHz	23 lbs
22	0.0253	0.64516	0.327	16.14	52.9392	7	0.92	42 kHz	18 lbs
23	0.0226	0.57404	0.259	20.36	66.7808	4.7	0.729	53 kHz	14.5 lbs
24	0.0201	0.51054	0.205	25.67	84.1976	3.5	0.577	68 kHz	11.5 lbs
25	0.0179	0.45466	0.162	32.37	106.1736	2.7	0.457	85 kHz	9 lbs

**Table 1:** AWG Cable Specifications Table

To calculate the rating of diode, according to the guides  $V_{RRM}$  should be at least 30% higher than  $V_{RV,diode}$  and  $I_F$  (average forward current) is at least 50% higher than the  $I_{s,rms}$ .

Then by using the equation  $V_{RV,diode} = V_{out} + V_{in,max} * n = 48 + 18 * 4 = 120 V$  We can say that  $V_{RRM}$  should be around 156 V and  $I_F$  should be around 2.9 A

For the capacitor selection part, by looking the project requirements maximum of %3 Voltage ripple is allowed so if below calculation is done

$\Delta V_o/V_o = \frac{D}{RCf} = 0.03 = \frac{0.51}{48*C*50000} \Rightarrow C = 7.1 \mu F$ . To stay in the safe region we shall

use 10  $\mu F$  and ESR values of the capacitor should be picked carefully as well to reduce losses and ripples. For maximum ESR value below equations is calculated

$$I_{c,rms,min} = \sqrt{I_{s,rms}^2 - I_{out}^2} = 1.62 A$$

$$ESR_{max} < \frac{\Delta V_{out}}{I_{s,peak}} = 1.44/1.9 = 0.76$$

So important values can be listed as below;

$$L_M = \frac{(V_{in,min}*D_{max})^2}{2*Pin*f_{sw}} = \frac{(12*0.505)^2}{2*56.5*50000} = 6.5 \mu H$$

$$\Delta I_L = \frac{V_{in,min}*D_{max}}{L_M*f_{sw}} = \frac{12*0.505}{6.5*10^{-6}*50000} = 18.65A$$

$$I_{EDC} = \frac{P_{in}}{V_{in,min}*D_{max}} = \frac{56.5}{12*0.505} = 9.32A$$

$$I_{DS,peak} = I_{EDC} + \Delta I/2 = 18.65A$$

$$I_{DS,rms} = \sqrt{(3 * I_{EDC}^2 + (\Delta I/2)^2) * D_{max}/3} = 7.65A$$

$$N_{P,min} = \frac{L_M*I_{over}}{B_{Sat}*A_e} * 10^6 = 4 turns$$

## 4. Magnetic Design

As it is stated in the analytical design part around these frequencies and power ratings ferrite cores are advised to use with flyback converters. Moreover, to reduce the leakage inductance likely closed (i.e. pot core) type core RM type is selected pot core reduces leakage inductance therefore reduces the need of snubber circuit (explained detailly in Snubber Design section). Specifically RM12 is selected, RM stands for rectangular modul and 12 is the size value; these core types were designed for efficient winding and high PCB packing densities.

**Figure 1: RM12 Core**

One of the most important things while considering the transformer design is winding area calculation, it should be checked that the calculated winding number and area cross section will fit the core or not. In the previous section we calculated there will be a total of 92 cables at the window, which makes  $24 \text{ mm}^2$  winding area. Since they are wired as parallel, it will probably be higher, therefore safe area  $50 \text{ mm}^2$  so to say. Winding area of the coil former is  $75 \text{ mm}^2$ , which makes fill factor 0.75. It is a reasonable fill factor since considering having a large safety margin.

Winding data for RM12/I coil former (DIL)

NUMBER OF SECTIONS	AVERAGE LENGTH OF TURN (mm)	WINDING AREA ( $\text{mm}^2$ )	WINDING WIDTH (mm)	TYPE NUMBER
1	61	75.0	14.3	CPV-RM12/I-1S-12PD

**Table 2: Coil Former Specifications Table**

In the [datasheet of the coil former](#), it says the average length of a single turn is 61 mm. AWG23 has  $66.8 \Omega/\text{km}$  resistance, which is  $6.68 * 10^{-5} \Omega/\text{m}$ . As cables will be wired as parallel, the total resistance can be calculated as the formula given below.

$$\rho = \frac{\text{Number of Turns} * 61 * 6.68 * 10^{-5}}{\text{Number of Paralleled Cables}}$$

$$\rho_{pri} = \frac{4 * 61 * 6.68 * 10^{-5}}{11} = 0.0015\Omega$$

$$\rho_{sec} = \frac{16 * 61 * 6.68 * 10^{-5}}{3} = 0.022\Omega$$

The AWG23 cable has 100% skin depth at the frequency about 50kHz. Therefore, AC resistance will be zero therefore total resistance is equal to DC resistance.

$$P_{p,copper} = I_{RMS}^2 * R = 7.65^2 * 0.0015 = 0.09 W \quad P_{s,copper} = 1.9^2 * 0.022 = 0.08 W$$

$$P_{total,copper} = P_{s,copper} + P_{p,copper} = 170 mWatts$$

According to the [datasheet of the core](#) N41 core has the following specs.

### Ungapped

Material	$A_L$ value nH	$\mu_e$	$P_V$ W/set	Ordering code -E without center hole
N41	6000 +30/-20%	1860	< 1.50 (200 mT, 25 kHz, 100 °C)	B65815E0000R041

**Table 3: Core Specifications Table**

So with 4 turns  $L_M = n^2 * A_L = 16 * 6000 * 10^{-9} = 96 \mu H$  so it's very high. We should reduce this. It can be reduced by introducing an air gap to the core by inserting an air gap this  $A_L$  value will decrease so that we can achieve around 8  $\mu H$ . Therefore we need

$$8 * 10^{-6} = 4^2 * A_L \Rightarrow A_L = 500 * 10^{-9}$$

Width of the air gap to achieve above value can be calculated by the following formula.

$$1/A_{L-desired} - 1/A_{L-old} = 1/A_{L-air} \text{ so } A_{L-air} = 545 * 10^{-9}$$

$$1/A_{L-air} = \text{length of air gap} / (A_{core} * \mu_{air}) \Rightarrow \text{length of air gap} = 0.29 \text{ mm}$$

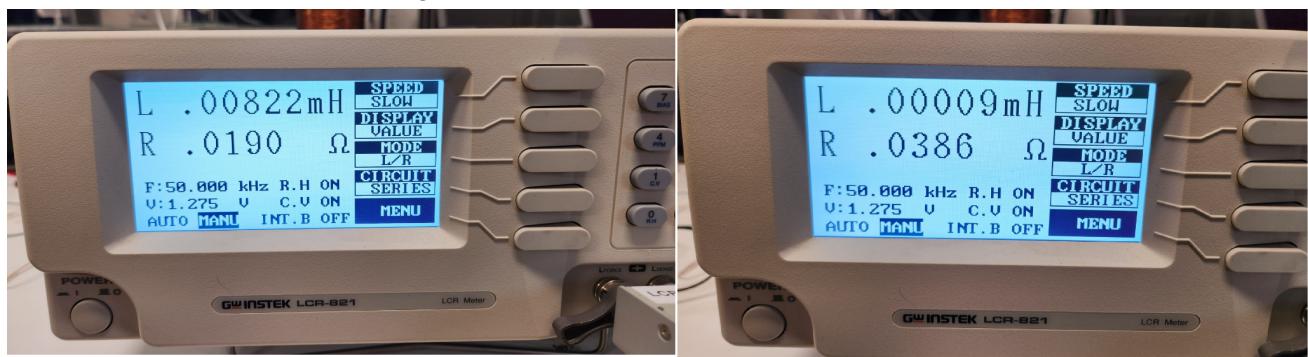
Therefore 0.29 mm air gap can be achieved by putting two or three pieces of A4 paper.

By trying both 2 A4 and 3 A4 it is observed to have 2 A4 to have around 8  $\mu H$  of mutual inductance.

Testing of the transformer is done by Hioki LCR meter.

- When we open circuited secondary side and measure the inductance of the primary side we measure the leakage inductance and mutual inductance together  $L_{leakage} + L_M$  and it is calculated as 0.00822 mH
- When we short circuited secondary side and measure the inductance of the primary side we measure only leakage inductance and it is calculated as 0.00009 mH

Photos of the measurements is given below



**Figure 2: LCR Measurement, Primary Opened at right Primary Shorted**

So we obtained  $8.13 \mu H L_m$  and  $0.09 \mu H L_{leak}$  so %1.1 leakage is obtained which is a very nice result thanks to the pot core.

Then to be certain of the winding rotation is done opposite (i.e. reverse dot notation) a sine wave generator is connected to the primary side and secondary side is measured by oscilloscope, as expected  $180^\circ$  of phase shift occurred at the secondary side and by looking the measurements from oscilloscope measurement button it can be seen that ;

$V_{pri,pk-pk} = 1.64 V$  ,  $V_{sec,pk-pk} = 0.424 V$  so nearly 4 times voltage multiplication is also achieved as well.

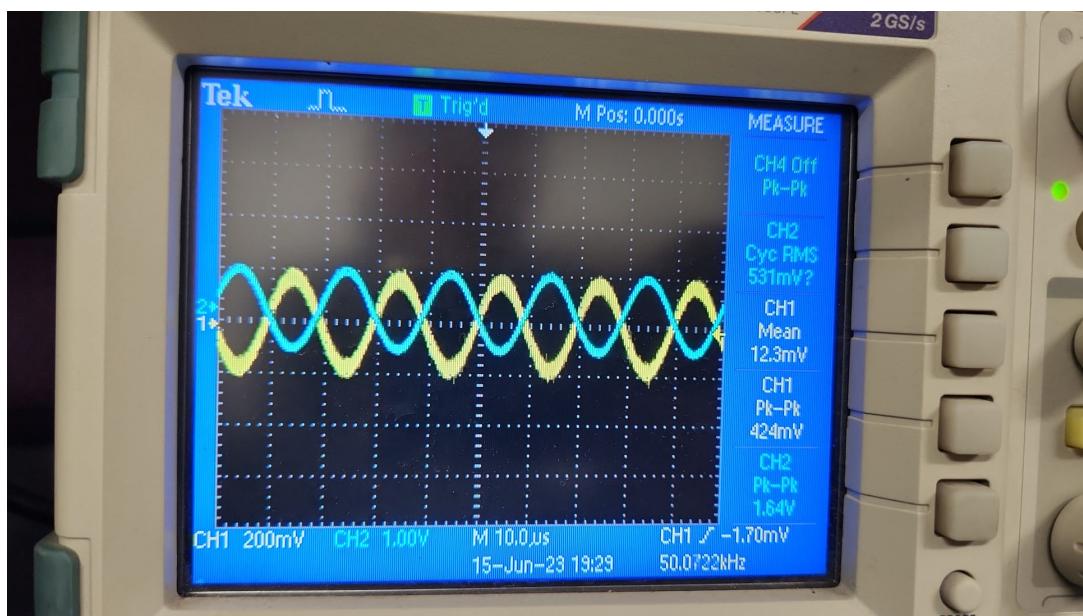


Figure 3: Oscilloscope measurement of primary and secondary sides.



Figure 3: Photo of our transformer we wended, also coil former and core clips compatible with core.

## 5. Component Selection

For the MOSFET [IRF540N](#) is chosen as it satisfies both current (18.65A) and voltage (45V) ratings with 28A and 100V ratings.

For the diode, [12TQ200\(S\)](#) is chosen as it satisfies both current (1.9 A<sub>avg</sub> & 4.6 A<sub>peak</sub>) and voltage (120V) ratings simultaneously. Moreover, it has around 0.75V forward voltage drop on it.

For the output capacitor, [100SXE18M](#) is chosen. According to the datasheet, ESR is calculated with the formula given below. Since it is a Aluminium-Polymer Capacitor it has small ESR which is 30 mOhm

For the controller, we chose [Texas Instruments UC3843](#) since it has an allowable voltage and frequency ratings in the necessary values and has the ability to operate until %93 duty cycle.

For the feedback voltage reference input which should go to the UC3843 we used a [TL-431](#) adjustable voltage reference and optocoupler [tcmt1107](#) components to construct a reference voltage input circuit

## 6. Snubber Design

For snubber designs the reference design guideline of the Ridley [Flyback Snubber Design](#) documentation is examined. The most critical snubber in a typical flyback converter is the snubber for the leakage inductor, although our leakage inductance ratio is around 1% at the cut off time di/dt of the current will be nearly infinite it will have a significant ringing on the main mosfet, to reduce this two different snubber types can be used.

Even after the RCD snubber implementation the voltage spikes and ringings were not reduced a good amount in the simulations so we decided to add an additional RC snubber in parallel with the mosfet as well and simulation result was decent after this implementation.

As it is stated in the ridley design pdf additional snubber may be necessary to add at the diode of the secondary side, from the LTspice simulations although the leakage ringins were not exceeding our rating values it was relatively high so we decided to add a parallel RC snubber to the secondary side diode as well. These snubbers will introduce power dissipation (especially the RCD clamp one) but it is a trade off that we thought it's beneficial to take it to have stable operation.

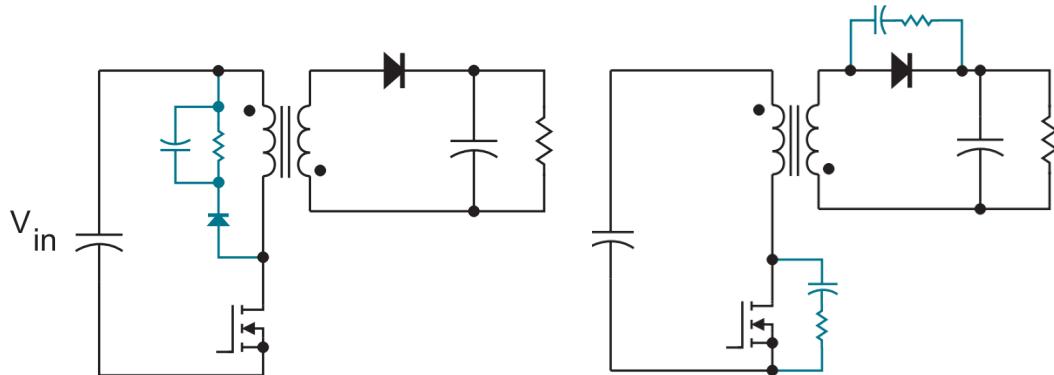


Figure 4: RCD Clamp Snubber

Figure 5: Parallel RC Snubber for Secondary Side Diode and Mosfet

For the values of snubbers more than one different documents were analyzed but the main one is the ridley one. Advised calculations for each different document are analyzed and roughly close components are selected.

Here the values for each different snubbers

- RCD Clamp :  $1.2\text{ k} // 1\text{ k} = 0.55\text{ Ohm}$   $220\text{ nF}$ , diode rating at least 20 A.
- FET Parallel RC :  $100\text{ Ohm}$   $4.7\text{ nF}$ .
- Diode Parallel RC :  $200\text{ Ohm}$   $470\text{ pF}$ .

## 7. Closed Loop Design (with UC3843A)

The most crucial part of the converter is the implementation of the controller. For this purpose, it is decided to use a member of the controller family UCx84x. Table 4 shows the members of the UCx84x family and their specific characteristics.

UVLO		TEMPERATURE RANGE	MAX DUTY CYCLE
TURNON AT 16 V TURNOFF AT 10 V SUITABLE FOR OFF-LINE APPLICATIONS	TURNON AT 8.4 V TURNOFF AT 7.6 V SUITABLE FOR DC-DC APPLICATIONS		
UC1842	UC1843	-55°C to 125°C	Up to 100%
UC2842	UC2843		
UC3842	UC3843		
UC1844	UC1845	-55°C to 125°C	Up to 50%
UC2844	UC2845	-40°C to 85°C	
UC3844	UC3845	0°C to 70°C	

Table 4: UCx84x controller family and their specific characteristics

It is decided to operate at the boundary of DCM-CCM. Maximum duty cycle was calculated around 52%. Moreover, input voltage range is specified as 12-18V. Based on these considerations, the optimum solution is UC1843. However, due to unavailability of UC1843 and high price of UC2843 compared to UC3843, the controller is chosen as UC3843. Figure X shows the functional block diagram of the selected controller

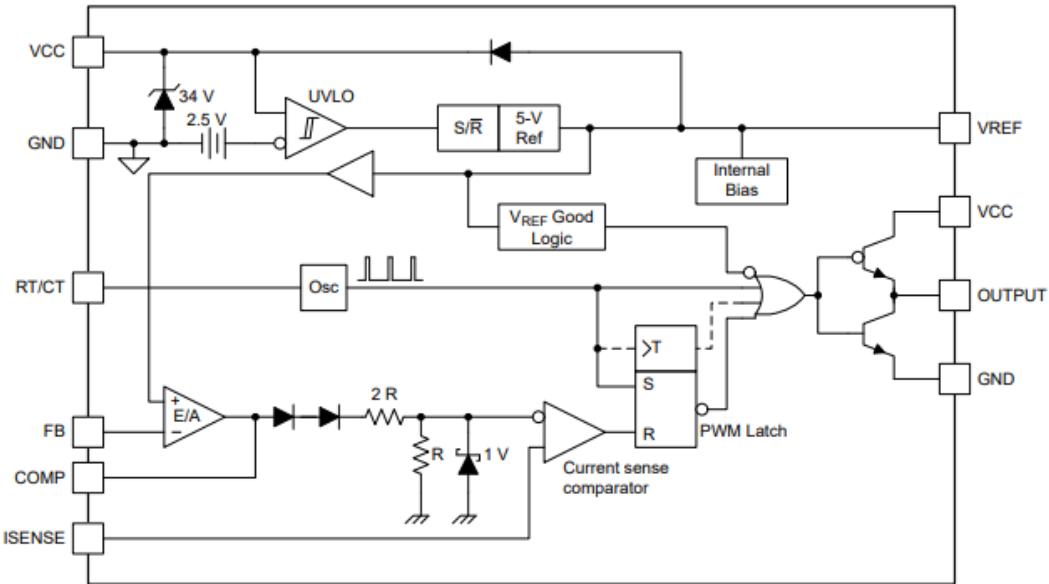


Figure 6: UCx84x controller functional block diagram

According to under voltage lock-out parameters provided in Figure 6, connecting the bias input of the controller directly to the input of the converter was sensible. A  $1\mu\text{F}$  capacitor between bias input and the ground as suggested in the datasheet and a diode was to be connected as a precaution in case of wrong connection of input.

RT/CT pin is the input to the internal oscillator. According to the datasheet,  $f_{\text{osc}} \approx 1.72/(R_T C_T)$ , where  $R_T$  and  $C_T$  is the timing resistor and the capacitor. The frequency was decided to be 50kHz. Figure 7 shows the timing capacitor and the deadtime relation. Therefore,  $C_T$  was chosen as low as possible,  $1\text{nF}$ . The corresponding  $R_T$  was  $34.4\text{k}\Omega$ .

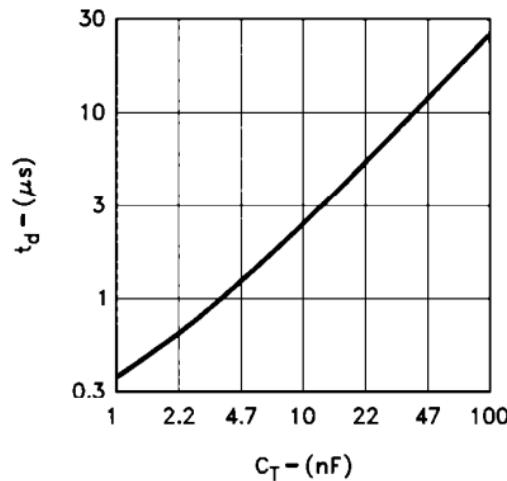
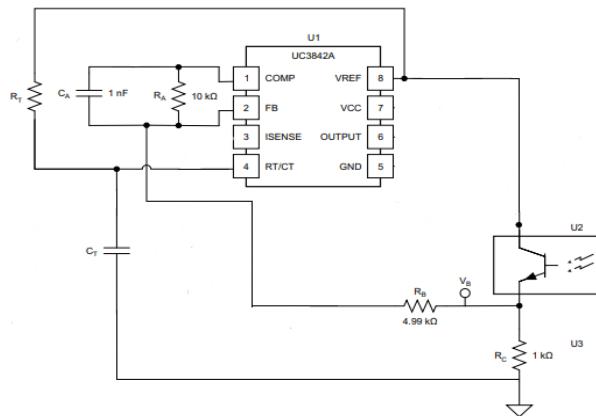


Figure 7: Timing capacitor and the deadtime relation

$R_T$  was connected between oscillator and  $V_{\text{REF}}$ , which has constant 5V output. Collector of the opto-coupler was also connected to that pin. Reflected current was drawn from that pin, which was capable of sourcing 10mA. Figure 8 shows the

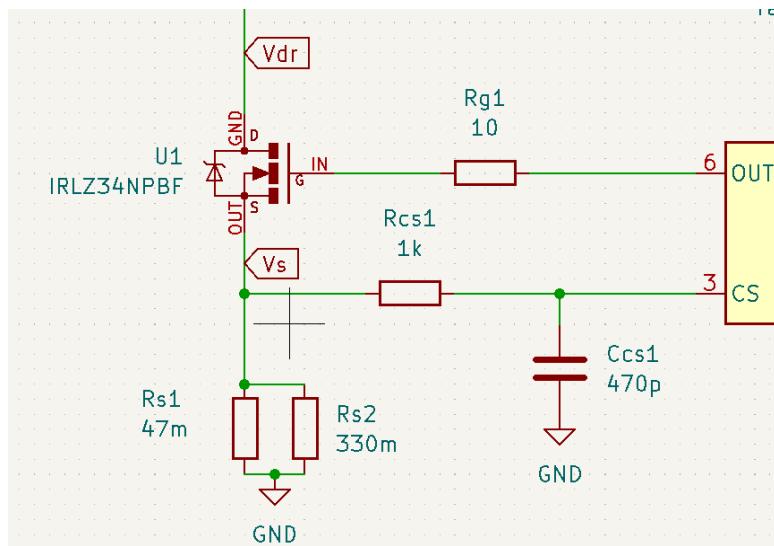
connection of timing components and the output of the feedback opto-coupler. The values were chosen as provided in the datasheet.



**Figure 8:** Opto-coupler,  $V_{REF}$ , FB pin connection given in the datasheet.

To drive the switch element, the internal gate driver of the controller was used and a  $10\Omega$  resistor was connected between the gate terminal of the MOSFET and the output pin.

The ISENSE pin is the input of the PWM comparator, which enables current to be limited. This pin is internally clamped to 1V. The corresponding shunt resistor is determined by peak ISENSE voltage divided by peak current of the MOSFET, around  $18.6\text{A}$ . Shunt resistor was calculated around  $42\text{m}\Omega$ . In addition, this shunt resistors should be capable of dissipating  $I_{max,avg}^2 \cdot R_{sh} \approx 3.8\text{W}$ , where  $I_{max,avg}$  is the average current at the minimum input voltage, 12V.  $42\text{m}\Omega$   $3.8\text{W}$  shunt resistor was hard to find. This problem was solved by paralleling  $330\text{m}\Omega$  3W and  $47\text{m}\Omega$  3W shunt resistors. In overall, approximately  $42.5\text{m}\Omega$  6W shunt resistor was obtained. The sensed peak current signal was passed through a RC low pass filter. The resistance and capacitance values of the low pass filter were chosen as provided in the datasheet,  $1\text{k}\Omega$  for the resistor and  $470\text{pF}$  for the capacitor. Figure 9 shows the gate driver and current sense connection.



**Figure 9:** Current sense and gate driver connection between MOSFET and controller

The feedback isolation was achieved by an optocoupler. TCMT1107 was chosen for the optocoupler. It isolates voltages up to 3.75kV<sub>RMS</sub>. Figure 10 shows the output feedback configuration of the feedback.

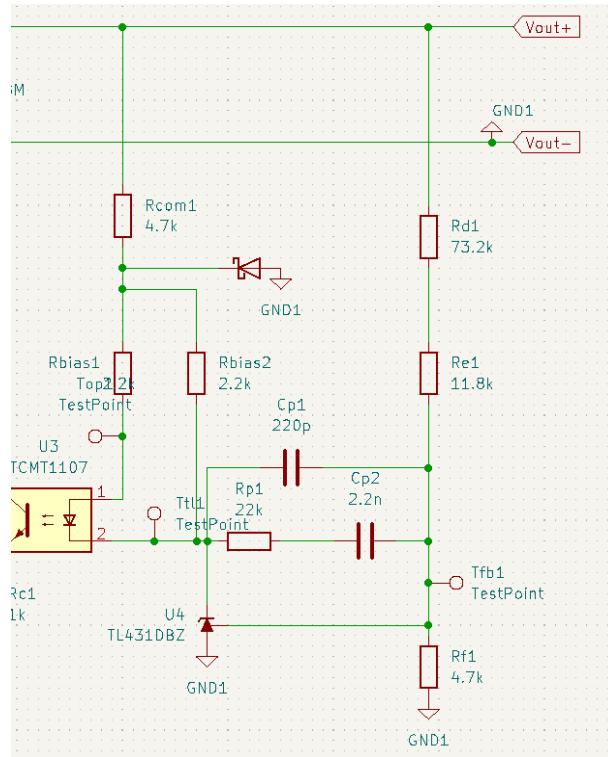
TL431 was used for the voltage reference. The reference pin was set to 2.5V. This voltage level was achieved by a simple voltage division. By taking from the output voltage, 4.7kΩ, and 85kΩ was chosen to set the reference voltage to 2.5V of TL431.

It is assumed that TL431 open loop operation mode gain is around 2. With this assumption, forward current was calculated as follows.

$$V_{out} - I_F * 6.9k - 2.5 * K_{TL431} - V_{F,max} = 0$$

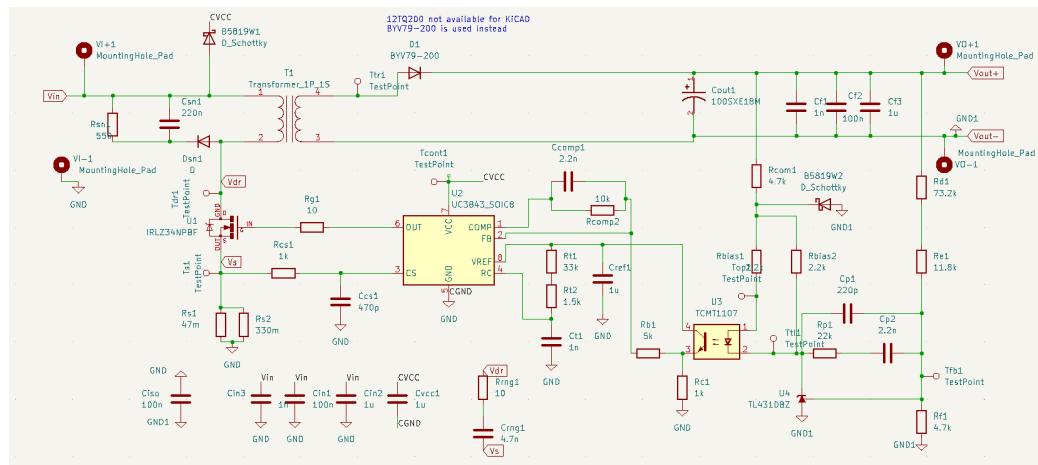
, where  $K_{TL431}$  is the gain of TL431,  $V_{F,max}$  is the maximum forward voltage drop on optocoupler

Then,  $I_F$  is calculated as 6mA. The corresponding current transfer ratio at that level was approximately 80%. Therefore, collector current of the optocoupler, which was drawn from  $V_{REF}$  pin of the controller, became 4.8mA. Collector emitter saturation voltage is typically 250mV according to the datasheet. Referring to Figure 10, (*Opto-coupler,  $V_{REF}$ , FB pin connection given in the datasheet.*) these results have concluded that feedback output voltage would be reflected to primary as intended. However, there was a pole constructed by  $R_{P1}$ ,  $C_{P1}$ , and  $C_{P2}$ . This pole located at a frequency such that zeros making converter operation unstable will be canceled. However, this pole determination required a very tough computation. As a beginner level designer, we thought that this calculation was beyond our control theory knowledge and also scope of the EE464 course. Therefore, we decided to use a pole constructed by these capacitors and resistor proposed by one of the Webench Power Designer. Figure 10 shows the chosen pole constructor components' values.



**Figure 10:** Opto-coupler, feedback resistors and voltage reference connection

Figure 11 shows the overall closed loop converter circuit schematic.



**Figure 11:** KiCAD model of the overall circuit of the designed converter

## 8. Thermal Analysis & Losses

$$P_{loss,cond.,MOSFET} = I_D^2 * R_{DS} * D = 7.65^2 * 44 * 10^{-3} * 0.52 = 1.34W$$

$$P_{loss,sw.,MOSFET} = V_{in} * I_{out} * f_{sw} * (t_{rise} + t_{fall}) = 18 * 1 * 50000 * (35 + 35) * 10^{-9} = 7.21 * 10^{-3} W$$

$$P_{total,MOSFET} = 1.35 W$$

$$P_{loss,cond.,diode} = V_f * I_{avg} * (1 - D) = 0.87 * 1.9 * 0.48 = 0.793W$$

Switching losses on the schottky diodes are negligible

$$P_{loss, ESR} = I^2 \times R = 1^2 \times 33 \times 10^{-3} = 33 \times 10^{-3} W$$

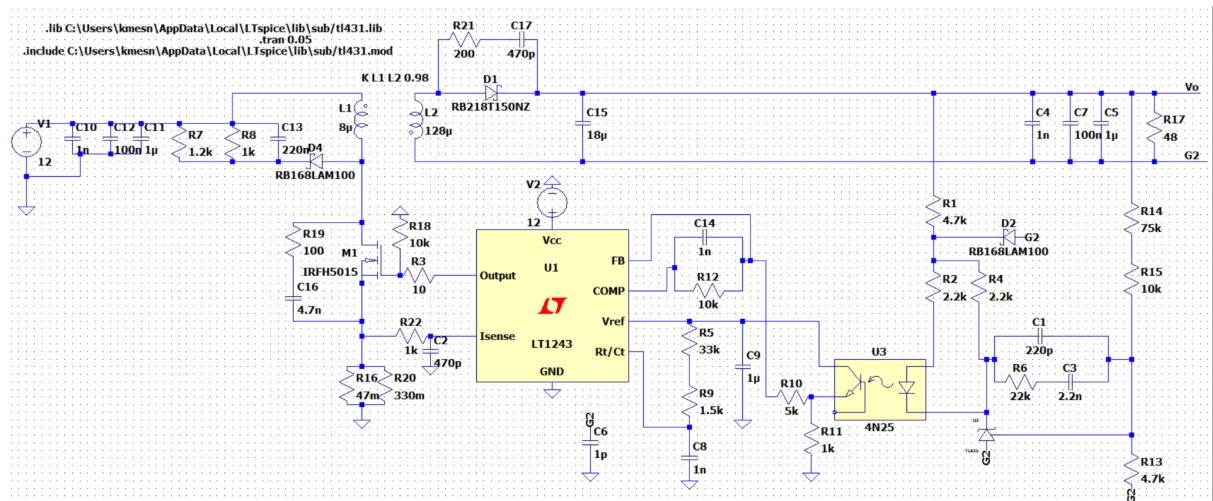
Core loss under specific conditions has been provided by the core manufacturer. In the datasheet it writes losses at specific frequency, our core was N41 material and N41 material has a loss less than 1.5 Watt at 25 kHz so at the switching frequency of 50kHz the core loss can be approximated as 2 Watts.

$$T_{junction} = T_{ambient} + P_{loss} * R_{th,eq}$$

$$T_{MOSFET} = T_{ambient} + P_{loss} * (R_{th,JC} + R_{th,CS} + R_{th,SA}) \\ = 17^{\circ}C + 2.35W \times (0.86^{\circ}C/W + 0.50^{\circ}C/W + 3.5^{\circ}C/W) = 28.421$$

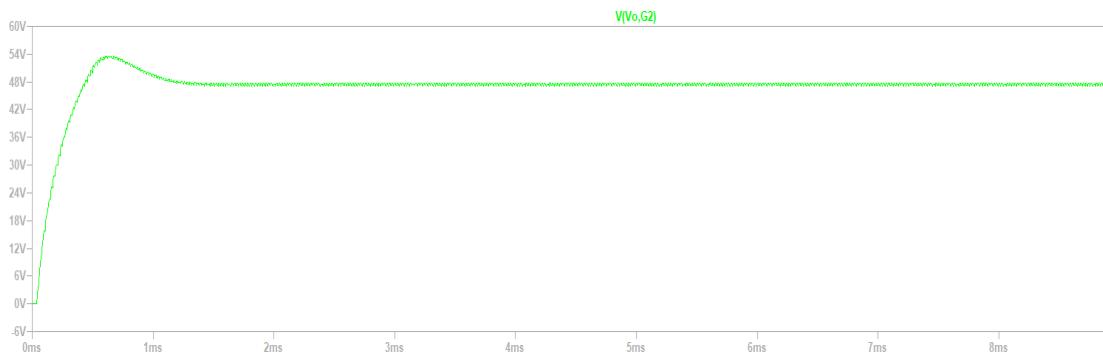
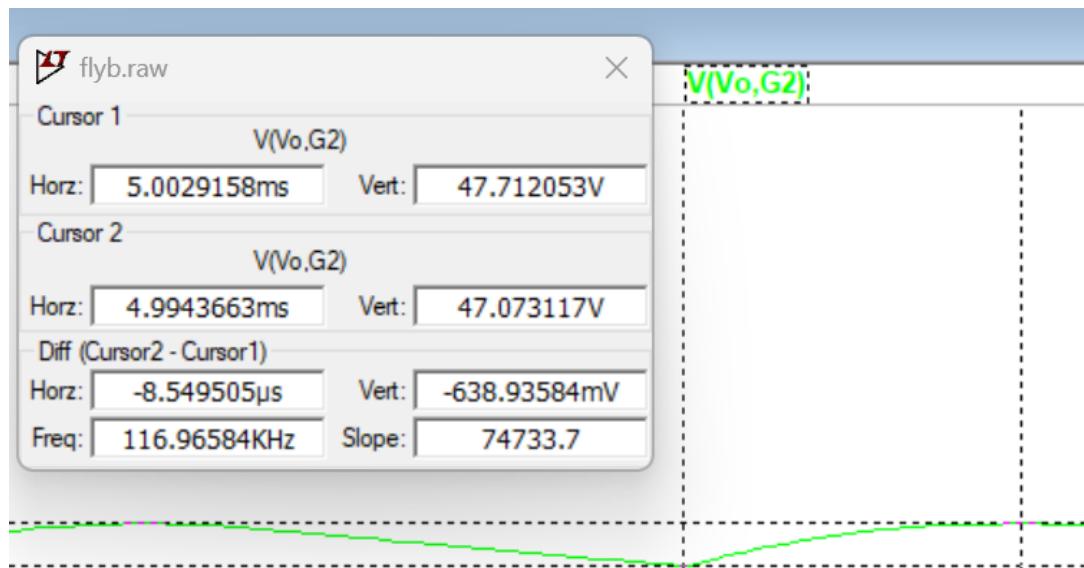
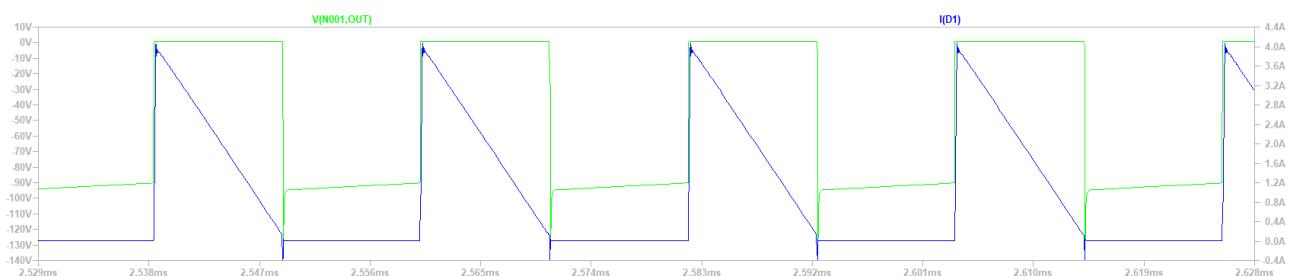
$$T_{Diode} = T_{ambient} + P_{loss} * (R_{th,JA}) = 17 + 24 \times 0.793 = 36.032$$

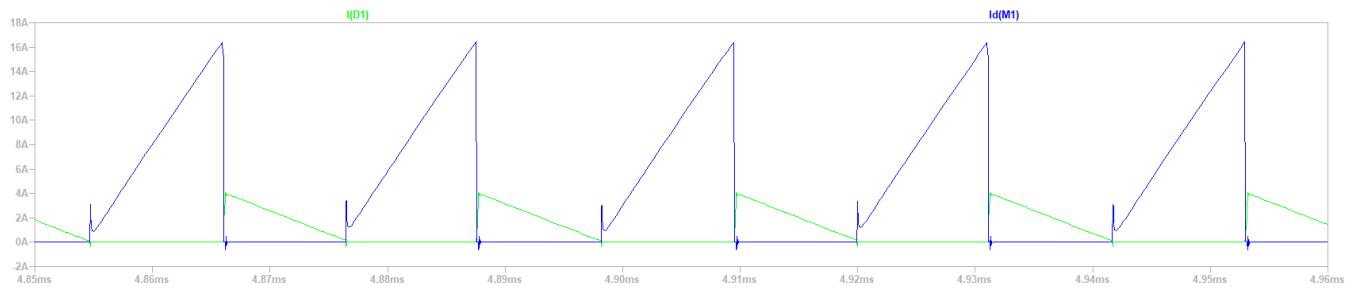
## 9. Simulations



**Figure 12:** LTSpice model of the overall circuit of the designed converter

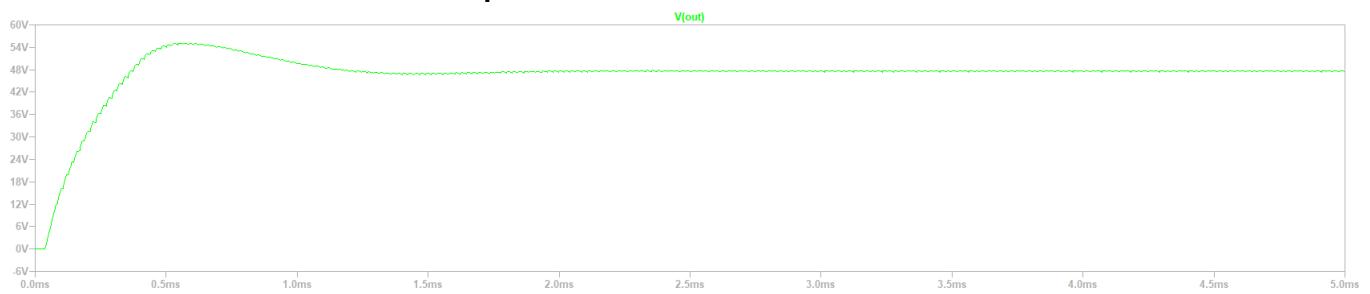
Since the real life implementation of our flyback controller project did not work, we implemented this on LTspice simulation program with all the real models included and all of the components are realized as real models not ideal models. Therefore these simulations will be as close to the real implementation as possible to the real life if implementations are nearly perfect without any flaws.

**Figure 13:** Output Voltage Waveform the LTSpice Simulation**Figure 14:** Output Voltage Ripple from the LTSpice Simulations**Figure 15:** Mosfet Drain to Source Voltage and Current from the LTSpice Simulations**Figure 16:** Diode Voltage and Current from the LTSpice Simulations

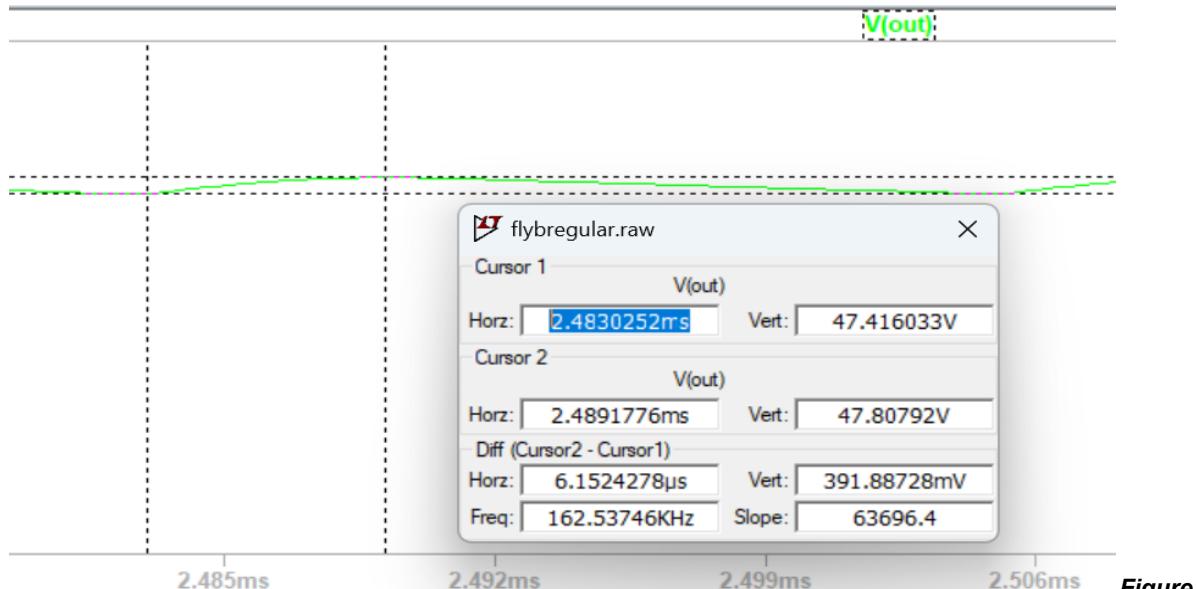


**Figure 17:** Mosfet Current and Diode Current from the LTSpice Simulations

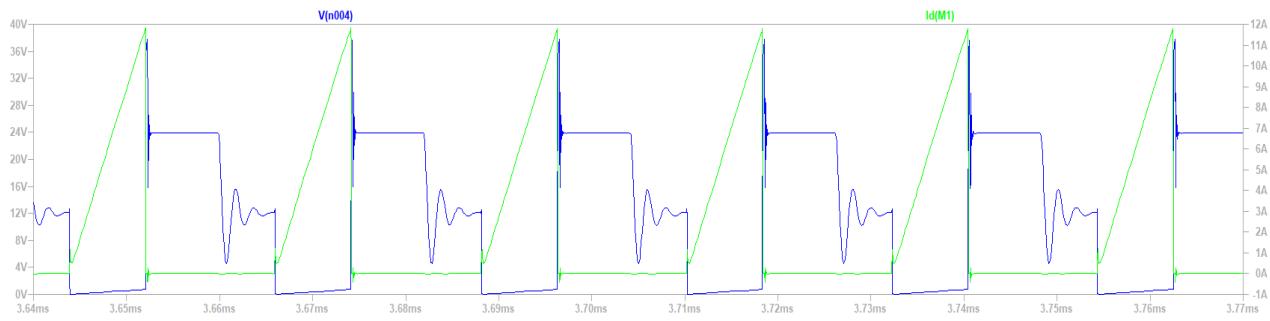
To observe the **%75 load output** resistance is increased to 96 Ohm.



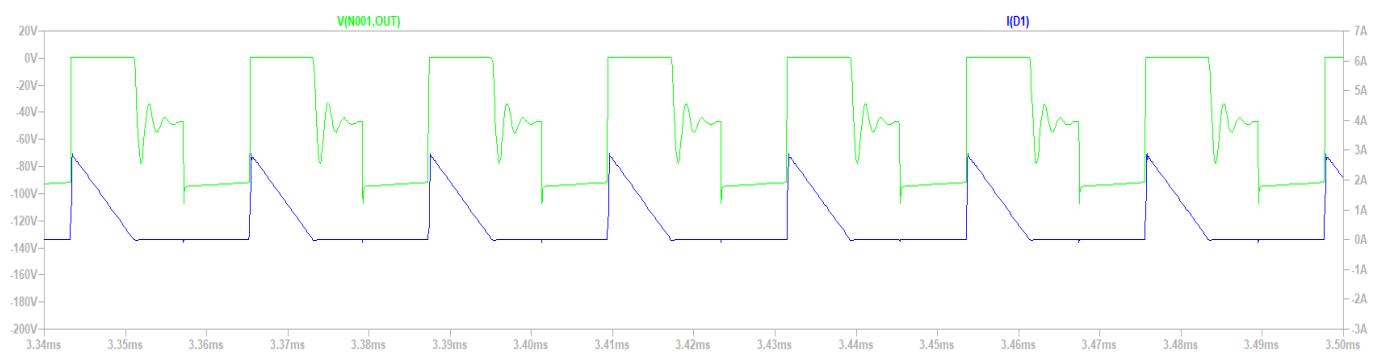
**Figure 18:** Output Voltage Waveform from the LTSpice Simulations



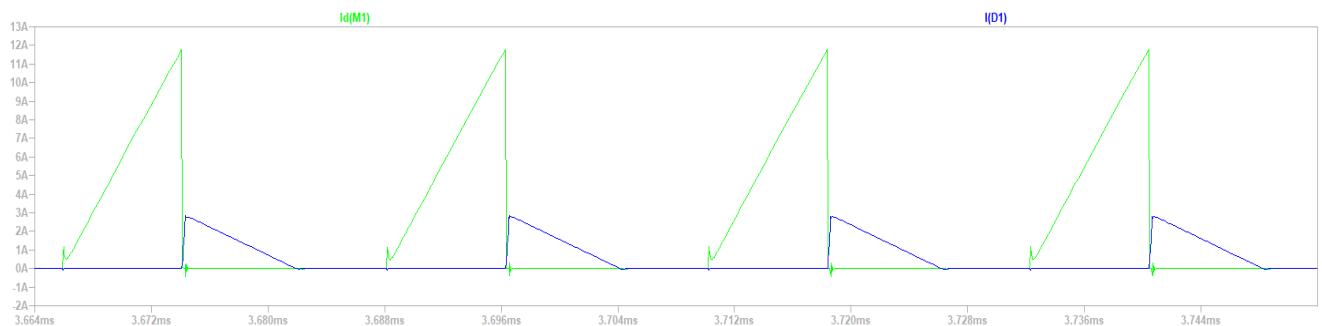
**Figure 19:** Output Voltage Ripple from the LTSpice Simulations



**Figure 20:** Mosfet Drain to Source Voltage and Current from the LTSpice Simulations



**Figure 21:** Diode Voltage and Current from the LTSpice Simulations



**Figure 22:** Mosfet Current and Diode Current from the LTSpice Simulations

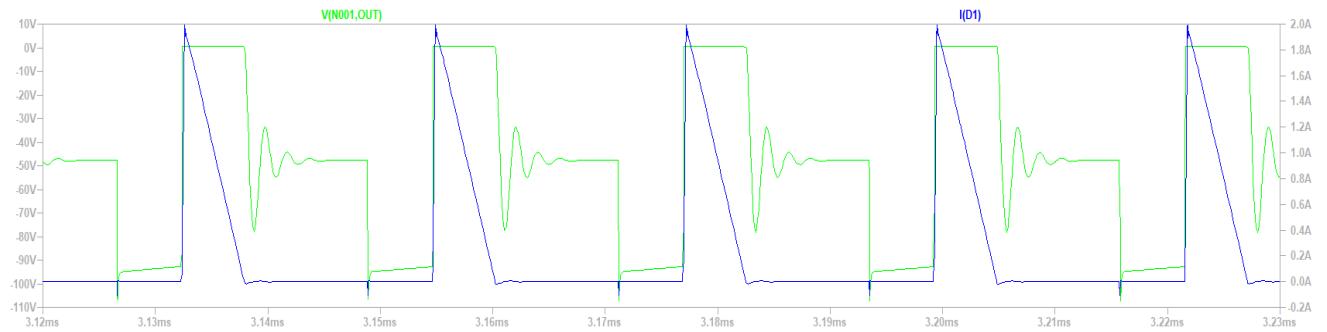
To observe the **%50 load** output resistance is increased to 192 Ohm



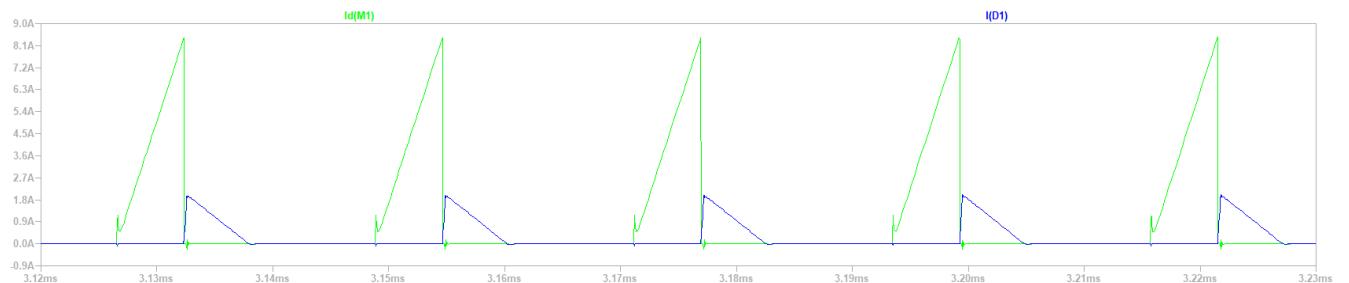
**Figure 23:** Output Voltage Waveform the LTSpice Simulations



**Figure 24:** Mosfet Drain to Source Voltage and Current from the LTSpice Simulations

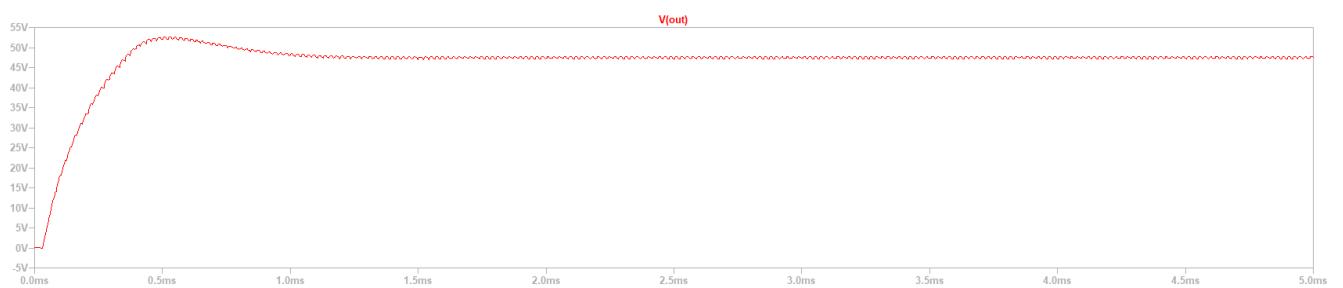


**Figure 25:** Diode Voltage and Current from the LTSpice Simulations



**Figure 26:** Mosfet Current and Diode Current from the LTSpice Simulations

For the input voltage of 18V since it is a less power demanding case and more stable and accurate there will be only full load simulation (output resistance is 48 ohm) results.



**Figure 27:** Output Voltage Waveform the LTSpice Simulations

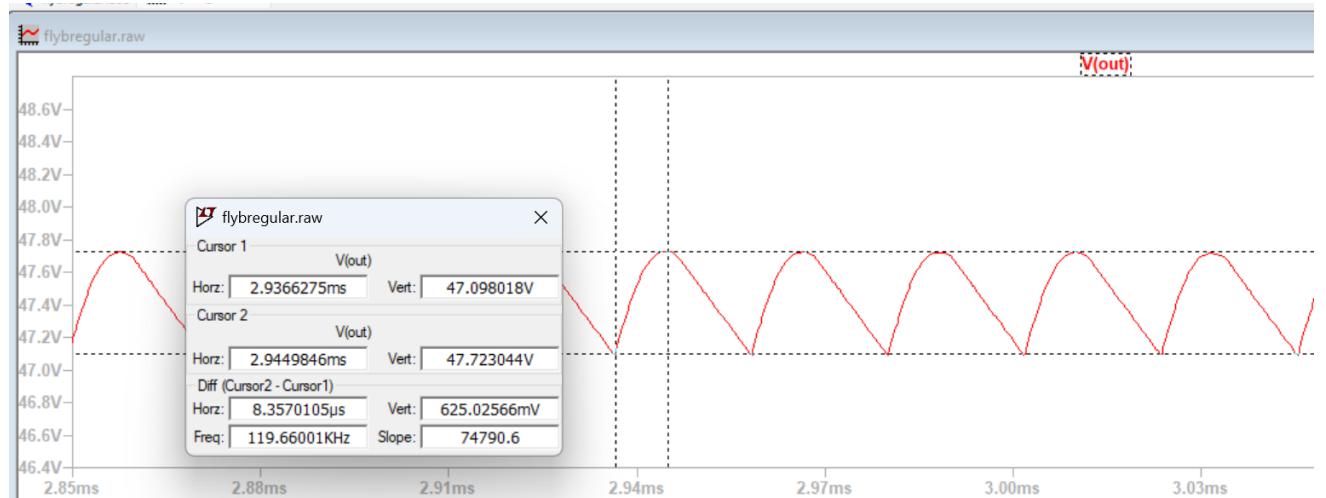


Figure 28: Output Voltage Ripple from the LTSpice Simulations

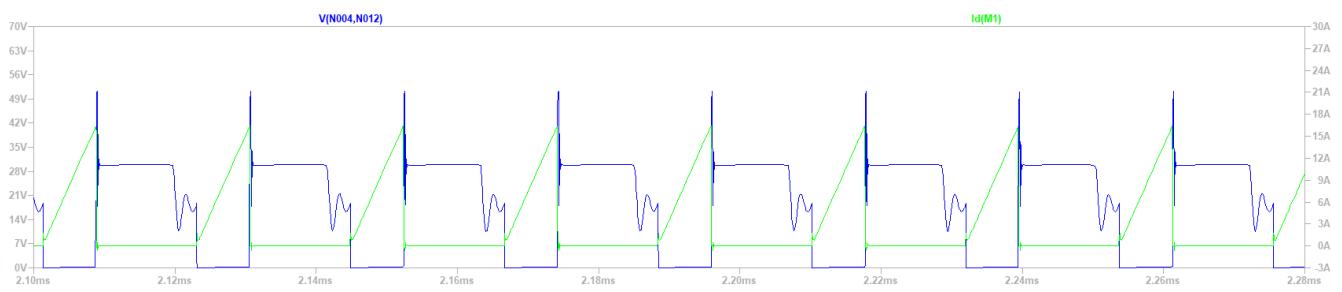


Figure 29: Mosfet Drain to Source Voltage and Current from the LTSpice Simulations

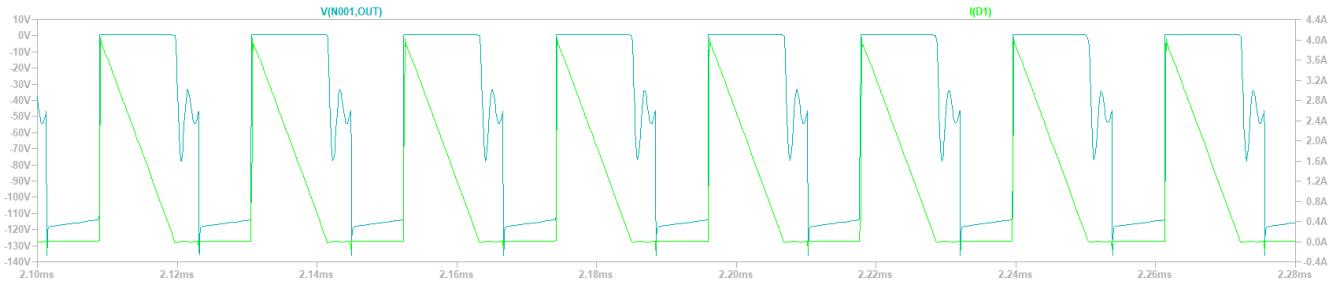


Figure 30: Diode Voltage and Current from the LTSpice Simulations

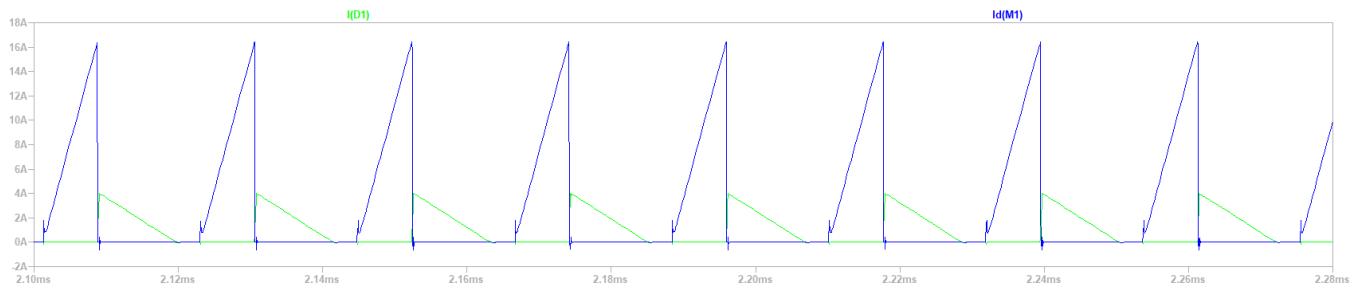


Figure 31: Mosfet Current and Diode Current from the LTSpice Simulations

Switching frequency can be observed by looking at the time steps of one period of the switching and it is measured around 46.37 kHz in all of the cases. And DCM operation is observable in the current plots.

To observe the power dissipation on snubbers, shunt resistors etc. components we could look at the power dissipation of each component but instead we used ltspice algorithm

to calculate total efficiency since the load current is swept between the load ratios %25,50,75,100 the efficiency report is at the end of this part.

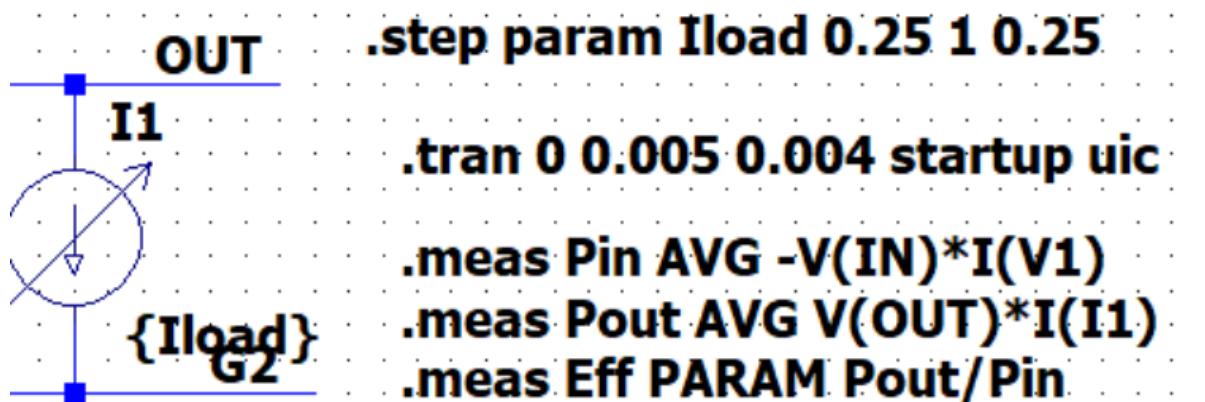


Figure 32: Efficiency Calculation Algorithm from the LTSpice Simulations

The screenshot shows the LTSpice error log window with the following content:

```

SPICE Error Log: C:\Users\kmesn\OneDrive\Masaüstü\flybregular.log

.step iload=0.75
.step iload=1

Measurement: pin
step      AVG(-v(in)*i(v1))  FROM          TO
  1        13.8876            0             0.001
  2        26.8762            0             0.001
  3        40.272             0             0.001
  4        54.0041            0             0.001

Measurement: pout
step      AVG(v(out)*i(i1))  FROM          TO
  1        11.9196            0             0.001
  2        23.7885            0             0.001
  3        35.6221            0             0.001
  4        47.4304            0             0.001

Measurement: eff
step      pout/pin
  1        0.858289
  2        0.885114
  3        0.884538
  4        0.878274

Date: Tue Jun 27 18:35:03 2023
Total elapsed time: 10.341 seconds.

tnom = 27

```

Figure 33: Efficiency Calculation Results from the LTSpice Simulations

Then by adding the core loss of 2 Watt we calculate the efficiency at the high load as %81.8 it's over the required efficiency ideally but there would obviously be more losses such as non-ideal conducting path losses due to pcb and losses due to heating etc. I honestly didn't think we could meet the efficiency condition at full load

## 10. PCB Design

To realize the design and the simulation, a two layer PCB was designed. Figure Y shows the designed PCB layout of the circuit.

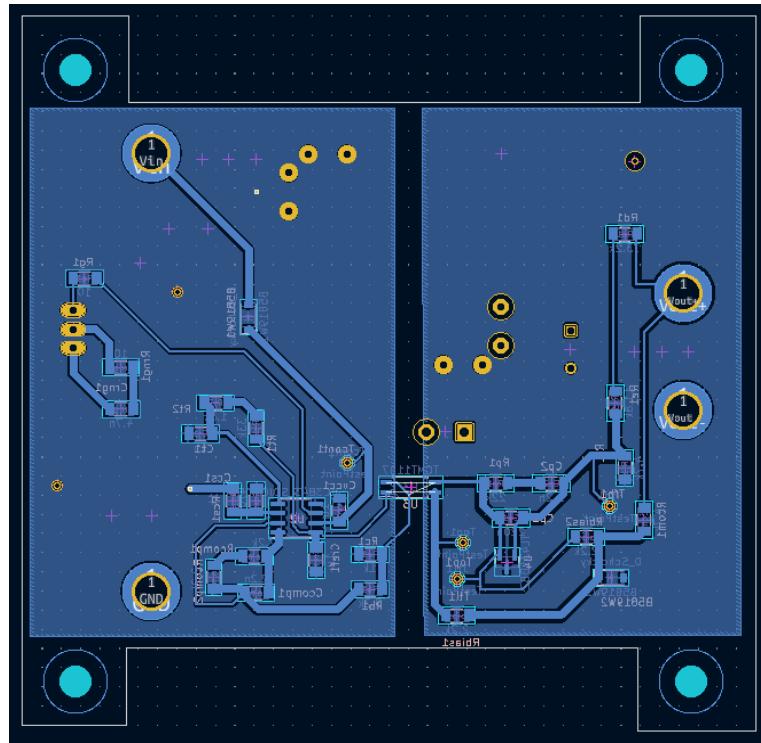


Figure 34: KiCAD PCB model of the overall circuit of the designed converter: Back Layer (Feedback)

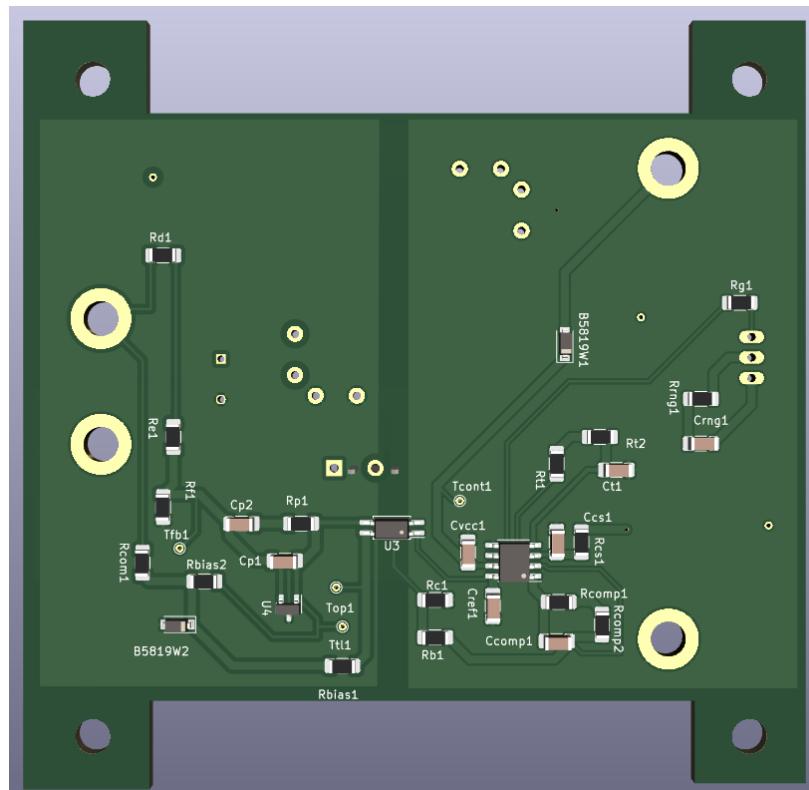
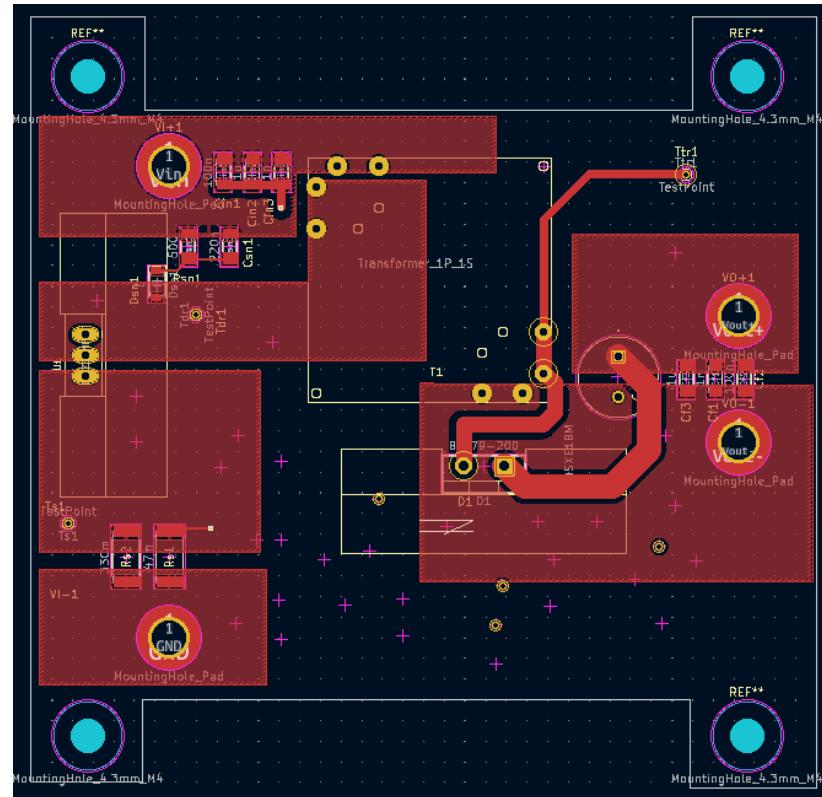
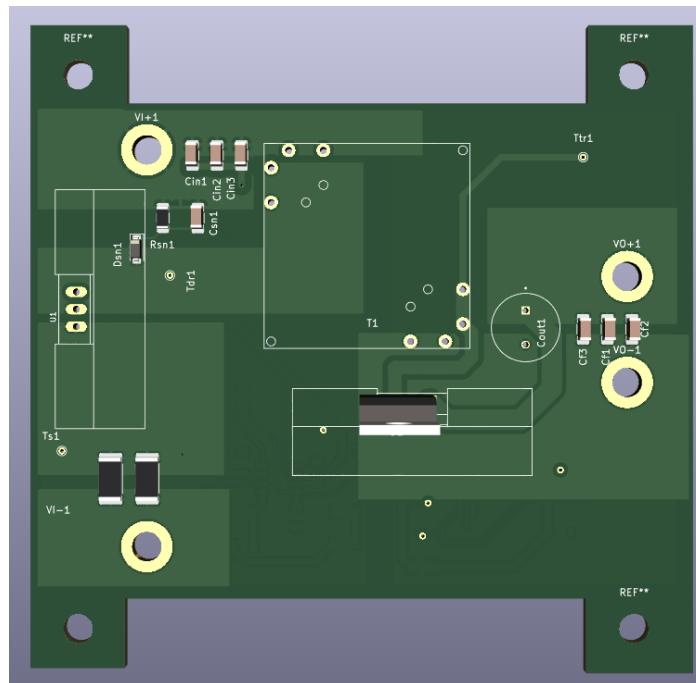


Figure 35: KiCAD PCB model of the overall circuit of the designed converter: 3D Model (Back Layer)

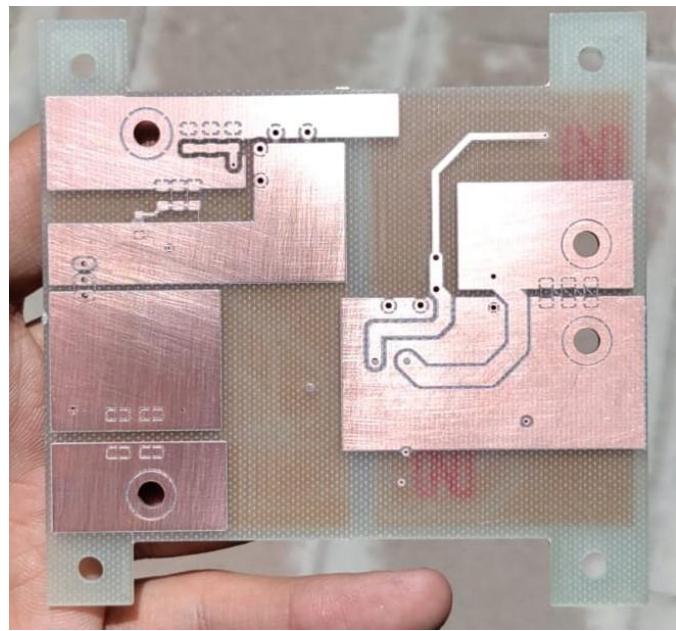


**Figure 36:** KiCAD PCB model of the overall circuit of the designed converter: Front Layer (Open Loop)

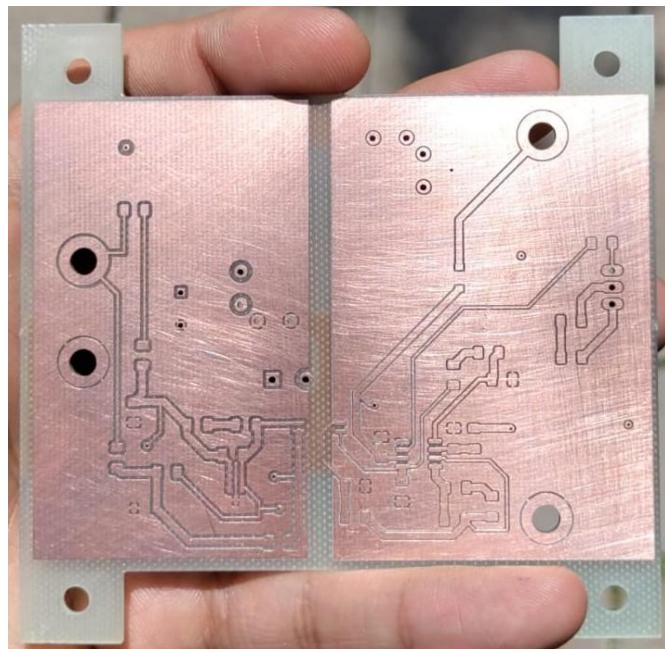


**Figure 37:** KiCAD PCB model of the overall circuit of the designed converter: 3D Model (Front Layer)

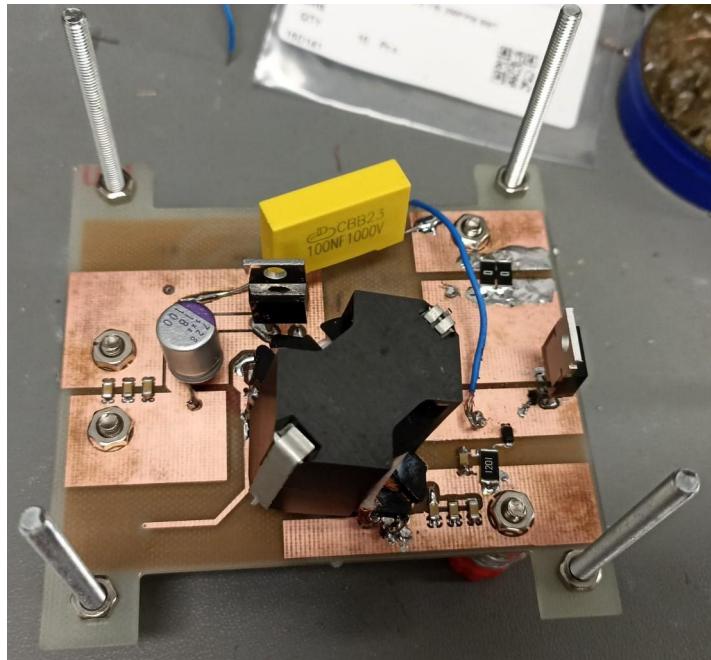
Some of the selected components, such as RM12 transformer, output bulk capacitor, do not have a 3D model for KiCAD. Therefore, only footprints of them are shown in the 3D model.



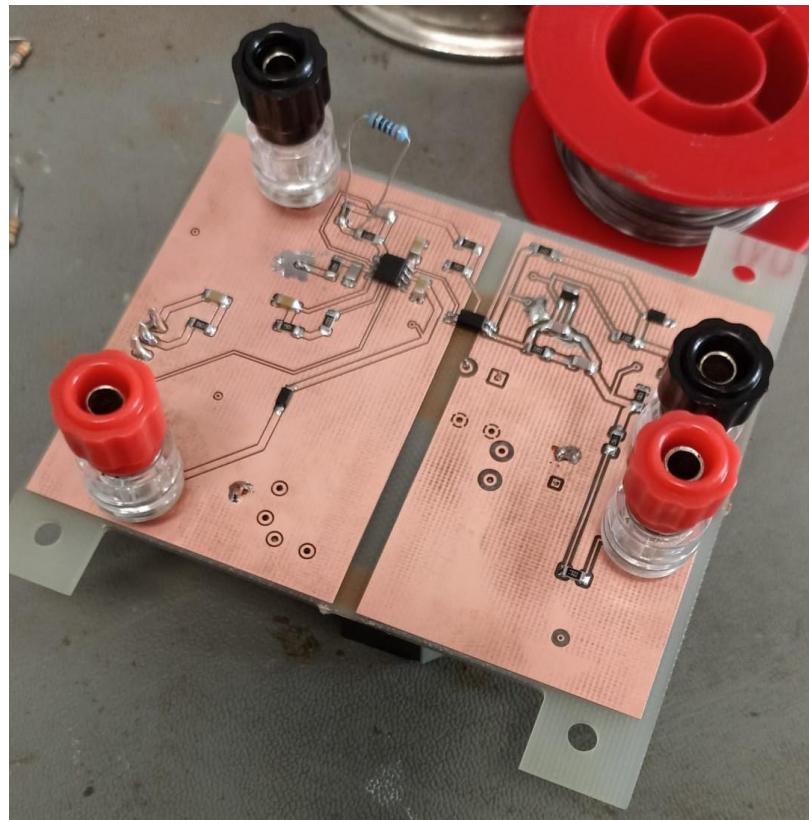
**Figure 38:** Real view of the PCB: Front Layer (Open Loop)



**Figure 39:** Real view of the PCB: Back Layer (Feedback)



**Figure 40:** Real view of the PCB: Front Layer (Soldered and Modified)



**Figure 41:** Real view of the PCB: Back Layer (Soldered and unmodified)

In Figure 41 (Real view of the PCB: Front Layer (Soldered and Modified) ), blue cable was soldered to monitor the source terminal of the MOSFET.

## 11. Why could we not complete it?

At the very beginning of the test procedure, the closed loop operation was achieved in an unstable manner.

Some videos of this operation have been uploaded. They can be viewed by clicking [here](#) & [here](#).

Also, the triangular wave was obtained. In figure 42 triangular wave can be seen.

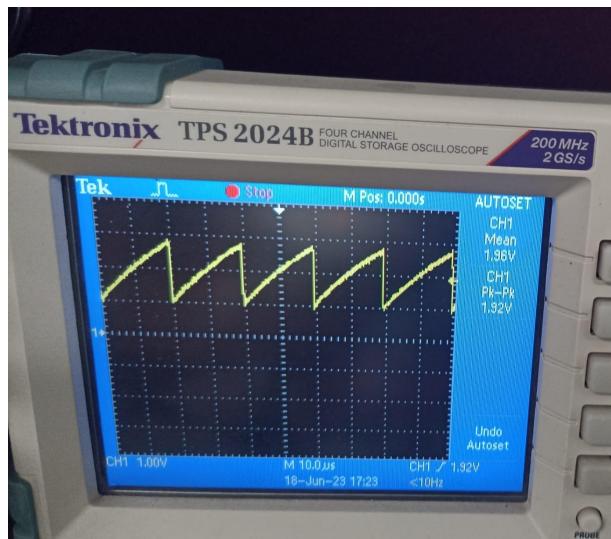


Figure 42: Triangular Wave

Possible reasons we thought that might cause this malfunction and applied solutions are given below.

- Damage on controller (i.e. its internal gate driver or  $V_{REF}$  pin could be damaged.)
  - The controller was changed (with the same package).
- Damage on opto-coupler.
  - The opto-coupler was changed several times (with the same and different packages.)
- Damage on shunt resistor. (Inability to test them due to its low resistivity)
  - The shunt resistors are changed with the one with higher power ratings

Those changes did not work. Moreover, due to the lack of a standalone gate driver or microcontroller, the open loop operation could not be tested. However, achievement of unstable operation verifies that the open-loop system functioned. Therefore, the source of malfunctionality might come from PCB design. The designed PCB was really small at first. It was intended to be designed such that it would have been the smallest solution that enables designers to make hand soldering. However, packages that were chosen for that purpose were even smaller than we had thought. Due to the small size, soldering and implementing was very difficult, there might be some clearance, creepage problems, some connection lines might be shorted to the wrong connection lines or some connections were shorted while soldering them and examining the circuit was difficult due to the small size. Therefore, analyzing and making modifications on that PCB was time consuming and hard to realize. Although

the connections, paths and pads were checked many times and could not find the problem that is the root of the malfunctionality.

## 12. Conclusion

In conclusion, the project aimed to design and implement an isolated DC-DC power supply. The report discussed the topology selection, design decisions, component selection, magnetic design, snubber and closed loop designs, and finally why the circuit did not work. The process of pcb design was also outlined, and test results of simulations were presented. Overall, the project did not work but we learned a lot from this project. We learned from our mistakes.

## 13. APPENDIX 1 : References

<https://keysan.me/ee464/>

<https://www.mouser.com/pdfdocs/2-8.pdf>

<https://www.onsemi.jp/pub/collateral/an-4137jp.pdf>

<https://www.ti.com/lit/ds/symlink/uc3843.pdf?ts=1687868342825&r>

[http://www.ridleyengineering.com/images/phocadownload/12\\_%20flyback\\_snubber\\_design.pdf](http://www.ridleyengineering.com/images/phocadownload/12_%20flyback_snubber_design.pdf)