ELECTRICAL & ELECTRONICS ENGINEERING DEPARTMENT

STATIC POWER CONVERSION II

FLYBACK CONVERTER DESIGN: SIMULATION RESULTS

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1. Introduction

Isolated DC/DC converters have several benefits over non-isolated converters. The main reason for the isolation is safety. Flyback converter is one of the isolated DC/DC converter topologies. This report focuses on how to determine open-loop parameters for the 48W flyback converter and verification of the determined parameters.

2. Open-Loop Parameters Selection

Flyback converter has the following gain relation.

$$V_o = \frac{D}{1-D} * \frac{N_S}{N_P} * V_{in}$$

According to the gain relation of the converter,

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} * \frac{N_S}{N_P} \quad -> \quad 4 \geq \frac{D}{1-D} * \frac{N_S}{N_P} \geq 2.67$$

Moreover, duty cycle is desired to be less than or equal to 0.5. Thus, turn ratio of the transformer is chosen as $n = \frac{N_S}{N_P} = 4$ and the switching frequency of the converter to be designed as 50 kHz.

Given turn ratio and frequency, the following parameters can be computed as follows.

$$V_{DS,max} = V_{in,max} + V_{Reflected} + V_{DS,max} * 0.3 \ (due\ to\ leakage\ ringing)$$

$$0.7V_{DS,max} = 18 + (48 + 0.7) * 1/4 \ \text{So} \ V_{DS,max} \approx 45\,V$$

$$D_{max} = \frac{V_R}{V_R + V_{in,min}} = 0.505$$

$$P_{in,max} = \frac{P_{out,max}}{eff} \ (assuming\ \%85\ efficiency) = 48/0.85 \approx 56.5\,W$$

$$I_P = \frac{2*P_{in,max}}{V_{in,min}*D_{max}} = \frac{2*56.5}{12*0.505} \approx 18.65\,A$$

$$L_{p,max} = \frac{V_{in,min}*D_{max}}{I_P*f_{sw}} = \frac{12*0.505}{18.65*50000} = 6.5 * 10^{-6} H = 6.5\,\mu H$$

For the core to be used is a ferrite core, with the assumption that B_{Sat} = 0.24 T. B_{Sat} values can be in the range of 0.2 - 0.34 Tesla according to papers. Moreover, we found a core that has 125 mm^2 A_e.

$$N_P = \frac{L_{p,max}*I_P}{B_{Sat}*A_e} = \frac{6.5*10^{-6}*18.65}{0.24*0.000125} \approx 4\,Turns$$

So, we will have 4 turns at the primary side. At this point, one issue about inductance factor of the core chosen arises. The problem is that primary inductance calculated from the given primary turns exceeds the primary inductance limit for the discontinuous conduction mode. However, datasheet contains any information about DC performance of the core. Therefore, it will be assumed that core will have 6.5 μH for 4 primary turns due to its non-provided DC performance. This issue will be investigated before the incorporation of the designed transformer.

$$I_{p,rms} = I_{p,peak} * \sqrt{D_{max}/3} = 18.65 * \sqrt{0.505/3} = 7.65\,A$$

$$I_{s,peak} = I_P * 1/4 = 4.67\,A \qquad I_{s,rms} = 4.67 * \sqrt{\frac{1-0.505}{3}} = 1.9\,A$$

According to the table above we should choose AWG23 for 50 kHz operation. However, it has a 0.729A maximum current capacity, so it can be wired as parallel.

For the primary side, wire should contain at least 11 cables to satisfy current condition. This means there will be 44 AWG23 cable at the window for primary. For Secondary only 3 parallel cables are needed for secondary wire. Thus, there will be 48 cables at the window. Each cable has 0.258 mm^2 area. There will be a total of 92 cables at the window, which makes 24 mm^2 winding area. Since they are wired as parallel, it will probably be higher, 30 mm^2 so to say. Winding area of the coil former is 75 mm^2, which makes fill factor 0.4. It is a reasonable fill factor.

Winding data for RM12/I coil former (DIL)

NUMBER OF SECTIONS	AVERAGE LENGTH OF TURN (mm)	WINDING AREA (mm^2)	WINDING WIDTH (mm)	TYPE NUMBER
1	61	75.0	14.3	CPV-RM12/I-1S-12PD

$$V_{RV,diode} = V_{out} + V_{in,max} * n = 48 + 18 * 4 = 120\,V$$

According to the design guides V_{RRM} should be at least 30% higher than $V_{RV,diode}$ and I_F (average forward current) is at least 50% higher than the $I_{s,rms}$. So V_{RRM} should be around 156 V and I_F should be around 2.9 A

$$C_{out,min} = \frac{I_{out,max} * N_{CP}}{f_{sw} * V_{Ripple}}$$

N_{CP} is the number of internal clock cycles needed by the control loop to reduce the duty cycle from maximum to minimum value. This usually takes around 10-20 switching periods.

$V_{o,ripple}$ will be 1.44V if the ripple voltage is set to be 3% of the average output voltage.

So $C_{out,min} = \frac{1*15}{50000*1.44} = 208.3 * 10^{-6} F = 208.3\,\mu F = 0.21\,mF$

$$I_{c,rms,min} = \sqrt{I_{s,rms}^{\ 2} - I_{Out}^{\ 2}} = 1.62\,A$$

$$ESR_{max} < \frac{\Delta V_{Out}}{I_{s,peak}} = 1.44/1.9 = 0.76$$

Above calculations are decent except the capacitor value which is probably too high it has very low ripple in simulations so we try a different approach

$\Delta V_O/V_O = \frac{D}{RCf} = 0.03 = \frac{0.51}{48*C*50000} => C = 7.1\ \mu F$. To stay in the safe region we shall use 10 µF

Winding data and area product for RM12/I coil former (DIL)

NUMBER OF SECTIONS	AVERAGE LENGTH OF TURN (mm)	WINDING AREA (mm^2)	WINDING WIDTH (mm)	AREA PRODUCT Ae x Aw (mm^4)	TYPE NUMBER
1	61	75.0	14.3	10950	CPV-RM12/I-1S-12PD

In the datasheet of the coil former, it says the average length of a single turn is 61 mm. AWG23 has 66.8 Ω/km resistance, which is $6.68 * 10^{-5}$Ω/m. As cables will be wired as parallel, the total resistance can be calculated as the formula given below.

$$\rho = \frac{Number\ of\ Turns * 61 * 6.68 * 10^{-5}}{Number\ of\ Paralleled\ Cables}$$

$$\rho_p = \frac{4*61*6.68*10^{-5}}{11} = 0.0015\Omega$$

$$\rho_s = \frac{16*61*6.68*10^{-5}}{3} = 0.022\Omega$$

The AWG23 cable has 100% skin depth at the frequency about 50kHz. Therefore, AC resistance will be equal to DC resistance.

$$P_{p,copper} = I_{RMS}^2 * R = 7.65^2 * 0.0015 = 0.09\,W \qquad P_{s,copper} = 1.9^2 * 0.022 = 0.08\,W$$

$$P_{total,copper} = P_{s,copper} + P_{p,copper} = 170\ mWatts$$

$$L_M = \frac{(V_{in,min} * D_{max})^2}{2*Pin*f_{sw}} = \frac{(12*0.505)^2}{2*56.5*50000} = 6.5\ \mu H$$

$$\Delta I_L = \frac{V_{inMin} * D_{max}}{L_M * f_{SW}} = \frac{12*0.505}{6.5*10^{-6}*50000} = 18.65A$$

$$I_{EDC} = \frac{P_{in}}{V_{in,min} * D_{max}} = \frac{56.5}{12*0.505} = 9.32A$$

$$I_{DS,peak} = I_{EDC} + \Delta I/2 = 18.65A$$

$$I_{DS,rms} = \sqrt{(3 * I_{EDC}^2 + (\Delta I/2)^2) * D_{max}/3} = 7.65A$$

$$N_{P,min} = \frac{L_M * I_{Over}}{B_{Sat} * A_e} * 10^6 = 4\ turns$$

The design parameters are verified theoretically.

c) Simulation Results of the Open-Loop Flyback Converter Parasitic Components Not Included

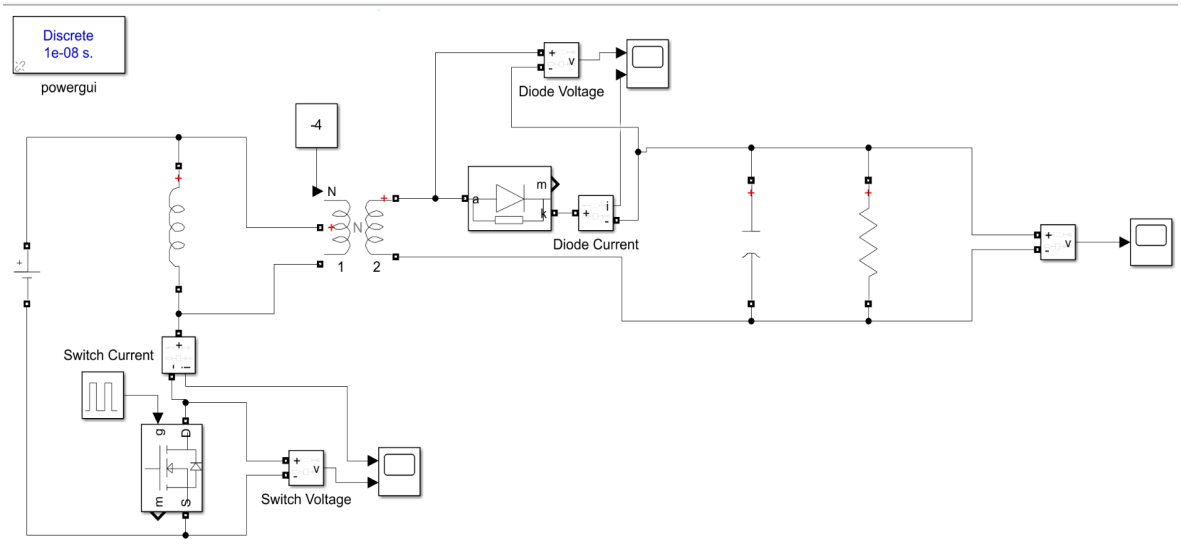

Figure 1 : *Simulation Circuit Constructed in MATLAB Simulink*

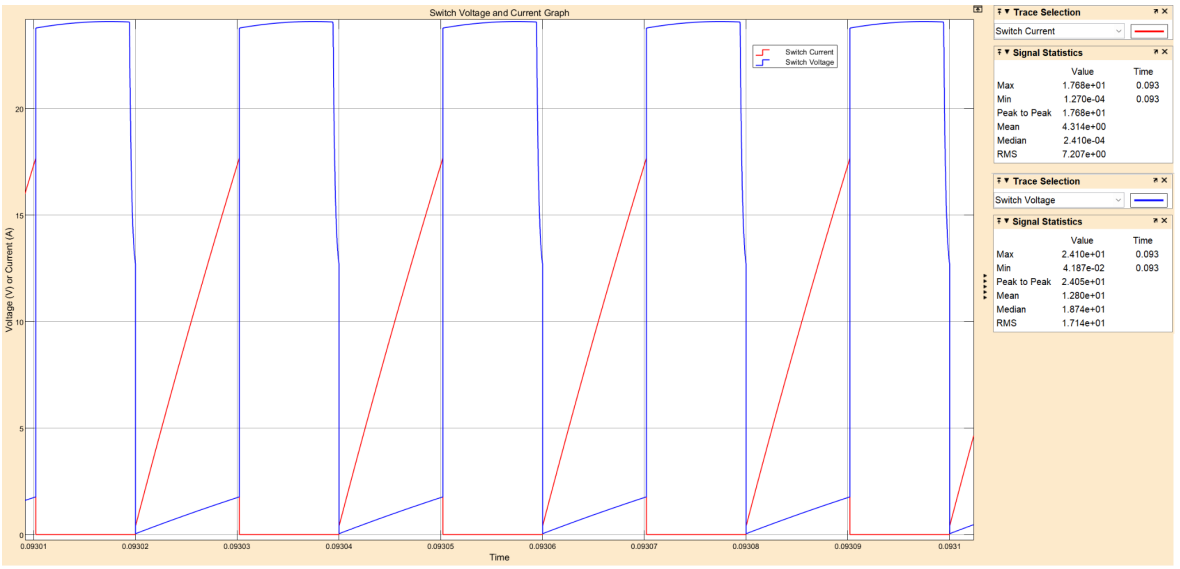

Figure 2 : *Switch Voltage and Current Graph for V_{in}=12V*

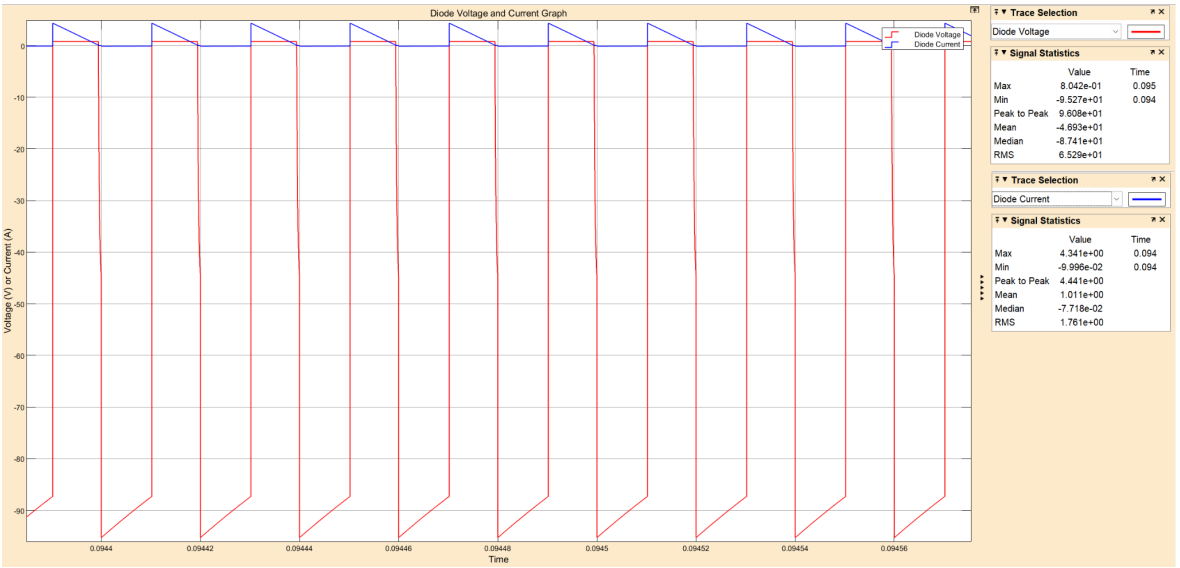

Figure 3 : *Diode Voltage and Current Graph V_{in}=12V*

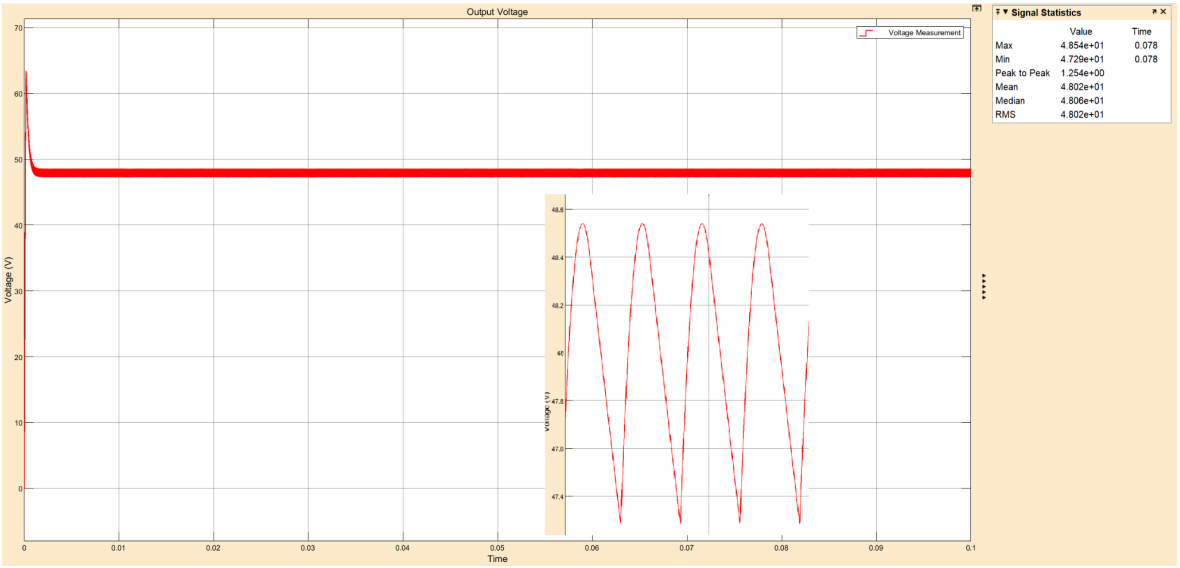

Figure 4 : *Output Voltage Graph V_{in}=12V*

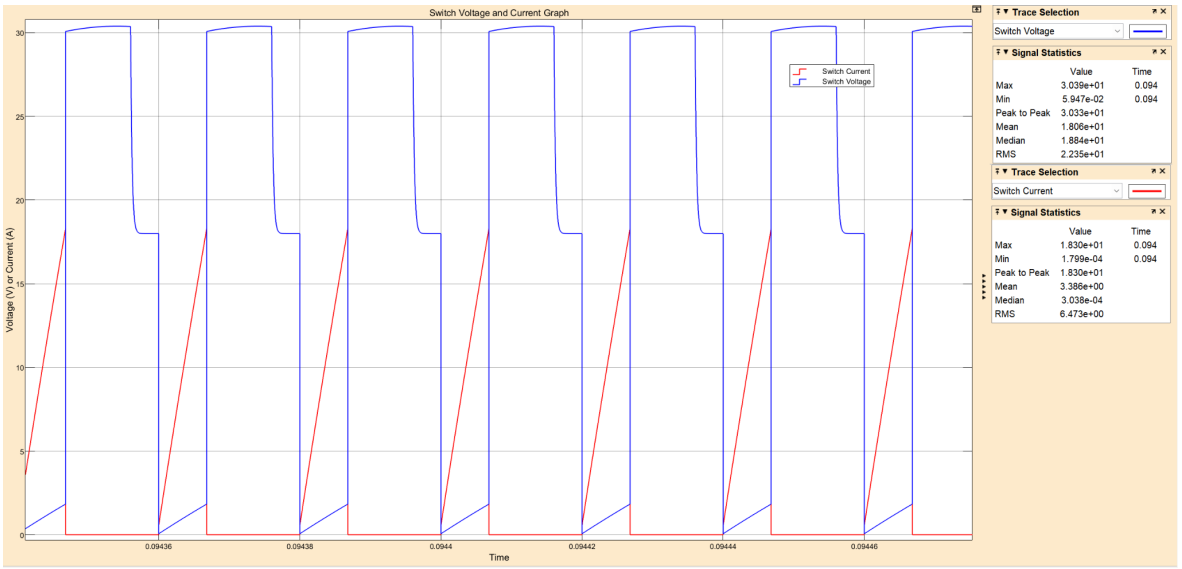

Figure 5 : *Switch Voltage and Current Graph Vin=18V*

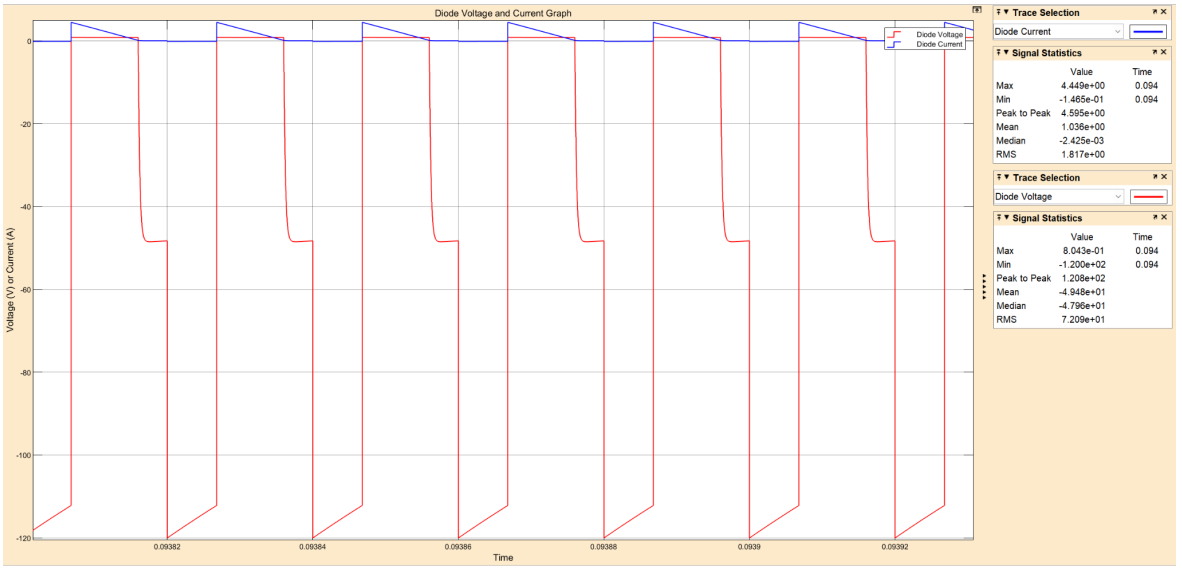

Figure 6 : *Diode Voltage and Current Graph Vin=18V*

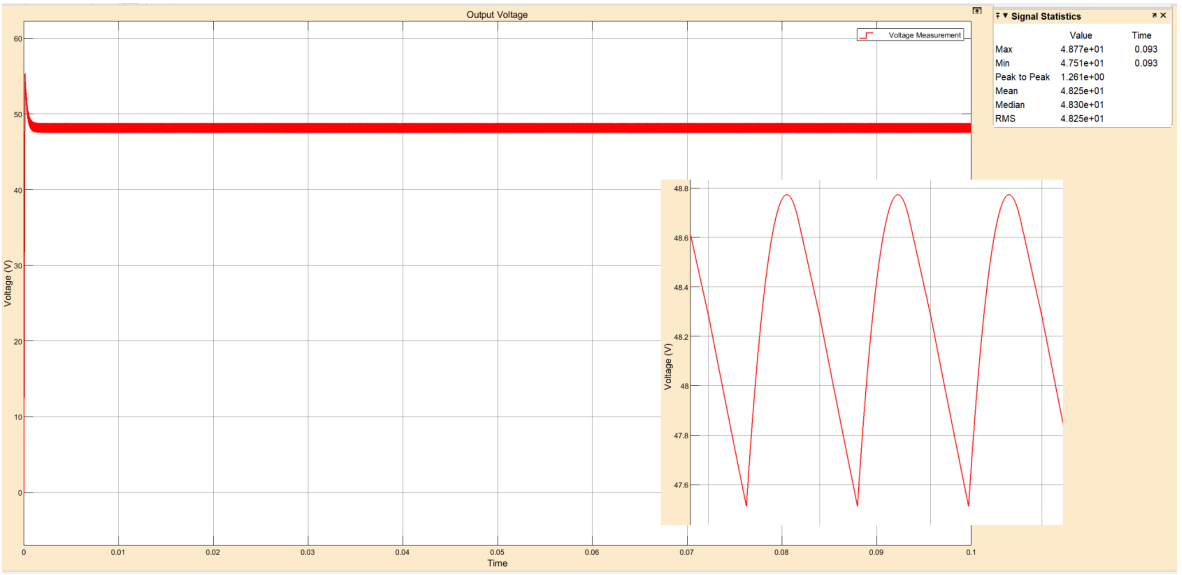

Figure 7 : *Output Voltage Graph Vin=18*

d)

DCM will occur at low Vin if it will occur, so at $V_{In} = 12\,V$ and we have N2/N1 =4, and Lm = 6.5 uH but it was chosen to operate at the vicinity of the boundary according to the design guides so let's assume it is 10 uH for this question to operate in the ccm mode. The other values were ; $f_{SW} = 50\,kHz \quad R = 48\,\Omega \quad D = 0.52 \quad C_{Out} = 10\,uF.$

so $\Delta I_L = \frac{V_{inMin} * D_{max}}{L_M * f_{SW}} = \frac{12*0.52}{10*10^{-6}*50000} = 12.5A \; then \; I_{LAvg} = 6.25\,A$ so at the secondary side 6.25/4= 1.56 A

e)

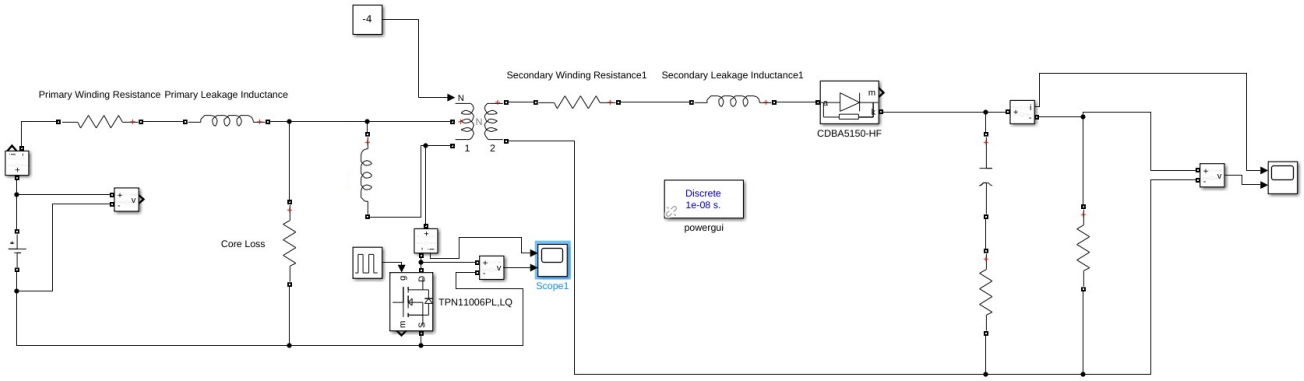

Figure 8: Schematic of the Flyback Converter with Parasitic Components

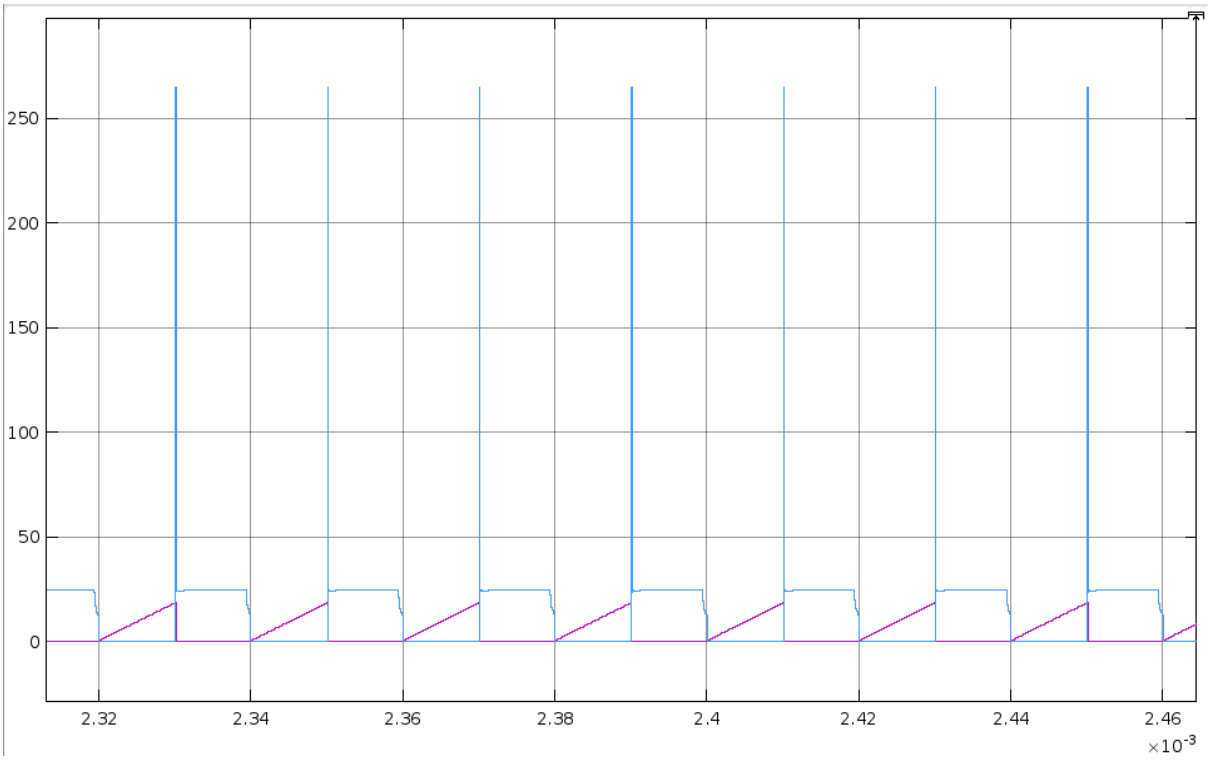

Figure 9 : V & I vs time graph of the Switch

f)

For the MOSFET, TPN11006PL,LQ is chosen as it satisfies both current (18.65A) and voltage (45V) ratings simultaneously. Moreover, it has around 10mΩ resistance.

$$P_{loss,cond.,MOSFET} = I_D^2 * R_{DS} * D = 7.65^2 * 12.3 * 10^{-3} * 0.52 = 0.374W$$

$$P_{loss,sw,,MOSFET} = V_{in} * I_{out} * f_{sw} * (t_{rise} + t_{fall}) = 18 * 1 * 50000 * (2.7 + 3.8) * 10^{-9} = 5.85 * 10^{-3} W$$

For the diode, CDBA5150-HF is chosen as it satisfies both current (1.9A_{avg} & 4.6A_{peak}) and voltage (120V) RATİNGS SİMULTANEOUSLY. Moreover, it has around 0.75V forward voltage drop on it.

$$P_{loss,cond,,diode} = V_f * I_{avg} * (1 - D) = 0.87 * 1.9 * 0.48 = 0.793W$$

Switching losses on the schottky diodes are negligible

For the output capacitor, ESK106M100AE3EA is chosen. According to the datasheet, ESR is calculated with the formula given below.

$$R_{ESR} = \frac{tan\delta}{\omega * C} = 63.66m\Omega$$

Core loss under specific conditions has been provided by the core manufacturer. However, there exists no data at 50kHz and 0.24T. However, there is a direct relation between frequency and core loss. Therefore, the core loss will be approximated as the half of the loss at 100kHz.

Leakage inductance is subjected to the winding method. Therefore, there can not be formulation about leakage inductance. For this converter, leakage inductance will be assumed to be 1% of the magnetizing inductance and the secondary side is assumed to be reflected inductance of primary leakage inductance.

$$L_{l,1} = 0.01 * L_M = \frac{L_{l,2}}{n^2} \quad -> L_{l,2} = L_{l,1} * n^2$$

References

1 https://www.mouser.com/pdfdocs/2-8.pdf
2 https://www.digikey.com/en/products/detail/ferroxcube/CPV-RM12-I-1S-12PD-TZ/7034242
3 https://www.ferroxcube.com/upload/media/product/file/Pr_ds/RM12_ILP.pdf
4 https://tr.farnell.com/awg-donusturme-hesaplayicisi
5 https://www.onsemi.jp/pub/collateral/an-4140jp.pdf