CSE 331 - Computer Organization
Project 4: Hello MIPS

Due date: January 16, Thursday – 17:00

In this project, you will use Altera Quartus II with Verilog. You will the 32-bit MIPS processor. The block that you will design will get no inputs from outside. You will have two memories: Data Memory and Instruction Memory. The instructions must be loaded to the instruction memory and the data must be in data memory. You will support **xor, xori, slt, sltiu, lw, lh, lb, sw, sb, j, jal, jr, beq**, **bne**, **add, sub, and, or, sra, srl, sll, sltu** and **addi, addiu, andi, ori, slti, lui** instructions. Insert two **new instructions** on your own to MIPS. **Find two suitable new instructions on your own, define them and design them.**

You will write test bench and simulate your design for verification. You will write the register and memory contents before and after the execution of instructions using **writememh** in your test bench verilog code. You will initialize memory contents using **readmemh**.

The data memory size will be 128KB whereas the instruction memory size will be 32KB. Remember that addressing for a 128KB memory only requires 17 bits instead of 32 bits in regular MIPS. Update your design accordingly.

(Bonus) Each new instruction other than the two, brings up additional 5pts until 20pts.

6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
R: op	rs	rt	rd	shamt	funct

6 bits	5 bits	5 bits	
I: op	rs	rt	address / immediate

6 bits	
J: op	target address

op: basic operation of the instruction (opcode)
rs: first source operand register
rt: second source operand register
rd: destination operand register
shamt: shift amount
funct: selects the specific variant of the opcode (function code)
address: offset for load/store instructions $(+/-2^{15})$
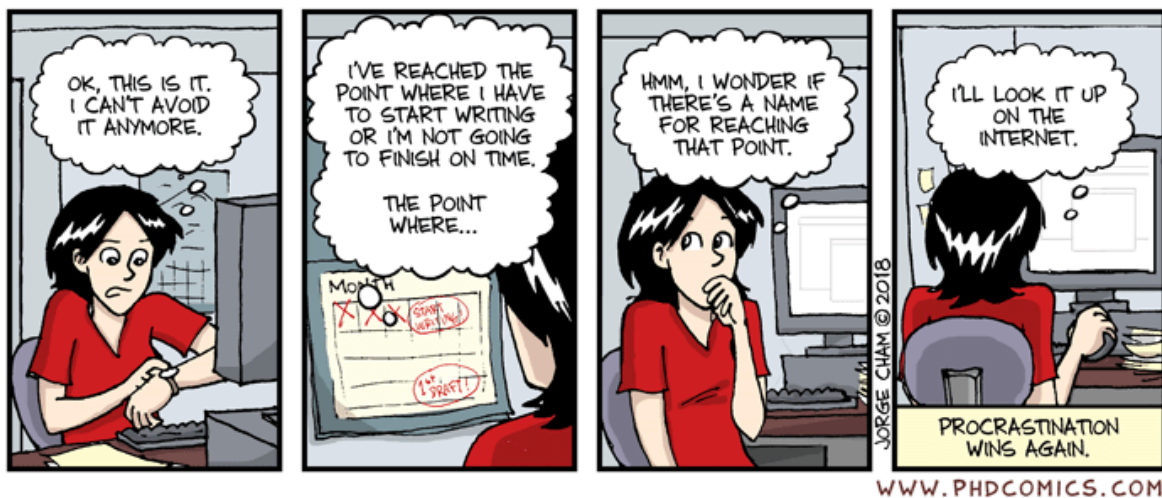immediate: constants for immediate instructions

Please be sure that your design simulates correctly. Designs that are not even simulating can get at most 20 points.

Two additional instructions is a MUST. If you do not design two new instructions designed by you, you will get no credits from the project.

Submit your Altera Project folder as a zip file to Moodle. We will simulate your design using not only your testbench but also our testbench to see whether all instructions are executing correctly or not.

No late submissions even if it is 1 minute. No medical reports. No excuses. No cry. So start early.

Any cheating attempt with the previous years' projects or with your friends or Internet will result in at least -100. No matter you gave or take the code. Protect your code. Do it yourself for your own good.

https://www.youtube.com/watch?v=arj7oStGLkU