Council for Technical Education and Vocational Training
Office of the Controller of Examinations
Sanothimi, Bhaktapur
Regular/Back Exam-2078/2079, Chaitra/Baishakh

Program: Diploma in Computer Engineering	**Full Marks: 80**
Year/ Part: II/II (2018 New)	**Pass Marks: 32**
Subject: Computer Architecture	**Time: 3 hrs.**

Candidates are required to give their answers in their own words as far as practicable. The figures in the margin indicate full marks.

Attempt Any Eight Questions.

1. Define the term fetch and decode. Explain different types of instruction. [4+6]

2. Explain the common bus system with diagram. [10]

3. Describe about instruction cycle. Explain briefly about Micro-program sequencer. [5+5]

4. Differentiate between RISC and CISC architecture. [10]

5. Write down the different types of interrupt. Describe about data manipulation instructions. [6+4]

6. Write down Booth Multiplication Algorithm. [10]

7. Define main memory and auxiliary memory. Discuss briefly on address mapping using pages. [4+6]

8. What is pipelining? Explain the terms delayed load and delayed branch. [2+8]

9. Write short notes on : (Any Two) [2x5=10]
   a) Arithmetic and Instruction pipeline
   b) Signed 2's complement
   c) Control memory

Good Luck !