Objective:

To design sequential circuits.

Syllabus:

UNIT – V: Sequential Logic Circuits Classification of Sequential Circuits, Latch and Flip-Flop, RS- Latch Using NAND and NOR Gates, Truth Tables, RS,JK,T and D flip flops, truth and excitation tables, conversion of flip flops, flip flops with asynchronous inputs (Preset and Clear).

Course Outcomes:

Student will be able to:

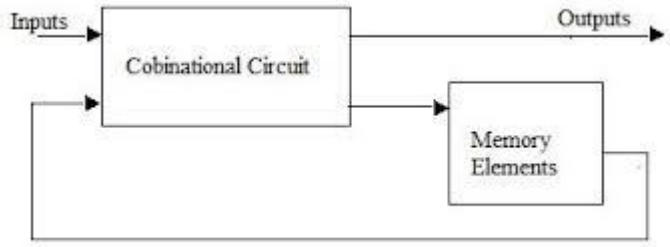
- Understand what a sequential circuit is?
- Understand about various latches.
- Understand various flip-flops.
- Perform conversion between flip-flops.
- Design sequential circuits.

Sequential logic circuits

Introduction

- A sequential circuit is a combinational circuit with some feedback from the outputs.
- In a sequential circuit, the output state depends on both the inputs and the outputs.
- The term “sequential” comes from the fact that the output depends not only on the current states, but on the states immediately preceding.

Now we will introduce a circuit in which the output is fed back to the input, giving the circuit memory.



- A combinational circuit with memory elements forming a feedback path.
- The binary information stored in memory defines the state.
- Outputs are determined by are determined by Inputs and present state and present state.
- Next state is also determined by Inputs and present state.

There are two types of sequential circuits. Their classification depends on the timing of their signals:

- Synchronous sequential circuits
- Asynchronous sequential circuits

Synchronous types use pulsed or level inputs and a clock input to drive the circuit
Asynchronous sequential circuits do not use a clock signal as synchronous circuits do. Instead the circuit is driven by the pulses of the inputs.

The difference between combinational circuits and sequential circuits.

Combinational Circuits	Sequential Circuits
o No Memory	Memory
o No flip-flops,	Flip-flops may be used
o only combinational gates	Combinational gates may be used
o No feedback	Feedback is allowed
o Output for a given set of Inputs is independent of order in which these inputs were changed, after the output stabilizes.	The order of input change is quite important and may produce significant differences in the output.

LATCHE AND FLIP-FLOPS

- In the same way that gates are the building blocks of combinatorial circuits, latches and flip-flops are the building blocks of sequential circuits.
- Latches can be built from gates, and flip-flops can be built from latches.
- The difference between a latch and a flip-flop is that a latch does not have a clock signal, whereas a flip-flop always does.
- Latches are asynchronous, which means that the output changes very soon after the input changes.
- A flip-flop is a synchronous version of the latch.

FLIP-FLOP

- Flip-flop can store either zero or one permanently until a change is made in the inputs. Hence flip-flop would work as 1-bit memory cell.
- The most important and basic type of a sequential circuit is a FLIP-FLOP.
  There are 4 kinds of Flip-Flops namely—
  - S-R flip-flop(the basic flip-flop)
  - D flip-flop(Delay flip-flop)
  - T flip-flop
  - JK flip-flop

S R flip-flop

The inputs of an S-R flip-flop are labeled R (reset) and S (set) and the outputs are labeled as Q and Q'.

D flip-flop

A D flip-flop has only one input (D) and two outputs (Q and Q'). In a D flip-flop, the output Q sets its value similar to the value of the input D.

T flip-flop

A T flip-flop has only one input (T) and two outputs (Q and Q'). In a T flip-flop, the output Q toggles its value depending on the value of the input T.

J-K Flip-Flop

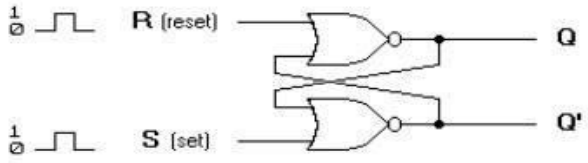
The J-K flip-flop is the most versatile of the basic flip-flops. It has two inputs, traditionally labeled J and K. If J and K are different then the output Q takes the value of J at the next clock edge.

SR flip-flop using NAND-NOR gates:

The SET-RESET flip flop is designed with the help of two NOR gates and also two NAND gates. These flip flops are also called S-R Latch.

S-R Flip Flop using NOR Gate

The design of such a flip flop includes two inputs, called the SET [S] and RESET [R]. There are also two outputs, Q and Q'. The diagram and truth table is shown below.



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after S=1, R=0)
0	1	0	1	
0	0	0	1	(after S=0, R=1)
1	1	0	0	

(b) Truth table

Basic flip-flop circuit with NOR gates

The flip flop has mainly four states. They are

S=1, R=0—Q=1, Q'=0

This state is also called the SET state.

S=0, R=1—Q=0, Q'=1

This state is known as the RESET state.

In both the states you can see that the outputs are just compliments of each other and that the value of Q follows the value of S.

S=0, R=0—Q & Q' = Remember

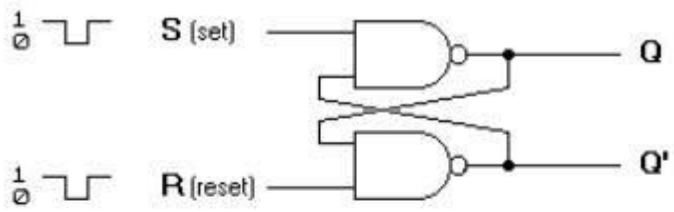
If both the values of S and R are switched to 0, then the circuit remembers the value of S and R in their previous state.

S=1, R=1—Q=0, Q'=0 [Invalid]

This is an invalid state because the values of both Q and Q' are 0. They are supposed to be compliments of each other. Normally, this state must be avoided.

S-R Flip Flop using NAND Gate

The circuit of the S-R flip flop using NAND Gate and its truth table is shown below.



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after S=1, R=0)
0	1	1	0	
1	1	1	0	(after S=0, R=1)
0	0	1	1	

(b) Truth table

Basic flip-flop circuit with NAND gates

Like the NOR Gate S-R flip flop, this one also has four states. They are

S=1, R=0—Q=0, Q'=1
This state is also called the SET state.

S=0, R=1—Q=1, Q'=0
This state is known as the RESET state.
In both the states the outputs are just compliments of each other and that the value of Q follows the compliment value of S.

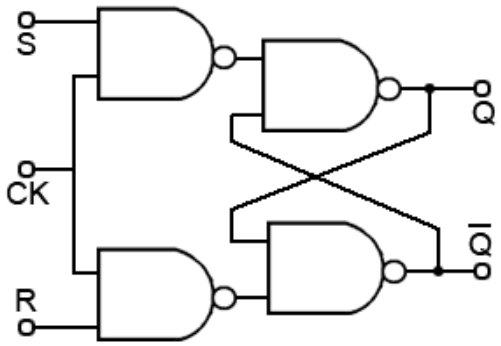
S=0, R=0—Q=1, & Q' =1 [Invalid]
If both the values of S and R are switched to 0 it is an invalid state because the values of both Q and Q' are 1. They are supposed to be compliments of each other. Normally, this state must be avoided.

S=1, R=1—Q & Q'= Remember
If both the values of S and R are switched to 1, then the circuit remembers the value of S and R in their previous state.

The Clocked SR Flip-flop

Figure below shows a useful variation on the basic SR flip-flop, the clocked SR flip-flop. By adding two extra NAND gates, the timing of the output changeover after a change of logic states

at S and R can be controlled by applying a logic 1 pulse to the clock (CK) input. Note that the inputs are now labeled S and R indicating that the inputs are now 'high activated'. This is because the two extra NAND gates are disabled while the CK input is low, therefore the outputs are completely isolated from the inputs and so retain any previous logic state, but when the CK input is high (during a clock pulse) the input NAND gates act as inverters.



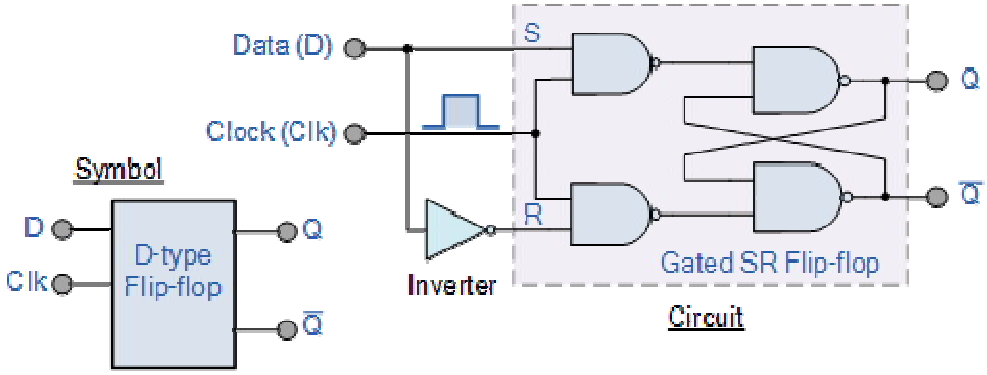
Truth Table for this Set-Reset Function

State	S	R	Q	Q	Description
Set	1	0	0	1	Set Q » 1
	1	1	0	1	no change
Reset	0	1	1	0	Reset Q » 0
	1	1	1	0	no change
Invalid	0	0	1	1	Invalid Condition

The main advantage of the CK input is that the output of this flip-flop can now be synchronized with many other circuits or devices that share the same clock. This arrangement could be used for a basic memory location by, for example, applying different logic states to a range of 8 flip-flops, and then applying a clock pulse to CK to cause the circuit to store a byte of data.

D Flip Flop

The circuit diagram and truth table is given below.



Truth Table for the D-type Flip Flop

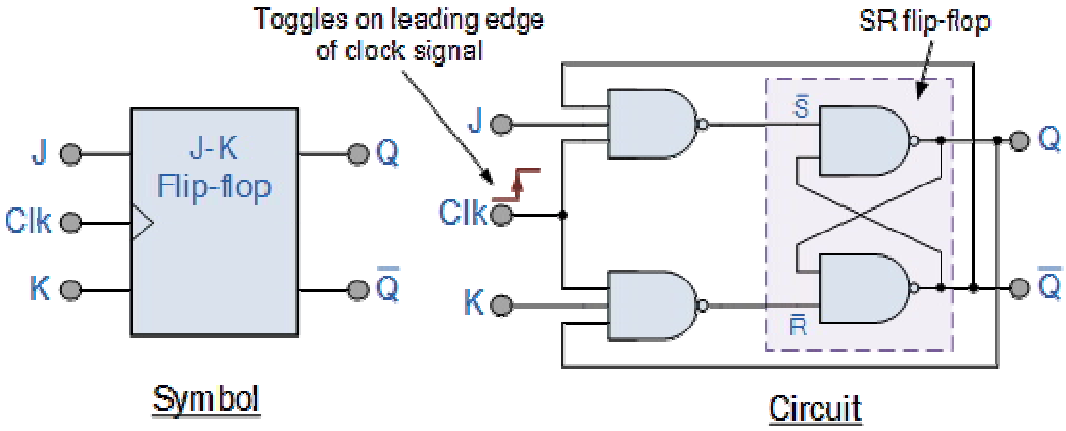
Clk	D	Q	Q	Description
↓ » 0	X	Q	Q	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

- D flip flop is actually a slight modification of the above explained clocked SR flip-flop.
- The D input is connected to the S input and the complement of the D input is connected to the R input.

- The D input is passed on to the flip flop when the value of CP is '1'. When CP is HIGH, the flip flop moves to the SET state. If it is '0', the flip flop switches to the CLEAR state.

J-K Flip Flop

The circuit diagram and truth-table of a J-K flip flop is shown below.



The Truth Table for the JK Function

	Input		Output		Description
	J	K	Q	Q	
same as for the SR Latch	0	0	0	0	Memory no change
	0	0	0	1	
	0	1	1	0	Reset Q » 0

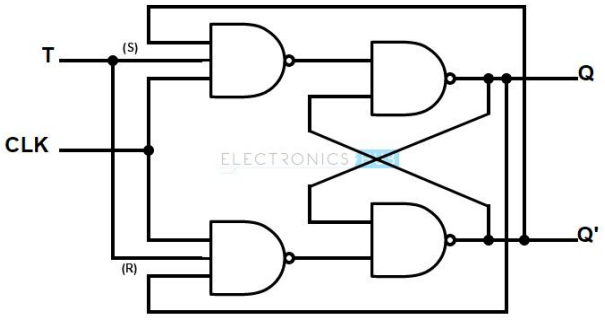
	0	1	0	1	
	1	0	0	1	Set Q » 1
	1	0	1	0	
toggle action	1	1	0	1	Toggle
	1	1	1	0	

A J-K flip flop can also be defined as a modification of the S-R flip flop. The only difference is that the intermediate state is more refined and precise than that of a S-R flip flop.

- The behavior of inputs J and K is same as the S and R inputs of the S-R flip flop. The letter J stands for SET and the letter K stands for CLEAR.
- When both the inputs J and K have a HIGH state, the flip-flop switch to the complement state. So, for a value of Q = 1, it switches to Q=0 and for a value of Q = 0, it switches to Q=1.
- The circuit includes two 3-input AND gates. The output Q of the flip flop is returned back as a feedback to the input of the AND along with other inputs like K and clock pulse [CP].
- So, if the value of CP is '1', the flip flop gets a CLEAR signal and with the condition that the value of Q was earlier 1.
- Similarly output Q' of the flip flop is given as a feedback to the input of the AND along with other inputs like J and clock pulse [CP].
- So the output becomes SET when the value of CP is 1 only if the value of Q' was earlier 1.

T Flip Flop

- This is a much simpler version of the J-K flip flop. Both the J and K inputs are connected together and thus are also called a single input J-K flip flop.
- When clock pulse is given to the flip flop, the output begins to toggle.



Inputs		Outputs		Comments
E	T	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	Q_n	$\overline{Q}_n$	No change
1	1	$\overline{Q}_n$	Q_n	Toggle

S.N.	Condition	Operation
1	**T = 0, J = K = 0**	The output Q and Q bar won't change
2	**T = 1, J = K = 1**	Output will toggle corresponding to every leading edge of clock signal.

Characteristic And Excitation Tables Of SR,D,JK, And T, Flip-Flops:

- A characterisitic table has the control input (D or T) as the first column, the current state as the middle column, and the next state as the last column.
- An excitation table has the current state as the first column, the next state as the second column, and the control bit as the third column.

EXCITATION TABLE OF RS Flip-flop:

The truth table of the RS flip-flops is as:

		Present		New	
R	S	Q_n	Q_n (bar)	Q	Q (bar)
0	0	1	0	1	0
0	1	1	0	1	0
1	0	1	0	0	1
1	1	0	1	INVALID	
0	0	0	1	0	1
0	1	0	1	1	0
1	0	0	1	0	1
1	1	0	1	INVALID	

Now to write the excitation table of this flip-flop we first write the various output changes possible as:

Q_n	Q_{n+1}	S	R
0	0		
0	1		
1	0		
1	1		

Now we can see from that truth table that to change **output from 0 to 0**, we can keep inputs S, R as 0, 0 or 0, 1 and we can write both the combinations as 0, X which means we just need to keep S=0 and R can have either of two possible values.
Similarly we can note that for output change from 0 to 1, we keep inputs at S=1, R=0.Similarly we can find the other cases and we get the table as:

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Similarly we can find out the excitation tables for other kind of flip-flops as shown next:
D Flip-flop: The excitation table of D flip-flop is as:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

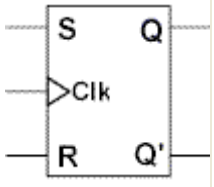
JK Flip-flop: The excitation table of JK flip-flop is as:

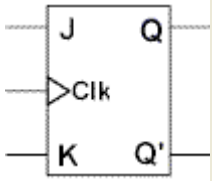
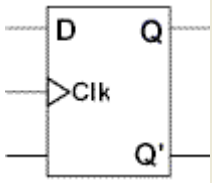
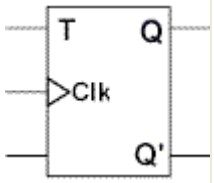
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

For output change from 0 to 1 we can either keep inputs J, K as 1, 0 or we can make use of toggle input combination J=1, K=1 to get compliment of the output.
Similarly the other case
T Flip-flop: The excitation table of T flip-flop is as:

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Summary Of Flip-Flops:

FLIP-FLOP NAME	FLIP-FLOP SYMBOL	CHARACTERISTIC TABLE	CHARACTERISTIC EQUATION	EXCITATION TABLE
SR		**S** **R** **Q(next)** 0 0 Q 0 1 0 1 0 1 1 1 ?	**Q(next) = S + R'Q** **SR = 0**	**Q** **Q(next)** **S** **R** 0 0 0 X 0 1 1 0 1 0 0 1 1 1 X 0

<table>
<tr>
<td>JK</td>
<td> 
</td>
<td>
<table>
<tr><th>J</th><th>K</th><th>Q(next)</th></tr>
<tr><td>0</td><td>0</td><td>Q</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>Q'</td></tr>
</table>
</td>
<td>Q(next) = JQ' + K'Q</td>
<td>
<table>
<tr><th>Q</th><th>Q(next)</th><th>J</th><th>K</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>X</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>X</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>0</td></tr>
</table>
</td>
</tr>
<tr>
<td>D</td>
<td> 
</td>
<td>
<table>
<tr><th>D</th><th>Q(next)</th></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
</table>
</td>
<td>Q(next) = D</td>
<td>
<table>
<tr><th>Q</th><th>Q(next)</th><th>D</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>
</td>
</tr>
<tr>
<td>T</td>
<td> 
</td>
<td>
<table>
<tr><th>T</th><th>Q(next)</th></tr>
<tr><td>0</td><td>Q</td></tr>
<tr><td>1</td><td>Q'</td></tr>
</table>
</td>
<td>Q(next) = TQ' + T'Q</td>
<td>
<table>
<tr><th>Q</th><th>Q(next)</th><th>T</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td>
</tr>
</table>

Conversions Of Flip-Flops:

- A Flip – flop is an electronic device which is having two stable states and a feedback path which is used to store 1 – bit of information by using the clock signal as input.
- Latches are also used to do the same task except that they do not use a clock signal.
- Hence to say it simply, “Flip – flops are clocked latches”. They are used to store only 1 – bit of information and it can remain in the same state until the clock signal affects the state of the input.

There are four types of flip – flops

- SR flip – flop
- D flip – flop
- JK flip – flop
- T flip – flop

- JK flip – flops and D flip – flops are the most widely used flip – flops. And so their availability in the form of integrated circuits (IC’s) is abundant. Numerous varieties of JK flip – flop and D flip – flop are available in the semiconductor market.

- The less popular SR flip – flop and T flip – flop are not available in the market as integrated circuits (IC's) (even though a very few number of SR flip – flops are available as IC's, they are not frequently used).

  There might be a situation where the less popular flip – flops are required in order to implement a logic circuit.
- In order use the less popular flip – flops, we will convert one type of flip – flop into another. Some of the most common flip – flop conversions are
  - SR Flip – flop to JK Flip – flop
  - SR Flip – flop to D Flip – flop
  - SR Flip – flop to T Flip – flop
  - JK Flip – flop to SR Flip – flop
  - JK Flip – flop to D Flip – flop
  - JK Flip – flop to T Flip – flop
  - D Flip – flop to SR Flip – flop
  - D Flip – flop to JK Flip – flop
  - D Flip – flop to T Flip – flop

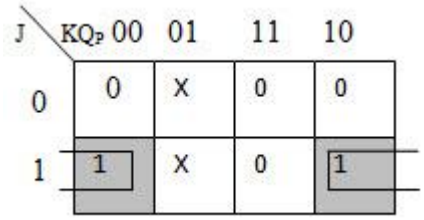
SR Flip – flop to other Flip – flops

SR Flip – flop to JK Flip – flop

- Here we are required to convert the SR flip – flop to JK flip – flop. So first we design a combinational circuit with J and K as its inputs and we connect its output to the input of our available flip flop i.e. an SR flip – flop. So its outputs are same as that of JK flip – flop.
- Let's write a truth table for the two inputs, J and K. For two inputs along with the Q_P, we get 8 possible combinations in truth table.
- Consider that when the two inputs are applied, Q_P is the present state and Q_N is the next state. For every combination of J, K ,Q_P , we find the corresponding QN state.
- Here Q_N will give the state values that to which the output of the JK flip – flop will jump after the present state, on applying the inputs.
- Now we write all the combinations of S and R in the truth table to get each Q_N value from corresponding Q_P. Hence these are the values of S and R that are used to change the state of flip flop from Q_P to Q_N.
- The conversion table from SR flip – flop to JK flip – flop is shown below.

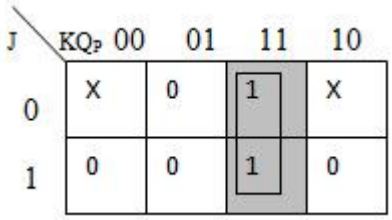
JK Inputs		Outputs		SR Inputs	
J	K	Q_P	Q_N	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

In order to deduce the Boolean equations of S and R in terms of J and K, we use Karnaugh maps from the above table.
The K – map for S is shown below.

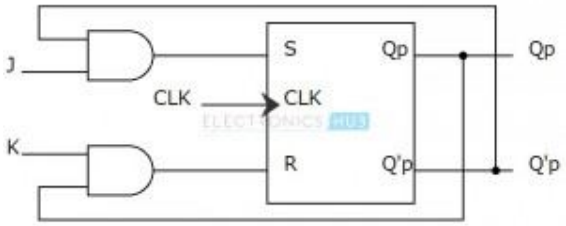


The Boolean equation for S is S = JQ'$_P$.

The K – map for R is shown below.



- The Boolean equation for R is R = KQ$_P$.
- The Boolean equations of S and R in terms of J, K and QP are: S = JQ'$_P$ and R = KQ$_P$
- The logic diagram of JK flip – flop implemented from SR flip – flop is shown below. Here J and K are external inputs to the circuit. S and R are the outputs of the designed combinational outputs.



SR Flip – flop to D Flip – flop

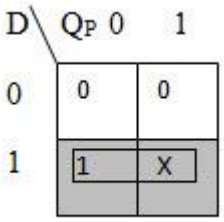
Converting the SR flip – flop to D flip – flop involves connecting the Data input (D) to the SR flip – flop.

Here the Data input is connected directly to the S input and the inverted D input (using a NOT gate) is connected to R input. The same can be derived from truth table and corresponding K – maps. S and R are the inputs of the flip – flop while Q_P and Q_P' are the present state and its complementary outputs of the flip – flop. We should design a combinational circuit such that its input is D and outputs are S and R. Outputs from the combinational circuit S and R are connected as inputs to the SR flip – flop.

The truth table for conversion of SR flip – flop to D flip – flop is shown below. The truth table is drawn for the D input and Q_P output to find the corresponding Q_N output.

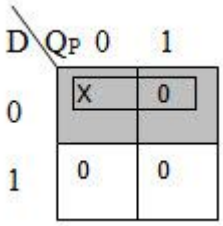
D Input	**Outputs**		**SR Inputs**	
D	**Q_P**	**Q_N**	**S**	**R**
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

The K – map to derive the Boolean equation of S in terms of D is shown below.



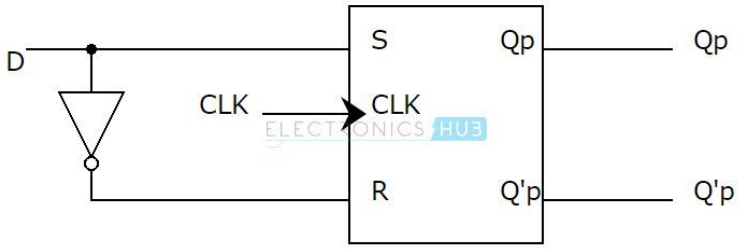
The Boolean equation of S is S = D.

The K – map to derive the Boolean equation of R in terms of D is shown below.



The Boolean equation of R is R = D'.

The Boolean equation for S and R in terms of D are: S = D and R = D'. The logic diagram of implementation of D flip – flop from SR flip – flop is shown below.



SR Flip – flop to T Flip – flop

The combinational circuit required in order to convert an SR flip – flop to T flip – flop can be constructed from the truth table. The input to the combinational circuit is T (Toggle input) and the outputs of the combinational circuit are S and R. Here S and R are the inputs of the actual flip – flop. The output and the complement output of the flip – flop are Q_P and Q'_P. The truth table consists of combinations of T and Q_P in order to get Q_N where Q_N is the next state output of the flip – flop. The combinations of S and R which results in Q_N are also tabulated in the same table. The conversion table is shown below.

T Input	Outputs		SR Inputs	
T	Q_P	Q_N	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

The K – map to derive the Boolean equation of S in terms of T and Q_P is shown below.

T \ Q_P	0	1
0	0	X
1	1	0

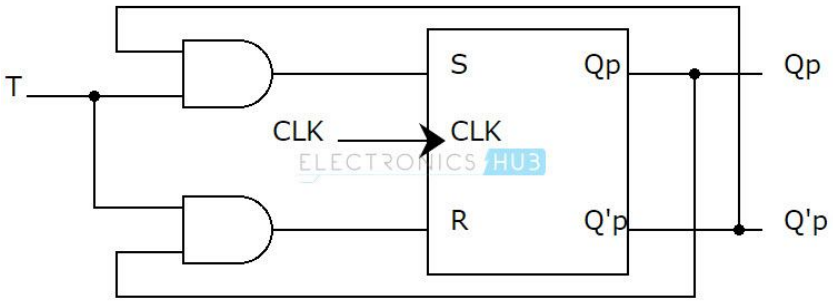
The Boolean equation of S is $S = TQ'_P$.

The K – map to derive the Boolean equation of R in terms of T and Q_P is shown below.

T \ Q_P	0	1
0	X	0
1	0	1

The Boolean equation for R is $R = TQ_P$.

The Boolean equations of S and R are: $S = TQ'_P$ and $R = TQ_P$. The logic circuit for the implementation of T flip – flop from SR flip – flop is shown below.



JK Flip – flop to other Flip – flops

JK Flip – flop to SR Flip – flop

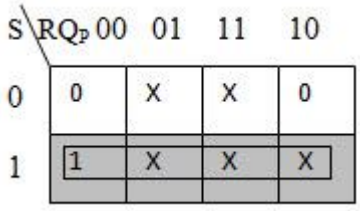
To convert the JK flip – flop into SR flip – flop, we design a combinational circuit with S and R as its inputs and J and K as its outputs. Here J and K are the inputs of actual flip – flop. So for making this conversion, we should obtain the J &amp, K values in terms of S, R and Q_P. Consider that when the two inputs S and R are applied, Q_P is the present state output and $Q_N$is the next state output. For each combination of S, R and Q_P, we find the corresponding $Q_N$state. Now, we prepare a truth table for the possible combination of the inputs S, R and Q_P. We can make 8 possible combinations for the two S and R inputs along with Q_P. For each combination of S and R inputs and Q_P we find the corresponding value of Q_N. Now we write all the values of J and K in the truth table to get each Q_N value from corresponding Q_P.

In SR flip – flop, when the 2 inputs are high i.e. S = 1 & R = 1, then the flip – flop will be in undefined state or forbidden state. So for this combination we consider the J, K inputs as 'Don't cares'.

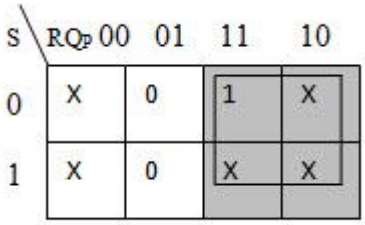
The conversion table for implementing SR flip – flop from JK flip – flop is shown below.

SR Inputs		Outputs		JK Inputs	
S	**R**	**Q_P**	**Q_N**	**J**	**K**
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	Invalid	Invalid	Don't Care	Don't Care
1	1	Invalid	Invalid	Don't Care	Don't Care

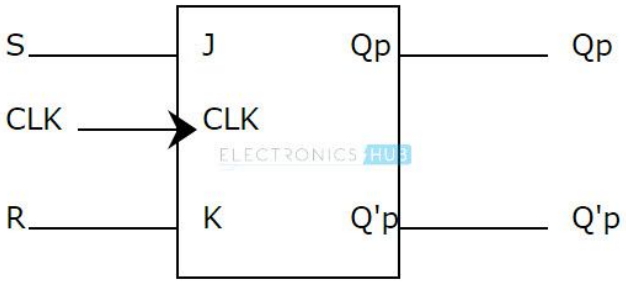
The K – map for J is shown below.



The Boolean equation for J is J = S.
The K – map for K is shown below.



The Boolean equation for K is K = R.
The Boolean equations for J and K in terms of S and R are: J = S and K = R. Hence, there is no requirement of any additional combinational circuit as S and R inputs are same as J and K inputs.
The logic circuit of implementing SR flip – flop from JK flip – flop is shown below.

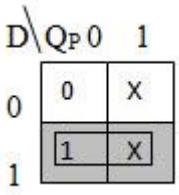


JK Flip – flop to D Flip – flop

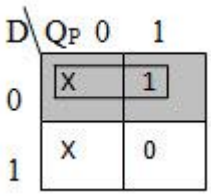
Converting the JK flip – flop to D flip – flop, involves in connecting the Data input (D) to the JK flip – flop through a combinational circuit. Here the Data input is connected directly to the J input and the inverted D input (using a NOT gate) is connected to K input.
The design of the combinational circuit should be in such a way that D is its input and J & K are its outputs. The outputs of the combinational circuit J & K are connected as inputs to the flip – flop. QP is the present state output of the flip – flop. Q'P is its complementary and QN is the next state output. The truth table for converting JK flip – flop to D flip – flop is shown below.

D Input	Outputs		JK Inputs	
D	Q_P	Q_N	J	K
0	0	0	X	X
0	1	0	0	1
1	0	1	1	X
1	1	0	X	0

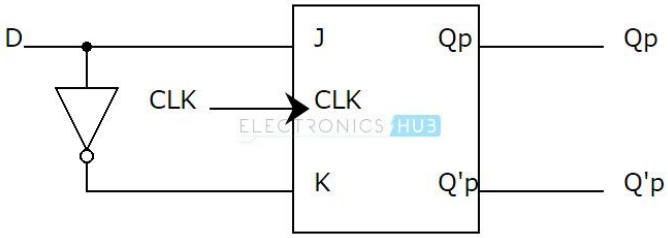
The K – maps in order to solve for J and K in terms of D and QP are shown below.
K – Map for J.



The Boolean equation for J is J = D.
K – Map for K.



The Boolean equation for K is K = D'.
The Boolean equations for J and K are J = D and K = D'. The logic diagram that represents the implementation of D flip – flop from JK flip – flop is shown below.

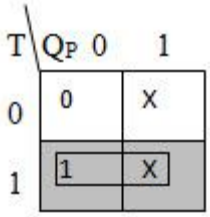


JK Flip – flop to T Flip – flop

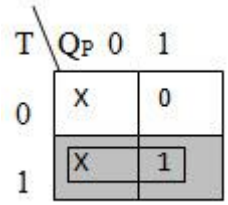
Converting the JK flip – flop to T flip flop, involves in connecting the Toggle input (T) directly to the J and K inputs. So toggle (T) will be the external input to the combinational circuit. Its output is connected to the Input of actual flip – flop (JK flip – flop).
We prepare a truth table by considering 4 possible combinations of the Toggle input (T) along with Q_P. Q_P and Q_P' are the present state output and its complement output of the flip – flop. Q_N is the next state output. The truth table is drawn for the T input and Q_P output to find the corresponding Q_N output.
The truth table is shown below.

T Input	Outputs		JK Inputs	
T	Q_P	Q_N	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

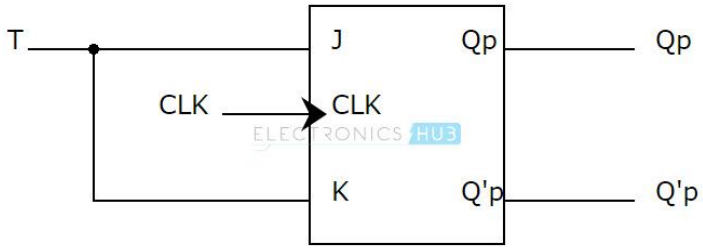
The K – map for solving the Boolean equations of J in terms of T and Q_P is shown below.



The Boolean equation for J is J = T.
The K – map for solving the Boolean equations of K in terms of T and Q_P is shown below



The Boolean equation for K is K = T.
The logic circuit for converting JK flip – flop to T flip – flop is shown below.



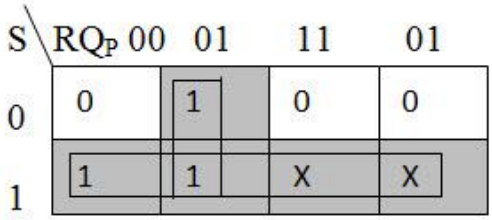
D Flip – flop to other Flip – flops

D Flip – flop to SR Flip – flop

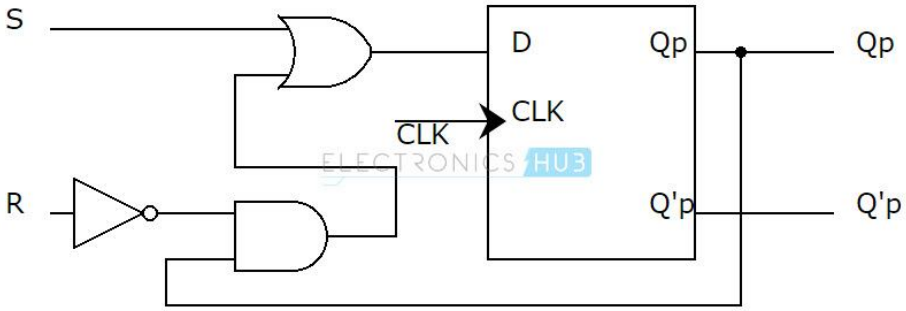
To convert the D flip – flop into SR flip – flop, a combinational circuit should be constructed where its inputs are S and R and its output is D. Here Data (D) is the input of actual flip – flop. The truth table is drawn with the 8 possible combinations of the two inputs S & R and Q_P. $Q_P$and Q_P' are the present state and its complement outputs of the flip – flop.
When the two inputs of SR flip – flop are high i.e. S = 1 and R = 1, then the Q_P value is invalid and hence the Data (D) inputs for the corresponding Q_P's are considered as 'Don't cares'.
The truth table for S, R and Q_P in order to get Q_N is shown below. It also consists of D inputs in order to get the same Q_N.

SR Inputs		Outputs		D Input
S	R	Q_P	Q_N	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	Invalid	Invalid	Don't Care
1	1	Invalid	Invalid	Don't Care

The K – map for solving the equation of D in terms of S, R and Q_P.



The Boolean equation of D is D = S + R'Q_P. The logic diagram using this equation to implement an SR flip – flop from D flip – flop is shown below.



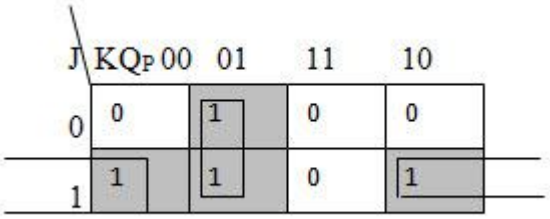
D Flip – flop to JK Flip – flop

When we need to convert the D flip – flop into JK flip – flop, J and K are the inputs of the combinational circuit with D as its output. Here Data (D) is the input of actual flip – flop. The truth table is drawn with the 8 possible combinations of the two inputs J & K along with Q_P. $Q_P$and Q_P' are the present state and its complement outputs of the flip – flop.

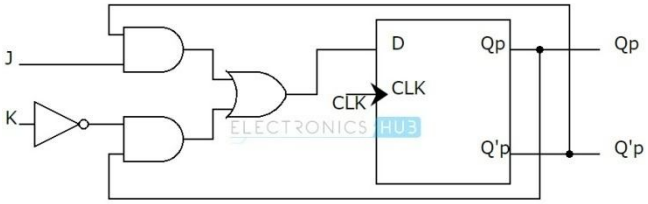
The truth table consists of combinations of J, K and Q_P in order to get Q_N. Here Q_N is the next state output of the flip – flop. The truth table also consists of D inputs that lead to Q_N output. The conversion table is shown below.

JK Inputs		Outputs		D Input
J	K	Q_P	Q_N	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

The K – map implementation of D in terms of J, K and Q_P is shown below.



The Boolean equation of D deduced from the above K – map is $D = JQ'_P + K'Q_P$. The logical representation of implementing JK flip – flop from D flip – flop is shown below.



D Flip – flop to T Flip – flop

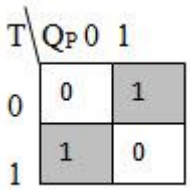
When we need to convert the D flip – flop into T flip – flop, T (Toggle input) is the input of the combinational circuit with D as its output. Here Data (D) is the input of actual flip – flop. The truth table is drawn with the 4 possible combinations of the input T along with Q_P. Q_P and Q_P' are the present state and its complement outputs of the flip – flop.

The truth table consists of combinations of T and Q_P in order to get Q_N. Here Q_N is the next state output of the flip – flop. The truth table also consists of D inputs that lead to Q_N output.

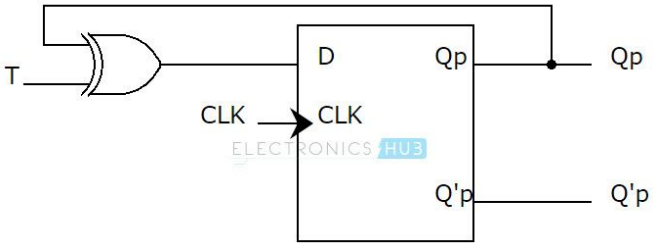
The conversion table is shown below.

T Input	Outputs		D Input
T	Q_P	Q_N	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

The K – map for D is shown below.

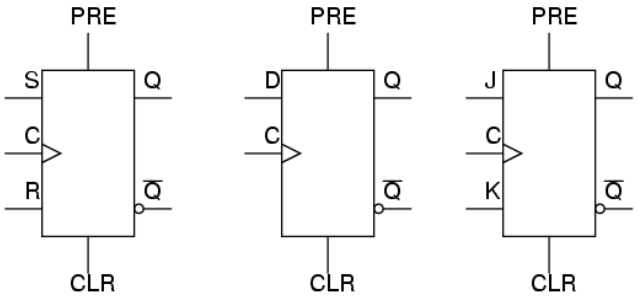


The Boolean equation of D in terms of T and Q_P is D = T'Q_P + TQ'$_P$. The logic circuit for implementing T flip – flop with D flip – flop is shown below.



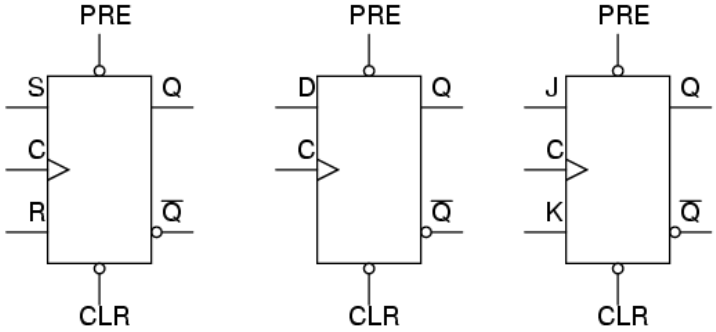
Flip Flop With Asynchronous Inputs (Preset And Clear):

- *Asynchronous* inputs on a flip-flop have control over the outputs (Q and not-Q) regardless of clock input status.
- These inputs are called the *preset* (PRE) and *clear* (CLR). The preset input drives the flip-flop to a set state while the clear input drives it to a reset state.
- It is possible to drive the outputs of a J-K flip-flop to an invalid condition using the asynchronous inputs, because all feedback within the multivibrator circuit is overridden.

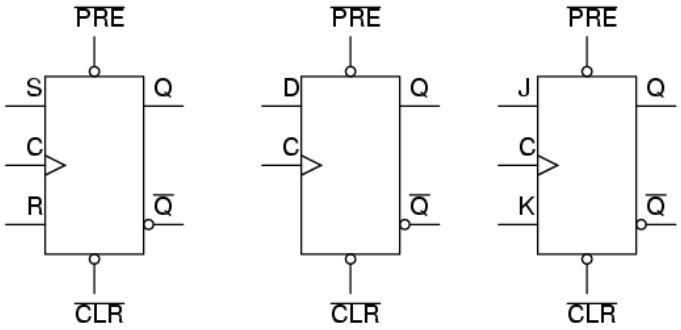


- When the preset input is activated, the flip-flop will be set (Q=1, not-Q=0) regardless of any of the synchronous inputs or the clock. When the clear input is activated, the flip-flop will be reset (Q=0, not-Q=1), regardless of any of the synchronous inputs or the clock. if both preset and clear inputs are activated we get an invalid state on the output,

- Asynchronous inputs, just like synchronous inputs, can be engineered to be active-high or active-low. If they're active-low, there will be an inverting bubble at that input lead on the block symbol, just like the negative edge-trigger clock inputs.



Sometimes the designations "PRE" and "CLR" will be shown with inversion bars above them, to further denote the negative logic of these inputs:



UNIT-V
Assignment-Cum-Tutorial Questions
SECTION-A

Objective Questions

1. Draw the block diagram of sequential circuit.
2. Write the differences between latch and flip-flop.
3. *A basic S-R flip-flop can be constructed by cross-coupling of which logic gates?*

   A. XOR or XNOR gates B. NOR or NAND gates [ ]

   C. AND or OR gates D. AND or NOR gates
4. The truth table for an S-R flip-flop has how many VALID entries? [ ]

   A. 4 B. 3 C. 2 D. 1
5. The output of SR flip flop when S=1, R=0 is [ ]

   A. 1 B. 0 C. No change D. High impedance
6. Which of the following is correct for a gated D-type flip-flop? [ ]

   A) Only one of the inputs can be HIGH at a time.

   B) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW.

   C) The output complement follows the input when enabled.

   D) The output toggles if one of the inputs is held HIGH.
7. When is a J-K flip-flop made to toggle? [ ]

   A. J = 0, K = 0B. J = 1, K = 0 C. J = 0, K = 1 D. J = 1, K = 1
8. For JK flip-flop J = 0, K=1, the output after clock pulse will be [ ]

   A. 1 B. no change. C. 0 D. high impedance.
9. Define race around condition.
10. Which table describes Input values of the flip flop when its present state and next state are known. [ ]

    A. function table B. truth table C. excitation table D. programming table
11. _____ and _____are the asynchronous inputs of a flip flop.
12. Flip flops are _____triggered sequential circuits
13. How are the sequential circuits specified in terms of time sequence? [ ]

    A. By Inputs B. By Outputs C. By Internal states D. All of the above

14. The behaviour of synchronous sequential circuit can be predicted by defining the signals at _____. [ ]

A. Discrete instants of time B. Continuous instants of time

C. Sampling instants of time D. At any instant of time

15. What is the storage capacity of any flipflop? [ ]

A. 1 bit B. 2 bits C. 16 bits D. Infinite bits

16. Why do the D flip-flops have designation as 'Data Flipflops'? [ ]

A. Due to its capability to receive data from flip-flop

B. Due to its capability to store data in flip-flop

C. Due to its capability to transfer the data into flip-flop

D. All of the above

17. The characteristic equation of D-flipflop implies that _____. [ ]

A. The next state is dependent on previous state

B. The next state is dependent on present state

C. The next state is independent of previous state

D. The next state is independent of present state

18. Which memory elements are utilized in asynchronous & synchronous circuits respectively? [ ]

A. Time- delay devices & registers B. Time- delay devices & flip-flops

C. Time- delay devices & counters D. Time-delay devices & latches

19. Which sequential circuits generate the feedback path due to the cross-coupled connection from output of one gate to the input of another gate? [ ]

A. synchronous B. asynchronous C. both D. none of the above

20. D flip flop is a circuit having [ ]

A. 2 NAND gates B. 3 NAND gates C. 4 NAND gates D. 5 NAND gates

21. If a active high SR latch has 0 on S input and 1 on R input and then R input goes to 0, the latch will be in _____ [ ]

A. SET B. RESET C. No Change D. Invalid.

22. Asynchronous inputs will cause the flip-flop to respond immediately with regard to the clock input. [ ]

A. TRUE B. FALSE C) can't say D) none of the above

SECTION-B

Descriptive Questions

1. Distinguish between combinational circuits and sequential circuits.
2. Draw the circuit diagram of J-K flip flop with NAND gates with positive edge triggering and explain its operation with the help of a truth table.
3. What are the various methods used for triggering flip-flops? What is meant by race around condition in flip-flops?
4. Draw the truth table, logic diagrams of J-K, R-S, D and T type flip flops.
5. Give the Excitation table and characteristic table and characteristic equations of SR, JK, D and T flip flops?
6. Write the procedure to convert one type of flip flop into another type.
7. Convert SR flip-flop into the following type of flip flop
   (i) JK (ii) D (iii) T
8. Realize the following flip flops using JK flip flop.
   (i) SR (ii) D (iii) T
9. How could a D-type flip-flop be used as following type of flip flops?
   (i) SR (ii) JK (iii) T
10. Design the following flip flops using T flip flop.
    (i) SR (ii) JK (iii) D

Section C:

Questions asked in GATE

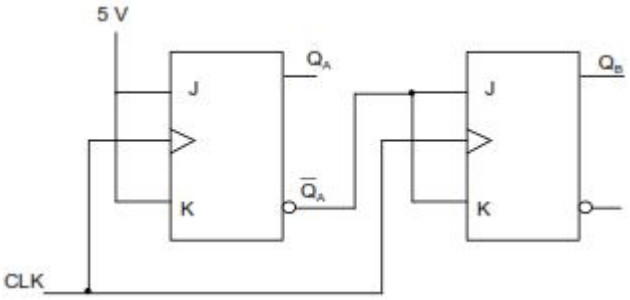
1. The next state table of a 2 bit saturating up-counter is given below. **[GATE 2017]**

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

. $T_1 = Q_0Q_1$ and $T_0 = Q'_0Q'_1$ **(B)** $T_1 = Q'_1Q_0$ and $T_0 = Q'_1 + Q'_0$

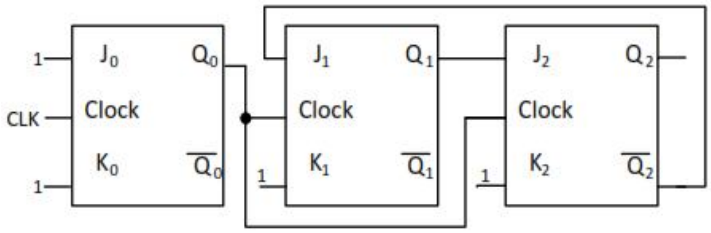
(C) $T_1 = Q_1 + Q_0$ and $T_0 = Q'_1 + Q'_0$ **(D)** $T_1 = Q'_1Q_0$ and $T_0 = Q_1 + Q_0$

2. The current state QA QB of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of the system is [GATE 2016]

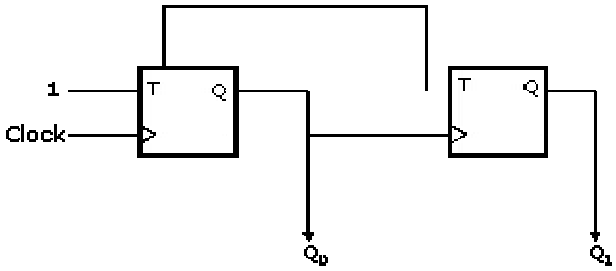


(A) 00 (B) 01 (C) 11 (D) 10

3. The figure shows a digital circuit constructed using negative edge triggered J-K flip flops. Assume a starting state of $\mathbf{Q_2Q_1Q_0}$=000. This state $\mathbf{Q_2Q_1Q_0}$=000 will repeat after _____ number of cycles of the clock CLK. **[GATE 2015]**



4. In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00,what are the next four values of Q_1Q_0? **[GATE 2010]**



(A) 11,10,01,00 **B)** 10,11,01,00 **C)** 10,00,01,11 **D)** 11,10,00,01