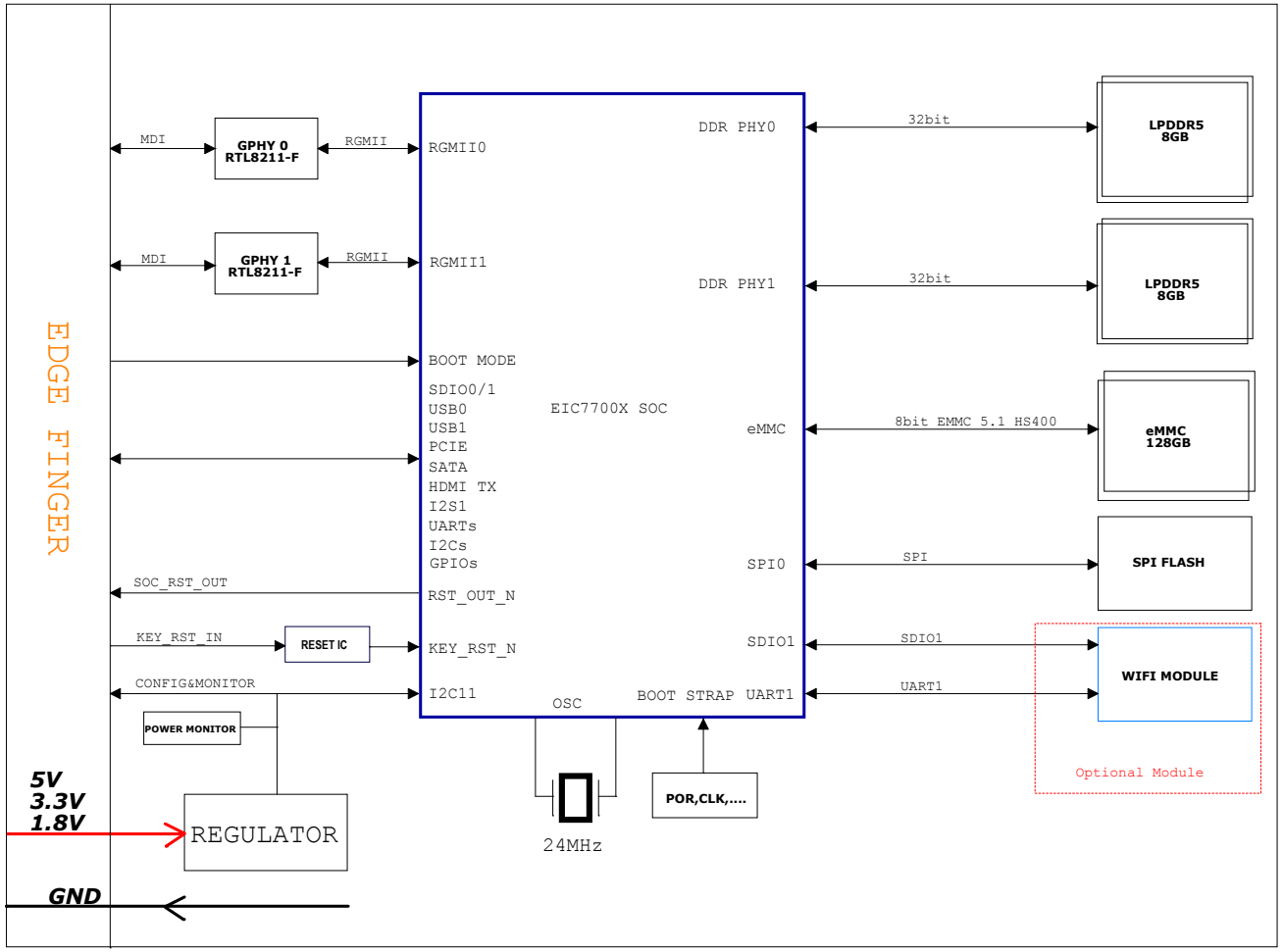
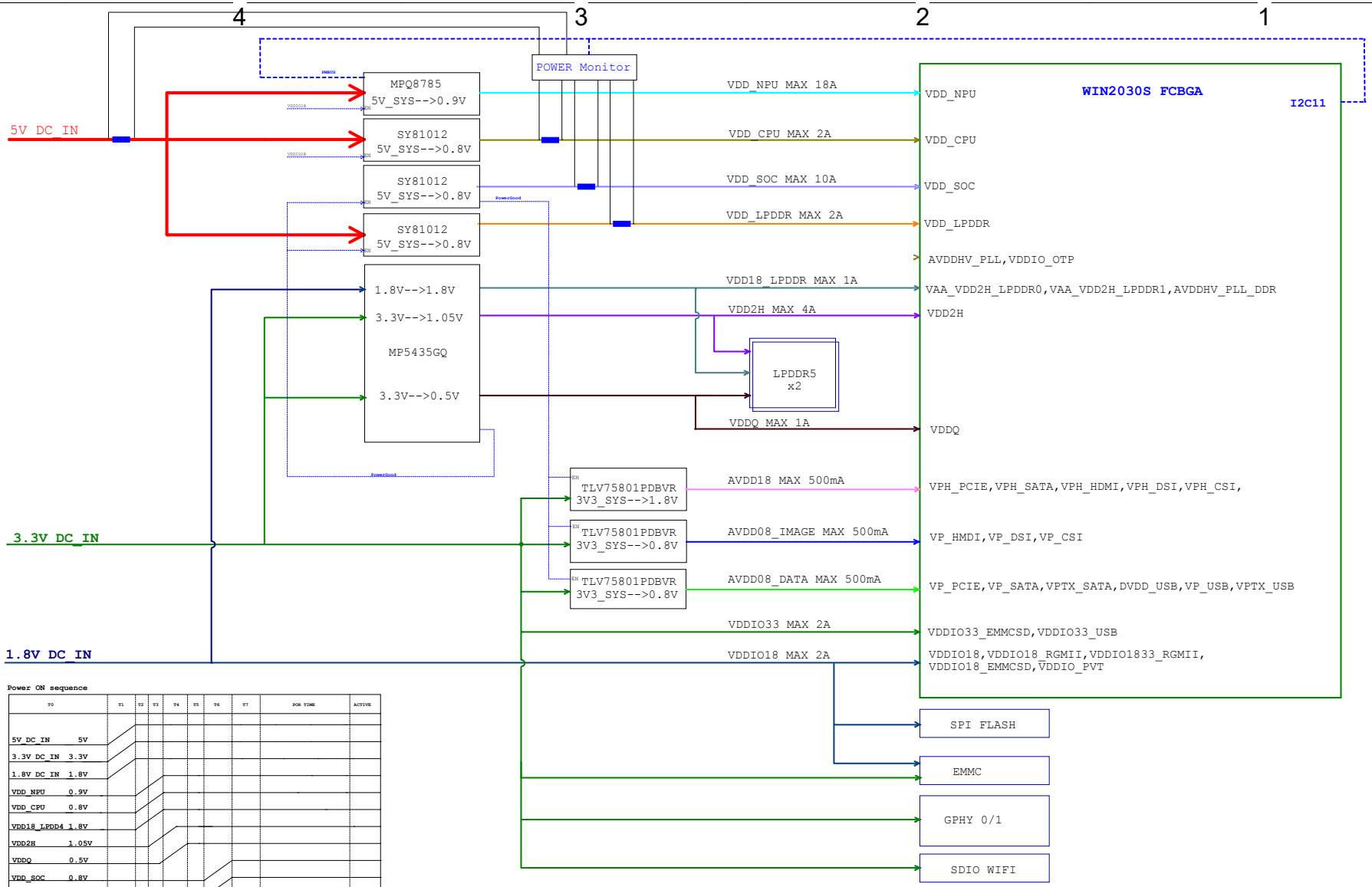
HiFive Premier P550 SOM BOARD Schematic



ESWIN		
Description: Block Diagram		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
Date: Tuesday, July 30, 2024	Sheet 1 of 28	



Description	POWER TREE
Size	D
Project Name	HiFive Premier P550
Rev	3.0
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ESWIN

EIC7700X SOC I2C MAP

Port	Pin name	SOC IO Voltage	Slave Device	Slave IO Vlotage	Slave Addr	COMMENTS
I2C11	I2C11_SCL/GPIO104 I2C11_SDA/GPIO106	1.8V	PMIC0 MP8785	1.8V	001_0010	Slave mount on SOM board I2C11 PIN alson mapped on edge finger
			Power Monitor(PAC1934)	1.8V	001_0000	

NOTE: All other I2C not mentioned here are mapped on edge finger

GPIO USED ON SOM

GPIO NUMBER	FUNCTION IN DESIGN	DIRECTION	ACTIVE
GPIO18	GPIO used as HOST_WAK_WLAN	Ouput	Low
GPIO19	GPIO used as HOST_WAK_BT	Ouput	LOW
GPIO20	GPIO used as WLAN_WAK_HOST	Input	Low
GPIO21	GPIO used as BT_WAK_HOST	Input	Low
GPIO106	GPHY0 Resetn	Output	Low
GPIO111	GPHY1 Resetn	Output	Low

NOTE: All other GPIO not mentioned here are mapped on edge finger

ESWIN

Description: Address Map

Size: C | Project Name: HiFive Premier P550 | Rev: 3.0

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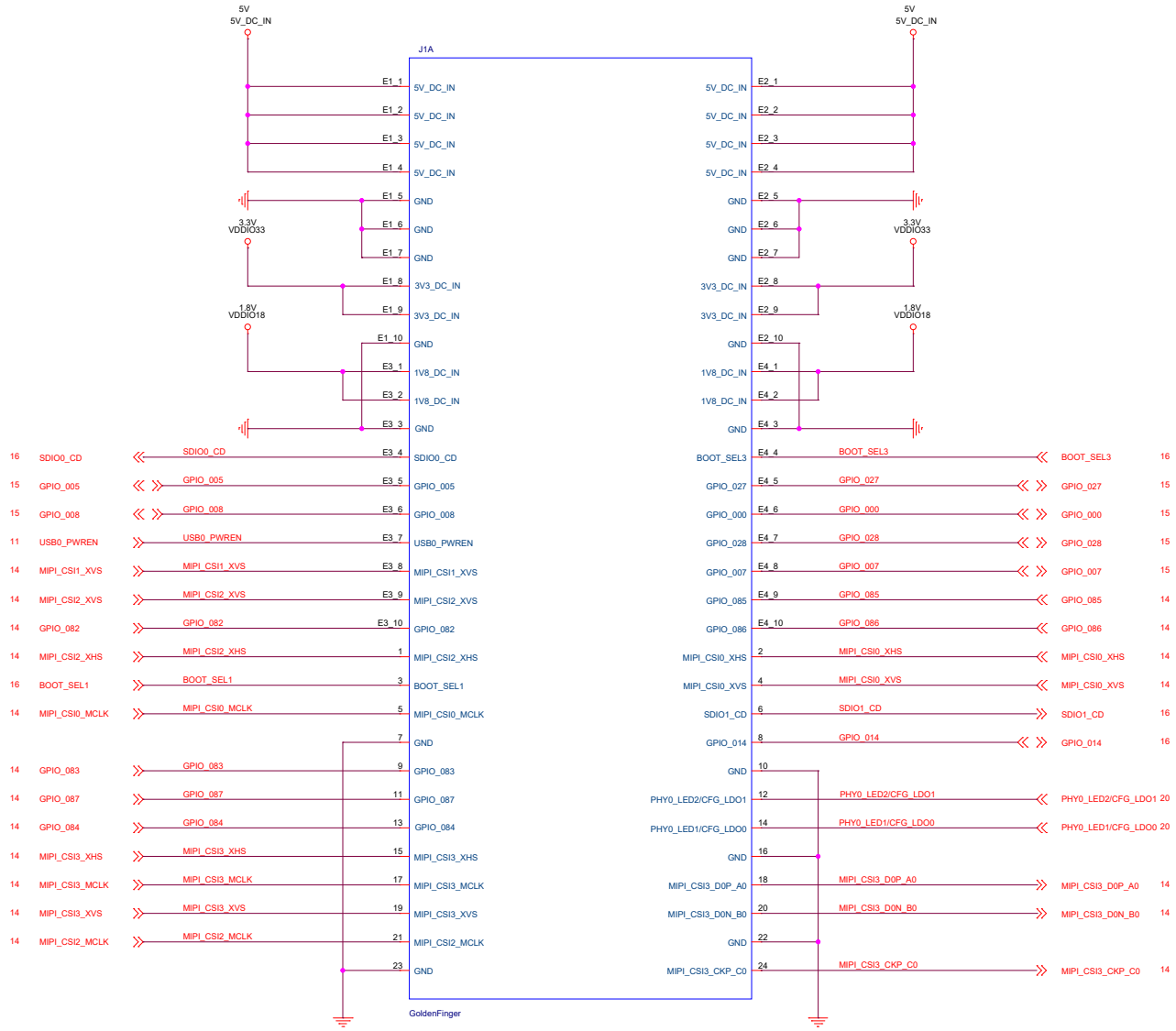
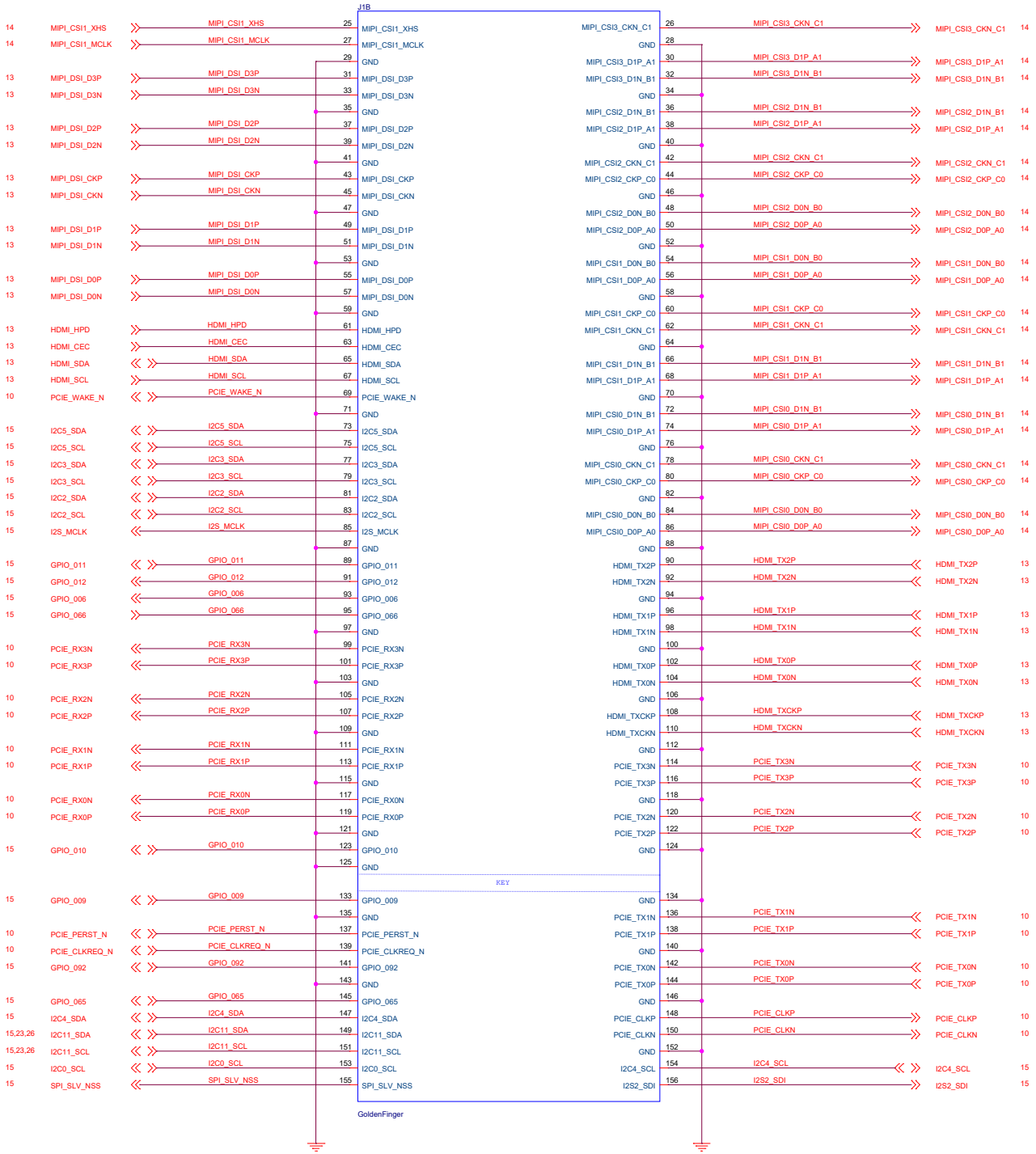


ESWIN		
Description: Edge Finger Part-1		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
Date: Tuesday, July 30, 2024	Sheet 4 of 28	



Description	Edge Finger Part-2
Size	C
Project Name	HiFive Premier P550
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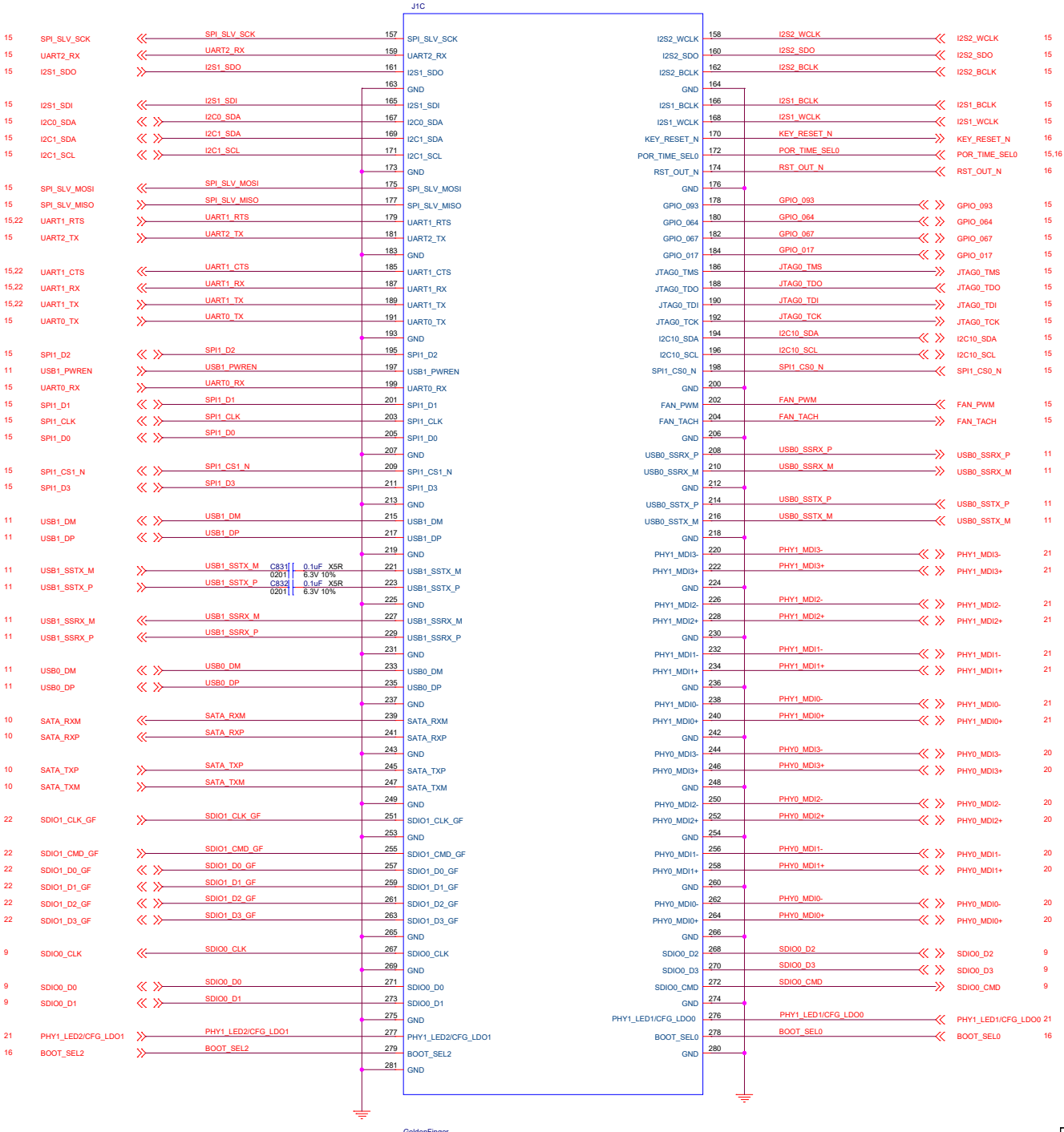
ESWIN



Description	Edge Finger Part-3
Size	C
Project Name	HiFive Premier P550
Rev	3.0
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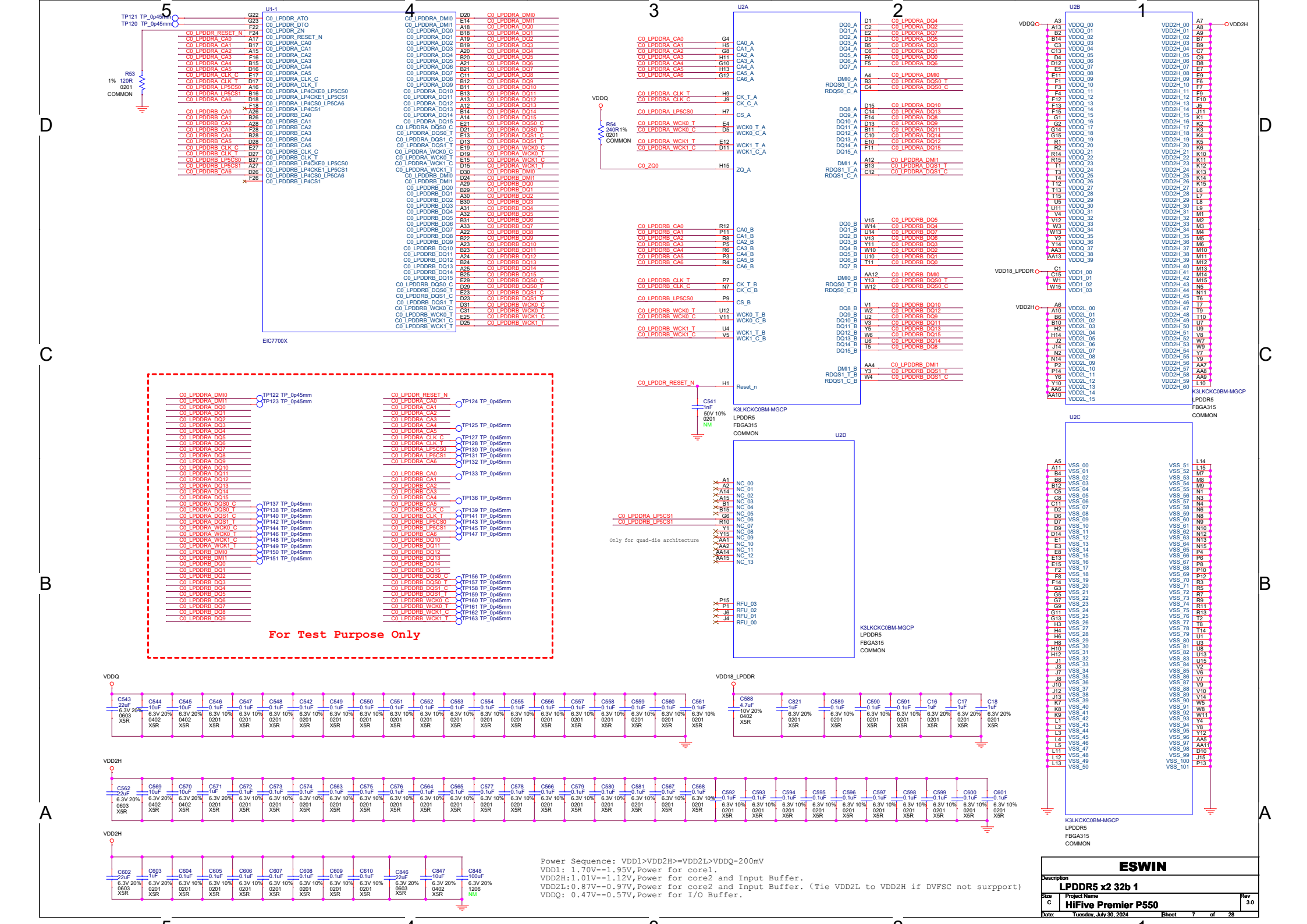
ESWIN


U1-1
EIC7700X
U2A
K3LKCKC0BM-MGCP
LPDDR5
FBGA315
COMMON
U2B
U2C
U2D
For Test Purpose Only
Only for quad-die architecture
Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V~-1.95V,Power for core1.
VDD2H:1.01V~-1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V~-0.97V,Power for core2 and Input Buffer. (Tie VDD2L to VDD2H if DVFSC not surpport)
VDDQ: 0.47V~-0.57V,Power for I/O Buffer.
ESWIN
Description
LPDDR5 x2 32b 1
Size
C
Project Name
HiFive Premier P550
Rev
3.0
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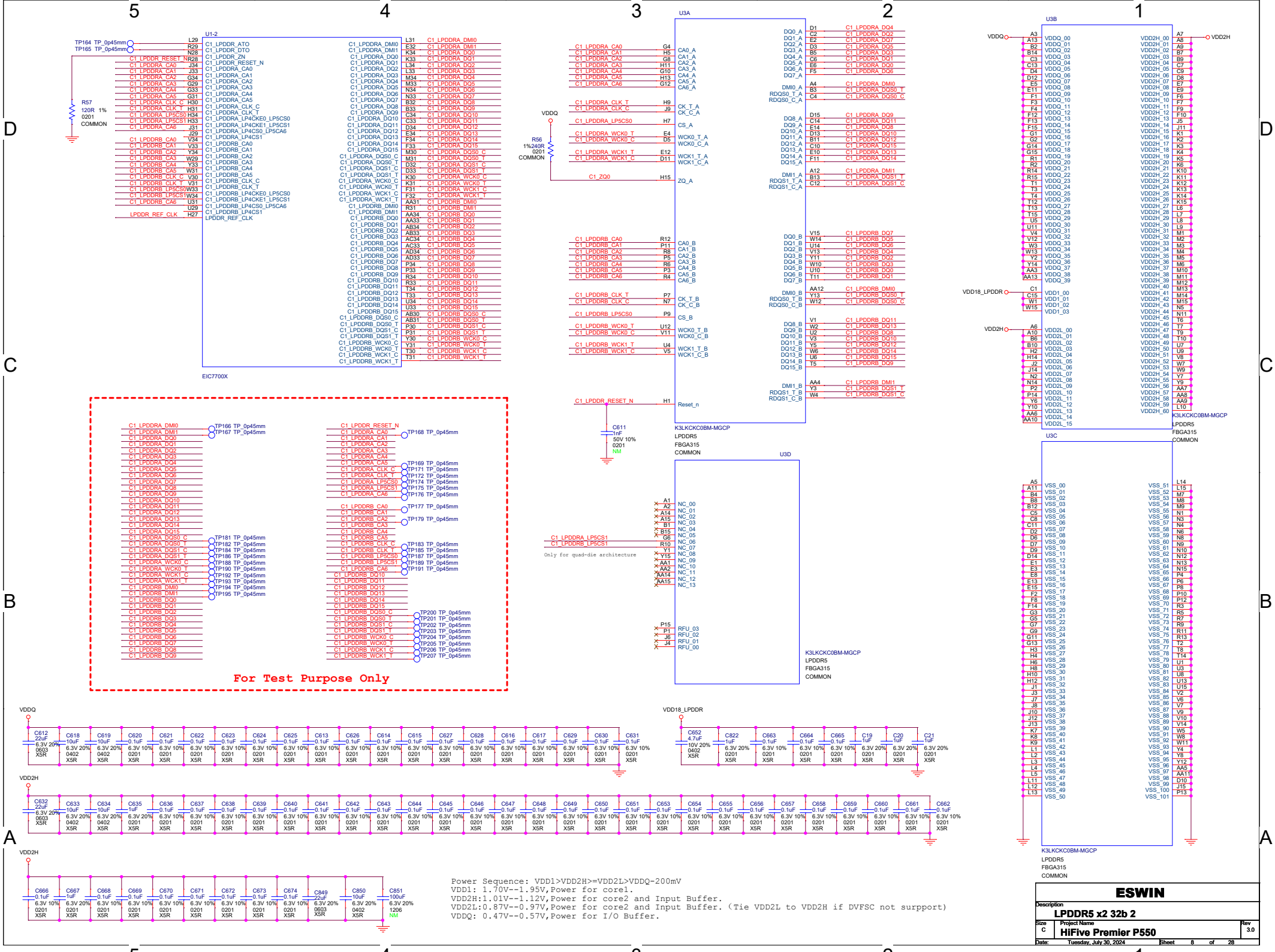
of
28


U1-2
EIC7700X
U3A
K3LKCKC0BM-MGCP
LPDDR5
FBGA315
COMMON
U3D
K3LKCKC0BM-MGCP
LPDDR5
FBGA315
COMMON
U3B
K3LKCKC0BM-MGCP
LPDDR5
FBGA315
COMMON
U3C
K3LKCKC0BM-MGCP
LPDDR5
FBGA315
COMMON
For Test Purpose Only
Only for quad-die architecture
Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for corel.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer. (Tie VDD2L to VDD2H if DVFSC not surpport)
VDDQ: 0.47V--0.57V,Power for I/O Buffer.
ESWIN
Description
LPDDR5 x2 32b 2
Size
C
Project Name
HiFive Premier P550
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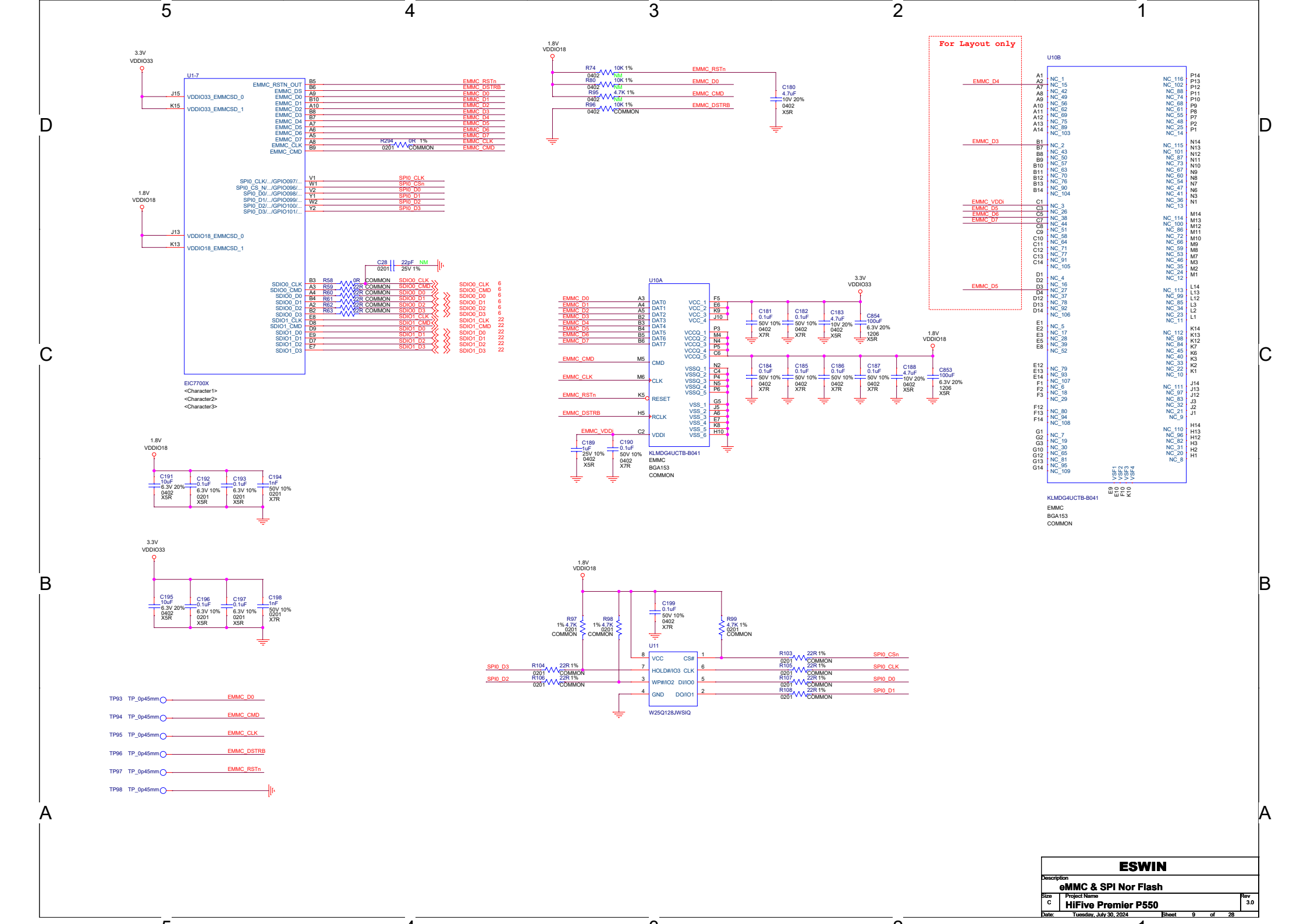
28


For Layout only
U1-7
EIC7700X
<Character1>
<Character2>
<Character3>
U10A
KLMDG4UCTB-B041
EMMC
BGA153
COMMON
U10B
U11
W25Q128JWSIQ
ESWIN
Description
eMMC & SPI Nor Flash
Size
C
Project Name
HiFive Premier P550
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3.0
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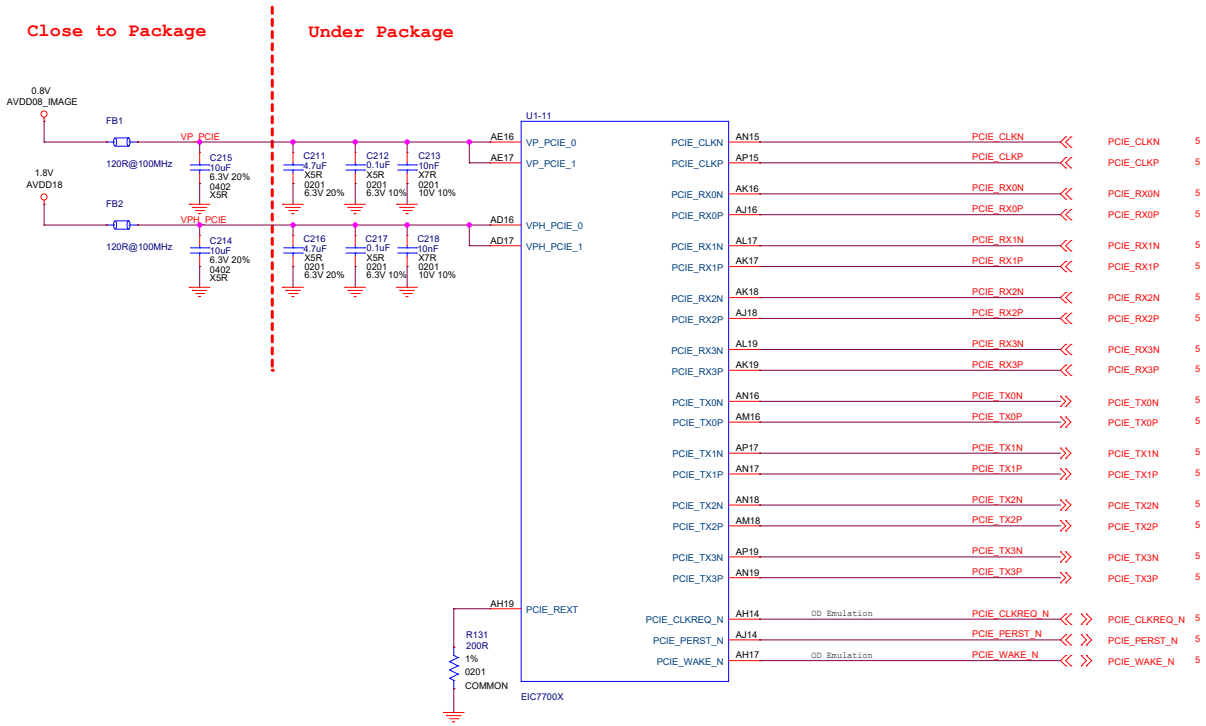
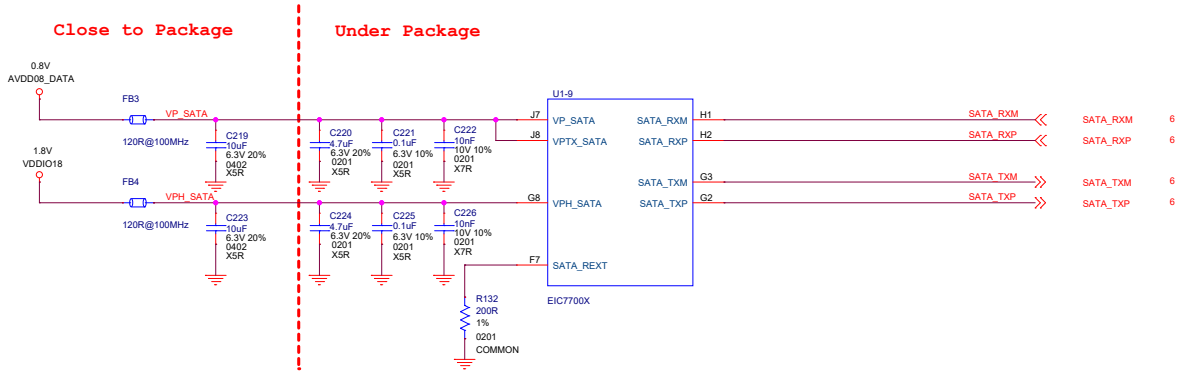
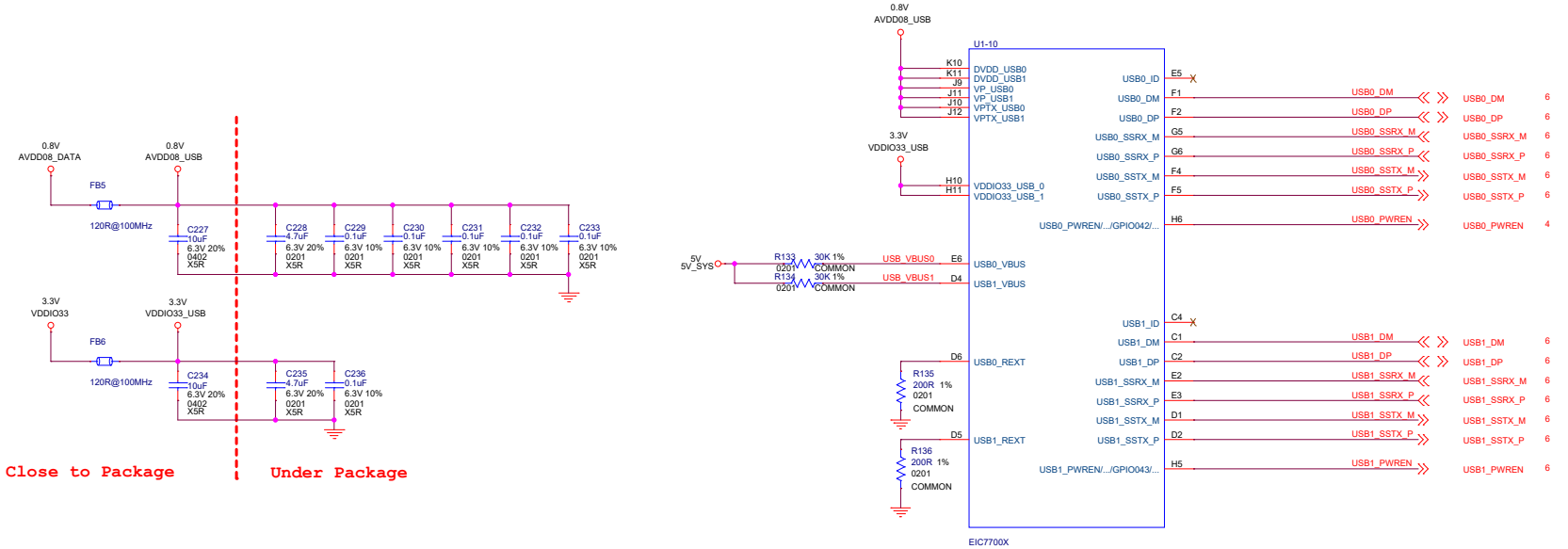
28

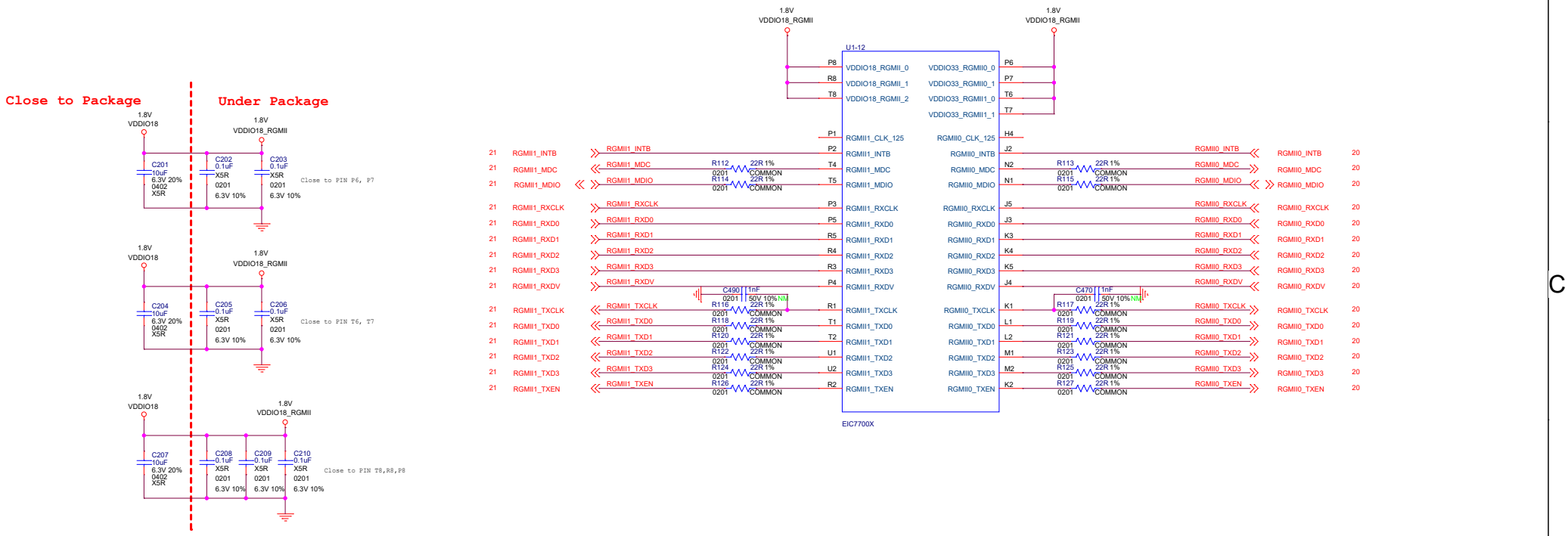




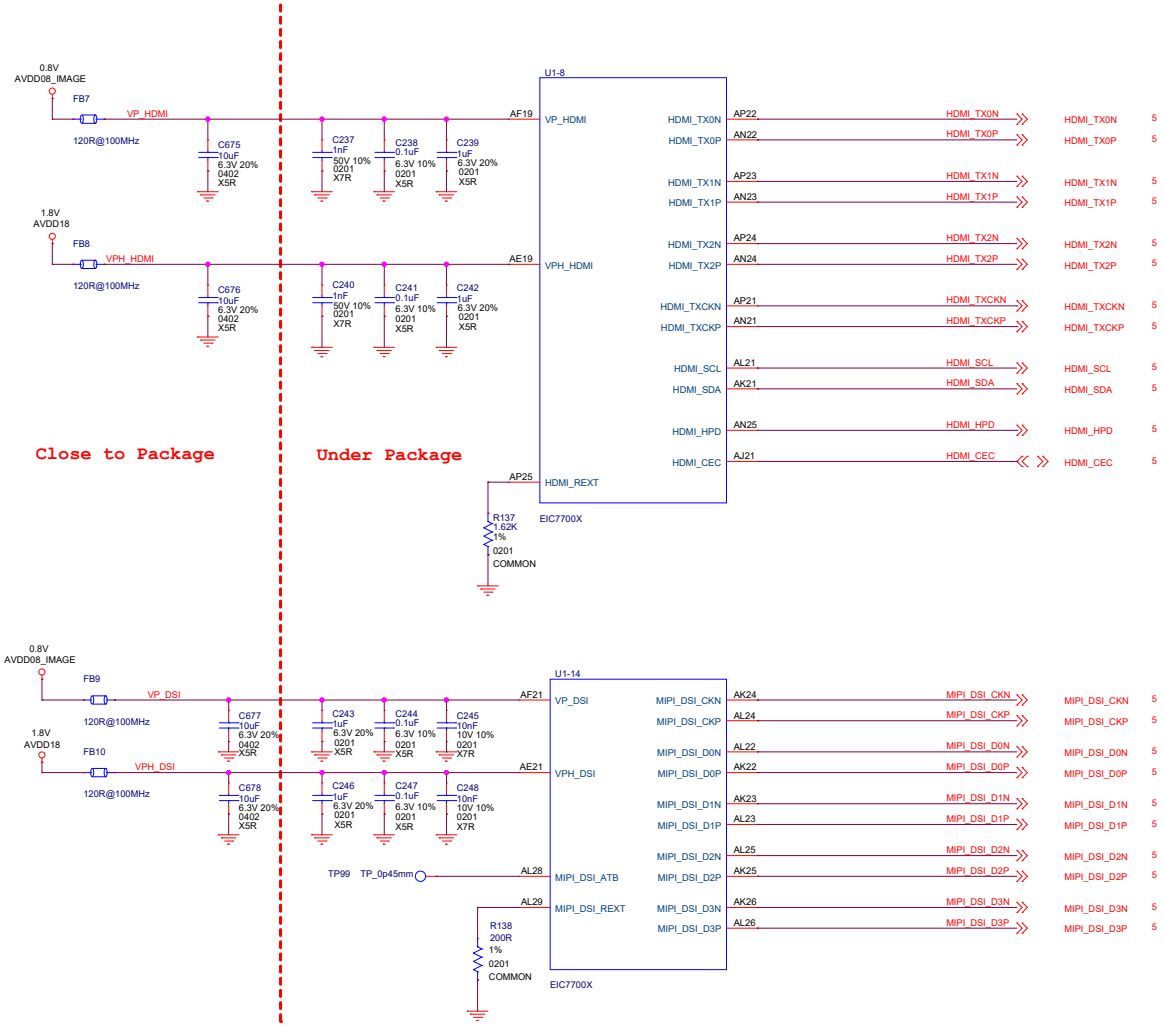
ESWIN		
Description: EIC7700X PCIE & SATA		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
Date: Tuesday, July 30, 2024	Sheet 10 of 28	



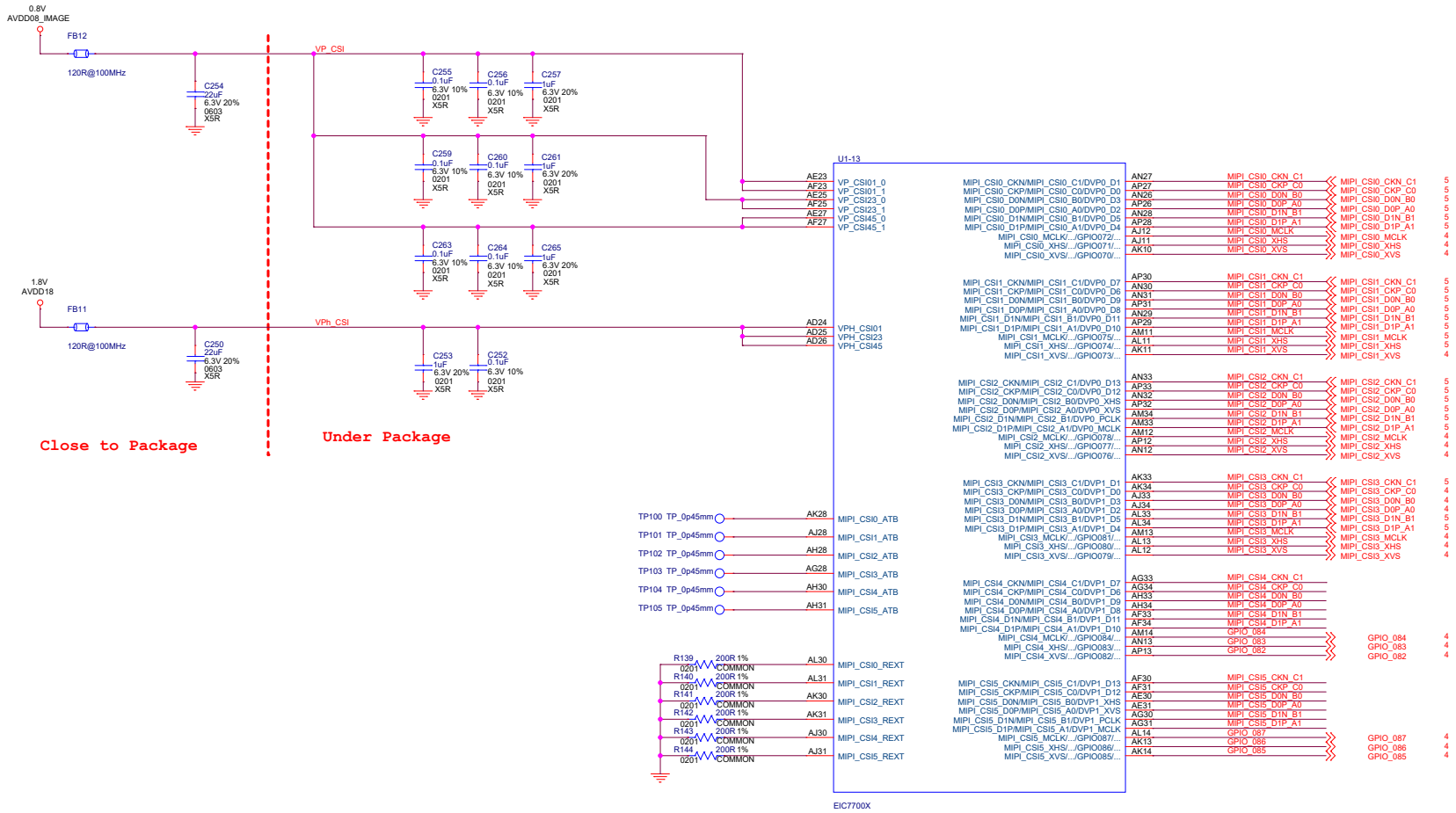
ESWIN		
Description: EIC7700X USB x2		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
Date: Tuesday, July 30, 2024	Sheet 11 of 28	



ESWIN	
Description	EIC7700X RGMII x2
Size: C	Project Name: HiFive Premier P550
Rev: 3.0	
Date: Tuesday, July 30, 2024	Sheet 12 of 28



ESWIN	
Description	EIC7700X HDMI TX & MIPI DSI TX
Size: C	Project Name: HiFive Premier P550
Rev: 3.0	
Date: Tuesday, July 30, 2024	Sheet 13 of 28



ESWIN		
Description: EIC7700X MIPI CSI RX		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
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U1-15
DDR_REFCLK_SEL/.../GPIO095/...
I2C8_SDA/MIPI_CSI_XTRIG1/GPIO093/UART3_RX
I2C8_SCL/MIPI_CSI_XTRIG0/GPIO092/UART3_TX
POR_TIME_SEL1/SD0_LED_CONTROL/GPIO034/...
POR_TIME_SEL0/EMMC_LED_CONTROL/GPIO029/...
GPIO028/.../.../...
GPIO027/SATA_ACT_LED/.../...
GPIO111/.../.../...
GPIO106/.../.../...
GPIO000/.../.../...
GPIO011/.../.../...
GPIO005/SPI2_D3/.../...
AK2 DDR_REFCLK_SEL DDR_REFCLK_SEL 16
AK1 GPIO_093 GPIO_093 6
AK4 GPIO_092 GPIO_092 5
AL3 POR_TIME_SEL1 POR_TIME_SEL1 16
AM2 POR_TIME_SEL0 POR_TIME_SEL0 6,16
AM1 GPIO_028 GPIO_028 4
AL1 GPIO_027 GPIO_027 4
AL4 PHY1_RESETn GPIO111 GPIO111 21
AL2 PHY0_RESETn GPIO106 GPIO106 20
AM4 GPIO_000 GPIO_000 4
AH3 GPIO_011 GPIO_011 5
AG1 GPIO_005 GPIO_005 4
EIC7700X
U1-6
JTAG0_TCK/SPI2_CLK/GPIO001/...
JTAG0_TDI/SPI2_D1/GPIO003/...
JTAG0_TDO/SPI2_D2/GPIO004/...
JTAG0_TMS/SPI2_D0/GPIO002/...
SPI3_CLK/.../GPIO089/...
SPI3_DI/.../GPIO090/...
SPI3_DO/.../GPIO091/...
SPI3_CS_N/.../GPIO088/...
FAN_TACH/.../GPIO069/...
FAN_PWM/.../GPIO068/...
JTAG1_TCK/.../GPIO007/...
JTAG1_TDI/.../GPIO009/...
JTAG1_TDO/.../GPIO010/...
JTAG1_TMS/.../GPIO008/...
JTAG2_TCK/.../GPIO064/...
JTAG2_TDI/.../GPIO066/...
JTAG2_TDO/.../GPIO067/...
JTAG2_TMS/.../GPIO065/...
JTAG2_TRST/.../GPIO017/...
SPI2_CS0_N/.../GPIO006/...
SPI2_CS1_N/.../GPIO012/...
FUNC0/FUNC1/FUNC2/FUNC3
AF1 JTAG0_TCK JTAG0_TCK 6
AP2 JTAG0_TDI JTAG0_TDI 6
AG2 JTAG0_TDO JTAG0_TDO 6
AH1 JTAG0_TMS JTAG0_TMS 6
AC4 SPI_SLV_SCK SPI_SLV_SCK 6
AD4 SPI_SLV_MOSI SPI_SLV_MOSI 6
AD5 SPI_SLV_MISO SPI_SLV_MISO 6
AC5 SPI_SLV_NSS SPI_SLV_NSS 5
AD1 FAN_TACH FAN_TACH 6
AD2 FAN_PWM FAN_PWM 6
R651 22R 1% 0201 COMMON
AG4 GPIO_007 GPIO_007 4
AG5 GPIO_009 GPIO_009 5
AH5 GPIO_010 GPIO_010 5
AH4 GPIO_008 GPIO_008 4
AJ2 GPIO_064 GPIO_064 6
AJ3 GPIO_066 GPIO_066 5
AJ1 GPIO_067 GPIO_067 6
AJ4 GPIO_065 GPIO_065 5
AH2 GPIO_017 GPIO_017 6
AJ5 GPIO_006 GPIO_006 5
AJ6 GPIO_012 GPIO_012 5
EIC7700X
FAN_PWM
C852 1nF 50V 10% 0201 NM
U1-17
I2C0_SCL/.../GPIO044/...
I2C0_SDA/.../GPIO045/...
I2C1_SCL/.../GPIO046/...
I2C1_SDA/.../GPIO047/...
I2C2_SCL/.../GPIO048/...
I2C2_SDA/.../GPIO049/...
I2C3_SCL/.../GPIO050/...
I2C3_SDA/.../GPIO051/...
I2C4_SCL/.../GPIO052/...
I2C4_SDA/.../GPIO053/...
I2C5_SCL/.../GPIO054/...
I2C5_SDA/.../GPIO055/...
I2C10_SCL/.../GPIO102/...
I2C10_SDA/.../GPIO103/...
I2C11_SCL/.../GPIO104/...
I2C11_SDA/.../GPIO105/...
AE5 I2C0_SCL I2C0_SCL 5
AF5 I2C0_SDA I2C0_SDA 6
AE3 I2C1_SCL I2C1_SCL 6
AE4 I2C1_SDA I2C1_SDA 6
AK8 I2C2_SCL I2C2_SCL 5
AL8 I2C2_SDA I2C2_SDA 5
AM8 I2C3_SCL I2C3_SCL 5
AL9 I2C3_SDA I2C3_SDA 5
AN8 I2C4_SCL I2C4_SCL 5
AP8 I2C4_SDA I2C4_SDA 5
AM9 I2C5_SCL I2C5_SCL 5
AL10 I2C5_SDA I2C5_SDA 5
AE1 I2C10_SCL I2C10_SCL 6
AE2 I2C10_SDA I2C10_SDA 6
AF4 I2C11_SCL I2C11_SCL 5,23,26
AF3 I2C11_SDA I2C11_SDA 5,23,26
R24 0201 2.2K 1% COMMON
R23 0201 2.2K 1% COMMON
1.8V VDDIO18
MP8785/PAC1934
EIC7700X
U1-16
I2S_MCLK/.../GPIO022/...
I2S0_BCLK/.../GPIO018/...
I2S0_SDI/.../GPIO020/...
I2S0_SDO/.../GPIO021/...
I2S0_WCLK/.../GPIO019/...
I2S1_BCLK/.../GPIO030/...
I2S1_SDI/.../GPIO032/...
I2S1_SDO/.../GPIO033/...
I2S1_WCLK/.../GPIO031/...
I2S2_BCLK/.../GPIO023/...
I2S2_SDI/.../GPIO025/...
I2S2_SDO/.../GPIO026/...
I2S2_WCLK/.../GPIO024/...
AL5 I2S_MCLK I2S_MCLK 5
AN6 GPIO_018 GPIO_018 22
AP7 GPIO_020 GPIO_020 22
AP6 GPIO_021 GPIO_021 22
AN7 GPIO_019 GPIO_019 22
AP4 I2S1_BCLK I2S1_BCLK 6
AP5 I2S1_SDI I2S1_SDI 6
AN5 I2S1_SDO I2S1_SDO 6
AN4 I2S1_WCLK I2S1_WCLK 6
AK5 I2S2_BCLK I2S2_BCLK 6
AM5 I2S2_SDI I2S2_SDI 5
AM6 I2S2_SDO I2S2_SDO 6
AL6 I2S2_WCLK I2S2_WCLK 6
EIC7700X
U1-18
SPI1_CLK/.../GPIO036/...
SPI1_D0/I2C9_SCL/GPIO037/UART4_TX
SPI1_D1/I2C9_SDA/GPIO038/UART4_RX
SPI1_D2/SD1_LED_CONTROL/GPIO039/...
SPI1_D3/PWM1/GPIO040/...
SPI1_CS0_N/.../GPIO035/...
SPI1_CS1_N/PWM2/GPIO041/...
AA1 SPI1_CLK SPI1_CLK 6
AA2 SPI1_D0 SPI1_D0 6
AC3 SPI1_D1 SPI1_D1 6
AC2 SPI1_D2 SPI1_D2 6
AB1 SPI1_D3 SPI1_D3 6
AC1 SPI1_CS0_N SPI1_CS0_N 6
AB2 SPI1_CS1_N SPI1_CS1_N 6
EIC7700X
U1-19
UART1_CTS/I2C6_SCL/GPIO060/...
UART1_RTS/I2C6_SDA/GPIO061/...
UART1_RX/.../GPIO059/...
UART1_TX/.../GPIO058/...
UART0_RX/.../GPIO057/...
UART0_TX/.../GPIO056/...
UART2_RX/I2C7_SDA/GPIO063/...
UART2_TX/I2C7_SCL/GPIO062/...
AA4 UART1_CTS UART1_CTS 6,22
AB5 UART1_RTS UART1_RTS 6,22
Y5 UART1_RX UART1_RX 6,22
AA5 UART1_TX UART1_TX 6,22
Y4 UART0_RX UART0_RX 6
Y3 UART0_TX UART0_TX 6
AB4 UART2_RX UART2_RX 6
AB3 UART2_TX UART2_TX 6
EIC7700X
ESWIN
Description
EIC7700X LOW SPEED IO
Size C
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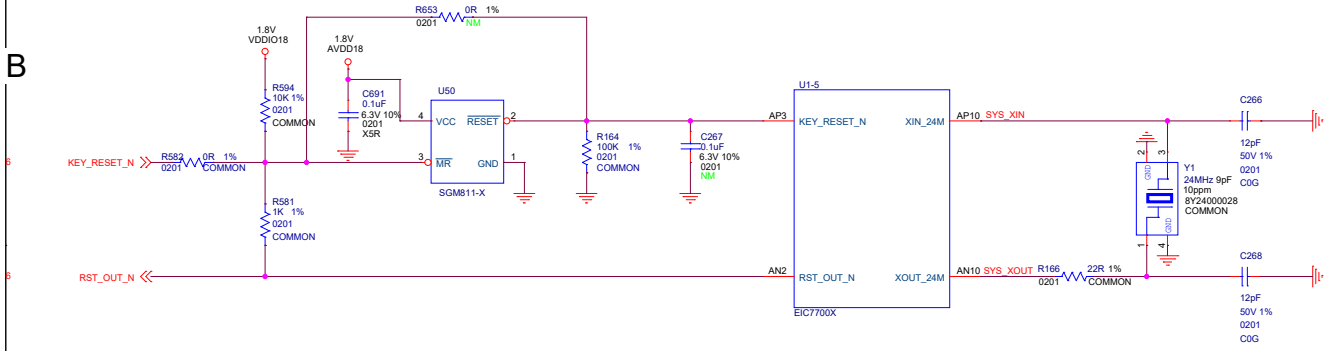
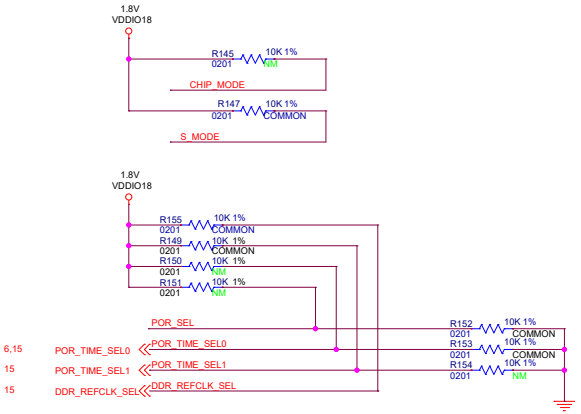
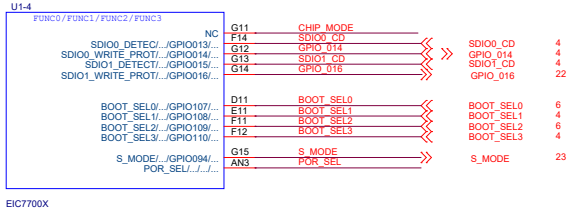
Strap Bit	Description	Pin	Default	Comments
CHIP MODE MODE SET3 MODE SET2 MODE SET1 MODE SET0	0xxxx : function mode 10000 : test0 10001 : test1 10010 : test2 10011 : test3 . . . 11111 : test15	G11: CHIP_MODE G14: MODE_SET3 G13: MODE_SET2 G12: MODE_SET1 F14: MODE_SET0	0xxxx	
POR SELECT	0 : Bypass Internal POR 1 : Internal POR	AN3: POR_SEL	0	
POR WAIT TIME[1] POR WAIT TIME[0]	00 : 2560us 01 : 20480us 10 : 81920us 11 : 327680us	AL3: GPIO34 AM2: GPIO29	10	
BOOT SELECT 3 BOOT SELECT 2 BOOT SELECT 1 BOOT SELECT 0	if OTP security bit = 1 bits : boot cpu : first boot : second boot xx00 : SCPU : ROM : UART xx01 : SCPU : ROM : eMMC xx10 : SCPU : ROM : SPI NOR xx11 : SCPU : ROM : USB if OTP security bit = 0 bits : boot cpu : first boot : second boot 0000 : SCPU : ROM : UART 0001 : SCPU : ROM : eMMC 0010 : SCPU : ROM : SPI NOR 0011 : SCPU : ROM : USB 0100 : SCPU : SPI NOR : UART 0101 : SCPU : SPI NOR : EMMC 0110 : SCPU : SPI NOR : SPI NOR 0111 : SCPU : SPI NOR : USB 1x00 : U84 : SPI NOR : UART 1x01 : U84 : SPI NOR : eMMC 1x10 : U84 : SPI NOR : SPI NOR 1x11 : U84 : SPI NOR : USB	F12: BOOT SELECT 3 F11: BOOT SELECT 2 E11: BOOT SELECT 1 D11: BOOT SELECT 0	xx01	
S_MODE	1 : Signle Die mode 0 : Dual Die mode	G15: S_MODE	1	This design is only for single die mode
LPDDR_REF_CLK	0 : Backup clock 1 : Main clock	AK2:GPIO95	1	This design is main clock only







ESWIN			
Description: EIC7700X SYSTEM CONFIG			
Size: C	Project Name: HiFive Premier P550		Rev: 3.0
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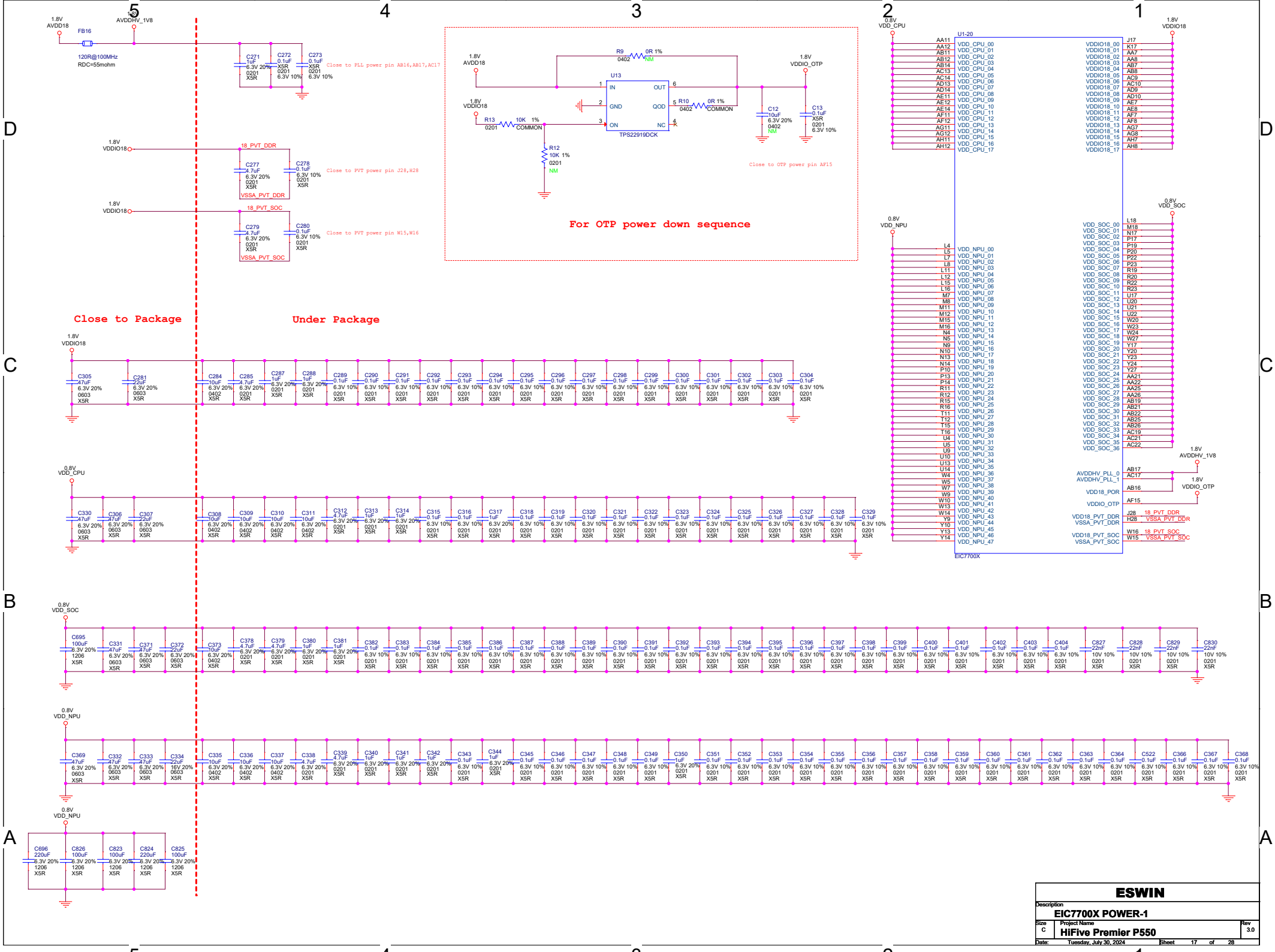
Close to Package
Under Package
For OTP power down sequence
U1-20
EIC7700X
ESWIN
EIC7700X POWER-1
HiFive Premier P550
Rev 3.0
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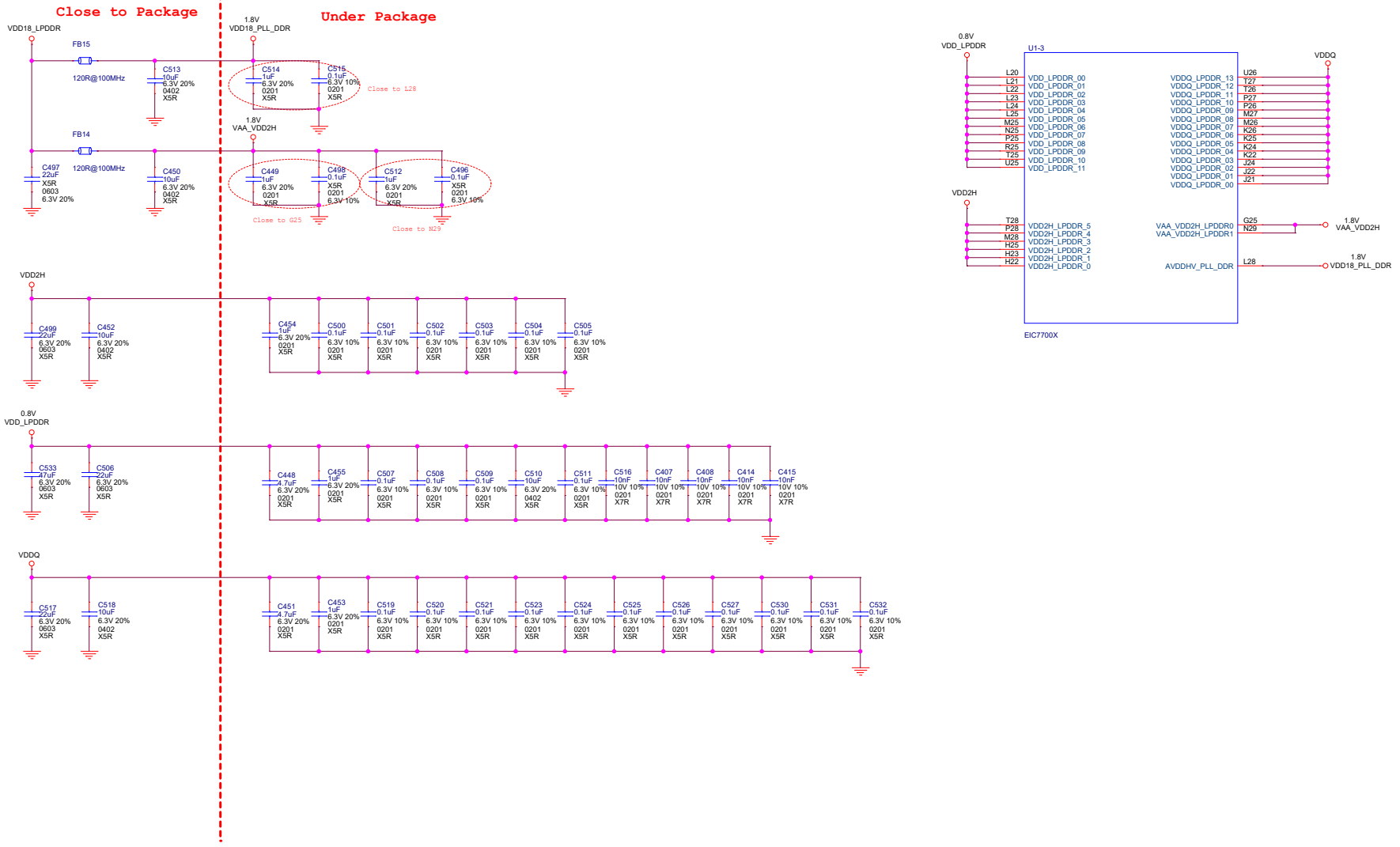

ESWIN		
Description: EIC7700X POWER-2		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
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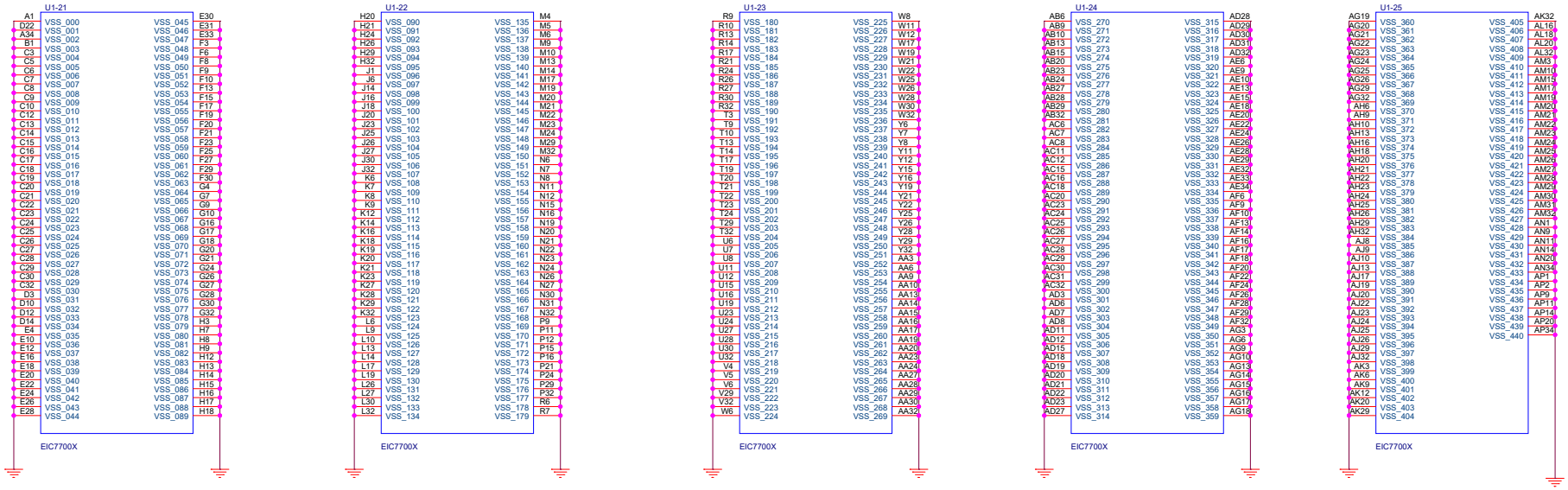

	ESWIN
Description	**EIC7700X GND**
Size: C	Project Name: HiFive Premier P550 — Rev: 3.0
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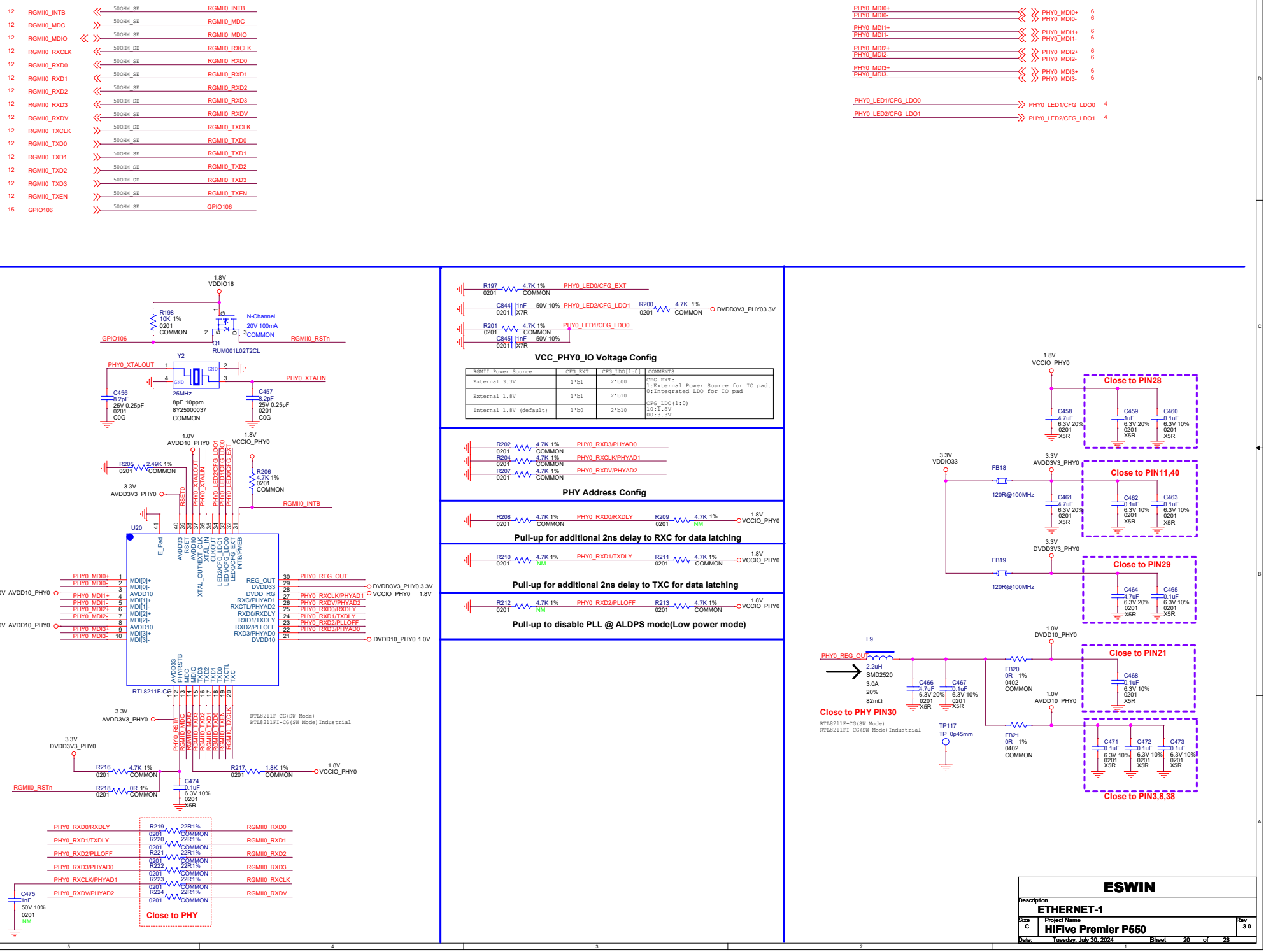
12 RGMII0_INTB 500HM_SE RGMII0_INTB
12 RGMII0_MDC 500HM_SE RGMII0_MDC
12 RGMII0_MDIO 500HM_SE RGMII0_MDIO
12 RGMII0_RXCLK 500HM_SE RGMII0_RXCLK
12 RGMII0_RXD0 500HM_SE RGMII0_RXD0
12 RGMII0_RXD1 500HM_SE RGMII0_RXD1
12 RGMII0_RXD2 500HM_SE RGMII0_RXD2
12 RGMII0_RXD3 500HM_SE RGMII0_RXD3
12 RGMII0_RXDV 500HM_SE RGMII0_RXDV
12 RGMII0_TXCLK 500HM_SE RGMII0_TXCLK
12 RGMII0_TXD0 500HM_SE RGMII0_TXD0
12 RGMII0_TXD1 500HM_SE RGMII0_TXD1
12 RGMII0_TXD2 500HM_SE RGMII0_TXD2
12 RGMII0_TXD3 500HM_SE RGMII0_TXD3
12 RGMII0_TXEN 500HM_SE RGMII0_TXEN
15 GPIO106 500HM_SE GPIO106
PHY0_MDI0+ PHY0_MDI0+ 6
PHY0_MDI0- PHY0_MDI0- 6
PHY0_MDI1+ PHY0_MDI1+ 6
PHY0_MDI1- PHY0_MDI1- 6
PHY0_MDI2+ PHY0_MDI2+ 6
PHY0_MDI2- PHY0_MDI2- 6
PHY0_MDI3+ PHY0_MDI3+ 6
PHY0_MDI3- PHY0_MDI3- 6
PHY0_LED1/CFG_LDO0 PHY0_LED1/CFG_LDO0 4
PHY0_LED2/CFG_LDO1 PHY0_LED2/CFG_LDO1 4
1.8V VDDIO18
R198 10K 1% 0201 COMMON
N-Channel 20V 100mA
Q1 RUM001L02T2CL
GPIO106
RGMII0_RSTn
Y2
PHY0_XTALOUT
PHY0_XTALIN
25MHz 8pF 10ppm 8Y25000037 COMMON
C456 8.2pF 25V 0.25pF 0201 C0G
C457 8.2pF 25V 0.25pF 0201 C0G
1.0V AVDD10_PHY0
1.8V VCCIO_PHY0
R205 2.49K 1% 0201 COMMON
R206 4.7K 1% 0201 COMMON
3.3V AVDD3V3_PHY0
RGMII0_INTB
U20
E_Pad
RTL8211F-CG
PHY0_MDI0+ PHY0_MDI0- PHY0_MDI1+ PHY0_MDI1- PHY0_MDI2+ PHY0_MDI2- PHY0_MDI3+ PHY0_MDI3-
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY0_REG_OUT
DVDD3V3_PHY0 3.3V
VCCIO_PHY0 1.8V
PHY0_RXCLK/PHYAD1 PHY0_RXDV/PHYAD2 PHY0_RXD0/RXDLY PHY0_RXD1/TXDLY PHY0_RXD2/PLLOFF PHY0_RXD3/PHYAD0
DVDD10_PHY0 1.0V
1.0V AVDD10_PHY0
1.0V AVDD10_PHY0
3.3V AVDD3V3_PHY0
3.3V DVDD3V3_PHY0
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
PHY0_RSTn RGMII0_MDC RGMII0_MDIO RGMII0_TXD3 RGMII0_TXD2 RGMII0_TXD1 RGMII0_TXD0 RGMII0_TXCTL RGMII0_TXCK
RGMII0_RSTn
R216 4.7K 1% 0201 COMMON
R217 1.8K 1% 0201 COMMON
1.8V VCCIO_PHY0
R218 0R 1% 0201 COMMON
C474 0.1uF 6.3V 10% 0201 X5R
PHY0_RXD0/RXDLY RGMII0_RXD0
PHY0_RXD1/TXDLY RGMII0_RXD1
PHY0_RXD2/PLLOFF RGMII0_RXD2
PHY0_RXD3/PHYAD0 RGMII0_RXD3
PHY0_RXCLK/PHYAD1 RGMII0_RXCLK
PHY0_RXDV/PHYAD2 RGMII0_RXDV
R219 22R1% 0201 COMMON
R220 22R1% 0201 COMMON
R221 22R1% 0201 COMMON
R222 22R1% 0201 COMMON
R223 22R1% 0201 COMMON
R224 22R1% 0201 COMMON
C475 1nF 50V 10% 0201 NM
Close to PHY
R197 4.7K 1% 0201 COMMON PHY0_LED0/CFG_EXT
C844 1nF 50V 10% 0201 X7R PHY0_LED2/CFG_LDO1
R200 4.7K 1% 0201 COMMON DVDD3V3_PHY03.3V
R201 4.7K 1% 0201 COMMON PHY0_LED1/CFG_LDO0
C845 1nF 50V 10% 0201 X7R
VCC_PHY0_IO Voltage Config
RGMII Power Source | CFG_EXT | CFG_LDO[1:0] | COMMENTS
External 3.3V | 1'b1 | 2'b00 | CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad
External 1.8V | 1'b1 | 2'b10 | CFG_LDO(1:0) 10:1.8V 00:3.3V
Internal 1.8V (default) | 1'b0 | 2'b10
R202 4.7K 1% 0201 COMMON PHY0_RXD3/PHYAD0
R204 4.7K 1% 0201 COMMON PHY0_RXCLK/PHYAD1
R207 4.7K 1% 0201 COMMON PHY0_RXDV/PHYAD2
PHY Address Config
R208 4.7K 1% 0201 COMMON PHY0_RXD0/RXDLY R209 4.7K 1% 0201 NM 1.8V VCCIO_PHY0
Pull-up for additional 2ns delay to RXC for data latching
R210 4.7K 1% 0201 NM PHY0_RXD1/TXDLY R211 4.7K 1% 0201 COMMON 1.8V VCCIO_PHY0
Pull-up for additional 2ns delay to TXC for data latching
R212 4.7K 1% 0201 NM PHY0_RXD2/PLLOFF R213 4.7K 1% 0201 COMMON 1.8V VCCIO_PHY0
Pull-up to disable PLL @ ALDPS mode(Low power mode)
1.8V VCCIO_PHY0
Close to PIN28
C458 4.7uF 6.3V 20% 0201 X5R
C459 1uF 6.3V 20% 0201 X5R
C460 0.1uF 6.3V 10% 0201 X5R
3.3V VDDIO33
FB18 120R@100MHz
3.3V AVDD3V3_PHY0
Close to PIN11,40
C461 4.7uF 6.3V 20% 0201 X5R
C462 0.1uF 6.3V 10% 0201 X5R
C463 0.1uF 6.3V 10% 0201 X5R
FB19 120R@100MHz
3.3V DVDD3V3_PHY0
Close to PIN29
C464 4.7uF 6.3V 20% 0201 X5R
C465 0.1uF 6.3V 10% 0201 X5R
L9
PHY0_REG_OUT
2.2uH SMD2520 3.0A 20% 82mΩ
C466 4.7uF 6.3V 20% 0201 X5R
C467 0.1uF 6.3V 10% 0201 X5R
Close to PHY PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
TP117 TP_0p45mm
1.0V DVDD10_PHY0
FB20 0R 1% 0402 COMMON
1.0V AVDD10_PHY0
FB21 0R 1% 0402 COMMON
Close to PIN21
C468 0.1uF 6.3V 10% 0201 X5R
C471 0.1uF 6.3V 10% 0201 X5R
C472 0.1uF 6.3V 10% 0201 X5R
C473 0.1uF 6.3V 10% 0201 X5R
Close to PIN3,8,38
ESWIN
Description
ETHERNET-1
Size C
Project Name
HiFive Premier P550
Rev 3.0
Date: Tuesday, July 30, 2024
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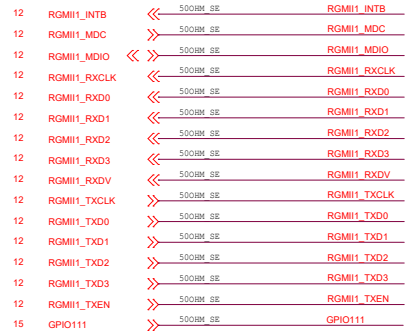
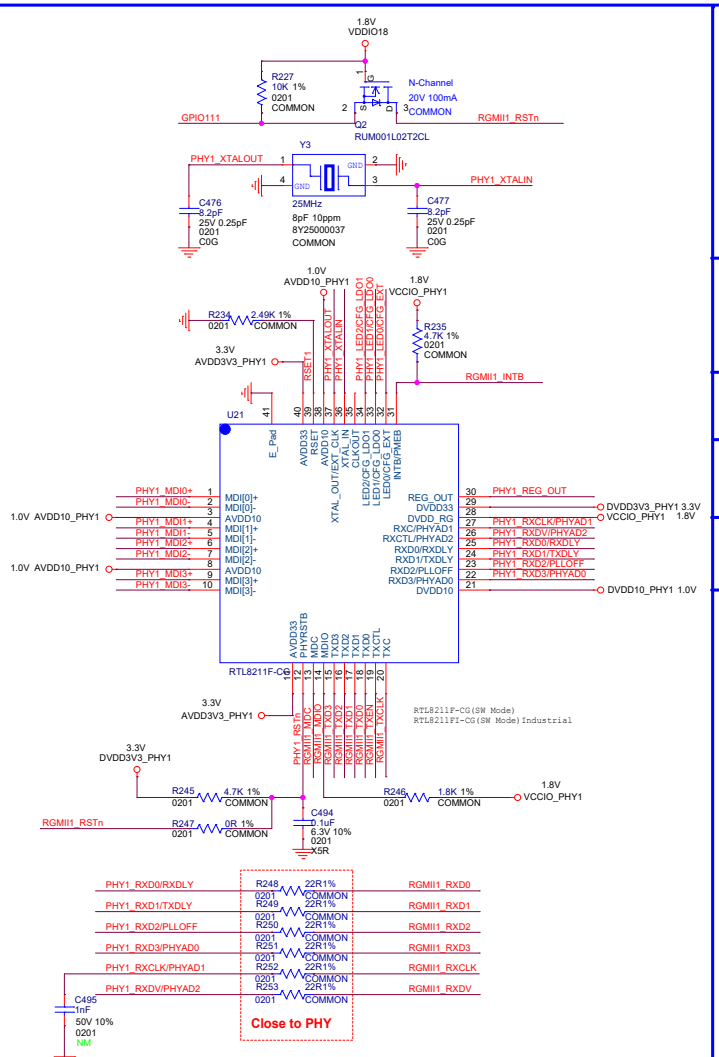
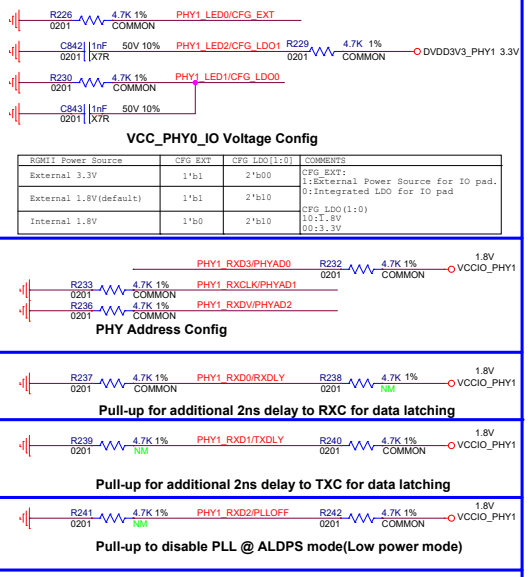
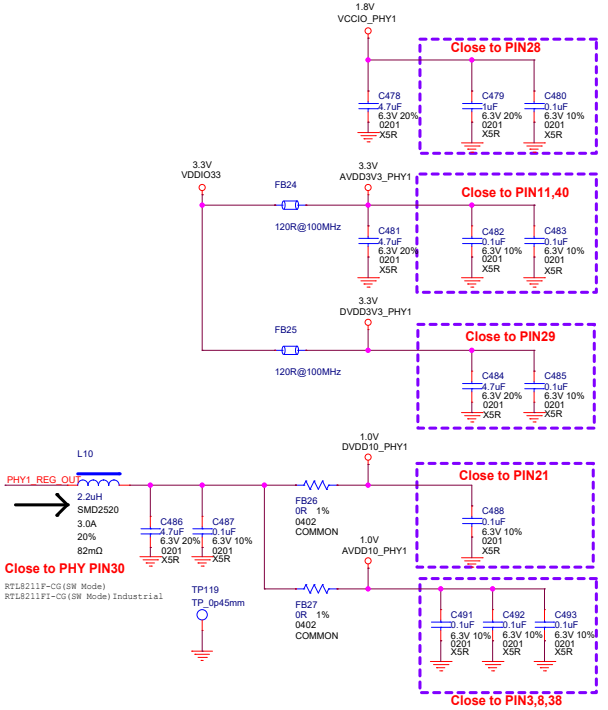






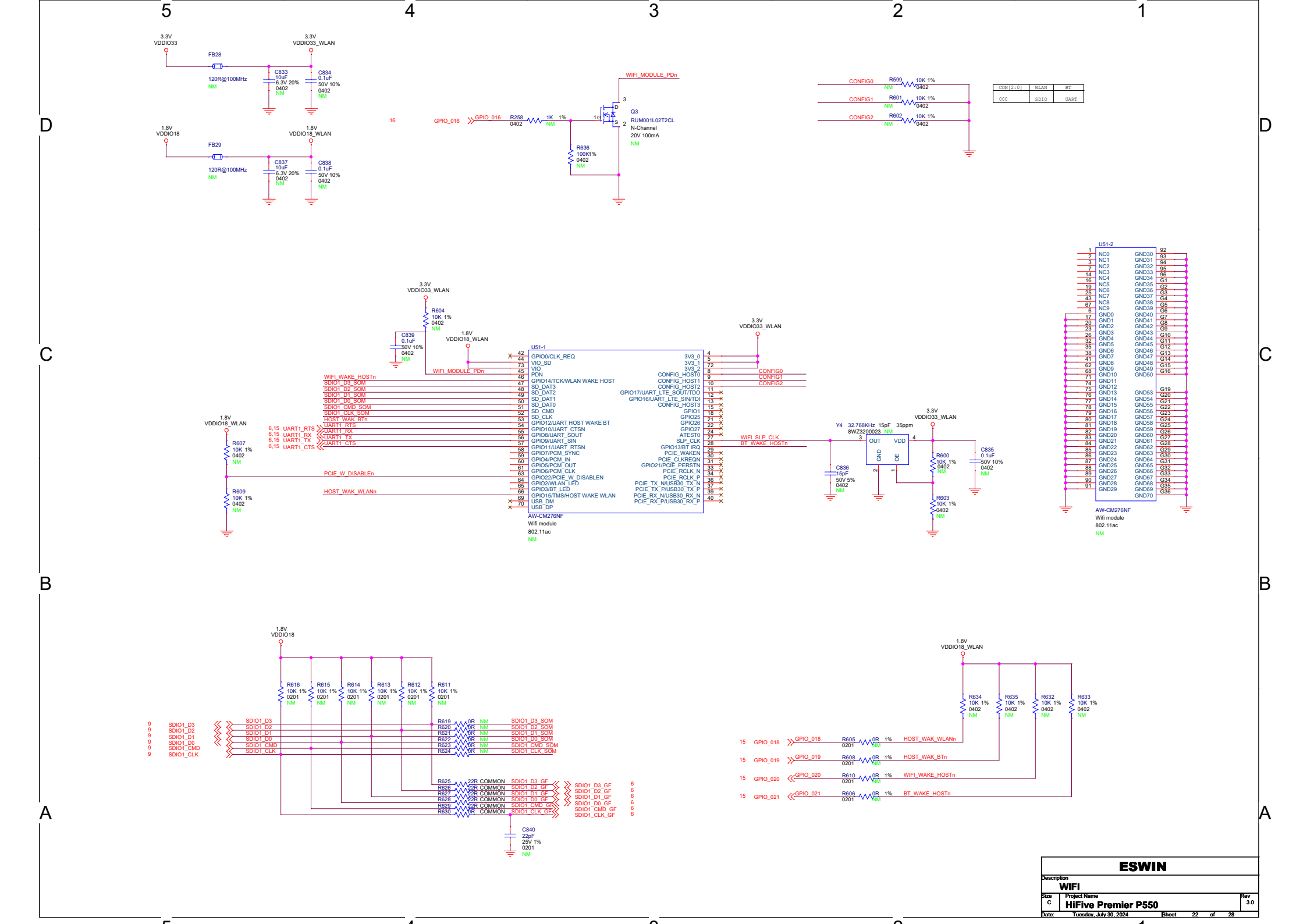


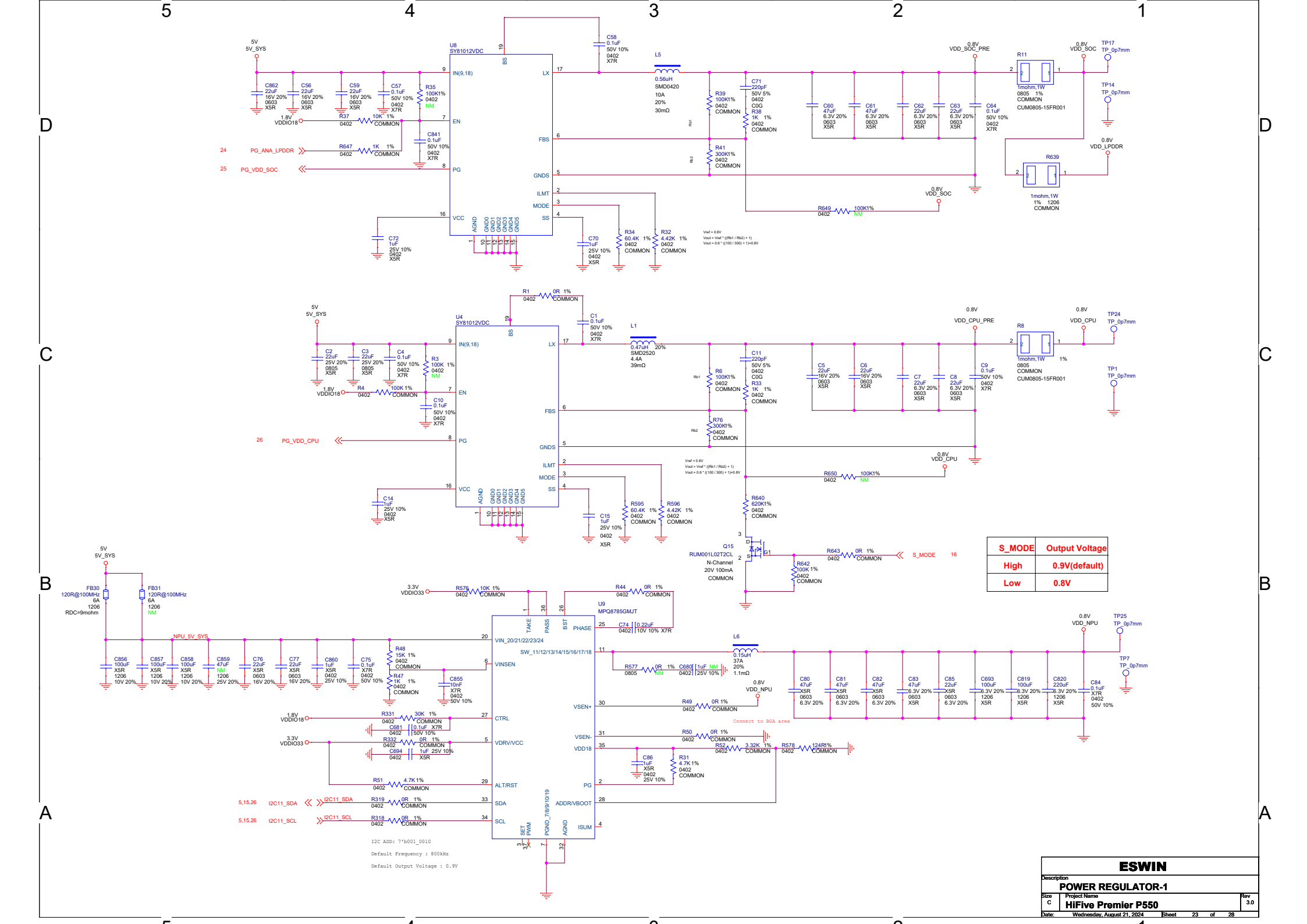
ESWIN

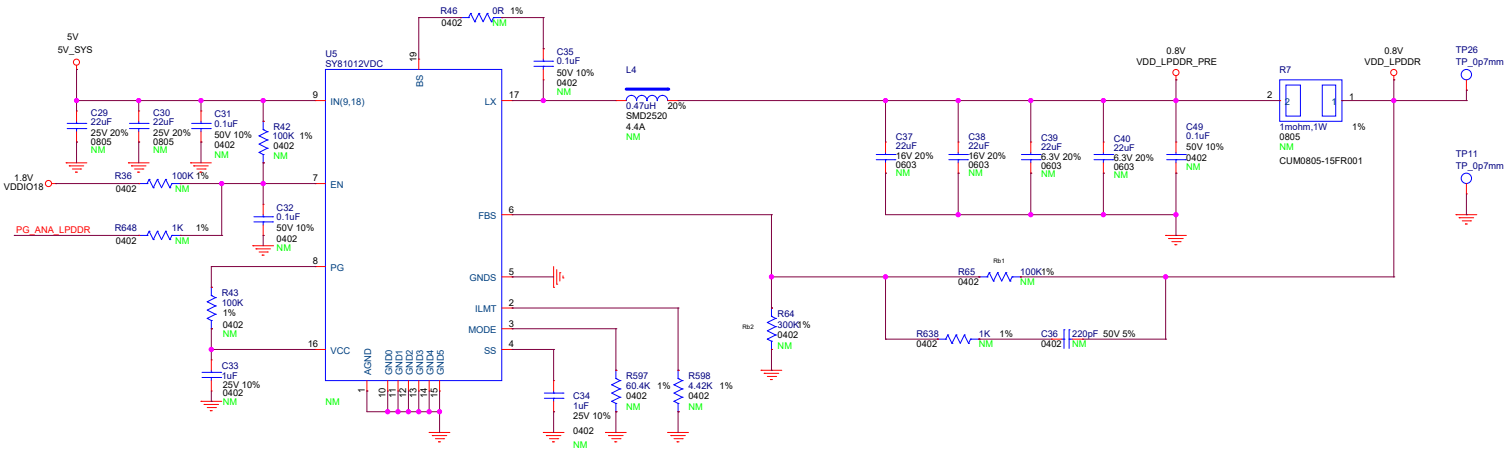
Description: ETHERNET-2

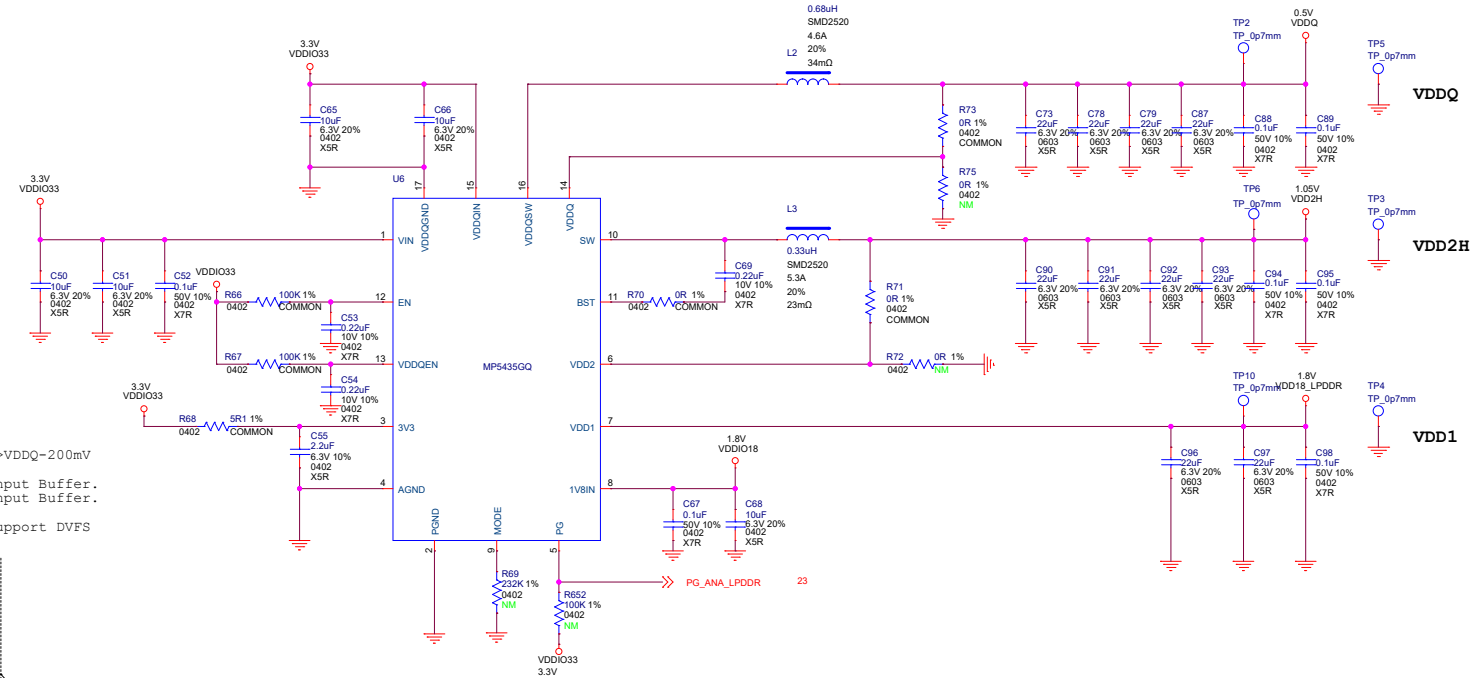
Size	Project Name	Rev
C	HiFive Premier P550	3.0

Date: Tuesday, July 30, 2024 Sheet 21 of 28

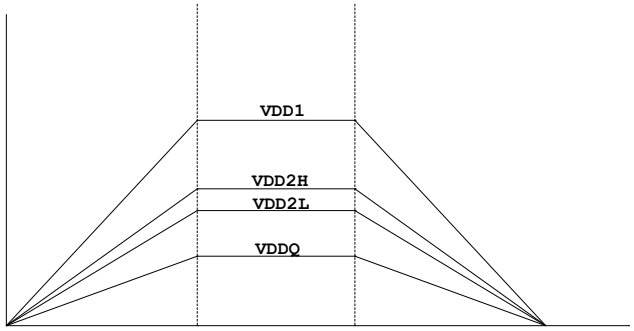

3.3V VDDIO33
3.3V VDDIO33_WLAN
FB28
120R@100MHz NM
C833 10uF 6.3V 20% 0402 NM
C834 0.1uF 50V 10% 0402 NM
1.8V VDDIO18
1.8V VDDIO18_WLAN
FB29
120R@100MHz NM
C837 10uF 6.3V 20% 0402 NM
C838 0.1uF 50V 10% 0402 NM
WIFI_MODULE_PDn
GPIO_016
R258 0402 1K 1% NM
Q3 RUM001L02T2CL N-Channel 20V 100mA NM
R636 100K1% 0402 NM
CONFIG0 R599 10K 1% 0402 NM
CONFIG1 R601 10K 1% 0402 NM
CONFIG2 R602 10K 1% 0402 NM
CON[2:0] WLAN BT
000 SDIO UART
R604 10K 1% 0402 NM
C839 0.1uF 50V 10% 0402 NM
U51-1
AW-CM276NF
Wifi module
802.11ac
NM
R607 10K 1% 0402 NM
R609 10K 1% 0402 NM
Y4 32.768KHz 15pF 35ppm 8WZ3200023 NM
C836 15pF 50V 5% 0402 NM
R600 10K 1% 0402 NM
R603 10K 1% 0402 NM
C835 0.1uF 50V 10% 0402 NM
U51-2
AW-CM276NF
Wifi module
802.11ac
NM
R616 10K 1% 0201 NM
R615 10K 1% 0201 NM
R614 10K 1% 0201 NM
R613 10K 1% 0201 NM
R612 10K 1% 0201 NM
R611 10K 1% 0201 NM
R619 0R NM
R620 0R NM
R621 0R NM
R622 0R NM
R623 0R NM
R624 0R NM
R625 22R COMMON
R626 22R COMMON
R627 22R COMMON
R628 22R COMMON
R629 22R COMMON
R630 0R COMMON
C840 22pF 25V 1% 0201 NM
R634 10K 1% 0402 NM
R635 10K 1% 0402 NM
R632 10K 1% 0402 NM
R633 10K 1% 0402 NM
R605 0R 1% 0201 NM
R608 0R 1% 0201 NM
R610 0R 1% 0201 NM
R606 0R 1% 0201 NM
ESWIN
Description WIFI
Size C
Project Name HiFive Premier P550
Rev 3.0
Date: Tuesday, July 30, 2024
Sheet 22 of 28


5V
5V_SYS
U8
SY81012VDC
IN(9,18)
EN
PG
VCC
BS
LX
FBS
GNDS
ILMT
MODE
SS
AGND
GND0
GND1
GND2
GND3
GND4
GND5
C862 22uF 16V 20% 0603 X5R
C56 22uF 16V 20% 0603 X5R
C59 22uF 16V 20% 0603 X5R
C57 0.1uF 50V 10% 0402 X7R
R35 100K1% 0402 NM
R37 10K 1% 0402 COMMON
1.8V VDDIO18
C841 0.1uF 50V 10% 0402 X7R
R647 1K 1% 0402 COMMON
24 PG_ANA_LPDDR
25 PG_VDD_SOC
C72 1uF 25V 10% 0402 X5R
C58 0.1uF 50V 10% 0402 X7R
L5 0.56uH SMD0420 10A 20% 30mΩ
R39 100K1% 0402 COMMON
R41 300K1% 0402 COMMON
C71 220pF 50V 5% 0402 C0G
R38 1K 1% 0402 COMMON
C70 1uF 25V 10% 0402 X5R
R34 60.4K 1% 0402 COMMON
R32 4.42K 1% 0402 COMMON
Vref = 0.6V
Vout = Vref * ((Rb1 / Rb2) + 1)
Vout = 0.6 * ((100 / 300) + 1)=0.8V
0.8V VDD_SOC_PRE
C60 47uF 6.3V 20% 0603 X5R
C61 47uF 6.3V 20% 0603 X5R
C62 22uF 6.3V 20% 0603 X5R
C63 22uF 6.3V 20% 0603 X5R
C64 0.1uF 50V 10% 0402 X7R
R11 1mohm,1W 0805 1% COMMON CUM0805-15FR001
0.8V VDD_SOC
TP17 TP_0p7mm
TP14 TP_0p7mm
R649 100K1% 0402 NM
R639 1mohm,1W 1% 1206 COMMON
0.8V VDD_LPDDR
U4
SY81012VDC
R1 0R 1% 0402 COMMON
C1 0.1uF 50V 10% 0402 X7R
L1 0.47uH 20% SMD2520 4.4A 39mΩ
C2 22uF 25V 20% 0805 X5R
C3 22uF 25V 20% 0805 X5R
C4 0.1uF 50V 10% 0402 X7R
R3 100K 1% 0402 NM
R4 100K 1% 0402 COMMON
C10 0.1uF 50V 10% 0402 X7R
26 PG_VDD_CPU
C14 1uF 25V 10% 0402 X5R
C15 1uF 25V 10% 0402 X5R
R595 60.4K 1% 0402 COMMON
R596 4.42K 1% 0402 COMMON
R6 100K1% 0402 COMMON
R33 1K 1% 0402 COMMON
C11 220pF 50V 5% 0402 C0G
R76 300K1% 0402 COMMON
C5 22uF 16V 20% 0603 X5R
C6 22uF 16V 20% 0603 X5R
C7 22uF 6.3V 20% 0603 X5R
C8 22uF 6.3V 20% 0603 X5R
C9 0.1uF 50V 10% 0402 X7R
0.8V VDD_CPU_PRE
R8 1mohm,1W 1% 0805 COMMON CUM0805-15FR001
0.8V VDD_CPU
TP24 TP_0p7mm
TP1 TP_0p7mm
R650 100K1% 0402 NM
R640 620K1% 0402 COMMON
Q15 RUM001L02T2CL N-Channel 20V 100mA COMMON
R643 0R 1% 0402 COMMON
S_MODE 16
R642 100K 1% 0402 COMMON
S_MODE | Output Voltage
High | 0.9V(default)
Low | 0.8V
FB30 120R@100MHz 6A 1206 RDC=9mohm
FB31 120R@100MHz 6A 1206 NM
NPU_5V_SYS
C856 100uF X5R 1206 10V 20%
C857 100uF X5R 1206 10V 20%
C858 100uF X5R 1206 10V 20%
C859 47uF X5R 1206 25V 20% NM
C76 22uF X5R 0603 16V 20%
C77 22uF X5R 0603 16V 20%
C860 1uF X5R 0402 25V 10%
C75 0.1uF X7R 0402 50V 10%
3.3V VDDIO33
R576 10K 1% 0402 COMMON
U9
MPQ8785GMJT
TAKE
PASS
BST
PHASE
R44 0R 1% 0402 COMMON
C74 0.22uF 0402 10V 10% X7R
VIN_20/21/22/23/24
SW_11/12/13/14/15/16/17/18
VINSEN
R48 15K 1% 0402 COMMON
R47 1K 1% 0402 COMMON
C855 10nF X7R 0402 50V 10%
CTRL
R331 30K 1% 0402 COMMON
C681 0.1uF X7R 0402 50V 10%
VDRV/VCC
R332 0R 1% 0402 COMMON
C694 1uF 25V 10% 0402 X5R
ALT/RST
R51 4.7K 1% 0402 COMMON
SDA
SCL
5,15,26 I2C11_SDA
5,15,26 I2C11_SCL
R319 0R 1% 0402 COMMON
R318 0R 1% 0402 COMMON
I2C ADD: 7'b001_0010
Default Frequency : 800kHz
Default Output Voltage : 0.9V
SET
PWM
PGND_7/8/9/10/19
AGND
ISUM
L6 0.15uH 37A 20% 1.1mΩ
R577 0R 1% 0805 NM
C680 1uF NM 0402 25V 10%
0.8V VDD_NPU
C80 47uF X5R 0603 6.3V 20%
C81 47uF X5R 0603 6.3V 20%
C82 47uF X5R 0603 6.3V 20%
C83 47uF X5R 0603 6.3V 20%
C85 22uF X5R 0603 6.3V 20%
C693 100uF X5R 1206 6.3V 20%
C819 100uF X5R 1206 6.3V 20%
C820 220uF X5R 1206 6.3V 20%
C84 0.1uF X7R 0402 50V 10%
TP25 TP_0p7mm
TP7 TP_0p7mm
VSEN+
VSEN-
VDD18
PG
ADDR/VBOOT
R49 0R 1% 0402 COMMON
Connect to BGA area
R50 0R 1% 0402 COMMON
R52 3.32K 1% 0402 COMMON
R578 124R1% 0402 COMMON
C86 1uF X5R 0402 25V 10%
R31 4.7K 1% 0402 COMMON
ESWIN
Description
POWER REGULATOR-1
Size C
Project Name
HiFive Premier P550
Rev 3.0
Date: Wednesday, August 21, 2024
Sheet 23 of 28





Power on/off Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.
In this design,tie VDD2L to VDD2H, not support DVFS



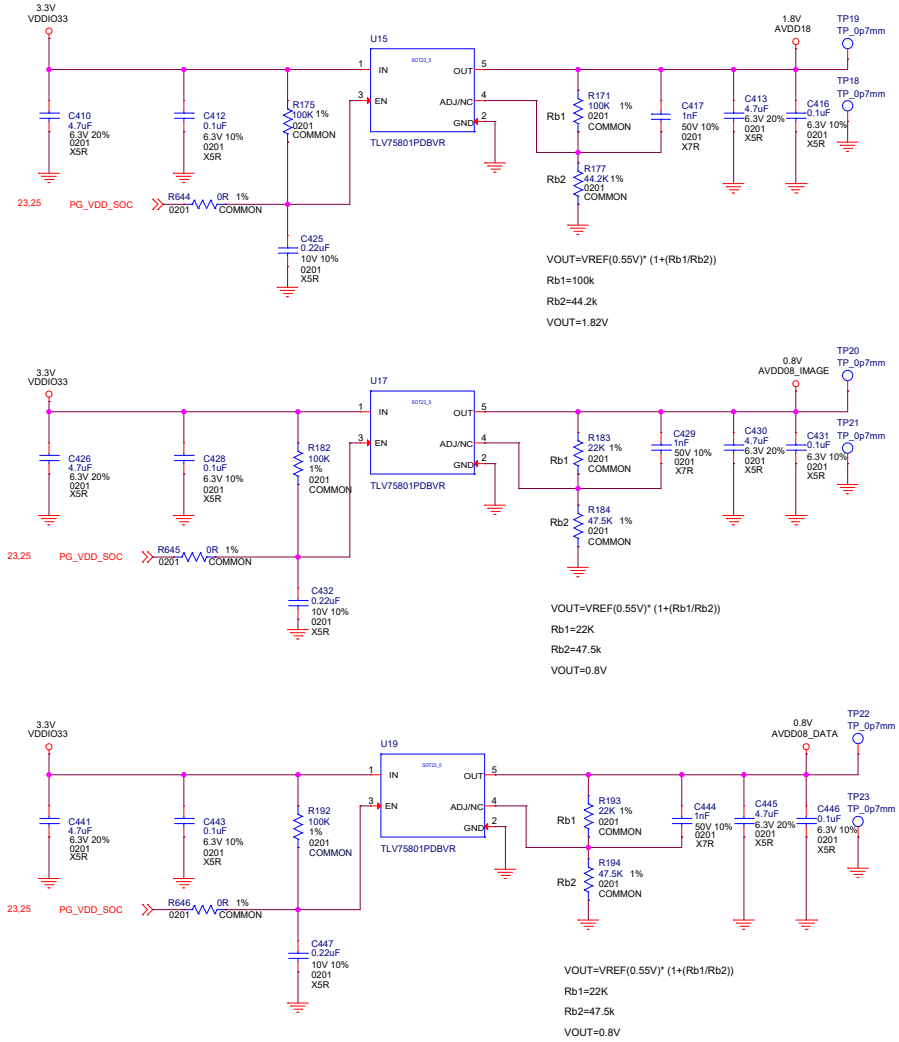
Ref	Value	VDD2	VDDQ	Description
R464	Float or 232K	1.065	0.505	LPDDR5
R464	100K	1.1	0.605	LPDDR4X/4

ESWIN

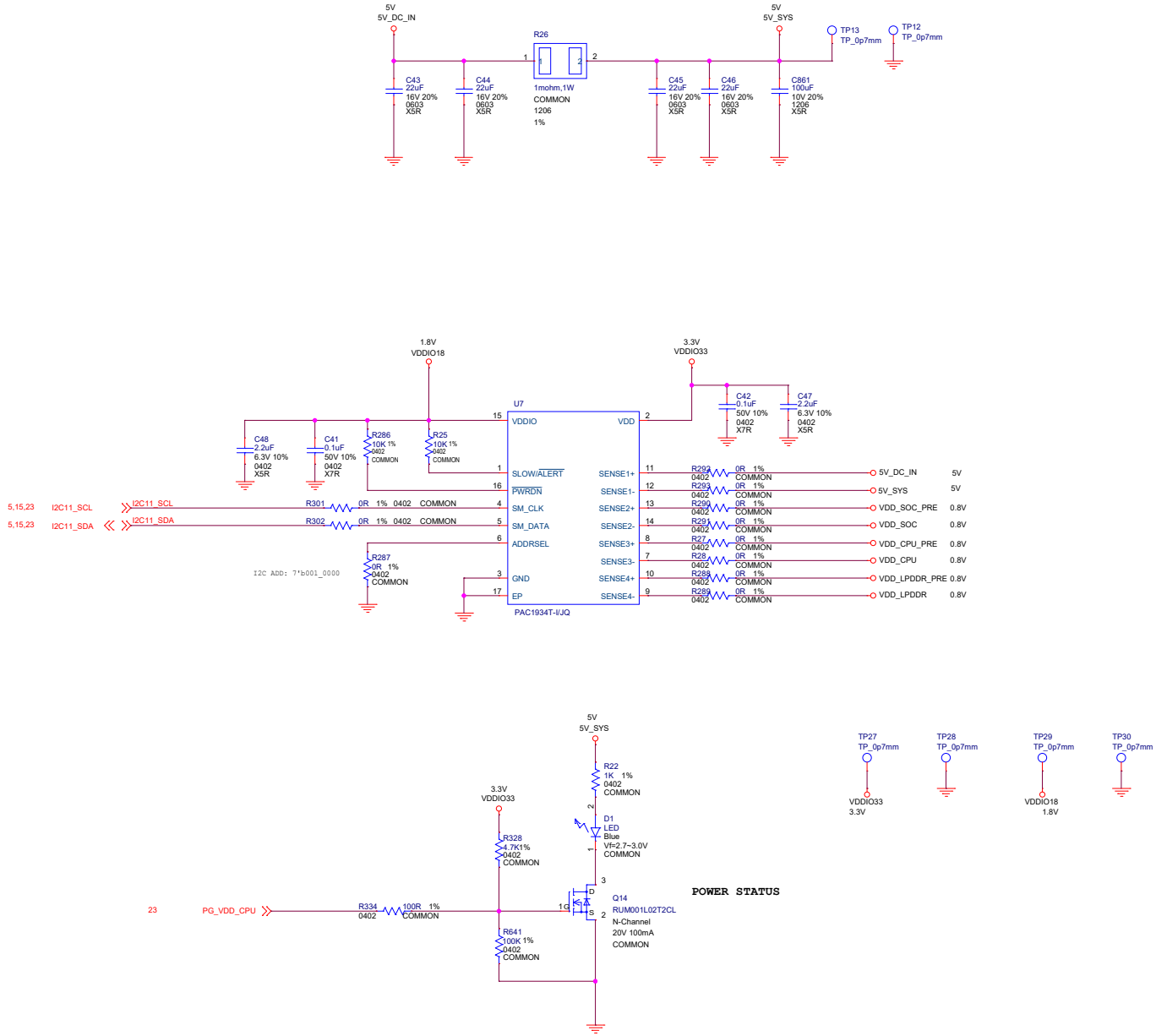
Description: **POWER REGULATOR-2**

Size: C | Project Name: **HiFive Premier P550** | Rev: 3.0

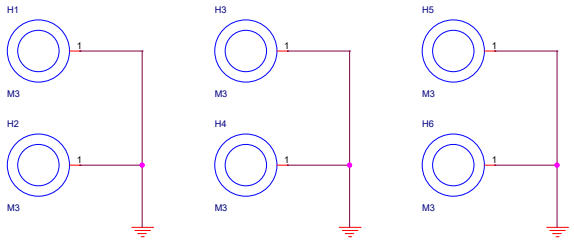
Date: Tuesday, July 30, 2024 | Sheet 24 of 28



ESWIN		
Description	POWER REGULATOR-3	
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
Date: Tuesday, July 30, 2024	Sheet 25 of 28	



ESWIN	
Description	POWER MONITOR
Size	C
Project Name	HiFive Premier P550
Rev	3.0
Date:	Tuesday, July 30, 2024
Sheet	26 of 28



ESWIN		
Description: MECHANICAL		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
Date: Tuesday, July 30, 2024	Sheet 27 of 28	

Revision History

Version	Issue Date	Author	Description
1.0	2024/03/08	Zhangwenqiu	Initial Release
2.0	2024/05/22	Zhangwenqiu	2.0 version release Fix issues
3.0	2024/07/30	Zhangwenqiu	1. Remove reserved DCDC U5 and related devices 2. Add C856,C857,C858,C860,C861,C862 ,FB30 for better power supply performance 3. Add R640 620K, R643 0R, for CPU 0.9V

ESWIN		
Description: REVERSION HISTORY		
Size: C	Project Name: HiFive Premier P550	Rev: 3.0
Date: Monday, August 26, 2024	Sheet 28 of 28	