

**ESWIN**

# EIC7700X SoC Technical Reference Manual

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## Change History

Version No	Date	Descriptions
V1.1	2024-1-31	

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## 7 Intelligent Accelerator

### 7.1 DSP

Please get in touch with ESWIN to request more detailed technical information.

[ibu\\_techsupport@eswincomputing.com>](mailto:<ibu_techsupport@eswincomputing.com>)

### 7.2 NPU

Please get in touch with ESWIN to request more detailed technical information.

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## 8 Video Input

### 8.1 Overview

The VI subsystem includes six Combo-PHYs, six CSI2-Hosts, and VICAPs, as well as two ISP8000s, DW200s, DVP2AXI, and Shutter modules. The Combo-PHYs are used to de-serialize sensor data and generate parallel data. The PHYs can be configured in MIPI, LVDS, SubLVDS, and IO modes. The CSI2-Hosts serve as controllers for MIPI, while the VICAPs serve as controllers for LVDS/HiSPi/SubLVDS. The ISP8000s are image processing modules. The DW200s are distortion correction modules. The DVP2AXI is a DMA module for image data write-in. The Shutter modules serve as synchronization control modules for primary and secondary cameras.

### 8.2 Block Diagram

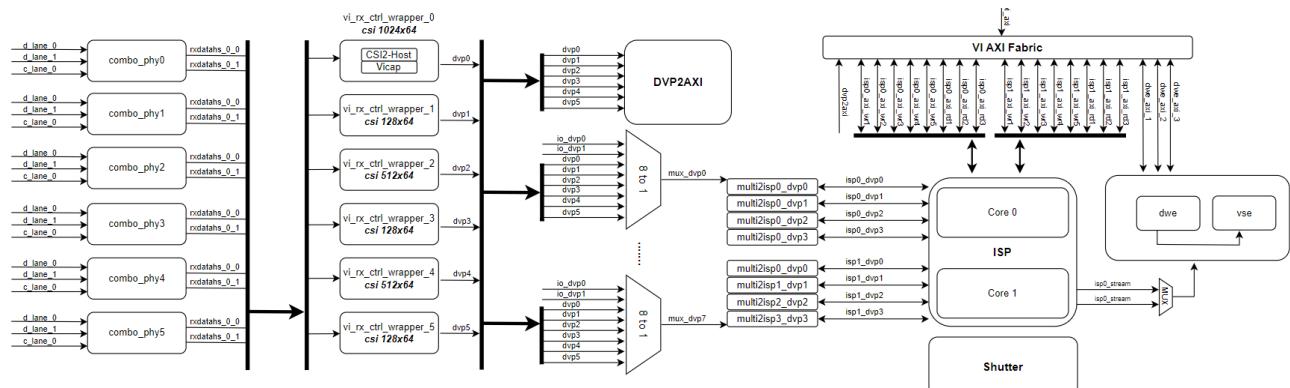


Figure 8-1 Video in block diagram

### 8.3 Function Description

#### 8.3.1 Combo PHY

Video In subsystem include 6 Combo PHY for Camera data input.

Key feature are:

- MIPI Alliance Specification for D-PHY Version 2.1 support
- MIPI Alliance Specification for C-PHY Version 1.2 support
- Shared analog pins implementation (10 pins for 2 data lanes / 1 clock lane in D-PHY and 9 pins for 2 trios in C-PHY)
- HS RX Passive Equalization and offset cancellation

- Flexible configuration clock (17-38.4 MHz)
- Advanced Peripheral Bus (APB) interface to access test control registers
- Mandatory external reference resistor (200 ohm) for calibration support
- PHY testability
- Power Collapsing
- SUB\_LVDS/SLVDS/HiSPi
- SUB\_LVDS/SLVDS/HiSPi Aggregation Mode (PHY can work as standalone or as aggregation mode):
  - rx2l+rx2l=rx4l)
- GPIO

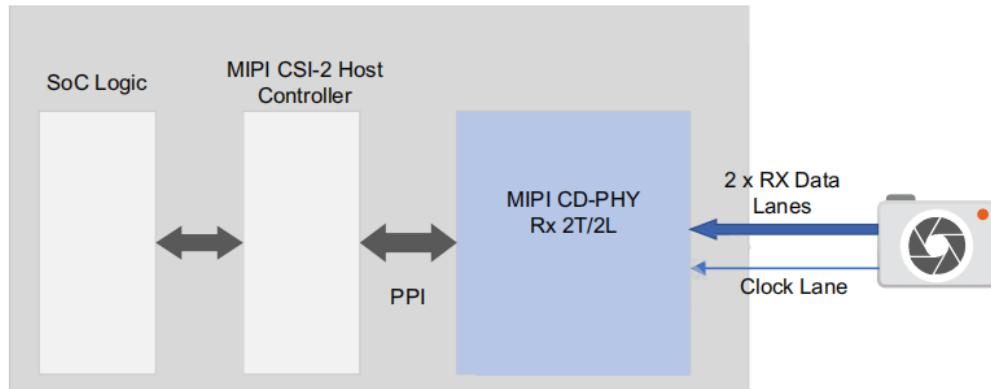


Figure 8-2 MIPI D-PHY System-Level Block Diagram

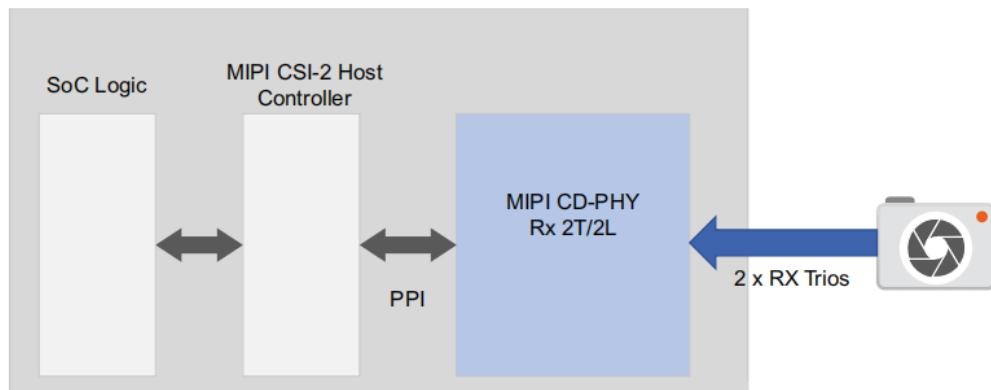


Figure 8-3 MIPI C-PHY System-Level Block Diagram

### 8.3.2 CSI2 Host

Video In subsystem include 6 CSI2 controller, it receives data from a CSI2 compliant camera sensor. An RX DPHY or Combo PHY acts as the physical layer.

Key feature are:

- Compliant with MIPI Alliance standards
- PHY-Protocol Interface(PPI) to MIPI DPHY, Supports PPI-8/PPI-16
- PHY-Protocol Interface(PPI) to MIPI CPHY, Supports PPI-8/PPI-16
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets

- 32-bit or 64-bit Image Data Interface(IDI) delivering data formatted as recommended in CSI-2 Specification
- Error detection and correction
- PPI Data Lanes De-Skew capability
- PPI Pattern Generator delivering data formatted
- Data scrambling for electromagnetic interference mitigation

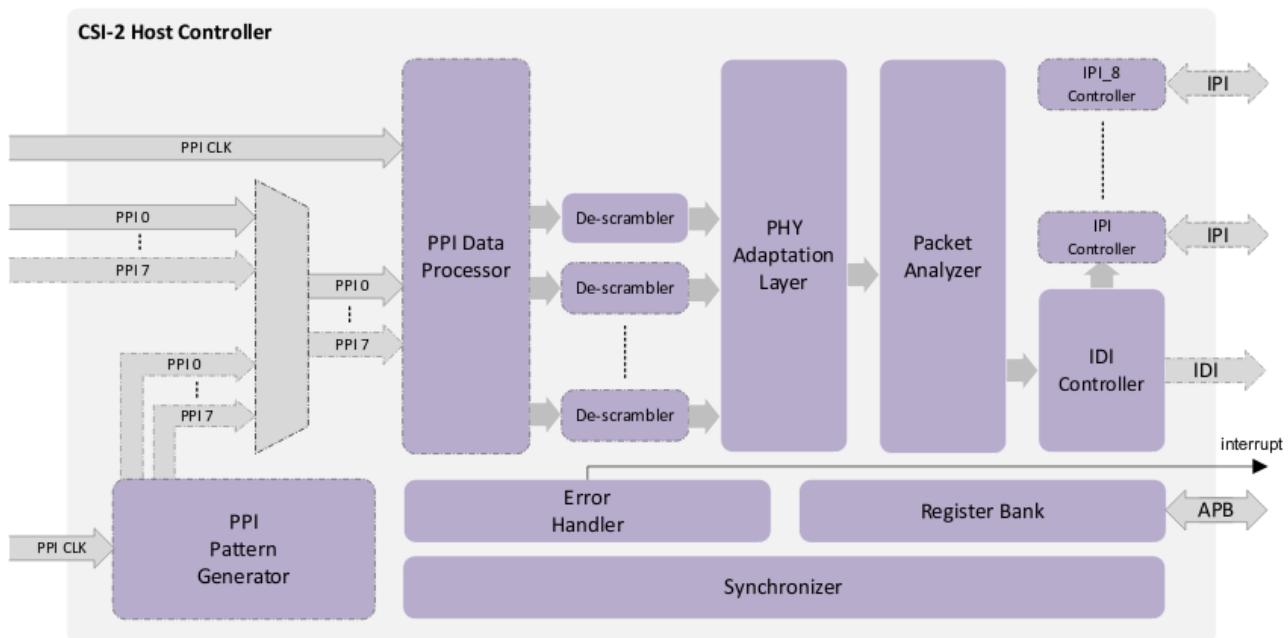


Figure 8-4 CSI-2 Host Block Diagram

### 8.3.3 VICAP

It converts the Combo-PHY serial video data received into 8-bit parallel data per clock for splitting and splicing. Then it extracts the synchronization code, decodes the video pixel data, and synchronizes the multi-Lane parallel word data, which contains all data of the HiSPi, SLVS, and SUB-LVDS protocols (including synchronization codes and other invalid information). The current module performs protocol analysis, separates the synchronization code and invalid information, and only sends the valid pixel and valid embedded data to the ISP end or writes them to memory through the DVP2AXI module. HiSPiRX specifically analyzes various sub-modes of the HiSPi protocol and outputs AIL (without crop and line tail invalid data discard); SLVS RX is used to parse the SLVS SUB-LVDS protocol and output pixel data and info data as well as OB data (without crop and line tail invalid data discard); crop dvp out mainly performs data serialization/deserialization conversion, performs crop and line tail invalid data discard, and outputs effective data with ID through the DVP interface.

Key feature are:

- Supports SUB-LVDS, SLVS, and HiSPi protocols.
- Supports pixel data bit widths of 8bit/10bit/12bit/14bit/16bit configurable.
- Supports synchronization code MSB/LSB and pixel data MSB/LSB configurable.
- Supports 1Lane/2Lane/4Lane/8Lane modes.
- Supports 5-word synchronization code in SLVS and SUB-LVDS modes (requires Lane replication transmission)

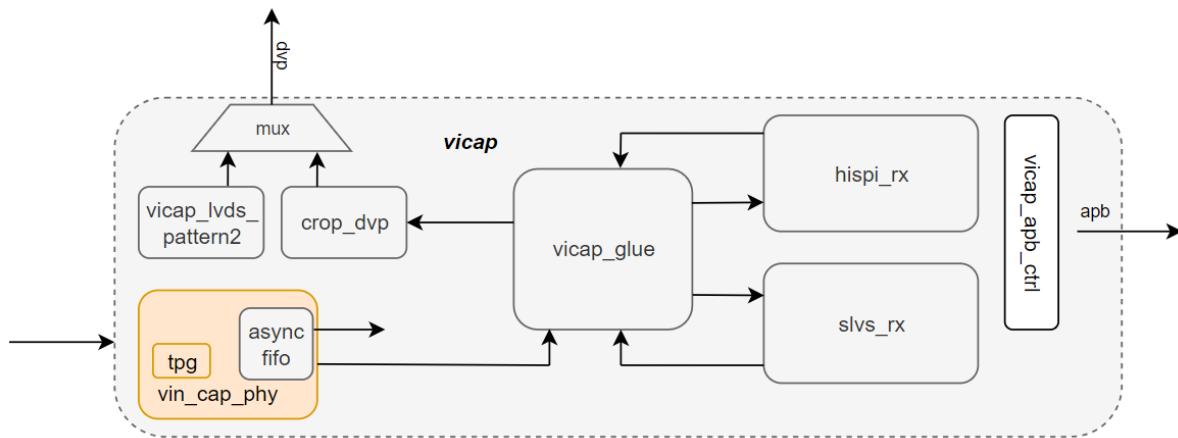


Figure 8-5 VICAP Block Diagram

### 8.3.4 DVP2AXI

Key feature are:

- Support for 6 simultaneous DVP interface inputs, of which 2 can be input from IO DVP
- Support for up to 3 virtual channels of multi-channel data input on 1 DVP, i.e. HDR mode
- Support for RAW8bit/10bit/12bit/14bit/16bit, RGB888, YUV8bit/10bit data input formats
- Support for YUV/RGB packed format stored in DDR
- Support for AXI outstanding with a maximum of 256 configurable options, AXI burst length with a maximum of 8/16, and data bit width of 128bit
- The starting address is aligned to 16 bytes, and support for writing embedded data to different address areas
- Support for virtual channel frame write complete interrupt and non-complete frame detection interrupt
- Support for exception handling, such as ensuring the integrity of AXI bus transmission during reset

### 8.3.5 Shutter

The Shutter module is mainly used in industrial inspection with two sensors for binocular vision. It is controlled by the SOC terminal to expose simultaneously and transmit data simultaneously to ensure synchronization between the two sensors.

Key feature are:

- XTRIG output mode supports external IO input Pulse/Level trigger, and the output pulse width of Pulse mode can be configured
- XTRIG output mode supports register configuration trigger XTRIG, and the output pulse width can be configured
- XVS and XHS output modes support VMAX and HMAX configurable, and XHS duty cycle can be configured
- XHS and XTRIG output modes support XHS features configurable, and XTRIG and XHS phase difference can be configured
- Supports loop count of 1 to 1024 configurable, or can configure infinite loop
- Supports two sets of configuration registers pipeline to generate corresponding output signals
- Supports polarity and phase half-cycle delay configuration for XTRIG and XVS output signals
- Supports XTRIG and XVS sharing the same PAD with selectable options to reduce chip peripheral connections
- Supports completion (sequential output or completion of all outputs) interrupt and Stop completion interrupt, idle status can be queried
- Supports rising edge/falling edge (configurable option) interrupt generation for XTRIG and XVS

- Supports software configuration of Stop end task, and ensures the current frame timing is intact

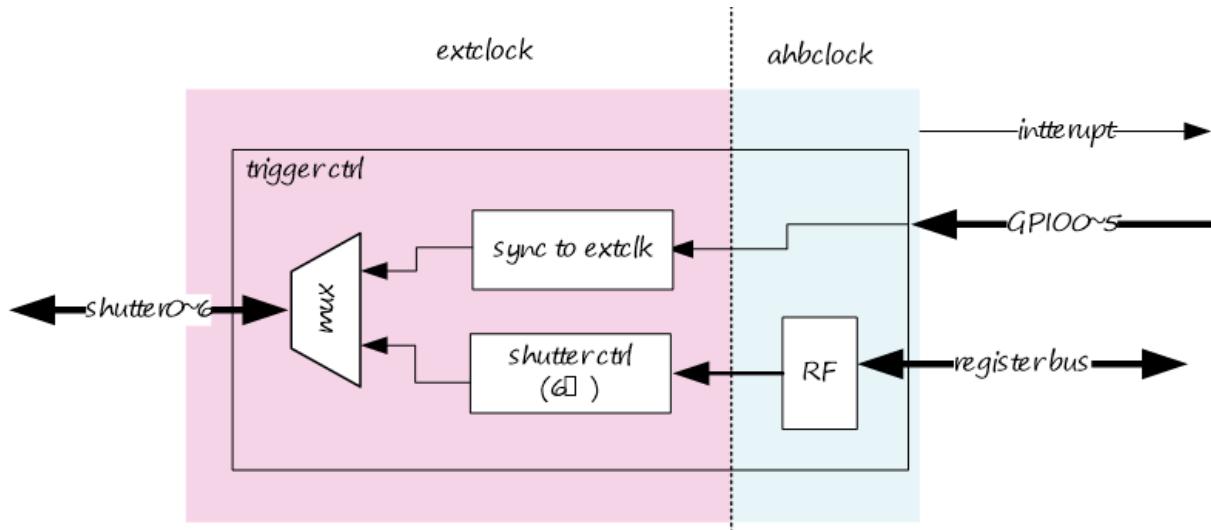


Figure 8-6 Shutter Block Diagram

It includes two parts. First, the shutter can be controlled by the GPIO of the chip through the upper computer, or it can be controlled by the AP inside the SOC. The specific shutter timing is determined by the register configuration. The hardware provides loop mode and free running mode, which outputs a fixed shutter control sequence according to the timing and frequency configured by the software. It can also be configured by the software to run freely. The shutter can be stopped by the software, and the hardware ensures the integrity of the shutter controlled by the current output frame.

#### 8.4 Register description

Sub Module	Address Range	Memory Region Size
vi_common_csr	0x5103_0000~0x5103_1fff	8K
shutter_ctrl	0x5103_2000~0x5103_3fff	8K
vi_dvp2axi	0x5103_4000~0x5103_7fff	16K
vicap0	0x5103_8000~0x5103_bfff	16K
vicap1	0x5103_c000~0x5103_ffff	16K
vicap2	0x5104_0000~0x5104_3fff	16K
vicap3	0x5104_4000~0x5104_7fff	16K
vicap4	0x5104_8000~0x5104_bfff	16K
vicap5	0x5104_c000~0x5104_ffff	16K
csi2 host0	0x5105_0000~0x5105_ffff	64K
csi2 host1	0x5106_0000~0x5106_ffff	64K
csi2 host2	0x5107_0000~0x5107_ffff	64K
csi2 host3	0x5108_0000~0x5108_ffff	64K
csi2 host4	0x5109_0000~0x5109_ffff	64K
csi2 host5	0x510a_0000~0x510a_ffff	64K
reserved	0x510b_0000~0x510b_ffff	64K

Sub Module	Address Range	Memory Region Size
combo-phy0	0x510c_0000~0x510d_ffff	128K
combo-phy1	0x510e_0000~0x510f_ffff	128K
combo-phy2	0x5110_0000~0x5111_ffff	128K
combo-phy3	0x5112_0000~0x5113_ffff	128K
combo-phy1	0x5114_0000~0x5115_ffff	128K
combo-phy1	0x5116_0000~0x5117_ffff	128K
reserved	0x5118_0000~0x511f_ffff	512K

#### 8.4.1 Common CSR

CSR Name	Offset	Access	Reset Value	Field Name	Description
phy_connect_mod_e	16'h0000	RO		Reserved	
		RW	1'd0	imx327_hdr_raw12_5	imx327hdrraw125enable,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_en_5	imx327hdrenable5,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_raw12_4	imx327hdrraw124enable,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_en_4	imx327hdrenable4,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_raw12_3	imx327hdrraw123enable,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_en_3	imx327hdrenable3,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_raw12_2	imx327hdrraw122enable,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_en_2	imx327hdrenable2,whenuse,needtasetthisbitto1.
		RW	1'd0	imx327_hdr_raw12_1	imx327hdrraw121enable,whenuse,needtasetthisbitto1.

CSR Name	Offset	Access	Reset Value	Field Name	Description
					sbitto1.
		RW	1'd0	imx327_hdr_en_1	imx327hdrenable1,whe nuse,needtasetthisbitto 1.
		RW	1'd0	imx327_hdr_raw12_0	imx327hdrraw120enabl e,whenuse,needtasetthi sbitto1.
		RW	1'd0	imx327_hdr_en_0	imx327hdrenable0,whe nuse,needtasetthisbitto 1.
		RW	1'd0	mipi_csi_tpg_clock_mu x_en	mipicsitestpatternclock muxenable,whenusetpg ,needtasetthisbitto1.
		RW	3'd5	phy_mode	phyconnectionmodeset tings: 0:phy0,1,2,3for8laneson esensor,phy4,5for4lane sonsensor 1:phy0,1,2,3for8lanesse nsor,phy4for2lanessens or,phy5for2lanessens or 2:phy0,1for4lanessens or,phy2,3for4lanessens or,phy4,5for4lanessens or 3:phy0,1for4lanessens or,phy2,3for4lanessens or,phy4for2lanessens or,phy5for2lanessens or 4:phy0,1for4lanessens or,phy2for2lanessens or,phy3for2lanessens or,phy4for2lanessens or,phy5for2lanessens or 5.phy0for2lanessens or,phy1for2lanessens or,phy2for2lanessens orphy3for2lanessens or,phy4for2lanessens orphy5for2lanessens or [note]8lanesjustforsub vds/slvs/hispi,mipicsic an'tsupport8lanes

CSR Name	Offset	Access	Reset Value	Field Name	Description
controller_sel	16'h0004	RO		Reserved	
		RW	1'd0	csi5_vicap5_sel	mipicscontrollerandmulti protocol controller(sub_lvds/slvs/hispi)select dataouttovi 0:mipicsi5output 1:multiprotocol5output
		RW	1'd0	csi4_vicap4_sel	mipicscontrollerandmulti protocol controller(sub_lvds/slvs/hispi)select dataouttovi 0:mipicsi4output 1:multiprotocol4output
		RW	1'd0	csi3_vicap3_sel	mipicscontrollerandmulti protocol controller(sub_lvds/slvs/hispi)select :dataouttovi 0:mipicsi3output 1:multiprotocol3output
		RW	1'd0	csi2_vicap2_sel	mipicscontrollerandmulti protocol controller(sub_lvds/slvs/hispi)select :dataouttovi 0:mipicsi2output 1:multiprotocol2output
		RW	1'd0	csi1_vicap1_sel	mipicscontrollerandmulti protocol controller(sub_lvds/slvs/hispi)select : 0:mipicsi1output 1:multiprotocol1output
		RW	1'd0	csi0_vicap0_sel	mipicscontrollerandmulti protocol controller(sub_lvds/slvs/hispi)select :dataouttovi 0:mipicsi0output 1:multiprotocol0output
isp_dvp_sel	16'h0008	RO		Reserved	

CSR Name	Offset	Access	Reset Value	Field Name	Description
		RW	1'd0	io_dvp1_valid_pol	io_dvp1datavalidpolarity 1'b0:highactive 1'b1:lowactive
		RW	1'd0	io_dvp1_hsync_pol	io_dvp1hsyncpolarity 1'b0:highactive 1'b1:lowactive
		RW	1'd0	io_dvp1_vsync_pol	io_dvp1vsyncpolarity 1'b0:highactive 1'b1:lowactive
		RW	1'd0	io_dvp0_valid_pol	io_dvp0datavalidpolarity 1'b0:highactive 1'b1:lowactive
		RW	1'd0	io_dvp0_hsync_pol	io_dvp0hsyncpolarity 1'b0:highactive 1'b1:lowactive
		RW	1'd0	io_dvp0_vsync_pol	io_dvp0vsyncpolarity 1'b0:highactive 1'b1:lowactive
		RW	3'd0	isp1_dvp3_sel	isp1dvp3inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1
		RW	3'd0	isp1_dvp2_sel	isp1dvp2inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1

CSR Name	Offset	Access	Reset Value	Field Name	Description
		RW	3'd0	isp0_dvp3_sel	isp0dvp3inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1
		RW	3'd0	isp0_dvp2_sel	isp0dvp2inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1
		RW	3'd0	isp1_dvp1_sel	isp1dvp1inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1
		RW	3'd0	isp1_dvp0_sel	isp1dvp0inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1

CSR Name	Offset	Access	Reset Value	Field Name	Description
		RW	3'd0	isp0_dvp1_sel	isp0dvp1inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1
		RW	3'd0	isp0_dvp0_sel	isp0dvp0inputselect: 0:controller0 1:controller1 2:controller2 3:controller3 4:controller4 5:controller5 6:io_dvp0 7:io_dvp1
isp0_dvp0_size	16'h000c	RW	16'd480	isp0_dvp0_height	isp0dvp0height
		RW	16'd640	isp0_dvp0_width	isp0dvp0width
isp0_dvp1_size	16'h0010	RW	16'd480	isp0_dvp1_height	isp0dvp1height
		RW	16'd640	isp0_dvp1_width	isp0dvp1width
isp1_dvp0_size	16'h0014	RW	16'd480	isp1_dvp0_height	isp1dvp0height
		RW	16'd640	isp1_dvp0_width	isp1dvp0width
isp1_dvp1_size	16'h0018	RW	16'd480	isp1_dvp1_height	isp1dvp1height
		RW	16'd640	isp1_dvp1_width	isp1dvp1width
multi2isp_blank	16'h001c	RO		Reserved	
		RW	8'd80	vblank_alm	vblankalarmthreshold
		RW	8'd8	hblank_alm	hblankalarmthreshold

CSR Name	Offset	Access	Reset Value	Field Name	Description
			0		
multi2isp0_dvp0	16'h0020	RO		Reserved	
		RW	3'd4	vh_gap_mul2isp0_dvp0	outputhsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp0_dvp0	0:output=input 1:output=invert(input)
		RW	4'd0	shift_bit_mul2isp0_dvp0	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp0_dvp0	0:upalign 1:downalign
multi2isp0_dvp1	16'h0024	RO		Reserved	
		RW	3'd4	vh_gap_mul2isp0_dvp1	outputhsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp0_dvp1	0:output=input 1:output=invert(input)
		RW	4'd0	shift_bit_mul2isp0_dvp1	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp0_dvp1	0:upalign 1:downalign
multi2isp1_dvp0	16'h0028	RO		Reserved	
		RW	3'd4	vh_gap_mul2isp1_dvp0	outputhsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp1_dvp0	0:output=input 1:output=invert(input)

CSR Name	Offset	Access	Reset Value	Field Name	Description
		RW	4'd0	shift_bit_mul2isp1_dvp0	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp1_dvp0	0:upalign 1:downalign
multi2isp1_dvp1	16'h002c	RO		Reserved	
		RW	3'd4	vh_gap_mul2isp1_dvp1	outputsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp1_dvp1	0:output=input 1:output=invert(input)
		RW	4'd0	shift_bit_mul2isp1_dvp1	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp1_dvp1	0:upalign 1:downalign
disable_isp_0	16'h0030	RO		Reserved	
		RW	1'd0	disable_isp_0	isp0disable
disable_isp_1	16'h0034	RO		Reserved	
		RW	1'd0	disable_isp_1	isp1disable
dewarp_start	16'h0038	RO		Reserved	
		RW	1'd0	dewarp_start	dewarpstartregister,not needtowrite
on_stream_sel	16'h003c	RO		Reserved	
		RW	1'd0	on_stream_sel	dewarponstreaminterfaceselect. 0:fromISP0 1:fromISP1
vi_clk_en	16'h0040	RO		Reserved	
		RW	1'd0	dvp2axi_dvp_clk_en	dvp2axiinternaldvpcloc

CSR Name	Offset	Access	Reset Value	Field Name	Description
					kenable
		RW	1'd0	isp1_dvp3_clk_en	isp1dvp3clockenable
		RW	1'd0	isp1_dvp2_clk_en	isp1dvp2clockenable
		RW	1'd0	isp0_dvp3_clk_en	isp0dvp3clockenable
		RW	1'd0	isp0_dvp2_clk_en	isp0dvp2clockenable
		RW	1'd0	ctrl5_dvp_clk_en	ctrl5dvpclockenable
		RW	1'd0	ctrl4_dvp_clk_en	ctrl4dvpclockenable
		RW	1'd0	ctrl3_dvp_clk_en	ctrl3dvpclockenable
		RW	1'd0	ctrl2_dvp_clk_en	ctrl2dvpclockenable
		RW	1'd0	ctrl1_dvp_clk_en	ctrl1dvpclockenable
		RW	1'd0	ctrl0_dvp_clk_en	ctrl0dvpclockenable
		RW	1'd0	isp1_dvp1_clk_en	isp1dvp1clockenable
		RW	1'd0	isp1_dvp0_clk_en	isp1dvp0clockenable
		RW	1'd0	isp0_dvp1_clk_en	isp0dvp1clockenable
		RW	1'd0	isp0_dvp0_clk_en	isp0dvp0clockenable
		RW	1'd0	dewarp_clk_en	dewarpclockenable
		RW	1'd0	isp1_clk_en	isp1coreclockenable
		RW	1'd0	isp0_clk_en	isp0coreclockenable
csi_combo_phy_id_err	16'h0044	RO		Reserved	
		RO	1'd0	csi5_id_err	csi5controllervirtualchaneldataoverlap
		RO	1'd0	csi4_id_err	csi4controllervirtualchaneldataoverlap
		RO	1'd0	csi3_id_err	csi3controllervirtualchaneldataoverlap
		RO	1'd0	csi2_id_err	csi2controllervirtualchaneldataoverlap
		RO	1'd0	csi1_id_err	csi1controllervirtualchaneldataoverlap
		RO	1'd0	csi0_id_err	csi0controllervirtualchaneldataoverlap
vi_cmn_int_en	16'h0048	RO		Reserved	
		RW	16'd0	cmn_int_en	interruptenable

CSR Name	Offset	Access	Reset Value	Field Name	Description
vi_cmn_int_mask	16'h004c	RO		Reserved	
		RW	16'd0	cmn_int_mask	interruptmask
vi_cmn_int_clear	16'h0050	RO		Reserved	
		W1P	16'd0	cmn_int_clr	intteruptclear
vi_cmn_int_status	16'h0054	RO		Reserved	
		RO	16'd0	cmn_int_st	intteruptstatus: bit0:multi2isp0dvp0hblanklessthanhblankthreshold bit1:multi2isp0dvp0vblanklessthanhblankthreshold bit2:multi2isp0dvp1hblanklessthanhblankthreshold bit3:multi2isp0dvp1vblanklessthanhblankthreshold bit4:multi2isp1dvp0hblanklessthanhblankthreshold bit5:multi2isp1dvp0vblanklessthanhblankthreshold bit6:multi2isp1dvp1hblanklessthanhblankthreshold bit7:multi2isp1dvp1vblanklessthanhblankthreshold bit8:multi2isp0dvp2hblanklessthanhblankthreshold bit9:multi2isp0dvp2vblanklessthanhblankthreshold bit10:multi2isp0dvp3hblanklessthanhblankthreshold

CSR Name	Offset	Access	Reset Value	Field Name	Description
					shold bit11:multi2isp0dvp3vb lanklessthanhblankthreshold bit12:multi2isp1dvp2hb lanklessthanhblankthreshold bit13:multi2isp1dvp2vb lanklessthanhblankthreshold bit14:multi2isp1dvp3hb lanklessthanhblankthreshold bit15:multi2isp1dvp3vb lanklessthanhblankthreshold
mul2isp0_dvp0_status	16'h0058	RO		Reserved	
		RO	8'd0	hblank_err_mul2isp0_dvp0	multi2isp0dvp0hblankerror
		RO	8'd0	vblank_err_mul2isp0_dvp0	multi2isp0dvp0vblankerror
mul2isp0_dvp1_status	16'h005c	RO		Reserved	
		RO	8'd0	hblank_err_mul2isp0_dvp1	multi2isp0dvp1hblankerror
		RO	8'd0	vblank_err_mul2isp0_dvp1	multi2isp0dvp1vblankerror
mul2isp1_dvp0_status	16'h0060	RO		Reserved	

CSR Name	Offset	Access	Reset Value	Field Name	Description
		RO	8'd0	hblank_err_mul2isp1_dvp0	multi2isp1dvp0hblankerr
		RO	8'd0	vblank_err_mul2isp1_dvp0	multi2isp1dvp0vblankerr
mul2isp1_dvp1_status	16'h0064	RO		Reserved	
		RO	8'd0	hblank_err_mul2isp1_dvp1	multi2isp1dvp1hblankerr
		RO	8'd0	vblank_err_mul2isp1_dvp1	multi2isp1dvp1vblankerr
phy_pclk_cfg	16'h0068	RO		Reserved	
		RO	1'd0	cfg_done	cfgclockgeneratedonestate
		RW	16'd4	divider_cfg	phypclkdivider,defaultis4div,canbeeendividerclock
dvp0_cnt_status	16'h006c	RO	16'd0	dvp0_row_cnt	dvp0inputrowcnt
		RO	16'd0	dvp0_col_cnt	dvp0inputcolcnt
dvp1_cnt_status	16'h0070	RO	16'd0	dvp1_row_cnt	dvp1inputrowcnt
		RO	16'd0	dvp1_col_cnt	dvp1inputcolcnt
dvp2_cnt_status	16'h0074	RO	16'd0	dvp2_row_cnt	dvp2inputrowcnt
		RO	16'd0	dvp2_col_cnt	dvp2inputcolcnt
dvp3_cnt_status	16'h0078	RO	16'd0	dvp3_row_cnt	dvp3inputrowcnt
		RO	16'd0	dvp3_col_cnt	dvp3inputcolcnt
dvp4_cnt_status	16'h007c	RO	16'd0	dvp4_row_cnt	dvp4inputrowcnt
		RO	16'd0	dvp4_col_cnt	dvp4inputcolcnt
dvp5_cnt_status	16'h0080	RO	16'd0	dvp5_row_cnt	dvp5inputrowcnt

CSR Name	Offset	Access	Reset Value	Field Name	Description
		RO	16'd0	dvp5_col_cnt	dvp5inputcolcnt
io_dvp0_cnt_status	16'h0084	RO	16'd0	io_dvp0_row_cnt	io_dvp0inputrowcnt
		RO	16'd0	io_dvp0_col_cnt	io_dvp0inputcolcnt
io_dvp1_cnt_status	16'h0088	RO	16'd0	io_dvp1_row_cnt	io_dvp1inputrowcnt
		RO	16'd0	io_dvp1_col_cnt	io_dvp1inputcolcnt
toisp0_dvp0_cnt_status	16'h008c	RO	16'd0	toisp0_dvp0_row_cnt	toisp0dvp0inputrowcnt
		RO	16'd0	toisp0_dvp0_col_cnt	toisp0dvp0inputcolcnt
toisp0_dvp1_cnt_status	16'h0090	RO	16'd0	toisp0_dvp1_row_cnt	toisp0dvp1inputrowcnt
		RO	16'd0	toisp0_dvp1_col_cnt	toisp0dvp1inputcolcnt
toisp1_dvp0_cnt_status	16'h0094	RO	16'd0	toisp1_dvp0_row_cnt	toisp1dvp0inputrowcnt
		RO	16'd0	toisp1_dvp0_col_cnt	toisp1dvp0inputcolcnt
toisp1_dvp1_cnt_status	16'h0098	RO	16'd0	toisp1_dvp1_row_cnt	toisp1dvp1inputrowcnt
		RO	16'd0	toisp1_dvp1_col_cnt	toisp1dvp1inputcolcnt
trig_io_sel	16'h00a0	RO		Reserved	
		RW	6'd0	trig_io_sel	Select the IO trigger signal for each shutter. 0:select the trigger PAD0, 1:select the trigger PAD1,
isp0_dvp2_size	16'h00a4	RW	16'd480	isp0_dvp2_height	isp0dvp2height
		RW	16'd640	isp0_dvp2_width	isp0dvp2width
isp0_dvp3_size	16'h00a8	RW	16'd480	isp0_dvp3_height	isp0dvp3height
		RW	16'd	isp0_dvp3_width	isp0dvp3width

CSR Name	Offset	Access	Reset Value	Field Name	Description
			640		
isp1_dvp2_size	16'h00 ac	RW	16'd 480	isp1_dvp2_height	isp1dvp2height
		RW	16'd 640	isp1_dvp2_width	isp1dvp2width
isp1_dvp3_size	16'h00 b0	RW	16'd 480	isp1_dvp3_height	isp1dvp3height
		RW	16'd 640	isp1_dvp3_width	isp1dvp3width
multi2isp0_dvp2	16'h00 b4	RO		Reserved	
		RW	3'd4	vh_gap_mul2isp0_dvp2	outputhsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp0_dvp2	0:output=input 1:output=invert(input)
		RW	4'd0	shift_bit_mul2isp0_dvp2	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp0_dvp2	0:upalign 1:downalign
multi2isp0_dvp3	16'h00 b8	RO		Reserved	
		RW	3'd4	vh_gap_mul2isp0_dvp3	outputhsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp0_dvp3	0:output=input 1:output=invert(input)
		RW	4'd0	shift_bit_mul2isp0_dvp3	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp0_dvp3	0:upalign 1:downalign
multi2isp1_dvp2	16'h00	RO		Reserved	

CSR Name	Offset	Access	Reset Value	Field Name	Description
	bc				
		RW	3'd4	vh_gap_mul2isp1_dvp2	outputhsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp1_dvp2	0:output=input 1:output=invert(input)
		RW	4'd0	shift_bit_mul2isp1_dvp2	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp1_dvp2	0:upalign 1:downalign
multi2isp1_dvp3	16'h00c0	RO		Reserved	
		RW	3'd4	vh_gap_mul2isp1_dvp3	outputhsyncdelayvsync cyclenumber 0:delay1T 1:delay2T 2:delay3T
		RW	1'd0	inv_mul2isp1_dvp3	0:output=input 1:output=invert(input)
		RW	4'd0	shift_bit_mul2isp1_dvp3	vblankalarmthreshold
		RO		Reserved	
		RW	1'd0	dir_en_mul2isp1_dvp3	0:upalign 1:downalign
toisp0_dvp2_cnt_status	16'h00c4	RO	16'd0	toisp0_dvp2_row_cnt	toisp0dvp2inputrowcnt
		RO	16'd0	toisp0_dvp2_col_cnt	toisp0dvp2inputcolcnt
toisp0_dvp3_cnt_status	16'h00c8	RO	16'd0	toisp0_dvp3_row_cnt	toisp0dvp3inputrowcnt
		RO	16'd0	toisp0_dvp3_col_cnt	toisp0dvp3inputcolcnt
toisp1_dvp2_cnt_status	16'h00cc	RO	16'd0	toisp1_dvp2_row_cnt	toisp1dvp2inputrowcnt
		RO	16'd	toisp1_dvp2_col_cnt	toisp1dvp2inputcolcnt

CSR Name	Offset	Access	Reset Value	Field Name	Description
			0		
toisp1_dvp3_cnt_status	16'h00d0	RO	16'd0	toisp1_dvp3_row_cnt	toisp1dvp3inputrowcnt
		RO	16'd0	toisp1_dvp3_col_cnt	toisp1dvp3inputcolcnt
isp_input_linesize_err	16'h00d4	RO		Reserved	
		RO	1'd0	isp1_dvp3_line_size_error	isp1dvp3linesizeerror,
		RO	1'd0	isp1_dvp2_line_size_error	isp1dvp2linesizeerror,
		RO	1'd0	isp1_dvp1_line_size_error	isp1dvp1linesizeerror,
		RO	1'd0	isp1_dvp0_line_size_error	isp1dvp0linesizeerror,
		RO	1'd0	isp0_dvp3_line_size_error	isp0dvp3linesizeerror,
		RO	1'd0	isp0_dvp2_line_size_error	isp0dvp2linesizeerror,
		RO	1'd0	isp0_dvp1_line_size_error	isp0dvp1linesizeerror,
		RO	1'd0	isp0_dvp0_line_size_error	isp0dvp0linesizeerror,
multi2isp_soft_reset_n	16'h00d8	RO		Reserved	
		RW	8'hff	multi2isp_soft_rstn	multi2ispsoftreset,active low
mmu_tbu0_vi_isp0	16'h1000	RW	8'b0	scu_vi_isp0_awmmusid	
		RW	8'b0	scu_vi_isp0_awmmusid	
		RW	8'b0	scu_vi_isp0_armmusid	
		RW	8'b0	scu_vi_isp0_armmussid	
mmu_tbu0_vi_isp1	16'h1004	RW	8'b0	scu_vi_isp1_awmmusid	
		RW	8'b0	scu_vi_isp1_awmmusid	
		RW	8'b0	scu_vi_isp1_armmusid	

CSR Name	Offset	Access	Reset Value	Field Name	Description
		RW	8'b0	scu_vi_isp1_armmussid	
mmu_tbu0_vi_dw200	16'h1008	RW	8'b0	scu_vi_dw200_awmmusid	
		RW	8'b0	scu_vi_dw200_awmmussid	
		RW	8'b0	scu_vi_dw200_armmusid	
		RW	8'b0	scu_vi_dw200_armmusid	
mmu_tbu0_vi_dvp	16'h100c	RW	8'b0	scu_vi_dvp_awmmusid	
		RW	8'b0	scu_vi_dvp_awmmussid	
		RW	8'b0	scu_vi_dvp_armmusid	
		RW	8'b0	scu_vi_dvp_armmussid	

#### 8.4.2 CSI2 Host CSR

##### VERSION

**Name:** Core version.

**Description:** Contains the version of DWC\_mipi\_csi2\_host coded in 32-bit ASCII code.

**Size:** 32 bits

**Offset:** 0x0

Bits	Name	Memory Access	Description
31:0	version	R	<p>This field indicates the version of the DWC_mipi_csi2_host.</p> <p><b>Value After Reset:</b> CSI2_HOST_VERSION_ID</p> <p><b>Exists:</b> Always</p>

##### N\_LANES

**Name:** Number of lanes.

**Description:** Configures the number of active lanes that the DWC\_mipi\_csi2\_host uses to receive the camera device data.

**Size:** 32 bits

**Offset:** 0x4

Bits	Name	Memory Access	Description
31:3			<b>Reserved Field:</b> Yes
2:0	n_lanes	R/W	<p>This can only be updated when the PHY lane is in stopstate. Number of active data lanes:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (DATALANE1): 1 Data Lane</li> <li>■ 0x1 (DATALANE2): 2 Data Lanes</li> <li>■ 0x2 (DATALANE3): 3 Data Lanes</li> <li>■ 0x3 (DATALANE4): 4 Data Lanes - Only on D-PHY</li> <li>■ 0x4 (DATALANE5): 5 Data Lanes - Only on D-PHY</li> <li>■ 0x5 (DATALANE6): 6 Data Lanes - Only on D-PHY</li> <li>■ 0x6 (DATALANE7): 7 Data Lanes - Only on D-PHY</li> <li>■ 0x7 (DATALANE8): 8 Data Lanes - Only on D-PHY</li> </ul> <p><b>Value After Reset:</b> CSI2_HOST_NUMBER_OF_LANES-1</p> <p><b>Exists:</b> Always</p>

**CSI2\_RESETN****Name:** Logic Reset.

**Description:** Controls the DWC\_mipi\_csi2\_host logic reset state. When activated, the internal logic of the controller goes into the reset state. The configuration is not reset to default values with this register, instead, only the internal controller logic is affected.

**Size:** 32 bits**Offset:** 0x8

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	csi2_resetn	R/W	<p>DWC_mipi_csi2_host reset output. Active Low.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always

**INT\_ST\_MAIN**

**Name:** Main interrupt status.

**Description:** Contains the status of individual interrupt sources, regardless of the contents of the associated interrupt mask registers, so it is possible to service the interrupt status registers by polling. Reading INT\_ST\_MAIN register clears the interrupt pin.

**Size:** 32 bits

**Offset:** 0xc

Bits	Name	Memory Access	Description
31:26			<b>Reserved Field:</b> Yes
25	status_int_st_ipi8_fatal	RC	Status of int_st_ipi8_fatal Value <b>After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_IPI_IF8>0
24	status_int_st_ipi7_fatal	RC	Status of int_st_ipi7_fatal Value <b>After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_IPI_IF7>0
23	status_int_st_ipi6_fatal	RC	Status of int_st_ipi6_fatal Value <b>After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_IPI_IF6>0
22	status_int_st_ipi5_fatal	RC	Status of int_st_ipi5_fatal Value <b>After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_IPI_IF5>0
21	status_int_st_ipi4_fatal	RC	Status of int_st_ipi4_fatal Value <b>After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> CSI2_HOST_IPI_IF4>0
20	status_int_st_ipi3_fatal	RC	Status of int_st_ipi3_fatal <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_IPI_IF3>0
19	status_int_st_ipi2_fatal	RC	Status of int_st_ipi2_fatal <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_IPI_IF2>0
18	status_int_st_ipi_fatal	RC	Status of int_st_ipi_fatal <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_IPI_IF>0
17	status_int_st_line	RC	Status of int_st_line <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
16	status_int_st_phy	RC	Status of int_st_phy. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:8			<b>Reserved Field:</b> Yes
7	status_int_st_ecc_corrected	RC	Status of int_st_ecc_corrected. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
6	status_int_st_data_id	RC	<p>Status of int_st_data_id.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	status_int_st_pld_crc_fatal	RC	<p>Status of int_st_pld_crc_fatal.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	status_int_st_crc_frame_fatal	RC	<p>Status of int_st_crc_frame_fatal.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	status_int_st_seq_frame_fatal	RC	<p>Status of int_st_seq_frame_fatal.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	status_int_st_bndry_frame_fatal	RC	<p>Status of int_st_bndry_frame_fatal.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	status_int_st_pkt_fatal	RC	<p>Status of int_st_pkt_fatal.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	status_int_st_phy_fatal	RC	<p>Status of int_st_phy_fatal.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**DATA\_IDS\_1**

**Name:** Data Type fields for Data ID Monitors 1.

**Description:** Programs Data Type fields for Data ID Monitors. Data ID is composed by a pair of data type and virtual channel present in register DATA\_IDS\_VC\_1.

**Size:** 32 bits

**Offset:** 0x10

Bits	Name	Memory Access	Description
31:30			<b>Reserved Field:</b> Yes
29:24	di3_dt	R/W	Data type for programmed data ID 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:22			<b>Reserved Field:</b> Yes
21:16	di2_dt	R/W	Data type for programmed data ID 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:14			<b>Reserved Field:</b> Yes
13:8	di1_dt	R/W	Data type for programmed data ID 1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	di0_dt	R/W	Data type for programmed data ID 0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**DATA\_IDS\_2**

**Name:** Data Type fields for Data ID Monitors 2.

**Description:** Programs Data Type fields for Data ID Monitors. Data ID is composed by a pair of data type and virtual channel programmed in register DATA\_IDS\_VC\_2. This register allows four additional data types.

**Size:** 32 bits

**Offset:** 0x14

Bits	Name	Memory Access	Description
31:30			<b>Reserved Field:</b> Yes
29:24	di7_dt	R/W	Data type for programmed data ID 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:22			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
21:16	di6_dt	R/W	Data type for programmed data ID 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:14			<b>Reserved Field:</b> Yes
13:8	di5_dt	R/W	Data type for programmed data ID 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	di4_dt	R/W	Data type for programmed data ID 4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

#### PHY\_CFG

**Name:** Select the PPI width.

**Description:** This bit is to select the PPI width to be used.

**Size:** 32 bits

**Offset:** 0x18

Bits	Name	Memory Access	Description
31:2			<b>Reserved Field:</b> Yes
1:0	dphyppi16	R/W	Select the PPI width: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (PPI8): PPI bus width of 8 bits</li> <li>■ 0x1 (PPI16): PPI bus width of 16 bits</li> <li>■ 0x2 (RSVD10): Reserved</li> <li>■ 0x3 (RSVD11): Reserved Value</li> </ul> <b>After Reset:</b> 0x0 <b>Exists:</b> Always

#### PHY\_MODE

**Name:** PHY Mode.

**Description:** This bit is to select the PHY interface to be used.

**Size:** 32 bits**Offset:** 0x1c

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	phy_mode	R/W	Select the PHY interface: <b>Values:</b> <ul style="list-style-type: none"><li>■ 0x0 (D-PHY): Select D-PHY</li><li>■ 0x1 (C-PHY): Select C-PHY</li></ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**DATA\_IDS\_VC\_1****Name:** Virtual Channel fields for Data ID Monitors 1.

Description: Programs Virtual Channel fields for Data ID Monitors. Data ID is composed by a pair of Virtual Channel and data types present in register DATA\_IDS\_1.

**Size:** 32 bits**Offset:** 0x30

Bits	Name	Memory Access	Description
31:29			<b>Reserved Field:</b> Yes
28	di3_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 3 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27:26	di3_vcx_0_1	R/W	Virtual channel extension for programmed data ID 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
25:24	di3_vc	R/W	Virtual channel for programmed data ID 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:21			<b>Reserved Field:</b> Yes
20	di2_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 2 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
19:18	di2_vcx_0_1	R/W	Virtual channel extension for programmed data ID 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
17:16	di2_vc	R/W	Virtual channel for programmed data ID 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:13			<b>Reserved Field:</b> Yes
12	di1_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 1 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
11:10	di1_vcx_0_1	R/W	Virtual channel extension for programmed data ID 1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
9:8	di1_vc	R/W	Virtual channel for programmed data ID 1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:5			<b>Reserved Field:</b> Yes
4	di0_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
3:2	di0_vcx_0_1	R/W	Virtual channel extension for programmed data ID 0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1:0	di0_vc	R/W	Virtual channel for programmed data ID 0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**DATA\_IDS\_VC\_2**

**Name:** Virtual Channel fields for Data ID Monitors 2.

**Description:** Programs Virtual Channel fields for Data ID Monitors. Data ID is composed

by a pair of Virtual Channel and data types present in register DATA\_IDS\_2.

**Size:** 32 bits

**Offset:** 0x34

Bits	Name	Memory Access	Description
31:29			<b>Reserved Field:</b> Yes
28	di7_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27:26	di7_vcx_0_1	R/W	Virtual channel extension for programmed data ID 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
25:24	di7_vc	R/W	Virtual channel for programmed data ID 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:21			<b>Reserved Field:</b> Yes
20	di6_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 6 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
19:18	di6_vcx_0_1	R/W	Virtual channel extension for programmed data ID 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
17:16	di6_vc	R/W	Virtual channel for programmed data ID 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:13			<b>Reserved Field:</b> Yes
12	di5_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 5 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
11:10	di5_vcx_0_1	R/W	Virtual channel extension for programmed data ID 5.

Bits	Name	Memory Access	Description
			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
9:8	di5_vc	R/W	Virtual channel for programmed data ID 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:5			<b>Reserved Field:</b> Yes
4	di4_vcx_2	R/W	Virtual channel extension extra bit for programmed data ID 4 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
3:2	di4_vcx_0_1	R/W	Virtual channel extension for programmed data ID 4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1:0	di4_vc	R/W	Virtual channel for programmed data ID 4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**PHY\_SHUTDOWNZ****Name:** PHY Shutdown.**Description:** Controls the PHY Shutdown mode. In this state, the PHY sets the analog and digital circuitry in the Reset state.**Size:** 32 bits**Offset:** 0x40

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	phy_shutdownz	R/W	Shutdown input. This line is used to place the complete macro in power down. All analog blocks are in power down mode and digital logic is cleared. Active Low. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**DPHY\_RSTZ****Name:** D-PHY reset.**Description:** Controls the PHY Reset mode. In this state, the PHY sets the digital circuitry in the Reset State.**Size:** 32 bits**Offset:** 0x44

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	dphy_rstz	R/W	PHY reset output. Active <b>Low. Value After Reset:</b> 0x0 <b>Exists:</b> Always

**PHY\_RX****Name:** RX PHY status.**Description:** Contains the status of RX-related signals from PHY: RXULPSESC\* RXCLKACTIVEHS (D-PHY). It contains information such as, if the clock lane is receiving high-speed clock signal, or if the data and clock lanes are in Ultra Low Power Mode (ULPM).**Size:** 32 bits**Offset:** 0x48

Bits	Name	Memory Access	Description
31:18			<b>Reserved Field:</b> Yes
17	phy_rxclkactivehs	R	Indicates that D-PHY clock lane is actively receiving a DDR clock <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_PHY == 1)   (CSI2_HOST_PHY == 2)) == 1
16	phy_rxulpsclknot	R	Active Low. This signal indicates that D-PHY Clock Lane module has entered the Ultra Low Power state <b>Value After Reset:</b> 0x1 <b>Exists:</b> ((CSI2_HOST_PHY == 1)   (CSI2_HOST_PHY == 2)) == 1
15:8			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
7	phy_rxulpsesc_7	R	<p>Lane module 7 has entered the Ultra Low Power mode</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;7</p>
6	phy_rxulpsesc_6	R	<p>Lane module 6 has entered the Ultra Low Power mode</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;6</p>
5	phy_rxulpsesc_5	R	<p>Lane module 5 has entered the Ultra Low Power mode</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;5</p>
4	phy_rxulpsesc_4	R	<p>Lane module 4 has entered the Ultra Low Power mode</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;4</p>
3	phy_rxulpsesc_3	R	<p>Lane module 3 has entered the Ultra Low Power mode</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;3</p>
2	phy_rxulpsesc_2	R	<p>Lane module 2 has entered the Ultra Low Power mode</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;2</p>
1	phy_rxulpsesc_1	R	<p>Lane module 1 has entered the Ultra Low Power mode</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;1</p>

Bits	Name	Memory Access	Description
0	phy_rxulpsesc_0	R	<p>Lane module 0 has entered the Ultra Low Power mode.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**PHY\_STOPSTATE**

**Name:** STOPSTATE PHY status.

**Description:** Contains the STOPSTATE signal status from PHY.

**Size:** 32 bits

**Offset:** 0x4c

Bits	Name	Memory Access	Description
31:17			<b>Reserved Field:</b> Yes
16	phy_stopstateclk	R	<p>D-PHY Clock lane in Stop state</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_PHY == 1)   (CSI2_HOST_PHY == 2)) == 1</p>
15:8			<b>Reserved Field:</b> Yes
7	phy_stopstatedata_7	R	<p>Data lane 7 in Stop state</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES)) &gt; 7</p>
6	phy_stopstatedata_6	R	<p>Data lane 6 in Stop state</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES)) &gt; 6</p>

**PHY\_TEST\_CTRL0**

**Name:** ESWIN D-PHY Test and Control interface 0.

**Description:** Control for vendor specific interface in the PHY. Controls the ESWIN D-PHY Test and Control interface. This register controls the TESTCLR and TESTCLK signals.

**Size:** 32 bits

**Offset:** 0x50

Bits	Name	Memory Access	Description
31:2			<b>Reserved Field:</b> Yes
1	phy_testclk	R/W	Clock to capture testdin bus contents into the macro, with testen signal controlling the operation selection. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	phy_testclr	R/W	When active, performs vendor specific interface initialization. Active High. Note: This line needs an initial high pulse after power up for analog programmability default values to be preset. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always

**PHY\_TEST\_CTRL1****Name:** ESWIN D-PHY Test and Control interface 1.**Description:** Control for vendor specific interface in the PHY. Controls the ESWIN D-PHY Test and Control interface. This register controls the TESTENABLE signal and the TESTDIN bus. Reading from this register retrieves the value from TESTDOUT.**Size:** 32 bits**Offset:** 0x54

Bits	Name	Memory Access	Description
31:17			<b>Reserved Field:</b> Yes
16	phy_testen	R/W	When asserted high, it configures an address write operation on the falling edge of testclk. When asserted low, it configures a data write operation on the rising edge of testclk. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:8	phy_testdout	R	Vendor-specific 8-bit data output for reading data and other probing functionalities. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
7:0	phy_testdin	R/W	<p>Test interface 8-bit data input for programming internal registers and accessing test functionalities.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**PHY2\_TEST\_CTRL0**

**Name:** ESWIN second D-PHY Test and Control interface 0.

**Description:** Control for vendor specific interface in the PHY. Controls the ESWIN D-PHY Test and Control interface. This register controls the TESTCLR and TESTCLK signals from the second D-PHY.

**Size:** 32 bits

**Offset:** 0x58

Bits	Name	Memory Access	Description
31:2			<b>Reserved Field:</b> Yes
1	phy2_testclk	R/W	<p>Clock to capture testdin bus contents into the macro, with testen signal controlling the operation selection.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	phy2_testclr	R/W	<p>When active, performs vendor specific interface initialization. Active High. Note: This line needs an initial high pulse after power up for analog programmability default values to be preset.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p>

**PHY2\_TEST\_CTRL1**

**Name:** ESWIN second D-PHY Test and Control interface 1.

**Description:** Control for vendor specific interface in the PHY. Controls the ESWIN D-PHY Test and Control interface. This register controls the TESTENABLE signal and the TESTDIN bus from the second D-PHY. Reading from this register retrieves the value from TESTDOUT.

**Size:** 32 bits

**Offset:** 0x5c

Bits	Name	Memory Access	Description
31:17			<b>Reserved Field:</b> Yes
16	phy2_testen	R/W	When asserted high, it configures an address write operation on the falling edge of testclk. When asserted low, it configures a data write operation on the rising edge of testclk. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:8	phy2_testdout	R	Vendor-specific 8-bit data output for reading data and other probing functionalities. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:0	phy2_testdin	R/W	Test interface 8-bit data input for programming internal registers and accessing test functionalities. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**PPI\_PG\_PATTERN\_VRES****Name:** PPI Pattern Generator vertical resolution.**Description:** This register configures the PPI pattern Generator's pattern vertical resolution.**Size:** 32 bits**Offset:** 0x60

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	ppi_pg_pattern_vres	R/W	This register configures the PPI pattern Generator's pattern vertical resolution. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**PPI\_PG\_PATTERN\_HRES****Name:** PPI Pattern Generator horizontal resolution.**Description:** This register configures the PPI pattern Generator's pattern horizontal resolution.**Size:** 32 bits

Offset: 0x64

Bits	Name	Memory Access	Description
31:26			<b>Reserved Field:</b> Yes
25:16	ppi_pg_pkt2pkt_time	R/W	This register configures the PPI pattern Generator's packet-to-packet time. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:0	ppi_pg_pattern_hres	R/W	This register configures the PPI pattern Generator's pattern horizontal resolution. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**PPI\_PG\_CONFIG****Name:** PPI Pattern Generator Configuration.**Description:** This register configures the PPI pattern Generator.**Size:** 32 bits

Offset: 0x68

Bits	Name	Memory Access	Description
31:19			<b>Reserved Field:</b> Yes
18	ppi_pg_vcx_2	R/W	This register configures the PPI pattern Generator's virtual channel extension for C-PHY <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
17:16	ppi_pg_vcx_0_1	R/W	This register configures the PPI pattern Generator's virtual channel extension. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:14	ppi_pg_vc	R/W	This register configures the PPI pattern Generator's virtual channel. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

13:8	ppi_pg_datatype	R/W	<p>This register configures the PPI pattern Generator's data type.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes
0	ppi_pg_pattern	R/W	<p>This register configures the PPI pattern Generator's pattern:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (VERTICAL): Vertical Pattern</li> <li>■ 0x1 (HORIZONTAL): Horizontal Pattern</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**PPI\_PG\_ENABLE**

**Name:** PPI Pattern Generator Enable.

**Description:** This register enables PPI pattern Generator.

**Size:** 32 bits

**Offset:** 0x6c

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	ppi_pg_enable	R/W	<p>This register enables PPI pattern Generator.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**PPI\_PG\_STATUS**

**Name:** PPI Pattern Generator status.

**Description:** This register indicates PPI Pattern Generator Status.

**Size:** 32 bits

**Offset:** 0x70

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes

0	ppi_pg_status	R	<p>PPI Pattern Generator status:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (INACTIVE): PPI PG is inactive</li> <li>■ 0x1 (ACTIVE): PPI PG is running</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
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**IPI\_MODE****Name:** IPI Mode.**Description:** This register selects how the IPI interface generates the video frame.**Size:** 32 bits**Offset:** 0x80

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_enable	R/W	<p>This register enables the interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
23:17			<b>Reserved Field:</b> Yes
16	ipi_cut_through	R/W	<p>This field indicates cut-through mode state:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	<p>This field indicates if color mode components are delivered as follows:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
0	ipi_mode	R/W	<p>This field indicates the video mode transmission type as follows:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (CAMMODE): Camera timing</li> <li>■ 0x1 (CTRLMODE): Controller timing</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI\_VCID****Name:** IPI Virtual Channel.**Description:** This register selects the virtual channel processed by IPI.**Size:** 32 bits**Offset:** 0x84

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcx_2	R/W	<p>Virtual channel extension extra bit of data to be processed by pixel interface 1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
3:2	ipi_vcx_0_1	R/W	<p>Virtual channel extension of data to be processed by pixel interface 1.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1:0	ip_vcid	R/W	<p>Virtual channel of data to be processed by pixel interface 1.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI\_DATA\_TYPE****Name:** IPI Data Type.**Description:** This register selects the data type processed by IPI.**Size:** 32 bits**Offset:** 0x88

Bits	Name	Memory	Description
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		Access	
31:9			<b>Reserved Field:</b> Yes
8	embedded_data	R/W	For Camera Timing Mode, this bit enables embedded data processing on IPI 1 interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	Data type of data to be processed by pixel interface 1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_MEM\_FLUSH****Name:** IPI Flush Memory.**Description:** This register control the flush of IPI memory.**Size:** 32 bits**Offset:** 0x8c

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	ipi_auto_flush	R/W	Memory is automatically flushed at each Frame Start. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	Flush IPI memory. This bit is auto clear. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_HSA\_TIME****Name:** IPI HSA.**Description:** This register configures the video Horizontal Synchronism Active (HSA) time.**Size:** 32 bits**Offset:** 0x90

Bits	Name	Memory Access	Description

31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	This field configures the Horizontal Synchronism Active period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_HBP\_TIME****Name:** IPI HBP.**Description:** This register configures the video Horizontal Back Porch (HBP) time.**Size:** 32 bits**Offset:** 0x94

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hbp_time	R/W	This field configures the Horizontal Back Porch period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_HSD\_TIME****Name:** IPI HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time.**Size:** 32 bits**Offset:** 0x98

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	This field configures the Horizontal Sync Delay period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_HLINE\_TIME****Name:** IPI HLINE.**Description:** This register configures the overall time for each video line.**Size:** 32 bits**Offset:** 0x9c

Bits	Name	Memory Access	Description
31:15			<b>Reserved Field:</b> Yes
14:0	ipi_hline_time	R/W	This field configures the size of the line time counted in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_SOFTRSTN****Name:** IPI Soft Reset.**Description:** Controls the IPI logic reset state. When activated, the internal logic of the IPI goes into the reset state. Only the internal IPI logic is affected.**Size:** 32 bits**Offset:** 0xa0

Bits	Name	Memory Access	Description
31:29			<b>Reserved Field:</b> Yes
28	ipi8_softrstn	R/W	This field resets IPI eight. Active Low <b>Value After Reset:</b> 0x1 <b>Exists:</b> CSI2_HOST_IPI_IF8==1
27:25			<b>Reserved Field:</b> Yes
24	ipi7_softrstn	R/W	This field resets IPI seven. Active Low <b>Value After Reset:</b> 0x1 <b>Exists:</b> CSI2_HOST_IPI_IF7==1
23:21			<b>Reserved Field:</b> Yes
20	ipi6_softrstn	R/W	This field resets IPI six. Active Low <b>Value After Reset:</b> 0x1 <b>Exists:</b> CSI2_HOST_IPI_IF6==1
19:17			<b>Reserved Field:</b> Yes
16	ipi5_softrstn	R/W	This field resets IPI five. Active Low <b>Value After Reset:</b> 0x1 <b>Exists:</b> CSI2_HOST_IPI_IF5==1
15:13			<b>Reserved Field:</b> Yes
12	ipi4_softrstn	R/W	This field resets IPI four. Active Low <b>Value After Reset:</b> 0x1 <b>Exists:</b> CSI2_HOST_IPI_IF4==1

Bits	Name	Memory Access	Description
11:9			<b>Reserved Field:</b> Yes
8	ipi3_softrstn	R/W	This field resets IPI three. Active Low <b>Value After Reset:</b> 0x1 <b>Exists:</b> CSI2_HOST_IPI_IF3==1
7:5			<b>Reserved Field:</b> Yes
4	ipi2_softrstn	R/W	This field resets IPI two. Active Low <b>Value After Reset:</b> 0x1 <b>Exists:</b> CSI2_HOST_IPI_IF2==1
3:1			<b>Reserved Field:</b> Yes
0	ipi_softrstn	R/W	This field resets IPI one. Active Low. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always

**IPI\_ADV\_FEATURES****Name:** IPI Advanced Features.**Description:** This register configures advanced features for IPI mode.**Size:** 32 bits**Offset:** 0xac

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_sync_event_mode	R/W	For Camera Timing Mode: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:22			<b>Reserved Field:</b> Yes
21	en_embedded	R/W	This register allows the use of embedded packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
20	en_blanking	R/W	<p>This register allows the use of blanking packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
19	en_null	R/W	<p>This register allows the use of null packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
18	en_line_start	R/W	<p>This register allows the use of line start packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
17	en_video	R/W	<p>This register allows the use of video packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
16	line_event_selection	R/W	<p>For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows: <b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	<p>Datatype to overwrite. <b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	<p>Ignore datatype of the header using the programmed datatype for decoding.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always

**IPI\_VSA\_LINES****Name:** IPI VSA.**Description:** This register configures the Vertical Synchronism Active (VSA) period.**Size:** 32 bits**Offset:** 0xb0

Bits	Name	Memory Access	Description
31:10			<b>Reserved Field:</b> Yes
9:0	ipi_vsa_lines	R/W	This field configures the Vertical Synchronism Active period measured in number of horizontal lines. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_VBP\_LINES****Name:** IPI VBP.**Description:** This register configures the Vertical Back Porch (VBP) period.**Size:** 32 bits**Offset:** 0xb4

Bits	Name	Memory Access	Description
31:10			<b>Reserved Field:</b> Yes
9:0	ipi_vbp_lines	R/W	This field configures the Vertical Back Porch period measured in number of horizontal lines. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_VFP\_LINES****Name:** IPI VFP.**Description:** This register configures the Vertical Front Porch (VFP) period.**Size:** 32 bits

**Offset:** 0xb8

Bits	Name	Memory Access	Description
31:10			<b>Reserved Field:</b> Yes
9:0	ipi_vfp_lines	R/W	This field configures the Vertical Front Porch period measured in number of horizontal lines. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI\_VACTIVE\_LINES****Name:** IPI VACTIVE.**Description:** This register configures the vertical resolution of the video.**Size:** 32 bits**Offset:** 0xbc

Bits	Name	Memory Access	Description
31:14			<b>Reserved Field:</b> Yes
13:0	ipi_vactive_lines	R/W	This field configures the Vertical Active period measured in number of horizontal lines. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**VC\_EXTENSION****Name:** Virtual Channel Extension.**Description:** This register activates extra bits for virtual channel. The Virtual Channel Extension (VCX) field is common to both options, but is a 2-bit field for D-PHY and a 3-bit field for C-PHY.**Size:** 32 bits**Offset:** 0xc8

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	vcx	R/W	This field indicates status of Virtual Channel Extension: -0: Virtual channel extension is enable -1: Legacy mode. Virtual channel extension is disabled <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**PHY\_CAL**

**Name:** PHY Calibration.

**Description:** Contains the CALIBRATION signal status from ESWIN D-PHY.

**Size:** 32 bits

**Offset:** 0xcc

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	rxskewcalhs	RC	A low-to-high transition on rxskewcalhs signal means that the PHY has initiated the de-skew calibration. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_PHY\_FATAL**

**Name:** Fatal interruption caused by PHY.

**Description:** Groups the fatal interruptions caused by PHY Packet discarded. Stores the source of the error. Reading INT\_ST\_PHY\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0xe0

Bits	Name	Memory Access	Description
31:19			<b>Reserved Field:</b> Yes
18	phy_rxinvalidcodehs_2	RC	High Speed Invalid Code Word Detection on lane 2 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_CPHY==1 & CSI2_HOST_NUMBER_OF_LANES>2)
17	phy_rxinvalidcodehs_1	RC	High Speed Invalid Code Word Detection on lane 1 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_CPHY==1 & CSI2_HOST_NUMBER_OF_LANES>1)
16	phy_rxinvalidcodehs_0	RC	High Speed Invalid Code Word Detection on lane 0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_PHY == 2)   (CSI2_HOST_PHY == 3))==1
15:9			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
8	err_deskew	RC	<p>Reports whenever data is lost due to an existent skew between lanes greater than 2 rxwordclkhs</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_DESKEW==1</p>
7	phy_errsotsynchs_7	RC	<p>Start of transmission error on data lane 7 (no synchronization achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;7</p>
6	phy_errsotsynchs_6	RC	<p>Start of transmission error on data lane 6 (no synchronization achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;6</p>
5	phy_errsotsynchs_5	RC	<p>Start of transmission error on data lane 5 (no synchronization achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;5</p>
4	phy_errsotsynchs_4	RC	<p>Start of transmission error on data lane 4 (no synchronization achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;4</p>
3	phy_errsotsynchs_3	RC	<p>Start of transmission error on data lane 3 (no synchronization achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;3</p>

Bits	Name	Memory Access	Description
2	phy_errsotsynchs_2	RC	<p>Start of transmission error on data lane 2 (no synchronization achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;2</p>
1	phy_errsotsynchs_1	RC	<p>Start of transmission error on data lane 1 (no synchronization achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;1</p>
0	phy_errsotsynchs_0	RC	<p>Start of transmission error on data lane 0 (no synchronization achieved).</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_PHY\_FATAL**

**Name:** Mask for fatal interruption caused by PHY.

**Description:** Interrupt mask for INT\_ST\_PHY\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0xe4

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	err_deskew	R/W	<p>Mask for err_deskew</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_DESKEW==1</p>
7	mask_phy_errsotsynchs_7	R/W	<p>Mask for phy_errsotsynchs_7</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;7</p>

Bits	Name	Memory Access	Description
6	mask_phy_errsotsynchs_6	R/W	<p>Mask for phy_errsotsynchs_6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;6</p>
5	mask_phy_errsotsynchs_5	R/W	<p>Mask for phy_errsotsynchs_5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;5</p>
4	mask_phy_errsotsynchs_4	R/W	<p>Mask for phy_errsotsynchs_4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;4</p>
3	mask_phy_errsotsynchs_3	R/W	<p>Mask for phy_errsotsynchs_3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;3</p>
2	mask_phy_errsotsynchs_2	R/W	<p>Mask for phy_errsotsynchs_2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;2</p>
1	mask_phy_errsotsynchs_1	R/W	<p>Mask for phy_errsotsynchs_1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;1</p>
0	mask_phy_errsotsynchs_0	R/W	<p>Mask for phy_errsotsynchs_0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>

**INT\_FORCE\_PHY\_FATAL**

**Name:** Force for fatal interruption caused by PHY.

**Description:** Interrupt Force register is used for test purposes, and allows triggering INT\_ST\_PHY\_FATAL interrupt events individually, without the need to activate the conditions that trigger the interrupt sources, since it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0xe8

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	err_deskew	R/W	Force err_deskew <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_DESKEW==1
7	force_phy_errsotsynchs_7	R/W	Force phy_errsotsynchs_7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))>7
6	force_phy_errsotsynchs_6	R/W	Force phy_errsotsynchs_6 <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))>6
5	force_phy_errsotsynchs_5	R/W	Force phy_errsotsynchs_5 <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))>5
4	force_phy_errsotsynchs_4	R/W	Force phy_errsotsynchs_4 <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))>4

Bits	Name	Memory Access	Description
3	force_phy_errsotsynchs_3	R/W	<p>Force phy_errsotsynchs_3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;3</p>
2	force_phy_errsotsynchs_2	R/W	<p>Force phy_errsotsynchs_2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;2</p>
1	force_phy_errsotsynchs_1	R/W	<p>Force phy_errsotsynchs_1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;1</p>
0	force_phy_errsotsynchs_0	R/W	<p>Force phy_errsotsynchs_0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_ST\_PKT\_FATAL**

**Name:** Fatal interruption caused during Packet Construction.

**Description:** Groups the fatal interruption related with Packet construction. Packet discarded. Notifies which interruption bit has caused the interruption. Stores the source of the error. Reading INT\_ST\_PKT\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0xf0

Bits	Name	Memory Access	Description
31:2			<b>Reserved Field:</b> Yes
1	shorter_payload	RC	D-PHY mode: Reported greater WC than received, unrecoverable. C-PHY mode: Reported greater WC than received, unrecoverable.

			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_ecc_double	RC	D-PHY mode: Header ECC contains at least 2 errors, unrecoverable. C-PHY mode: Header CRC unrecoverable. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_PKT\_FATAL**

**Name:** Mask for fatal interruption caused during Packet Construction.

**Description:** Interrupt mask for INT\_ST\_PKT\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0xf4

Bits	Name	Memory Access	Description
31:2			<b>Reserved Field:</b> Yes
1	mask_shorter_payload	R/W	Mask for shorter_payload. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	mask_err_ecc_double	R/W	Mask for err_ecc_double. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_FORCE\_PKT\_FATAL**

**Name:** Force for fatal interruption caused during Packet Construction.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_PKT\_FATAL interrupt events individually, without the need to activate the conditions that trigger the interrupt sources, since it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0xf8

Bits	Name	Memory Access	Description
31:2			<b>Reserved Field:</b> Yes
1	force_shorter_payload	R/W	Force shorter_payload. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	force_err_ecc_double	R/W	Force err_ecc_double. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_PHY****Name:** Interruption caused by PHY.

**Description:** Interruption caused by PHY. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_PHY register does not clear the interrupt pin.

**Size:** 32 bits**Offset:** 0x110

Bits	Name	Memory Access	Description
31:24			<b>Reserved Field:</b> Yes
23	phy_erresc_7	RC	Escape Entry Error on data lane 7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))>7
22	phy_erresc_6	RC	Escape Entry Error on data lane 6 <b>Value After Reset:</b> 0x0 <b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))>6

Bits	Name	Memory Access	Description
21	phy_erresc_5	RC	<p>Escape Entry Error on data lane 5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;5</p>
20	phy_erresc_4	RC	<p>Escape Entry Error on data lane 4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;4</p>
19	phy_erresc_3	RC	<p>Escape Entry Error on data lane 3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;3</p>
18	phy_erresc_2	RC	<p>Escape Entry Error on data lane 2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;2</p>
17	phy_erresc_1	RC	<p>Escape Entry Error on data lane 1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;1</p>
16	phy_erresc_0	RC	<p>Escape Entry Error on data lane 0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:8			<b>Reserved Field:</b> Yes
7	phy_errsoths_7	RC	<p>Start of transmission error on data lane 7 (synchronization can still be achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;7</p>

Bits	Name	Memory Access	Description
6	phy_errsoths_6	RC	<p>Start of transmission error on data lane 6 (synchronization can still be achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;6</p>
5	phy_errsoths_5	RC	<p>Start of transmission error on data lane 5 (synchronization can still be achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;5</p>
4	phy_errsoths_4	RC	<p>Start of transmission error on data lane 4 (synchronization can still be achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;4</p>
3	phy_errsoths_3	RC	<p>Start of transmission error on data lane 3 (synchronization can still be achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;3</p>
2	phy_errsoths_2	RC	<p>Start of transmission error on data lane 2 (synchronization can still be achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;2</p>
1	phy_errsoths_1	RC	<p>Start of transmission error on data lane 1 (synchronization can still be achieved)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;1</p>

Bits	Name	Memory Access	Description
0	phy_errsoths_0	RC	<p>Start of transmission error on data lane 0 (synchronization can still be achieved).</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_PHY**

**Name:** Mask for interruption caused by PHY.

**Description:** Interrupt mask for INT\_ST\_PHY controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x114

Bits	Name	Memory Access	Description
31:24			<b>Reserved Field:</b> Yes
23	mask_phy_erresc_7	R/W	<p>Mask for phy_erresc_7</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;7</p>
22	mask_phy_erresc_6	R/W	<p>Mask for phy_erresc_6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;6</p>
21	mask_phy_erresc_5	R/W	<p>Mask for phy_erresc_5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;5</p>
20	mask_phy_erresc_4	R/W	<p>Mask for phy_erresc_4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ((CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES))&gt;4</p>

Bits	Name	Memory Access	Description
19	mask_phy_erresc_3	R/W	<p>Mask for phy_erresc_3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;3</p>
18	mask_phy_erresc_2	R/W	<p>Mask for phy_erresc_2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;2</p>
17	mask_phy_erresc_1	R/W	<p>Mask for phy_erresc_1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;1</p>
16	mask_phy_erresc_0	R/W	<p>Mask for phy_erresc_0. <b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:8			<b>Reserved Field:</b> Yes
7	mask_phy_errsoths_7	R/W	<p>Mask for phy_errsoths_7</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;7</p>
6	mask_phy_errsoths_6	R/W	<p>Mask for phy_errsoths_6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;6</p>
5	mask_phy_errsoths_5	R/W	<p>Mask for phy_errsoths_5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;5</p>

Bits	Name	Memory Access	Description
4	mask_phy_errsoths_4	R/W	<p>Mask for phy_errsoths_4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;4</p>
3	mask_phy_errsoths_3	R/W	<p>Mask for phy_errsoths_3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;3</p>
2	mask_phy_errsoths_2	R/W	<p>Mask for phy_errsoths_2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;2</p>
1	mask_phy_errsoths_1	R/W	<p>Mask for phy_errsoths_1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;1</p>
0	mask_phy_errsoths_0	R/W	<p>Mask for phy_errsoths_0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

#### INT\_FORCE\_PHY

**Name:** Force for interruption caused by PHY.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_PHY interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x118

Bits	Name	Memory Access	Description
31:24			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
23	force_phy_eresc_7	R/W	<p>Force phy_eresc_7</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;7</p>
22	force_phy_eresc_6	R/W	<p>Force phy_eresc_6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;6</p>
21	force_phy_eresc_5	R/W	<p>Force phy_eresc_5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;5</p>
20	force_phy_eresc_4	R/W	<p>Force phy_eresc_4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;4</p>
19	force_phy_eresc_3	R/W	<p>Force phy_eresc_3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;3</p>
18	force_phy_eresc_2	R/W	<p>Force phy_eresc_2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;2</p>
17	force_phy_eresc_1	R/W	<p>Force phy_eresc_1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;1</p>

Bits	Name	Memory Access	Description
16	force_phy_erresc_0	R/W	<p>Force phy_erresc_0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:8			<b>Reserved Field:</b> Yes
7	force_phy_errsoths_7	R/W	<p>Force phy_errsoths_7</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;7</p>
6	force_phy_errsoths_6	R/W	<p>Force phy_errsoths_6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;6</p>
5	force_phy_errsoths_5	R/W	<p>Force phy_errsoths_5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;5</p>
4	force_phy_errsoths_4	R/W	<p>Force phy_errsoths_4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;4</p>
3	force_phy_errsoths_3	R/W	<p>Force phy_errsoths_3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;3</p>
2	force_phy_errsoths_2	R/W	<p>Force phy_errsoths_2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;2</p>

Bits	Name	Memory Access	Description
1	force_phy_errsoths_1	R/W	<p>Force phy_errsoths_1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> ( (CSI2_HOST_DPHY_NUMBER_OF_LANES) + (CSI2_HOST_CPHY_NUMBER_OF_LANES) - (CSI2_HOST_NUMBER_OF_OVERLAPPING_LANES) )&gt;1</p>
0	force_phy_errsoths_0	R/W	<p>Force phy_errsoths_0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_ST\_LINE**

**Name:** Interruption occurred during Line construction.

**Description:** Interruption related with Line construction. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_LINE register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x130

Bits	Name	Memory Access	Description
31:24			<b>Reserved Field:</b> Yes
23	err_l_seq_di7	RC	<p>Error in the sequence of lines for vc7 and dt7</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
22	err_l_seq_di6	RC	<p>Error in the sequence of lines for vc6 and dt6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
21	err_l_seq_di5	RC	<p>Error in the sequence of lines for vc5 and dt5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
20	err_l_seq_di4	RC	<p>Error in the sequence of lines for vc4 and dt4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
19	err_l_seq_di3	RC	<p>Error in the sequence of lines for vc3 and dt3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;0</p>

Bits	Name	Memory Access	Description
18	err_l_seq_di2	RC	Error in the sequence of lines for vc2 and dt2 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
17	err_l_seq_di1	RC	Error in the sequence of lines for vc1 and dt1 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
16	err_l_seq_di0	RC	Error in the sequence of lines for vc0 and dt0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
15:8			<b>Reserved Field:</b> Yes
7	err_l_bndry_match_di7	RC	Error matching line start with line end for vc7 and dt7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
6	err_l_bndry_match_di6	RC	Error matching line start with line end for vc6 and dt6 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
5	err_l_bndry_match_di5	RC	Error matching line start with line end for vc5 and dt5 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
4	err_l_bndry_match_di4	RC	Error matching line start with line end for vc4 and dt4 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
3	err_l_bndry_match_di3	RC	Error matching line start with line end for vc3 and dt3 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
2	err_l_bndry_match_di2	RC	Error matching line start with line end for vc2 and dt2 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0

Bits	Name	Memory Access	Description
1	err_l_bndry_match_di1	RC	Error matching line start with line end for vc1 and dt1 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
0	err_l_bndry_match_di0	RC	Error matching line start with line end for vc0 and dt0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0

**INT\_MSK\_LINE**

**Name:** Mask for interruption occurred during Line construction.

**Description:** Interrupt mask for INT\_ST\_LINE controls which interrupt status bits trigger the inter-rupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x134

Bits	Name	Memory Access	Description
31:24			<b>Reserved Field:</b> Yes
23	mask_err_l_seq_di7	R/W	Mask for err_l_seq_di7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
22	mask_err_l_seq_di6	R/W	Mask for err_l_seq_di6 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
21	mask_err_l_seq_di5	R/W	Mask for err_l_seq_di5 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
20	mask_err_l_seq_di4	R/W	Mask for err_l_seq_di4 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
19	mask_err_l_seq_di3	R/W	Mask for err_l_seq_di3 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0

Bits	Name	Memory Access	Description
18	mask_err_l_seq_di2	R/W	<p>Mask for err_l_seq_di2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;0</p>
17	mask_err_l_seq_di1	R/W	<p>Mask for err_l_seq_di1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;0</p>
16	mask_err_l_seq_di0	R/W	<p>Mask for err_l_seq_di0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;0</p>
15:8			<b>Reserved Field:</b> Yes
7	mask_err_l_bndry_match_di7	R/W	<p>Mask for err_l_bndry_match_di7</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
6	mask_err_l_bndry_match_di6	R/W	<p>Mask for err_l_bndry_match_di6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
5	mask_err_l_bndry_match_di5	R/W	<p>Mask for err_l_bndry_match_di5</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
4	mask_err_l_bndry_match_di4	R/W	<p>Mask for err_l_bndry_match_di4</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;1</p>
3	mask_err_l_bndry_match_di3	R/W	<p>Mask for err_l_bndry_match_di3</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;0</p>
2	mask_err_l_bndry_match_di2	R/W	<p>Mask for err_l_bndry_match_di2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;0</p>
1	mask_err_l_bndry_match_di1	R/W	<p>Mask for err_l_bndry_match_di1</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> CSI2_HOST_N_DATA_IDS&gt;0</p>
0	mask_err_l_bndry_match_di0	R/W	<p>Mask for err_l_bndry_match_di0</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> CSI2_HOST_N_DATA_IDS>0

**INT\_FORCE\_LINE**

**Name:** Force for interruption occurred during Line construction.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_LINE interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x138

Bits	Name	Memory Access	Description
31:24			<b>Reserved Field:</b> Yes
23	force_err_l_seq_di7	R/W	Force err_l_seq_di7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
22	force_err_l_seq_di6	R/W	Force err_l_seq_di6 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
21	force_err_l_seq_di5	R/W	Force err_l_seq_di5 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
20	force_err_l_seq_di4	R/W	Force err_l_seq_di4 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
19	force_err_l_seq_di3	R/W	Force err_l_seq_di3 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
18	force_err_l_seq_di2	R/W	Force err_l_seq_di2 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0

Bits	Name	Memory Access	Description
17	force_err_l_seq_di1	R/W	Force err_l_seq_di1 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
16	force_err_l_seq_di0	R/W	Force err_l_seq_di0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
15:8			<b>Reserved Field:</b> Yes
7	force_err_l_bndry_match_di7	R/W	Force err_l_bndry_match_di7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
6	force_err_l_bndry_match_di6	R/W	Force err_l_bndry_match_di6 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
5	force_err_l_bndry_match_di5	R/W	Force err_l_bndry_match_di5 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
4	force_err_l_bndry_match_di4	R/W	Force err_l_bndry_match_di4 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>1
3	force_err_l_bndry_match_di3	R/W	Force err_l_bndry_match_di3 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
2	force_err_l_bndry_match_di2	R/W	Force err_l_bndry_match_di2 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
1	force_err_l_bndry_match_di1	R/W	Force err_l_bndry_match_di1 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0
0	force_err_l_bndry_match_di0	R/W	Force err_l_bndry_match_di0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> CSI2_HOST_N_DATA_IDS>0

**INT\_ST\_IPI\_FATAL**

**Name:** Fatal Interruption caused by IPI interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x140

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	Reporting internal FIFO overflow on pulse delay block. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	int_event_fifo_overflow	RC	Reporting internal FIFO overflow during IPI data processing. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	pixel_if_hline_err	RC	Horizontal line time error (only available in controller mode). <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	pixel_if_fifo_nempty_fs	RC	Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame. There are some scenarios where synchronization events of new frame can be lost on IPI interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	pixel_if_frame_sync_err	RC	Whenever in Controller mode, notifies if a new frame is received but previous has not been completed. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
1	pixel_if_fifo_overflow	RC	<p>The FIFO of pixel interface has lost information because some data arrived and FIFO is already full.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	pixel_if_fifo_underflow	RC	<p>The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_IPI\_FATAL**

**Name:** Mask for fatal interruption caused by IPI interface.

**Description:** Interrupt mask for INT\_ST\_IPI\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x144

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	msk_int_pulse_delay_overflow	R/W	<p>Mask int_pulse_delay_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	msk_int_event_fifo_overflow	R/W	<p>Mask int_event_fifo_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	msk_pixel_if_hline_err	R/W	<p>Mask pixel_if_hline_err.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
3	msk_pixel_if_fifo_nempty_fs	R/W	<p>Mask pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
2	msk_frame_sync_err	R/W	<p>Mask for pixel_if_frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
1	msk_pixel_if_fifo_overflow	R/W	<p>Mask for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
0	msk_pixel_if_fifo_underflow	R/W	<p>Mask for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>

**INT\_FORCE\_IPI\_FATAL**

**Name:** Force for fatal interruption caused by IPI interface.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI\_- FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x148

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	<p>Force int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
5	force_int_event_fifo_overflow	R/W	<p>Force int_event_fifo_overflow . <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
4	force_pixel_if_hline_err	R/W	<p>Force pixel_if_hline_err.</p> <p><b>Value After Reset:</b> 0x0      <b>Exists:</b> Always</p>
3	force_pixel_if_fifo_nempty_fs	R/W	<p>Force pixel_if_fifo_nempty_fs.</p> <p><b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
2	force_frame_sync_err	R/W	<p>Force for frame_sync_err. <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always</p>
1	force_pixel_if_fifo_overflow	R/W	<p>Force for pixel_if_fifo_overflow.</p> <p><b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
0	force_pixel_if_fifo_underflow	R/W	<p>Force for pixel_if_fifo_underflow.</p> <p><b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>

**INT\_ST\_IPI2\_FATAL**

**Name:** Fatal interruption caused by IPI2 interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI2\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x150

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	Reporting internal FIFO overflow on pulse delay block.

			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	int_event_fifo_overflow	RC	Reporting internal FIFO overflow during IPI data processing. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	pixel_if_hline_err	RC	Horizontal line time error (only available in controller mode). <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	pixel_if_fifo_nempty_fs	RC	Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame. There are some scenarios where synchronization events of new frame can be lost on IPI interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	pixel_if_frame_sync_err	RC	Whenever in Controller mode, notifies if a new frame is received but previous has not been completed. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	pixel_if_fifo_overflow	RC	The FIFO of pixel interface has lost information because some data arrived and FIFO is already full. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	pixel_if_fifo_underflow	RC	The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_IPI2\_FATAL**

**Name:** Mask for fatal interruption caused by IPI2 interface.

**Description:** Interrupt mask for INT\_ST\_IPI2\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x154

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	msk_int_pulse_delay_overflow	R/W	Mask int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	msk_int_event_fifo_overflow	R/W	Mask int_event_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	msk_pixel_if_hline_err	R/W	Mask pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	msk_pixel_if_fifo_nempty_fs	R/W	Mask pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	msk_frame_sync_err	R/W	Mask for pixel_if_frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	msk_pixel_if_fifo_overflow	R/W	Mask for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
0	msk_pixel_if_fifo_underflow	R/W	<p>Mask for pixel_if_fifo_underflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_FORCE\_IPI2\_FATAL**

**Name:** Force for fatal interruption caused by IPI2 interface.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI2\_- FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x158

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	<p>Force int_pulse_delay_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	force_int_event_fifo_overflow	R/W	<p>Force int_event_fifo_overflow</p> <p>. <b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	force_pixel_if_hline_err	R/W	<p>Force pixel_if_hline_err.</p> <p><b>Value After Reset:</b> 0x0      <b>Exists:</b> Always</p>
3	force_pixel_if_fifo_nempty_fs	R/W	<p>Force pixel_if_fifo_nempty_fs.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	force_frame_sync_err	R/W	Force for frame_sync_err. <b>Value</b>

Bits	Name	Memory Access	Description
			<b>After Reset:</b> 0x0 <b>Exists:</b> Always
1	force_pixel_if_fifo_overflow	R/W	Force for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	force_pixel_if_fifo_underflow	R/W	Force for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_IPI3\_FATAL**

**Name:** Fatal interruption caused by IPI3 interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI3\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x160

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	Reporting internal FIFO overflow on pulse delay block. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	int_event_fifo_overflow	RC	Reporting internal FIFO overflow during IPI data processing. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	pixel_if_hline_err	RC	Horizontal line time error (only available in controller mode). <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
3	pixel_if_fifo_nempty_fs	RC	<p>Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame.</p> <p>There are some scenarios where synchronization events of new frame can be lost on IPI interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	pixel_if_frame_sync_err	RC	<p>Whenever in Controller mode, notifies if a new frame is received but previous has not been completed.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	pixel_if_fifo_overflow	RC	<p>The FIFO of pixel interface has lost information because some data arrived and FIFO is already full.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	pixel_if_fifo_underflow	RC	<p>The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_IPI3\_FATAL**

**Name:** Mask for fatal interruption caused by IPI3 interface.

**Description:** Interrupt mask for INT\_ST\_IPI3\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x164

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	msk_int_pulse_delay_overflow	R/W	Mask int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	msk_int_event_fifo_overflow	R/W	Mask int_event_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	msk_pixel_if_hline_err	R/W	Mask pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	msk_pixel_if_fifo_nempty_fs	R/W	Mask pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	msk_frame_sync_err	R/W	Mask for pixel_if_frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	msk_pixel_if_fifo_overflow	R/W	Mask for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	msk_pixel_if_fifo_underflow	R/W	Mask for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_FORCE\_IPI3\_FATAL**

**Name:** Force for fatal interruption caused by IPI3 interface.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI3\_- FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex

to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x168

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	Force int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	force_int_event_fifo_overflow	R/W	Force int_event_fifo_overflow . <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	force_pixel_if_hline_err	R/W	Force pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	force_pixel_if_fifo_nempty_fs	R/W	Force pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	force_frame_sync_err	R/W	Force for frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	force_pixel_if_fifo_overflow	R/W	Force for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	force_pixel_if_fifo_underflow	R/W	Force for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_IPI4\_FATAL**

**Name:** Fatal interruption caused by IPI4 interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI4\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x170

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	Reporting internal FIFO overflow on pulse delay block. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	int_event_fifo_overflow	RC	Reporting internal FIFO overflow during IPI data processing. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	pixel_if_hline_err	RC	Horizontal line time error (only available in controller mode). <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	pixel_if_fifo_nempty_fs	RC	Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame. There are some scenarios where synchronization events of new frame can be lost on IPI interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	pixel_if_frame_sync_err	RC	Whenever in Controller mode, notifies if a new frame is received but previous has not been completed. <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
1	pixel_if_fifo_overflow	RC	The FIFO of pixel interface has lost information because some data arrived and FIFO is already full. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	pixel_if_fifo_underflow	RC	The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_IPI4\_FATAL**

**Name:** Mask for fatal interruption caused by IPI4 interface.

**Description:** Interrupt mask for INT\_ST\_IPI4\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x174

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	msk_int_pulse_delay_overflow	R/W	Mask int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	msk_int_event_fifo_overflow	R/W	Mask int_event_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	msk_pixel_if_hline_err	R/W	Mask pixel_if_hline_err.

Bits	Name	Memory Access	Description
			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	msk_pixel_if_fifo_nempty_fs	R/W	Mask pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	msk_frame_sync_err	R/W	Mask for pixel_if_frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	msk_pixel_if_fifo_overflow	R/W	Mask for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	msk_pixel_if_fifo_underflow	R/W	Mask for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_FORCE\_IPI4\_FATAL**

**Name:** Force for fatal interruption caused by IPI4 interface.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI4\_- FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x178

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	Force int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

5	force_int_event_fifo_overflow	R/W	<p>Force int_event_fifo_overflow . <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
4	force_pixel_if_hline_err	R/W	<p>Force pixel_if_hline_err. <b>Value After Reset:</b> 0x0      <b>Exists:</b> Always</p>
3	force_pixel_if_fifo_nempty_fs	R/W	<p>Force pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
2	force_frame_sync_err	R/W	<p>Force for frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
1	force_pixel_if_fifo_overflow	R/W	<p>Force for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>
0	force_pixel_if_fifo_underflow	R/W	<p>Force for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always</p>

**IPI2\_MODE**

**Name:** IPI2 Mode.

**Description:** This register selects how the IPI interface 2 generates the video frame.

**Size:** 32 bits

**Offset:** 0x200

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
24	ipi_enable	R/W	<p>This register enables the interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
23:17			<b>Reserved Field:</b> Yes
16	ipi_cut_through	R/W	<p>This field indicates cut-through mode state:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	<p>This field indicates if color mode components are delivered as follows:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:0			<b>Reserved Field:</b> Yes

**IPI2\_VCID****Name:** IPI2 Virtual Channel.**Description:** This register selects the virtual channel processed by IPI2.**Size:** 32 bits**Offset:** 0x204

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcx_2	R/W	<p>Virtual channel extension extra bit of data to be processed by pixel interface 2</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

3:2	ipi_vcx_0_1	R/W	Virtual channel extension of data to be processed by pixel interface 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1:0	ipi_vcidx	R/W	Virtual channel of data to be processed by pixel interface 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI2\_DATA\_TYPE****Name:** IPI2 Data Type.**Description:** This register selects the data type processed by IPI2.**Size:** 32 bits**Offset:** 0x208

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	embedded_data	R/W	For Camera Timing Mode, this bit enables embedded data processing on IPI 2 interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	Data type of data to be processed by pixel interface 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI2\_MEM\_FLUSH****Name:** IPI2 Flush Memory.**Description:** This register control the flush of IPI2 memory.**Size:** 32 bits**Offset:** 0x20c

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
8	ipi_auto_flush	R/W	<p>Memory is automatically flushed at each Frame Start.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	<p>Flush IPI2 memory. This bit is auto clear.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI2\_HSA\_TIME****Name:** IPI2 HSA.**Description:** This register configures the video Horizontal Synchronism Active (HSA) time for pixel Interface 2.**Size:** 32 bits**Offset:** 0x210

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	<p>This field configures the Horizontal Synchronism Active period in pixclk cycles.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI2\_HBP\_TIME****Name:** IPI2 HBP.**Description:** This register configures the video Horizontal Back Porch (HBP) time for pixel Interface 2.**Size:** 32 bits**Offset:** 0x214

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hbp_time	R/W	<p>This field configures the Horizontal Back Porch period in pixclk cycles.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always

**IPI2\_HSD\_TIME****Name:** IPI2 HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time for pixel Interface 2.**Size:** 32 bits**Offset:** 0x218

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	This field configures the Horizontal Sync Delay period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI2\_ADV\_FEATURES****Name:** IPI2 Advanced Features.**Description:** This register configures advanced features for IPI2 mode.**Size:** 32 bits**Offset:** 0x21c

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_sync_event_mode	R/W	For Camera Timing Mode: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:22			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
21	en_embedded	R/W	<p>This register allows the use of embedded packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
20	en_blanking	R/W	<p>This register allows the use of blanking packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
19	en_null	R/W	<p>This register allows the use of null packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
18	en_line_start	R/W	<p>This register allows the use of line start packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
17	en_video	R/W	<p>This register allows the use of video packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
16	line_event_selection	R/W	<p>For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows: <b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	<p>Datatype to overwrite.</p> <p><b>Value After</b></p>

Bits	Name	Memory Access	Description
			<b>Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	Ignore datatype of the header using the programmed datatype for decoding. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI3\_MODE****Name:** IPI3 Mode.**Description:** This register selects how the IPI interface 3 generates the video frame.**Size:** 32 bits**Offset:** 0x220

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_enable	R/W	This register enables the interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:17			<b>Reserved Field:</b> Yes
16	ipi_cut_through	R/W	This field indicates cut-through mode state: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	This field indicates if color mode components are delivered as follows: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul>

			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:0			<b>Reserved Field:</b> Yes

**IPI3\_VCID****Name:** IPI3 Virtual Channel.**Description:** This register selects the virtual channel processed by IPI3.**Size:** 32 bits**Offset:** 0x224

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcx_2	R/W	Virtual channel extension extra bit of data to be processed by pixel interface 3 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
3:2	ipi_vcx_0_1	R/W	Virtual channel extension of data to be processed by pixel interface 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1:0	ipi_vcld	R/W	Virtual channel of data to be processed by pixel interface 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI3\_DATA\_TYPE****Name:** IPI3 Data Type.**Description:** This register selects the data type processed by IPI3.**Size:** 32 bits**Offset:** 0x228

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes

8	embedded_data	R/W	For Camera Timing Mode, this bit enables embedded data processing on pixel interface 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	Data type of data to be processed by pixel interface 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI3\_MEM\_FLUSH****Name:** IPI3 Flush Memory.**Description:** This register control the flush of IPI3 memory.**Size:** 32 bits**Offset:** 0x22c

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	ipi_auto_flush	R/W	Memory is automatically flushed at each Frame Start. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	Flush IPI3 memory. This bit is auto clear. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI3\_HSA\_TIME****Name:** IPI3 HSA.**Description:** This register configures the video Horizontal Synchronism Active (HSA) time for pixel Interface 3.**Size:** 32 bits**Offset:** 0x230

Bits	Name	Memory	Description

		Access	
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	This field configures the Horizontal Synchronism Active period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI3\_HBP\_TIME****Name:** IPI3 HBP.**Description:** This register configures the video Horizontal Back Porch (HBP) time for pixel Interface 3.**Size:** 32 bits**Offset:** 0x234

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hbp_time	R/W	This field configures the Horizontal Back Porch period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI3\_HSD\_TIME****Name:** IPI3 HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time for pixel Interface 3.**Size:** 32 bits**Offset:** 0x238

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	This field configures the Horizontal Sync Delay period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI3\_ADV\_FEATURES**

**Name:** IPI3 Advanced Features.

**Description:** This register configures advanced features for IPI3 mode.

**Size:** 32 bits

**Offset:** 0x23c

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_sync_event_mode	R/W	<p>For Camera Timing Mode:  <b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
23:22			<b>Reserved Field:</b> Yes
21	en_embedded	R/W	<p>This register allows the use of embedded packets for IPI synchronization events.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
20	en_blanking	R/W	<p>This register allows the use of blanking packets for IPI synchronization events.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
19	en_null	R/W	<p>This register allows the use of null packets for IPI synchronization events.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
18	en_line_start	R/W	<p>This register allows the use of line start packets for IPI synchronization events.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
17	en_video	R/W	<p>This register allows the use of video packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
16	line_event_selection	R/W	<p>For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows: <b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	<p>Datatype to overwrite.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	<p>Ignore datatype of the header using the programmed datatype for decoding.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI4\_MODE**

**Name:** IPI4 Mode.

**Description:** This register selects how the IPI interface 4 generates the video frame.

**Size:** 32 bits

**Offset:** 0x240

Bits	Name	Memory	Description
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		Access	
31:25			<b>Reserved Field:</b> Yes
24	ipi_enable	R/W	This register enables the interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:17			<b>Reserved Field:</b> Yes
16	ipi_cut_through	R/W	This field indicates cut-through mode state: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	This field indicates if color mode components are delivered as follows: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:0			<b>Reserved Field:</b> Yes

**IPI4\_VCID****Name:** IPI4 Virtual Channel.**Description:** This register selects the virtual channel processed by IPI4.**Size:** 32 bits**Offset:** 0x244

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcx_2	R/W	Virtual channel extension extra bit of data to be processed by pixel interface 4 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
3:2	ipi_vcx_0_1	R/W	<p>Virtual channel extension of data to be processed by pixel interface 4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1:0	ipi_vcidx	R/W	<p>Virtual channel of data to be processed by pixel interface 4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI4\_DATA\_TYPE**

**Name:** IPI4 Data Type.

**Description:** This register selects the data type processed by IPI4.

**Size:** 32 bits

**Offset:** 0x248

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	embedded_data	R/W	<p>For Camera Timing Mode, this bit enables embedded data processing on pixel interface 4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	<p>Data type of data to be processed by pixel interface 4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI4\_MEM\_FLUSH**

**Name:** IPI4 Flush Memory.

**Description:** This register control the flush of IPI4 memory.

**Size:** 32 bits

**Offset:** 0x24c

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	ipi_auto_flush	R/W	Memory is automatically flushed at each Frame Start. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	Flush IPI4 memory. This bit is auto clear. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI4\_HSA\_TIME****Name:** IPI4 HSA.**Description:** This register configures the video Horizontal Synchronism Active (HSA) time for pixel Interface 4.**Size:** 32 bits**Offset:** 0x250

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	This field configures the Horizontal Synchronism Active period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI4\_HBP\_TIME****Name:** IPI4 HBP.**Description:** This register configures the video Horizontal Back Porch (HBP) time for pixel Interface 4.**Size:** 32 bits**Offset:** 0x254

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
11:0	ipi_hbp_time	R/W	<p>This field configures the Horizontal Back Porch period in pixclk cycles.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI4\_HSD\_TIME****Name:** IPI4 HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time for pixel Interface 4.**Size:** 32 bits**Offset:** 0x258

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	<p>This field configures the Horizontal Sync Delay period in pixclk cycles.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI4\_ADV\_FEATURES****Name:** IPI4 Advanced Features.**Description:** This register configures advanced features for IPI4 mode.**Size:** 32 bits**Offset:** 0x25c

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_sync_event_mode	R/W	<p>For Camera Timing Mode:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul>

Bits	Name	Memory Access	Description
			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:22			<b>Reserved Field:</b> Yes
21	en_embedded	R/W	This register allows the use of embedded packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
20	en_blanking	R/W	This register allows the use of blanking packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
19	en_null	R/W	This register allows the use of null packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
18	en_line_start	R/W	This register allows the use of line start packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
17	en_video	R/W	This register allows the use of video packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
16	line_event_selection	R/W	For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	Datatype to overwrite. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	Ignore datatype of the header using the programmed datatype for decoding. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_BNDRY\_FRAME\_FATAL**

**Name:** Fatal Interruption caused by Frame Boundaries.

**Description:** Fatal interruption related with matching Frame Start with Frame End for a specific virtual channel. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_BNDRY\_FRAME\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x280

Bits	Name	Memory Access	Description
31	err_f_bndry_match_vc31	RC	Error matching Frame Start with Frame End for virtual channel 31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
30	err_f_bndry_match_vc30	RC	Error matching Frame Start with Frame End for virtual channel 30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
29	err_f_bndry_match_vc29	RC	Error matching Frame Start with Frame End for virtual channel 29 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
28	err_f_bndry_match_vc28	RC	Error matching Frame Start with Frame End for virtual channel 28 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_f_bndry_match_vc27	RC	Error matching Frame Start with Frame End for virtual channel 27 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_f_bndry_match_vc26	RC	Error matching Frame Start with Frame End for virtual channel 26 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
25	err_f_bndry_match_vc25	RC	Error matching Frame Start with Frame End for virtual channel 25 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_f_bndry_match_vc24	RC	Error matching Frame Start with Frame End for virtual channel 24 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
23	err_f_bndry_match_vc23	RC	Error matching Frame Start with Frame End for virtual channel 23 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
22	err_f_bndry_match_vc22	RC	Error matching Frame Start with Frame End for virtual channel 22 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
21	err_f_bndry_match_vc21	RC	Error matching Frame Start with Frame End for virtual channel 21 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
20	err_f_bndry_match_vc20	RC	Error matching Frame Start with Frame End for virtual channel 20 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
19	err_f_bndry_match_vc19	RC	Error matching Frame Start with Frame End for virtual channel 19 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
18	err_f_bndry_match_vc18	RC	Error matching Frame Start with Frame End for virtual channel 18 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
17	err_f_bndry_match_vc17	RC	Error matching Frame Start with Frame End for virtual channel 17 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
16	err_f_bndry_match_vc16	RC	Error matching Frame Start with Frame End for virtual channel 16 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
15	err_f_bndry_match_vc15	RC	Error matching Frame Start with Frame End for virtual channel 15. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
14	err_f_bndry_match_vc14	RC	Error matching Frame Start with Frame End for virtual channel 14. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
13	err_f_bndry_match_vc13	RC	Error matching Frame Start with Frame End for virtual channel 13. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
12	err_f_bndry_match_vc12	RC	Error matching Frame Start with Frame End for virtual channel 12. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
11	err_f_bndry_match_vc11	RC	Error matching Frame Start with Frame End for virtual channel 11. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
10	err_f_bndry_match_vc10	RC	Error matching Frame Start with Frame End for virtual channel 10. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
9	err_f_bndry_match_vc9	RC	Error matching Frame Start with Frame End for virtual channel 9. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
8	err_f_bndry_match_vc8	RC	Error matching Frame Start with Frame End for virtual channel 8. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7	err_f_bndry_match_vc7	RC	Error matching Frame Start with Frame End for virtual channel 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
6	err_f_bndry_match_vc6	RC	Error matching Frame Start with Frame End for virtual channel 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	err_f_bndry_match_vc5	RC	Error matching Frame Start with Frame End for virtual channel 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	err_f_bndry_match_vc4	RC	Error matching Frame Start with Frame End for virtual channel 4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	err_f_bndry_match_vc3	RC	Error matching Frame Start with Frame End for virtual channel 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	err_f_bndry_match_vc2	RC	Error matching Frame Start with Frame End for virtual channel 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_f_bndry_match_vc1	RC	Error matching Frame Start with Frame End for virtual channel 1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_f_bndry_match_vc0	RC	Error matching Frame Start with Frame End for virtual channel 0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_BNDRY\_FRAME\_FATAL**

**Name:** Mask for fatal interruption caused by Frame Boundaries.

**Description:** Interrupt mask for INT\_ST\_BNDRY\_FRAME\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

Offset: 0x284

Bits	Name	Memory Access	Description
31	err_f_bndry_match_vc31	R/W	<p>Mask for err_f_bndry_match_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_f_bndry_match_vc30	R/W	<p>Mask for err_f_bndry_match_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_f_bndry_match_vc29	R/W	<p>Mask for err_f_bndry_match_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_f_bndry_match_vc28	R/W	<p>Mask for err_f_bndry_match_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_f_bndry_match_vc27	R/W	<p>Mask for err_f_bndry_match_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_f_bndry_match_vc26	R/W	<p>Mask for err_f_bndry_match_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_f_bndry_match_vc25	R/W	<p>Mask for err_f_bndry_match_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_f_bndry_match_vc24	R/W	<p>Mask for err_f_bndry_match_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_f_bndry_match_vc23	R/W	<p>Mask for err_f_bndry_match_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_f_bndry_match_vc22	R/W	<p>Mask for err_f_bndry_match_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
21	err_f_bndry_match_vc21	R/W	<p>Mask for err_f_bndry_match_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_f_bndry_match_vc20	R/W	<p>Mask for err_f_bndry_match_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_f_bndry_match_vc19	R/W	<p>Mask for err_f_bndry_match_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_f_bndry_match_vc18	R/W	<p>Mask for err_f_bndry_match_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_f_bndry_match_vc17	R/W	<p>Mask for err_f_bndry_match_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_f_bndry_match_vc16	R/W	<p>Mask for err_f_bndry_match_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_f_bndry_match_vc15	R/W	<p>Mask for err_f_bndry_match_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_f_bndry_match_vc14	R/W	<p>Mask for err_f_bndry_match_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_f_bndry_match_vc13	R/W	<p>Mask for err_f_bndry_match_vc13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_f_bndry_match_vc12	R/W	<p>Mask for err_f_bndry_match_vc12.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
11	err_f_bndry_match_vc11	R/W	<p>Mask for err_f_bndry_match_vc11.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
10	err_f_bndry_match_vc10	R/W	<p>Mask for err_f_bndry_match_vc10.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
9	err_f_bndry_match_vc9	R/W	<p>Mask for err_f_bndry_match_vc9.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
8	err_f_bndry_match_vc8	R/W	<p>Mask for err_f_bndry_match_vc8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7	err_f_bndry_match_vc7	R/W	<p>Mask for err_f_bndry_match_vc7.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
6	err_f_bndry_match_vc6	R/W	<p>Mask for err_f_bndry_match_vc6.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	err_f_bndry_match_vc5	R/W	<p>Mask for err_f_bndry_match_vc5.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	err_f_bndry_match_vc4	R/W	<p>Mask for err_f_bndry_match_vc4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	err_f_bndry_match_vc3	R/W	<p>Mask for err_f_bndry_match_vc3.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	err_f_bndry_match_vc2	R/W	<p>Mask for err_f_bndry_match_vc2.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	err_f_bndry_match_vc1	R/W	<p>Mask for err_f_bndry_match_vc1.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	err_f_bndry_match_vc0	R/W	<p>Mask for err_f_bndry_match_vc0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_FORCE\_BNDRY\_FRAME\_FATAL**

**Name:** Force for fatal interruption caused by Frame Boundaries.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_BN- DRY\_FRAME\_FATAL interrupt events individually, without the need to activate the conditions that trigger the interrupt sources, since it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x288

Bits	Name	Memory Access	Description
31	err_f_bndry_match_vc31	R/W	Force err_f_bndry_match_vc31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
30	err_f_bndry_match_vc30	R/W	Force err_f_bndry_match_vc30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
29	err_f_bndry_match_vc29	R/W	Force err_f_bndry_match_vc29 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
28	err_f_bndry_match_vc28	R/W	Force err_f_bndry_match_vc28 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_f_bndry_match_vc27	R/W	Force err_f_bndry_match_vc27 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_f_bndry_match_vc26	R/W	Force err_f_bndry_match_vc26 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
25	err_f_bndry_match_vc25	R/W	Force err_f_bndry_match_vc25 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_f_bndry_match_vc24	R/W	Force err_f_bndry_match_vc24 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
23	err_f_bndry_match_vc23	R/W	<p>Force err_f_bndry_match_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_f_bndry_match_vc22	R/W	<p>Force err_f_bndry_match_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_f_bndry_match_vc21	R/W	<p>Force err_f_bndry_match_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_f_bndry_match_vc20	R/W	<p>Force err_f_bndry_match_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_f_bndry_match_vc19	R/W	<p>Force err_f_bndry_match_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_f_bndry_match_vc18	R/W	<p>Force err_f_bndry_match_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_f_bndry_match_vc17	R/W	<p>Force err_f_bndry_match_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_f_bndry_match_vc16	R/W	<p>Force err_f_bndry_match_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_f_bndry_match_vc15	R/W	<p>Force err_f_bndry_match_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_f_bndry_match_vc14	R/W	<p>Force err_f_bndry_match_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_f_bndry_match_vc13	R/W	<p>Force err_f_bndry_match_vc13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
12	err_f_bndry_match_vc12	R/W	<p>Force err_f_bndry_match_vc12.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
11	err_f_bndry_match_vc11	R/W	<p>Force err_f_bndry_match_vc11.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
10	err_f_bndry_match_vc10	R/W	<p>Force err_f_bndry_match_vc10.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
9	err_f_bndry_match_vc9	R/W	<p>Force err_f_bndry_match_vc9.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
8	err_f_bndry_match_vc8	R/W	<p>Force err_f_bndry_match_vc8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7	err_f_bndry_match_vc7	R/W	<p>Force err_f_bndry_match_vc7.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
6	err_f_bndry_match_vc6	R/W	<p>Force err_f_bndry_match_vc6.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	err_f_bndry_match_vc5	R/W	<p>Force err_f_bndry_match_vc5.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	err_f_bndry_match_vc4	R/W	<p>Force err_f_bndry_match_vc4.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
3	err_f_bndry_match_vc3	R/W	Force err_f_bndry_match_vc3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	err_f_bndry_match_vc2	R/W	Force err_f_bndry_match_vc2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_f_bndry_match_vc1	R/W	Force err_f_bndry_match_vc1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_f_bndry_match_vc0	R/W	Force err_f_bndry_match_vc0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_SEQ\_FRAME\_FATAL**

**Name:** Fatal Interruption caused by Frame Sequence.

**Description:** Fatal interruption related with incorrect Frame sequence for a specific virtual channel. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_SEQ\_FRAME\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x290

Bits	Name	Memory Access	Description
31	err_f_seq_vc31	RC	Incorrect Frame sequence detected in virtual channel 31 <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> (CSI2_HOST_PHY == 2)==1
30	err_f_seq_vc30	RC	Incorrect Frame sequence detected in virtual channel 30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
29	err_f_seq_vc29	RC	Incorrect Frame sequence detected in virtual channel 29 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
28	err_f_seq_vc28	RC	Incorrect Frame sequence detected in virtual channel 28 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_f_seq_vc27	RC	Incorrect Frame sequence detected in virtual channel 27 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_f_seq_vc26	RC	Incorrect Frame sequence detected in virtual channel 26 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
25	err_f_seq_vc25	RC	Incorrect Frame sequence detected in virtual channel 25 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_f_seq_vc24	RC	Incorrect Frame sequence detected in virtual channel 24 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
23	err_f_seq_vc23	RC	Incorrect Frame sequence detected in virtual channel 23 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
22	err_f_seq_vc22	RC	<p>Incorrect Frame sequence detected in virtual channel 22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_f_seq_vc21	RC	<p>Incorrect Frame sequence detected in virtual channel 21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_f_seq_vc20	RC	<p>Incorrect Frame sequence detected in virtual channel 20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_f_seq_vc19	RC	<p>Incorrect Frame sequence detected in virtual channel 19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_f_seq_vc18	RC	<p>Incorrect Frame sequence detected in virtual channel 18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_f_seq_vc17	RC	<p>Incorrect Frame sequence detected in virtual channel 17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_f_seq_vc16	RC	<p>Incorrect Frame sequence detected in virtual channel 16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_f_seq_vc15	RC	<p>Incorrect Frame sequence detected in virtual channel 15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_f_seq_vc14	RC	<p>Incorrect Frame sequence detected in virtual channel 14.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
13	err_f_seq_vc13	RC	Incorrect Frame sequence detected in virtual channel 13. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
12	err_f_seq_vc12	RC	Incorrect Frame sequence detected in virtual channel 12. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
11	err_f_seq_vc11	RC	Incorrect Frame sequence detected in virtual channel 11. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
10	err_f_seq_vc10	RC	Incorrect Frame sequence detected in virtual channel 10. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
9	err_f_seq_vc9	RC	Incorrect Frame sequence detected in virtual channel 9. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
8	err_f_seq_vc8	RC	Incorrect Frame sequence detected in virtual channel 8. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7	err_f_seq_vc7	RC	Incorrect Frame sequence detected in virtual channel 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
6	err_f_seq_vc6	RC	Incorrect Frame sequence detected in virtual channel 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
5	err_f_seq_vc5	RC	Incorrect Frame sequence detected in virtual channel 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	err_f_seq_vc4	RC	Incorrect Frame sequence detected in virtual channel 4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	err_f_seq_vc3	RC	Incorrect Frame sequence detected in virtual channel 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	err_f_seq_vc2	RC	Incorrect Frame sequence detected in virtual channel 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_f_seq_vc1	RC	Incorrect Frame sequence detected in virtual channel 1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_f_seq_vc0	RC	Incorrect Frame sequence detected in virtual channel 0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_SEQ\_FRAME\_FATAL**

**Name:** Mask for fatal interruption caused by Frame Sequence.

**Description:** Interrupt mask for INT\_ST\_SEQ\_FRAME\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x294

Bits	Name	Memory Access	Description
31	err_f_seq_vc31	R/W	<p>Mask for err_f_seq_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_f_seq_vc30	R/W	<p>Mask for err_f_seq_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_f_seq_vc29	R/W	<p>Mask for err_f_seq_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_f_seq_vc28	R/W	<p>Mask for err_f_seq_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_f_seq_vc27	R/W	<p>Mask for err_f_seq_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_f_seq_vc26	R/W	<p>Mask for err_f_seq_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_f_seq_vc25	R/W	<p>Mask for err_f_seq_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_f_seq_vc24	R/W	<p>Mask for err_f_seq_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_f_seq_vc23	R/W	<p>Mask for err_f_seq_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_f_seq_vc22	R/W	<p>Mask for err_f_seq_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_f_seq_vc21	R/W	<p>Mask for err_f_seq_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
20	err_f_seq_vc20	R/W	<p>Mask for err_f_seq_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_f_seq_vc19	R/W	<p>Mask for err_f_seq_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_f_seq_vc18	R/W	<p>Mask for err_f_seq_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_f_seq_vc17	R/W	<p>Mask for err_f_seq_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_f_seq_vc16	R/W	<p>Mask for err_f_seq_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_f_seq_vc15	R/W	<p>Mask for err_f_seq_vc15. <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always</p>
14	err_f_seq_vc14	R/W	<p>Mask for err_f_seq_vc14. <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always</p>
13	err_f_seq_vc13	R/W	<p>Mask for err_f_seq_vc13. <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always</p>
12	err_f_seq_vc12	R/W	<p>Mask for err_f_seq_vc12. <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
11	err_f_seq_vc11	R/W	<p>Mask for err_f_seq_vc11. <b>Value</b>  <b>After Reset:</b> 0x0  <b>Exists:</b> Always</p>
10	err_f_seq_vc10	R/W	<p>Mask for err_f_seq_vc10. <b>Value</b>  <b>After Reset:</b> 0x0  <b>Exists:</b> Always</p>
9	err_f_seq_vc9	R/W	<p>Mask for err_f_seq_vc9.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
8	err_f_seq_vc8	R/W	<p>Mask for err_f_seq_vc8.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
7	err_f_seq_vc7	R/W	<p>Mask for err_f_seq_vc7.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
6	err_f_seq_vc6	R/W	<p>Mask for err_f_seq_vc6.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
5	err_f_seq_vc5	R/W	<p>Mask for err_f_seq_vc5.  <b>Value After</b></p>

Bits	Name	Memory Access	Description
			<b>Reset:</b> 0x0 <b>Exists:</b> Always
4	err_f_seq_vc4	R/W	Mask for err_f_seq_vc4. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
3	err_f_seq_vc3	R/W	Mask for err_f_seq_vc3. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
2	err_f_seq_vc2	R/W	Mask for err_f_seq_vc2. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
1	err_f_seq_vc1	R/W	Mask for err_f_seq_vc1. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
0	err_f_seq_vc0	R/W	Mask for err_f_seq_vc0. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_FORCE\_SEQ\_FRAME\_FATAL**

**Name:** Force for fatal interruption caused by Frame Sequence.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_SEQ\_- FRAME\_FATAL interrupt events individually. There is no need to

activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x298

Bits	Name	Memory Access	Description
31	err_f_seq_vc31	R/W	<p>Force err_f_seq_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_f_seq_vc30	R/W	<p>Force err_f_seq_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_f_seq_vc29	R/W	<p>Force err_f_seq_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_f_seq_vc28	R/W	<p>Force err_f_seq_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_f_seq_vc27	R/W	<p>Force err_f_seq_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_f_seq_vc26	R/W	<p>Force err_f_seq_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_f_seq_vc25	R/W	<p>Force err_f_seq_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_f_seq_vc24	R/W	<p>Force err_f_seq_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_f_seq_vc23	R/W	<p>Force err_f_seq_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
22	err_f_seq_vc22	R/W	<p>Force err_f_seq_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_f_seq_vc21	R/W	<p>Force err_f_seq_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_f_seq_vc20	R/W	<p>Force err_f_seq_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_f_seq_vc19	R/W	<p>Force err_f_seq_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_f_seq_vc18	R/W	<p>Force err_f_seq_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_f_seq_vc17	R/W	<p>Force err_f_seq_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_f_seq_vc16	R/W	<p>Force err_f_seq_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_f_seq_vc15	R/W	<p>Force err_f_seq_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_f_seq_vc14	R/W	<p>Force err_f_seq_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
13	err_f_seq_vc13	R/W	<p>Force err_f_seq_vc13.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_f_seq_vc12	R/W	<p>Force err_f_seq_vc12.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
11	err_f_seq_vc11	R/W	<p>Force err_f_seq_vc11.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
10	err_f_seq_vc10	R/W	<p>Force err_f_seq_vc10.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
9	err_f_seq_vc9	R/W	<p>Force err_f_seq_vc9.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
8	err_f_seq_vc8	R/W	<p>Force err_f_seq_vc8.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
7	err_f_seq_vc7	R/W	<p>Force err_f_seq_vc7.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
6	err_f_seq_vc6	R/W	<p>Force err_f_seq_vc6.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	err_f_seq_vc5	R/W	<p>Force err_f_seq_vc5.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	err_f_seq_vc4	R/W	<p>Force err_f_seq_vc4.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	err_f_seq_vc3	R/W	<p>Force err_f_seq_vc3.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	err_f_seq_vc2	R/W	<p>Force err_f_seq_vc2.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
1	err_f_seq_vc1	R/W	<p>Force err_f_seq_vc1.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	err_f_seq_vc0	R/W	<p>Force err_f_seq_vc0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_ST\_CRC\_FRAME\_FATAL**

**Name:** Fatal Interruption caused by Frame CRC.

**Description:** Fatal interruption related with Frames with at least one CRC error for a specific virtual channel. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_CRC\_FRAME\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x2a0

Bits	Name	Memory Access	Description
31	err_frame_data_vc31	RC	<p>Last received Frame in virtual channel 31, had at least one CRC error</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_frame_data_vc30	RC	<p>Last received Frame in virtual channel 30, had at least one CRC error</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_frame_data_vc29	RC	<p>Last received Frame in virtual channel 29, had at least one CRC error</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
28	err_frame_data_vc28	RC	Last received Frame in virtual channel 28, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_frame_data_vc27	RC	Last received Frame in virtual channel 27, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_frame_data_vc26	RC	Last received Frame in virtual channel 26, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
25	err_frame_data_vc25	RC	Last received Frame in virtual channel 25, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_frame_data_vc24	RC	Last received Frame in virtual channel 24, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
23	err_frame_data_vc23	RC	Last received Frame in virtual channel 23, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
22	err_frame_data_vc22	RC	Last received Frame in virtual channel 22, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
21	err_frame_data_vc21	RC	Last received Frame in virtual channel 21, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
20	err_frame_data_vc20	RC	Last received Frame in virtual channel 20, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
19	err_frame_data_vc19	RC	Last received Frame in virtual channel 19, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
18	err_frame_data_vc18	RC	Last received Frame in virtual channel 18, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
17	err_frame_data_vc17	RC	Last received Frame in virtual channel 17, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
16	err_frame_data_vc16	RC	Last received Frame in virtual channel 16, had at least one CRC error <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
15	err_frame_data_vc15	RC	Last received Frame in virtual channel 15, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
14	err_frame_data_vc14	RC	Last received Frame in virtual channel 14, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
13	err_frame_data_vc13	RC	Last received Frame in virtual channel 13, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
12	err_frame_data_vc12	RC	Last received Frame in virtual channel 12, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
11	err_frame_data_vc11	RC	Last received Frame in virtual channel 11, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
10	err_frame_data_vc10	RC	Last received Frame in virtual channel 10, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
9	err_frame_data_vc9	RC	Last received Frame in virtual channel 9, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
8	err_frame_data_vc8	RC	Last received Frame in virtual channel 8, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7	err_frame_data_vc7	RC	Last received Frame in virtual channel 7, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
6	err_frame_data_vc6	RC	Last received Frame in virtual channel 6, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	err_frame_data_vc5	RC	Last received Frame in virtual channel 5, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
4	err_frame_data_vc4	RC	Last received Frame in virtual channel 4, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	err_frame_data_vc3	RC	Last received Frame in virtual channel 3, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	err_frame_data_vc2	RC	Last received Frame in virtual channel 2, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_frame_data_vc1	RC	Last received Frame in virtual channel 1, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_frame_data_vc0	RC	Last received Frame in virtual channel 0, had at least one CRC error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_CRC\_FRAME\_FATAL**

**Name:** Mask for fatal interruption caused by Frame CRC.

**Description:** Interrupt mask for INT\_ST\_CRC\_FRAME\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x2a4

Bits	Name	Memory Access	Description
31	err_frame_data_vc31	R/W	Mask for err_frame_data_vc31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
30	err_frame_data_vc30	R/W	<p>Mask for err_frame_data_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_frame_data_vc29	R/W	<p>Mask for err_frame_data_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_frame_data_vc28	R/W	<p>Mask for err_frame_data_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_frame_data_vc27	R/W	<p>Mask for err_frame_data_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_frame_data_vc26	R/W	<p>Mask for err_frame_data_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_frame_data_vc25	R/W	<p>Mask for err_frame_data_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_frame_data_vc24	R/W	<p>Mask for err_frame_data_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_frame_data_vc23	R/W	<p>Mask for err_frame_data_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_frame_data_vc22	R/W	<p>Mask for err_frame_data_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_frame_data_vc21	R/W	<p>Mask for err_frame_data_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_frame_data_vc20	R/W	<p>Mask for err_frame_data_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
19	err_frame_data_vc19	R/W	<p>Mask for err_frame_data_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_frame_data_vc18	R/W	<p>Mask for err_frame_data_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_frame_data_vc17	R/W	<p>Mask for err_frame_data_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_frame_data_vc16	R/W	<p>Mask for err_frame_data_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_frame_data_vc15	R/W	<p>Mask for err_frame_data_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_frame_data_vc14	R/W	<p>Mask for err_frame_data_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_frame_data_vc13	R/W	<p>Mask for err_frame_data_vc13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_frame_data_vc12	R/W	<p>Mask for err_frame_data_vc12.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
11	err_frame_data_vc11	R/W	<p>Mask for err_frame_data_vc11.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
10	err_frame_data_vc10	R/W	<p>Mask for err_frame_data_vc10.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
9	err_frame_data_vc9	R/W	<p>Mask for err_frame_data_vc9.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
8	err_frame_data_vc8	R/W	<p>Mask for err_frame_data_vc8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7	err_frame_data_vc7	R/W	<p>Mask for err_frame_data_vc7.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
6	err_frame_data_vc6	R/W	<p>Mask for err_frame_data_vc6.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	err_frame_data_vc5	R/W	<p>Mask for err_frame_data_vc5.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	err_frame_data_vc4	R/W	<p>Mask for err_frame_data_vc4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	err_frame_data_vc3	R/W	<p>Mask for err_frame_data_vc3.</p> <p><b>Value After Reset:</b></p>

Bits	Name	Memory Access	Description
			0x0 <b>Exists:</b> Always
2	err_frame_data_vc2	R/W	Mask for err_frame_data_vc2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_frame_data_vc1	R/W	Mask for err_frame_data_vc1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_frame_data_vc0	R/W	Mask for err_frame_data_vc0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_FORCE\_CRC\_FRAME\_FATAL**

**Name:** Force for fatal interruption caused by Frame CRC.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_CRC\_- FRAME\_FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x2a8

Bits	Name	Memory Access	Description
31	err_frame_data_vc31	R/W	Force err_frame_data_vc31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
30	err_frame_data_vc30	R/W	Force err_frame_data_vc30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
29	err_frame_data_vc29	R/W	Force err_frame_data_vc29 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
28	err_frame_data_vc28	R/W	Force err_frame_data_vc28 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_frame_data_vc27	R/W	Force err_frame_data_vc27 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_frame_data_vc26	R/W	Force err_frame_data_vc26 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
25	err_frame_data_vc25	R/W	Force err_frame_data_vc25 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_frame_data_vc24	R/W	Force err_frame_data_vc24 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
23	err_frame_data_vc23	R/W	Force err_frame_data_vc23 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
22	err_frame_data_vc22	R/W	Force err_frame_data_vc22 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
21	err_frame_data_vc21	R/W	Force err_frame_data_vc21 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
20	err_frame_data_vc20	R/W	Force err_frame_data_vc20 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
19	err_frame_data_vc19	R/W	Force err_frame_data_vc19 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
18	err_frame_data_vc18	R/W	Force err_frame_data_vc18 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
17	err_frame_data_vc17	R/W	Force err_frame_data_vc17 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
16	err_frame_data_vc16	R/W	Force err_frame_data_vc16 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
15	err_frame_data_vc15	R/W	Force err_frame_data_vc15. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
14	err_frame_data_vc14	R/W	Force err_frame_data_vc14. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
13	err_frame_data_vc13	R/W	Force err_frame_data_vc13. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
12	err_frame_data_vc12	R/W	Force err_frame_data_vc12. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
11	err_frame_data_vc11	R/W	Force err_frame_data_vc11. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
10	err_frame_data_vc10	R/W	Force err_frame_data_vc10. <b>Value After Reset:</b>

Bits	Name	Memory Access	Description
			0x0 <b>Exists:</b> Always
9	err_frame_data_vc9	R/W	Force err_frame_data_vc9. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
8	err_frame_data_vc8	R/W	Force err_frame_data_vc8. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7	err_frame_data_vc7	R/W	Force err_frame_data_vc7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
6	err_frame_data_vc6	R/W	Force err_frame_data_vc6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	err_frame_data_vc5	R/W	Force err_frame_data_vc5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	err_frame_data_vc4	R/W	Force err_frame_data_vc4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	err_frame_data_vc3	R/W	Force err_frame_data_vc3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
2	err_frame_data_vc2	R/W	Force err_frame_data_vc2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_frame_data_vc1	R/W	Force err_frame_data_vc1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_frame_data_vc0	R/W	Force err_frame_data_vc0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_PLD\_CRC\_FATAL**

**Name:** Fatal Interruption caused by Payload CRC.

**Description:** Fatal interruption related with Payload Checksum error. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_PLD\_CRC\_- FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x2b0

Bits	Name	Memory Access	Description
31	err_crc_vc31	RC	Payload Checksum error detected on virtual channel 31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
30	err_crc_vc30	RC	Payload Checksum error detected on virtual channel 30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
29	err_crc_vc29	RC	Payload Checksum error detected on virtual channel 29 <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> (CSI2_HOST_PHY == 2)==1
28	err_crc_vc28	RC	Payload Checksum error detected on virtual channel 28 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_crc_vc27	RC	Payload Checksum error detected on virtual channel 27 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_crc_vc26	RC	Payload Checksum error detected on virtual channel 26 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
25	err_crc_vc25	RC	Payload Checksum error detected on virtual channel 25 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_crc_vc24	RC	Payload Checksum error detected on virtual channel 24 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
23	err_crc_vc23	RC	Payload Checksum error detected on virtual channel 23 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
22	err_crc_vc22	RC	Payload Checksum error detected on virtual channel 22 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
21	err_crc_vc21	RC	Payload Checksum error detected on virtual channel 21 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
20	err_crc_vc20	RC	<p>Payload Checksum error detected on virtual channel 20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_crc_vc19	RC	<p>Payload Checksum error detected on virtual channel 19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_crc_vc18	RC	<p>Payload Checksum error detected on virtual channel 18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_crc_vc17	RC	<p>Payload Checksum error detected on virtual channel 17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_crc_vc16	RC	<p>Payload Checksum error detected on virtual channel 16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_crc_vc15	RC	<p>Payload Checksum error detected on virtual channel 15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_crc_vc14	RC	<p>Payload Checksum error detected on virtual channel 14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_crc_vc13	RC	<p>Payload Checksum error detected on virtual channel 13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_crc_vc12	RC	<p>Payload Checksum error detected on virtual channel 12.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
11	err_crc_vc11	RC	Payload Checksum error detected on virtual channel 11. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
10	err_crc_vc10	RC	Payload Checksum error detected on virtual channel 10. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
9	err_crc_vc9	RC	Payload Checksum error detected on virtual channel 9. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
8	err_crc_vc8	RC	Payload Checksum error detected on virtual channel 8. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7	err_crc_vc7	RC	Payload Checksum error detected on virtual channel 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
6	err_crc_vc6	RC	Payload Checksum error detected on virtual channel 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	err_crc_vc5	RC	Payload Checksum error detected on virtual channel 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	err_crc_vc4	RC	Payload Checksum error detected on virtual channel 4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
3	err_crc_vc3	RC	<p>Payload Checksum error detected on virtual channel 3.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	err_crc_vc2	RC	<p>Payload Checksum error detected on virtual channel 2.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	err_crc_vc1	RC	<p>Payload Checksum error detected on virtual channel 1.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	err_crc_vc0	RC	<p>Payload Checksum error detected on virtual channel 0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_PLD\_CRC\_FATAL**

**Name:** Mask for fatal interruption caused by Payload CRC.

**Description:** Interrupt mask for INT\_ST\_PLD\_CRC\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x2b4

Bits	Name	Memory Access	Description
31	err_crc_vc31	R/W	<p>Mask for err_crc_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
30	err_crc_vc30	R/W	<p>Mask for err_crc_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_crc_vc29	R/W	<p>Mask for err_crc_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_crc_vc28	R/W	<p>Mask for err_crc_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_crc_vc27	R/W	<p>Mask for err_crc_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_crc_vc26	R/W	<p>Mask for err_crc_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_crc_vc25	R/W	<p>Mask for err_crc_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_crc_vc24	R/W	<p>Mask for err_crc_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_crc_vc23	R/W	<p>Mask for err_crc_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_crc_vc22	R/W	<p>Mask for err_crc_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_crc_vc21	R/W	<p>Mask for err_crc_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_crc_vc20	R/W	<p>Mask for err_crc_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
19	err_crc_vc19	R/W	<p>Mask for err_crc_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_crc_vc18	R/W	<p>Mask for err_crc_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_crc_vc17	R/W	<p>Mask for err_crc_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_crc_vc16	R/W	<p>Mask for err_crc_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_crc_vc15	R/W	<p>Mask for err_crc_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_crc_vc14	R/W	<p>Mask for err_crc_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_crc_vc13	R/W	<p>Mask for err_crc_vc13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_crc_vc12	R/W	<p>Mask for err_crc_vc12.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
11	err_crc_vc11	R/W	<p>Mask for err_crc_vc11.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
10	err_crc_vc10	R/W	<p>Mask for err_crc_vc10.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
9	err_crc_vc9	R/W	<p>Mask for err_crc_vc9.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
8	err_crc_vc8	R/W	<p>Mask for err_crc_vc8.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7	err_crc_vc7	R/W	<p>Mask for err_crc_vc7.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
6	err_crc_vc6	R/W	<p>Mask for err_crc_vc6.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
5	err_crc_vc5	R/W	<p>Mask for err_crc_vc5.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	err_crc_vc4	R/W	<p>Mask for err_crc_vc4.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	err_crc_vc3	R/W	<p>Mask for err_crc_vc3.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	err_crc_vc2	R/W	<p>Mask for err_crc_vc2.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	err_crc_vc1	R/W	<p>Mask for err_crc_vc1.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	err_crc_vc0	R/W	<p>Mask for err_crc_vc0.</p> <p><b>Value After</b></p> <p><b>Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_FORCE\_PLD\_CRC\_FATAL**

**Name:** Force for fatal interruption caused by Payload CRC.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_PLD\_CRC\_FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x2b8

Bits	Name	Memory Access	Description
31	err_crc_vc31	R/W	<p>Force err_crc_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_crc_vc30	R/W	<p>Force err_crc_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_crc_vc29	R/W	<p>Force err_crc_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_crc_vc28	R/W	<p>Force err_crc_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_crc_vc27	R/W	<p>Force err_crc_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_crc_vc26	R/W	<p>Force err_crc_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_crc_vc25	R/W	<p>Force err_crc_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_crc_vc24	R/W	<p>Force err_crc_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
23	err_crc_vc23	R/W	<p>Force err_crc_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_crc_vc22	R/W	<p>Force err_crc_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_crc_vc21	R/W	<p>Force err_crc_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_crc_vc20	R/W	<p>Force err_crc_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_crc_vc19	R/W	<p>Force err_crc_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_crc_vc18	R/W	<p>Force err_crc_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_crc_vc17	R/W	<p>Force err_crc_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_crc_vc16	R/W	<p>Force err_crc_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_crc_vc15	R/W	<p>Force err_crc_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_crc_vc14	R/W	<p>Force err_crc_vc14.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
13	err_crc_vc13	R/W	Force err_crc_vc13. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
12	err_crc_vc12	R/W	Force err_crc_vc12. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
11	err_crc_vc11	R/W	Force err_crc_vc11. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
10	err_crc_vc10	R/W	Force err_crc_vc10. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
9	err_crc_vc9	R/W	Force err_crc_vc9. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
8	err_crc_vc8	R/W	Force err_crc_vc8. <b>Value After</b> <b>Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
7	err_crc_vc7	R/W	Force err_crc_vc7. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
6	err_crc_vc6	R/W	Force err_crc_vc6. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
5	err_crc_vc5	R/W	Force err_crc_vc5. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
4	err_crc_vc4	R/W	Force err_crc_vc4. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
3	err_crc_vc3	R/W	Force err_crc_vc3. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
2	err_crc_vc2	R/W	Force err_crc_vc2. <b>Value After</b> <b>Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
1	err_crc_vc1	R/W	Force err_crc_vc1. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
0	err_crc_vc0	R/W	Force err_crc_vc0. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_DATA\_ID**

**Name:** Interruption caused by Data Type.

**Description:** Interruption related with unrecognized or unimplemented data type detected in a specific virtual channel. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_DATA\_ID register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x2c0

Bits	Name	Memory Access	Description
31	err_id_vc31	RC	Unrecognized or unimplemented data type detected in virtual channel 31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
30	err_id_vc30	RC	Unrecognized or unimplemented data type detected in virtual channel 30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
29	err_id_vc29	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_id_vc28	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_id_vc27	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_id_vc26	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_id_vc25	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_id_vc24	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_id_vc23	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_id_vc22	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
21	err_id_vc21	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_id_vc20	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_id_vc19	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_id_vc18	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_id_vc17	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_id_vc16	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_id_vc15	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_id_vc14	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
13	err_id_vc13	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_id_vc12	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 12.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
11	err_id_vc11	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 11.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
10	err_id_vc10	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 10.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
9	err_id_vc9	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 9.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
8	err_id_vc8	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7	err_id_vc7	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 7.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
6	err_id_vc6	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 6.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
5	err_id_vc5	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 5.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	err_id_vc4	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	err_id_vc3	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 3.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	err_id_vc2	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 2.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	err_id_vc1	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 1.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	err_id_vc0	RC	<p>Unrecognized or unimplemented data type detected in virtual channel 0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_DATA\_ID**

**Name:** Mask for interruption caused by Data Type.

**Description:** Interrupt mask for INT\_ST\_DATA\_ID controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x2c4

Bits	Name	Memory Access	Description
31	err_id_vc31	R/W	<p>Mask for err_id_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_id_vc30	R/W	<p>Mask for err_id_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_id_vc29	R/W	<p>Mask for err_id_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_id_vc28	R/W	<p>Mask for err_id_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_id_vc27	R/W	<p>Mask for err_id_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_id_vc26	R/W	<p>Mask for err_id_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_id_vc25	R/W	<p>Mask for err_id_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_id_vc24	R/W	<p>Mask for err_id_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_id_vc23	R/W	<p>Mask for err_id_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_id_vc22	R/W	<p>Mask for err_id_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_id_vc21	R/W	<p>Mask for err_id_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
20	err_id_vc20	R/W	<p>Mask for err_id_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_id_vc19	R/W	<p>Mask for err_id_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_id_vc18	R/W	<p>Mask for err_id_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_id_vc17	R/W	<p>Mask for err_id_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_id_vc16	R/W	<p>Mask for err_id_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_id_vc15	R/W	<p>Mask for err_id_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_id_vc14	R/W	<p>Mask for err_id_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_id_vc13	R/W	<p>Mask for err_id_vc13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_id_vc12	R/W	<p>Mask for err_id_vc12.</p>

Bits	Name	Memory Access	Description
			<b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
11	err_id_vc11	R/W	Mask for err_id_vc11. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
10	err_id_vc10	R/W	Mask for err_id_vc10. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
9	err_id_vc9	R/W	Mask for err_id_vc9. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
8	err_id_vc8	R/W	Mask for err_id_vc8. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
7	err_id_vc7	R/W	Mask for err_id_vc7. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
6	err_id_vc6	R/W	Mask for err_id_vc6. <b>Value After</b> <b>Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
5	err_id_vc5	R/W	Mask for err_id_vc5. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
4	err_id_vc4	R/W	Mask for err_id_vc4. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
3	err_id_vc3	R/W	Mask for err_id_vc3. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
2	err_id_vc2	R/W	Mask for err_id_vc2. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
1	err_id_vc1	R/W	Mask for err_id_vc1. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
0	err_id_vc0	R/W	Mask for err_id_vc0. <b>Value After</b> <b>Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always

**INT\_FORCE\_DATA\_ID**

**Name:** Force for interruption caused by Data Type.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_- DATA\_ID interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x2c8

Bits	Name	Memory Access	Description
31	err_id_vc31	R/W	<p>Force err_id_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_id_vc30	R/W	<p>Force err_id_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_id_vc29	R/W	<p>Force err_id_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
28	err_id_vc28	R/W	<p>Force err_id_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_id_vc27	R/W	<p>Force err_id_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_id_vc26	R/W	<p>Force err_id_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_id_vc25	R/W	<p>Force err_id_vc25</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_id_vc24	R/W	Force err_id_vc24 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
23	err_id_vc23	R/W	Force err_id_vc23 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
22	err_id_vc22	R/W	Force err_id_vc22 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
21	err_id_vc21	R/W	Force err_id_vc21 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
20	err_id_vc20	R/W	Force err_id_vc20 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
19	err_id_vc19	R/W	Force err_id_vc19 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
18	err_id_vc18	R/W	Force err_id_vc18 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
17	err_id_vc17	R/W	Force err_id_vc17 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
16	err_id_vc16	R/W	Force err_id_vc16 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
15	err_id_vc15	R/W	Force err_id_vc15. <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
14	err_id_vc14	R/W	Force err_id_vc14. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
13	err_id_vc13	R/W	Force err_id_vc13. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
12	err_id_vc12	R/W	Force err_id_vc12. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
11	err_id_vc11	R/W	Force err_id_vc11. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
10	err_id_vc10	R/W	Force err_id_vc10. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
9	err_id_vc9	R/W	Force err_id_vc9. <b>Value After</b> <b>Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
8	err_id_vc8	R/W	Force err_id_vc8. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
7	err_id_vc7	R/W	Force err_id_vc7. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
6	err_id_vc6	R/W	Force err_id_vc6. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
5	err_id_vc5	R/W	Force err_id_vc5. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
4	err_id_vc4	R/W	Force err_id_vc4. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
3	err_id_vc3	R/W	Force err_id_vc3. <b>Value After</b> <b>Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
2	err_id_vc2	R/W	Force err_id_vc2. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
1	err_id_vc1	R/W	Force err_id_vc1. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always
0	err_id_vc0	R/W	Force err_id_vc0. <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_ECC\_Corrected**

**Name:** Interruption caused by Header single bit errors.

**Description:** Interruption related with header error detected and corrected for a specific virtual channel. Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_ECC\_Corrected register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x2d0

Bits	Name	Memory Access	Description
31	err_ecc_corrected31	RC	C-PHY mode: Header CRC recoverable on virtual channel 31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
30	err_ecc_corrected30	RC	C-PHY mode: Header CRC recoverable on virtual channel 30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
29	err_ecc_corrected29	RC	C-PHY mode: Header CRC recoverable on virtual channel 29 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
28	err_ecc_corrected28	RC	C-PHY mode: Header CRC recoverable on virtual channel 28 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_ecc_corrected27	RC	C-PHY mode: Header CRC recoverable on virtual channel 27 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_ecc_corrected26	RC	C-PHY mode: Header CRC recoverable on virtual channel 26 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
25	err_ecc_corrected25	RC	C-PHY mode: Header CRC recoverable on virtual channel 25 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
24	err_ecc_corrected24	RC	C-PHY mode: Header CRC recoverable on virtual channel 24 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
23	err_ecc_corrected23	RC	C-PHY mode: Header CRC recoverable on virtual channel 23 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
22	err_ecc_corrected22	RC	C-PHY mode: Header CRC recoverable on virtual channel 22 <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> (CSI2_HOST_PHY == 2)==1
21	err_ecc_corrected21	RC	C-PHY mode: Header CRC recoverable on virtual channel 21 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
20	err_ecc_corrected20	RC	C-PHY mode: Header CRC recoverable on virtual channel 20 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
19	err_ecc_corrected19	RC	C-PHY mode: Header CRC recoverable on virtual channel 19 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
18	err_ecc_corrected18	RC	C-PHY mode: Header CRC recoverable on virtual channel 18 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
17	err_ecc_corrected17	RC	C-PHY mode: Header CRC recoverable on virtual channel 17 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
16	err_ecc_corrected16	RC	C-PHY mode: Header CRC recoverable on virtual channel 16 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
15	err_ecc_corrected_vc15	RC	D-PHY mode: Header error detected and corrected on virtual channel 15. C-PHY mode: Header CRC recoverable on virtual channel 15. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
14	err_ecc_corrected_vc14	RC	D-PHY mode: Header error detected and corrected on virtual channel 14. C-PHY mode: Header CRC recoverable on virtual channel 14. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
13	err_ecc_corrected_vc13	RC	D-PHY mode: Header error detected and corrected on virtual channel 13. C-PHY mode: Header CRC recoverable on virtual channel 13. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
12	err_ecc_corrected_vc12	RC	D-PHY mode: Header error detected and corrected on virtual channel 12. C-PHY mode: Header CRC recoverable on virtual channel 12. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
11	err_ecc_corrected_vc11	RC	D-PHY mode: Header error detected and corrected on virtual channel 11. C-PHY mode: Header CRC recoverable on virtual channel 11. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
10	err_ecc_corrected_vc10	RC	D-PHY mode: Header error detected and corrected on virtual channel 10. C-PHY mode: Header CRC recoverable on virtual channel 10. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
9	err_ecc_corrected_vc9	RC	D-PHY mode: Header error detected and corrected on virtual channel 9. C-PHY mode: Header CRC recoverable on virtual channel 9. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
8	err_ecc_corrected_vc8	RC	D-PHY mode: Header error detected and corrected on virtual channel 8. C-PHY mode: Header CRC recoverable on virtual channel 8. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
7	err_ecc_corrected_vc7	RC	D-PHY mode: Header error detected and corrected on virtual channel 7. C-PHY mode: Header CRC recoverable on virtual channel 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
6	err_ecc_corrected_vc6	RC	D-PHY mode: Header error detected and corrected on virtual channel 6. C-PHY mode: Header CRC recoverable on virtual channel 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	err_ecc_corrected_vc5	RC	D-PHY mode: Header error detected and corrected on virtual channel 5. C-PHY mode: Header CRC recoverable on virtual channel 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	err_ecc_corrected_vc4	RC	D-PHY mode: Header error detected and corrected on virtual channel 4. C-PHY mode: Header CRC recoverable on virtual channel 4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	err_ecc_corrected_vc3	RC	D-PHY mode: Header error detected and corrected on virtual channel 3. C-PHY mode: Header CRC recoverable on virtual channel 3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	err_ecc_corrected_vc2	RC	D-PHY mode: Header error detected and corrected on virtual channel 2. C-PHY mode: Header CRC recoverable on virtual channel 2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_ecc_corrected_vc1	RC	D-PHY mode: Header error detected and corrected on virtual channel 1. C-PHY mode: Header CRC recoverable on virtual channel 1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
0	err_ecc_corrected_vc0	RC	D-PHY mode: Header error detected and corrected on virtual channel 0. C-PHY mode: Header CRC recoverable on virtual channel 0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_ECC\_CORRECTED**

**Name:** Mask for interruption caused by Header single bit errors.

**Description:** Interrupt mask for INT\_ST\_ECC\_Corrected controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x2d4

Bits	Name	Memory Access	Description
31	err_ecc_corrected31	R/W	Mask for err_ecc_corrected_vc31 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
30	err_ecc_corrected30	R/W	Mask for err_ecc_corrected_vc30 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
29	err_ecc_corrected29	R/W	Mask for err_ecc_corrected_vc29 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
28	err_ecc_corrected28	R/W	Mask for err_ecc_corrected_vc28 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
27	err_ecc_corrected27	R/W	Mask for err_ecc_corrected_vc27 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
26	err_ecc_corrected26	R/W	Mask for err_ecc_corrected_vc26 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1

Bits	Name	Memory Access	Description
25	err_ecc_corrected25	R/W	<p>Mask for err_ecc_corrected_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_ecc_corrected24	R/W	<p>Mask for err_ecc_corrected_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_ecc_corrected23	R/W	<p>Mask for err_ecc_corrected_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_ecc_corrected22	R/W	<p>Mask for err_ecc_corrected_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_ecc_corrected21	R/W	<p>Mask for err_ecc_corrected_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_ecc_corrected20	R/W	<p>Mask for err_ecc_corrected_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_ecc_corrected19	R/W	<p>Mask for err_ecc_corrected_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
18	err_ecc_corrected18	R/W	<p>Mask for err_ecc_corrected_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_ecc_corrected17	R/W	<p>Mask for err_ecc_corrected_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_ecc_corrected16	R/W	<p>Mask for err_ecc_corrected_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_ecc_corrected_vc15	R/W	<p>Mask for err_ecc_corrected_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
14	err_ecc_corrected_vc14	R/W	<p>Mask for err_ecc_corrected_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_ecc_corrected_vc13	R/W	<p>Mask for err_ecc_corrected_vc13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_ecc_corrected_vc12	R/W	<p>Mask for err_ecc_corrected_vc12.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
11	err_ecc_corrected_vc11	R/W	<p>Mask for err_ecc_corrected_vc11.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
10	err_ecc_corrected_vc10	R/W	<p>Mask for err_ecc_corrected_vc10.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
9	err_ecc_corrected_vc9	R/W	<p>Mask for err_ecc_corrected_vc9.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
8	err_ecc_corrected_vc8	R/W	<p>Mask for err_ecc_corrected_vc8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7	err_ecc_corrected_vc7	R/W	<p>Mask for err_ecc_corrected_vc7.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
6	err_ecc_corrected_vc6	R/W	<p>Mask for err_ecc_corrected_vc6.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	err_ecc_corrected_vc5	R/W	<p>Mask for err_ecc_corrected_vc5.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	err_ecc_corrected_vc4	R/W	<p>Mask for err_ecc_corrected_vc4.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
3	err_ecc_corrected_vc3	R/W	<p>Mask for err_ecc_corrected_vc3.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	err_ecc_corrected_vc2	R/W	<p>Mask for err_ecc_corrected_vc2.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	err_ecc_corrected_vc1	R/W	<p>Mask for err_ecc_corrected_vc1.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	err_ecc_corrected_vc0	R/W	<p>Mask for err_ecc_corrected_vc0.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_FORCE\_ECC\_CORRECTED**

**Name:** Force for interruption caused by Header single bit errors.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_EC\_C\_CORRECTED interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x2d8

Bits	Name	Memory Access	Description
31	err_ecc_corrected31	R/W	<p>Force err_ecc_corrected_vc31</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
30	err_ecc_corrected30	R/W	<p>Force err_ecc_corrected_vc30</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
29	err_ecc_corrected29	R/W	<p>Force err_ecc_corrected_vc29</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
28	err_ecc_corrected28	R/W	<p>Force err_ecc_corrected_vc28</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
27	err_ecc_corrected27	R/W	<p>Force err_ecc_corrected_vc27</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
26	err_ecc_corrected26	R/W	<p>Force err_ecc_corrected_vc26</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
25	err_ecc_corrected25	R/W	<p>Force err_ecc_corrected_vc25</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
24	err_ecc_corrected24	R/W	<p>Force err_ecc_corrected_vc24</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
23	err_ecc_corrected23	R/W	<p>Force err_ecc_corrected_vc23</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
22	err_ecc_corrected22	R/W	<p>Force err_ecc_corrected_vc22</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
21	err_ecc_corrected21	R/W	<p>Force err_ecc_corrected_vc21</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
20	err_ecc_corrected20	R/W	<p>Force err_ecc_corrected_vc20</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
19	err_ecc_corrected19	R/W	<p>Force err_ecc_corrected_vc19</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>

Bits	Name	Memory Access	Description
18	err_ecc_corrected18	R/W	<p>Force err_ecc_corrected_vc18</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
17	err_ecc_corrected17	R/W	<p>Force err_ecc_corrected_vc17</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
16	err_ecc_corrected16	R/W	<p>Force err_ecc_corrected_vc16</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
15	err_ecc_corrected_vc15	R/W	<p>Force err_ecc_corrected_vc15.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
14	err_ecc_corrected_vc14	R/W	<p>Force err_ecc_corrected_vc14.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
13	err_ecc_corrected_vc13	R/W	<p>Force err_ecc_corrected_vc13.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
12	err_ecc_corrected_vc12	R/W	<p>Force err_ecc_corrected_vc12.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
11	err_ecc_corrected_vc11	R/W	<p>Force err_ecc_corrected_vc11.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
10	err_ecc_corrected_vc10	R/W	<p>Force err_ecc_corrected_vc10.</p> <p><b>Value After Reset:</b> 0x0</p>

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
9	err_ecc_corrected_vc9	R/W	Force err_ecc_corrected_vc9. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
8	err_ecc_corrected_vc8	R/W	Force err_ecc_corrected_vc8. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7	err_ecc_corrected_vc7	R/W	Force err_ecc_corrected_vc7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
6	err_ecc_corrected_vc6	R/W	Force err_ecc_corrected_vc6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	err_ecc_corrected_vc5	R/W	Force err_ecc_corrected_vc5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	err_ecc_corrected_vc4	R/W	Force err_ecc_corrected_vc4. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	err_ecc_corrected_vc3	R/W	Force err_ecc_corrected_vc3. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
2	err_ecc_corrected_vc2	R/W	Force err_ecc_corrected_vc2. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	err_ecc_corrected_vc1	R/W	Force err_ecc_corrected_vc1. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	err_ecc_corrected_vc0	R/W	Force err_ecc_corrected_vc0. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

## SCRAMBLING

**Name:** Data De-Scrambling.

**Description:** This register configures the De-scrambler block.

**Size:** 32 bits

**Offset:** 0x300

Bits	Name	Memory Access	Description
31:1			<b>Reserved Field:</b> Yes
0	scramble_enable	R/W	Enables data de-scrambling on the controller side. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

## SCRAMBLING\_SEED1

**Name:** De-scrambler seed for lane1.

**Description:** This register configures the seed used by De-scrambler block for lane 1

**Size:** 32 bits

**Offset:** 0x304

Bits	Name	Memory Access	Description

31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane1	R/W	Seed used by De-scrambler block for lane 1 <b>Value After Reset:</b> 0x1008 <b>Exists:</b> Always

**SCRAMBLING\_SEED2****Name:** De-scrambler seed for lane2.**Description:** This register configures the seed used by De-scrambler block for lane 2**Size:** 32 bits**Offset:** 0x308

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane2	R/W	Seed used by De-scrambler block for lane 2 <b>Value After Reset:</b> 0x1188 <b>Exists:</b> Always

**SCRAMBLING\_SEED3****Name:** De-scrambler seed for lane3.**Description:** This register configures the seed used by De-scrambler block for lane 3**Size:** 32 bits**Offset:** 0x30c

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane3	R/W	Seed used by De-scrambler block for lane 3 <b>Value After Reset:</b> 0x1248 <b>Exists:</b> Always

**SCRAMBLING\_SEED4****Name:** De-scrambler seed for lane4.**Description:** This register configures the seed used by De-scrambler block for lane 4**Size:** 32 bits**Offset:** 0x310

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane4	R/W	Seed used by De-scrambler block for lane 4 <b>Value After Reset:</b> 0x13c8 <b>Exists:</b> Always

**SCRAMBLING\_SEED5****Name:** De-scrambler seed for lane5.**Description:** This register configures the seed used by De-scrambler block for lane 5**Size:** 32 bits**Offset:** 0x314

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane5	R/W	Seed used by De-scrambler block for lane 5 <b>Value After Reset:</b> 0x1428 <b>Exists:</b> Always

**SCRAMBLING\_SEED6****Name:** De-scrambler seed for lane6.**Description:** This register configures the seed used by De-scrambler block for lane 6**Size:** 32 bits**Offset:** 0x318

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane6	R/W	Seed used by De-scrambler block for lane 6 <b>Value After Reset:</b> 0x15a8 <b>Exists:</b> Always

**SCRAMBLING\_SEED7****Name:** De-scrambler seed for lane7.**Description:** This register configures the seed used by De-scrambler block for lane 7**Size:** 32 bits

**Offset:** 0x31c

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane7	R/W	Seed used by De-scrambler block for lane 7 <b>Value After Reset:</b> 0x1668 <b>Exists:</b> Always

#### SCRAMBLING\_SEED8

**Name:** De-scrambler seed for lane8.

**Description:** This register configures the seed used by De-scrambler block for lane 8

**Size:** 32 bits

**Offset:** 0x320

Bits	Name	Memory Access	Description
31:16			<b>Reserved Field:</b> Yes
15:0	scramble_seed_lane8	R/W	Seed used by De-scrambler block for lane 8 <b>Value After Reset:</b> 0x17e8 <b>Exists:</b> Always

#### INT\_ST\_IPI5\_FATAL

**Name:** Fatal interruption caused by IPI5 interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI5\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x4e0

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	Reporting internal FIFO overflow on pulse delay block. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
5	int_event_fifo_overflow	RC	<p>Reporting internal FIFO overflow during IPI data processing.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	pixel_if_hline_err	RC	<p>Horizontal line time error (only available in controller mode).</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	pixel_if_fifo_nempty_fs	RC	<p>Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame.</p> <p>There are some scenarios where synchronization events of new frame can be lost on IPI interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	pixel_if_frame_sync_err	RC	<p>Whenever in Controller mode, notifies if a new frame is received but previous has not been completed.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	pixel_if_fifo_overflow	RC	<p>The FIFO of pixel interface has lost information because some data arrived and FIFO is already full.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	pixel_if_fifo_underflow	RC	<p>The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_IPI5\_FATAL**

**Name:** Mask for fatal interruption caused by IPI5 interface.

**Description:** Interrupt mask for INT\_ST\_IPI5\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits**Offset:** 0x4e4

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	msk_int_pulse_delay_overflow	R/W	Mask int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	msk_int_event_fifo_overflow	R/W	Mask int_event_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	msk_pixel_if_hline_err	R/W	Mask pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	msk_pixel_if_fifo_nempty_fs	R/W	Mask pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	msk_frame_sync_err	R/W	Mask for pixel_if_frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	msk_pixel_if_fifo_overflow	R/W	Mask for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	msk_pixel_if_fifo_underflow	R/W	Mask for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_FORCE\_IPI5\_FATAL****Name:** Force for fatal interruption caused by IPI5 interface.

Description: Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI5 - FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x4e8

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	Force int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	force_int_event_fifo_overflow	R/W	Force int_event_fifo_overflow . <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	force_pixel_if_hline_err	R/W	Force pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	force_pixel_if_fifo_nempty_fs	R/W	Force pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	force_frame_sync_err	R/W	Force for frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	force_pixel_if_fifo_overflow	R/W	Force for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
0	force_pixel_if_fifo_underflow	R/W	<p>Force for pixel_if_fifo_underflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_ST\_IPI6\_FATAL**

**Name:** Fatal interruption caused by IPI6 interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI6\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x4f0

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	<p>Reporting internal FIFO overflow on pulse delay block.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	int_event_fifo_overflow	RC	<p>Reporting internal FIFO overflow during IPI data processing.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	pixel_if_hline_err	RC	<p>Horizontal line time error (only available in controller mode).</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
3	pixel_if_fifo_nempty_fs	RC	<p>Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame.</p> <p>There are some scenarios where synchronization events of new frame can be lost on IPI interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
2	pixel_if_frame_sync_err	RC	<p>Whenever in Controller mode, notifies if a new frame is received but previous has not been completed.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	pixel_if_fifo_overflow	RC	<p>The FIFO of pixel interface has lost information because some data arrived and FIFO is already full.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	pixel_if_fifo_underflow	RC	<p>The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_IPI6\_FATAL**

**Name:** Mask for fatal interruption caused by IPI6 interface.

**Description:** Interrupt mask for INT\_ST\_IPI6\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x4f4

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	msk_int_pulse_delay_overflow	R/W	<p>Mask int_pulse_delay_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	msk_int_event_fifo_overflow	R/W	<p>Mask int_event_fifo_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	msk_pixel_if_hline_err	R/W	<p>Mask pixel_if_hline_err.</p>

Bits	Name	Memory Access	Description
			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	msk_pixel_if_fifo_nempty_fs	R/W	Mask pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	msk_frame_sync_err	R/W	Mask for pixel_if_frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	msk_pixel_if_fifo_overflow	R/W	Mask for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	msk_pixel_if_fifo_underflow	R/W	Mask for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_FORCE\_IPI6\_FATAL**

**Name:** Force for fatal interruption caused by IPI6 interface.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI6\_- FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x4f8

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	Force int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

Bits	Name	Memory Access	Description
5	force_int_event_fifo_overflow	R/W	Force int_event_fifo_overflow . <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	force_pixel_if_hline_err	R/W	Force pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	force_pixel_if_fifo_nempty_fs	R/W	Force pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	force_frame_sync_err	R/W	Force for frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	force_pixel_if_fifo_overflow	R/W	Force for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	force_pixel_if_fifo_underflow	R/W	Force for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_ST\_IPI7\_FATAL**

**Name:** Fatal interruption caused by IPI7 interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI7\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x500

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	Reporting internal FIFO overflow on pulse delay block. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	int_event_fifo_overflow	RC	Reporting internal FIFO overflow during IPI data processing. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	pixel_if_hline_err	RC	Horizontal line time error (only available in controller mode). <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	pixel_if_fifo_nempty_fs	RC	Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame. There are some scenarios where synchronization events of new frame can be lost on IPI interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	pixel_if_frame_sync_err	RC	Whenever in Controller mode, notifies if a new frame is received but previous has not been completed. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	pixel_if_fifo_overflow	RC	The FIFO of pixel interface has lost information because some data arrived and FIFO is already full. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
0	pixel_if_fifo_underflow	RC	The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**INT\_MSK\_IPI7\_FATAL**

**Name:** Mask for fatal interruption caused by IPI7 interface.

**Description:** Interrupt mask for INT\_ST\_IPI7\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x504

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	msk_int_pulse_delay_overflow	R/W	Mask int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	msk_int_event_fifo_overflow	R/W	Mask int_event_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	msk_pixel_if_hline_err	R/W	Mask pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	msk_pixel_if_fifo_nempty_fs	R/W	Mask pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	msk_frame_sync_err	R/W	Mask for pixel_if_frame_sync_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1	msk_pixel_if_fifo_overflow	R/W	Mask for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

0	msk_pixel_if_fifo_underflow	R/W	Mask for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
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**INT\_FORCE\_IPI7\_FATAL**

**Name:** Force for fatal interruption caused by IPI7 interface.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI7\_- FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits

**Offset:** 0x508

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	Force int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	force_int_event_fifo_overflow	R/W	Force int_event_fifo_overflow . <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	force_pixel_if_hline_err	R/W	Force pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	force_pixel_if_fifo_nempty_fs	R/W	Force pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
2	force_frame_sync_err	R/W	Force for frame_sync_err. <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b>

Bits	Name	Memory Access	Description
			Always
1	force_pixel_if_fifo_overflow	R/W	<p>Force for pixel_if_fifo_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	force_pixel_if_fifo_underflow	R/W	<p>Force for pixel_if_fifo_underflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_ST\_IPI8\_FATAL**

**Name:** Fatal interruption caused by IPI8 interface.

**Description:** Groups and notifies which interruption bits caused the interruption. Stores the source of the error. Reading INT\_ST\_IPI8\_FATAL register does not clear the interrupt pin.

**Size:** 32 bits

**Offset:** 0x510

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	int_pulse_delay_overflow	RC	<p>Reporting internal FIFO overflow on pulse delay block.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	int_event_fifo_overflow	RC	<p>Reporting internal FIFO overflow during IPI data processing.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	pixel_if_hline_err	RC	<p>Horizontal line time error (only available in controller mode).</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
3	pixel_if_fifo_nempty_fs	RC	<p>Controller timing mode: The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked. Camera timing mode: The FIFO of pixel interface is not empty at the start of a new frame.</p> <p>There are some scenarios where synchronization events of new frame can be lost on IPI interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	pixel_if_frame_sync_err	RC	<p>Whenever in Controller mode, notifies if a new frame is received but previous has not been completed.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	pixel_if_fifo_overflow	RC	<p>The FIFO of pixel interface has lost information because some data arrived and FIFO is already full.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	pixel_if_fifo_underflow	RC	<p>The FIFO has become empty before the expected number of pixels (calculated from the packet header) could be extracted to the pixel interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_MSK\_IPI8\_FATAL**

**Name:** Mask for fatal interruption caused by IPI8 interface.

**Description:** Interrupt mask for INT\_ST\_IPI8\_FATAL controls which interrupt status bits trigger the interrupt pin. Bit at 1 - Enable the interrupt source. Bit at 0 - Interrupt source is masked.

**Size:** 32 bits

**Offset:** 0x514

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
6	msk_int_pulse_delay_overflow	R/W	<p>Mask int_pulse_delay_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
5	msk_int_event_fifo_overflow	R/W	<p>Mask int_event_fifo_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
4	msk_pixel_if_hline_err	R/W	<p>Mask pixel_if_hline_err.</p> <p><b>Value After Reset:</b></p> <p>0x0 <b>Exists:</b></p> <p>Always</p>
3	msk_pixel_if_fifo_nempty_fs	R/W	<p>Mask pixel_if_fifo_nempty_fs.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
2	msk_frame_sync_err	R/W	<p>Mask for pixel_if_frame_sync_err.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
1	msk_pixel_if_fifo_overflow	R/W	<p>Mask for pixel_if_fifo_overflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
0	msk_pixel_if_fifo_underflow	R/W	<p>Mask for pixel_if_fifo_underflow.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**INT\_FORCE\_IPI8\_FATAL**

**Name:** Force for fatal interruption caused by IPI8 interface.

**Description:** Interrupt force register is used for test purposes, and allows triggering INT\_ST\_IPI8\_- FATAL interrupt events individually. There is no need to activate the conditions that trigger the interrupt sources, because it may be extremely complex to generate stimuli for that purpose. This register is auto-clear.

**Size:** 32 bits**Offset:** 0x518

Bits	Name	Memory Access	Description
31:7			<b>Reserved Field:</b> Yes
6	force_int_pulse_delay_overflow	R/W	Force int_pulse_delay_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
5	force_int_event_fifo_overflow	R/W	Force int_event_fifo_overflow . <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
4	force_pixel_if_hline_err	R/W	Force pixel_if_hline_err. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
3	force_pixel_if_fifo_nempty_fs	R/W	Force pixel_if_fifo_nempty_fs. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

2	force_frame_sync_err	R/W	Force for frame_sync_err. <b>Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always
1	force_pixel_if_fifo_overflow	R/W	Force for pixel_if_fifo_overflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

0	force_pixel_if_fifo_underflow	R/W	Force for pixel_if_fifo_underflow. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
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**IPI5\_MODE****Name:** IPI5 Mode.**Description:** This register selects how the IPI interface 5 generates the video frame.**Size:** 32 bits**Offset:** 0x5c0

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_enable	R/W	This register enables the interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:17			<b>Reserved Field:</b> Yes
16	ipi_cut_through	R/W	This field indicates cut-through mode state: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	This field indicates if color mode components are delivered as follows: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:0			<b>Reserved Field:</b> Yes

**IPI5\_VCID****Name:** IPI5 Virtual Channel.**Description:** This register selects the virtual channel processed by IPI5.**Size:** 32 bits

**Offset:** 0x5c4

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcxt_2	R/W	Virtual channel extension extra bit of data to be processed by pixel interface 5 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
3:2	ipi_vcxt_0_1	R/W	Virtual channel extension of data to be processed by pixel interface 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1:0	ipi_vcxt	R/W	Virtual channel of data to be processed by pixel interface 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI5\_DATA\_TYPE****Name:** IPI5 Data type.**Description:** This register selects the data type processed by IPI5.**Size:** 32 bits**Offset:** 0x5c8

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	embedded_data	R/W	For Camera Timing Mode, this bit enables embedded data processing on pixel interface 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	Data type of data to be processed by pixel interface 5. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI5\_MEM\_FLUSH****Name:** IPI5 Flush Memory.**Description:** This register controls the flush of IPI5 memory.**Size:** 32 bits**Offset:** 0x5cc

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	ipi_auto_flush	R/W	Memory is automatically flushed at each Frame Start. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	Flush IPI5 memory. This bit is auto clear. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI5\_HSA\_TIME****Name:** IPI5 HSA.**Description:** This register configures the video Horizontal Synchronization Active (HSA) time for pixel Interface 5.**Size:** 32 bits**Offset:** 0x5d0

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	This field configures the Horizontal Synchronization Active period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI5\_HBP\_TIME****Name:** IPI5 HBP.**Description:** This register configures the video Horizontal Back Porch (HBP) time for pixel Interface 5.

**Size:** 32 bits**Offset:** 0x5d4

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hbp_time	R/W	This field configures the Horizontal Back Porch period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI5\_HSD\_TIME****Name:** IPI5 HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time for pixel Interface 5.**Size:** 32 bits**Offset:** 0x5d8

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	This field configures the Horizontal Sync Delay period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI5\_ADV\_FEATURES****Name:** IPI5 Advanced Features.**Description:** This register configures advanced features for IPI5 mode.**Size:** 32 bits**Offset:** 0x5dc

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
24	ipi_sync_event_mode	R/W	<p>For Camera Timing Mode:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
23:22			<b>Reserved Field:</b> Yes
21	en_embedded	R/W	<p>This register allows the use of embedded packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
20	en_blanking	R/W	<p>This register allows the use of blanking packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
19	en_null	R/W	<p>This register allows the use of null packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
18	en_line_start	R/W	<p>This register allows the use of line start packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
17	en_video	R/W	<p>This register allows the use of video packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
16	line_event_selection	R/W	<p>For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows: <b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	<p>Datatype to overwrite. <b>Value</b>  <b>After Reset:</b> 0x0  <b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	<p>Ignore datatype of the header using the programmed datatype for decoding.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>

### IPI6\_MODE

**Name:** IPI6 Mode.

**Description:** This register selects how the IPI interface 6 generates the video frame.

**Size:** 32 bits

**Offset:** 0x5e0

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_enable	R/W	<p>This register enables the interface.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always</p>
23:17			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
16	ipi_cut_through	R/W	<p>This field indicates cut-through mode state:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	<p>This field indicates if color mode components are delivered as follows:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:0			<b>Reserved Field:</b> Yes

**IPI6\_VCID****Name:** IPI6 Virtual Channel.**Description:** This register selects the virtual channel processed by IPI6.**Size:** 32 bits**Offset:** 0x5e4

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcx_2	R/W	<p>Virtual channel extension extra bit of data to be processed by pixel interface 6</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
3:2	ipi_vcx_0_1	R/W	<p>Virtual channel extension of data to be processed by pixel interface 6.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

1:0	ipi_vcids	R/W	Virtual channel of data to be processed by pixel interface 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
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**IPI6\_DATA\_TYPE****Name:** IPI6 Data Type.**Description:** This register selects the data type processed by IPI6.**Size:** 32 bits**Offset:** 0x5e8

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	embedded_data	R/W	For Camera Timing Mode, this bit enables embedded data processing on pixel interface 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	Data type of data to be processed by pixel interface 6. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI6\_MEM\_FLUSH****Name:** IPI6 Flush Memory.**Description:** This register controls the flush of IPI6 memory.**Size:** 32 bits**Offset:** 0x5ec

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	ipi_auto_flush	R/W	Memory is automatically flushed at each Frame Start. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	Flush IPI6 memory. This bit is auto clear. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI6\_HSA\_TIME****Name:** IPI6 HSA.**Description:** This register configures the video Horizontal Synchronism Active (HSA) time for pixel Interface 6.**Size:** 32 bits**Offset:** 0x5f0

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	This field configures the Horizontal Synchronism Active period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI6\_HBP\_TIME****Name:** IPI6 HBP.**Description:** This register configures the video Horizontal Back Porch (HBP) time for pixel Interface 6.**Size:** 32 bits**Offset:** 0x5f4

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hbp_time	R/W	This field configures the Horizontal Back Porch period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI6\_HSD\_TIME****Name:** IPI6 HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time for pixel

Interface 6.

**Size:** 32 bits

**Offset:** 0x5f8

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	This field configures the Horizontal Sync Delay period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

#### IPI6\_ADV\_FEATURES

**Name:** IPI6 Advanced Features.

**Description:** This register configures advanced features for IPI6 mode.

**Size:** 32 bits

**Offset:** 0x5fc

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_sync_event_mode	R/W	For Camera Timing Mode: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:22			<b>Reserved Field:</b> Yes
21	en_embedded	R/W	This register allows the use of embedded packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
20	en_blanking	R/W	This register allows the use of blanking packets for IPI synchronization events. <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
19	en_null	R/W	<p>This register allows the use of null packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
18	en_line_start	R/W	<p>This register allows the use of line start packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
17	en_video	R/W	<p>This register allows the use of video packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
16	line_event_selection	R/W	<p>For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows: <b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	<p>Datatype to overwrite. <b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	<p>Ignore datatype of the header using the programmed datatype for decoding.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI7\_MODE****Name:** IPI7 Mode.**Description:** This register selects how the IPI interface 7 generates the video frame.**Size:** 32 bits**Offset:** 0x600

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_enable	R/W	This register enables the interface. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:17			<b>Reserved Field:</b> Yes
16	ipi_cut_through	R/W	This field indicates cut-through mode state: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	This field indicates if color mode components are delivered as follows: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:0			<b>Reserved Field:</b> Yes

**IPI7\_VCID****Name:** IPI7 Virtual Channel.**Description:** This register selects the virtual channel processed by IPI7.**Size:** 32 bits**Offset:** 0x604

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcx_2	R/W	Virtual channel extension extra bit of data to be processed by pixel interface 7 <b>Value After Reset:</b> 0x0 <b>Exists:</b> (CSI2_HOST_PHY == 2)==1
3:2	ipi_vcx_0_1	R/W	Virtual channel extension of data to be processed by pixel interface 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
1:0	ipi_vcld	R/W	Virtual channel of data to be processed by pixel interface 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI7\_DATA\_TYPE****Name:** IPI7 Data Type.**Description:** This register selects the data type processed by IPI7.**Size:** 32 bits**Offset:** 0x608

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	embedded_data	R/W	For Camera Timing Mode, this bit enables embedded data processing on pixel interface 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	Data type of data to be processed by pixel interface 7. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI7\_MEM\_FLUSH****Name:** IPI7 Flush Memory.

**Description:** This register control the flush of IPI7 memory.

**Size:** 32 bits

**Offset:** 0x60c

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	ipi_auto_flush	R/W	Memory is automatically flushed at each Frame Start. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	Flush IPI7 memory. This bit is auto clear. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

#### IPI7\_HSA\_TIME

**Name:** IPI7 HSA.

**Description:** This register configures the video Horizontal Synchronism Active (HSA) time for pixel Interface 7.

**Size:** 32 bits

**Offset:** 0x610

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	This field configures the Horizontal Synchronism Active period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

#### IPI7\_HBP\_TIME

**Name:** IPI7 HBP.

**Description:** This register configures the video Horizontal Back Porch (HBP) time for pixel Interface 7.

**Size:** 32 bits

**Offset:** 0x614

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hbp_time	R/W	This field configures the Horizontal Back Porch period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI7\_HSD\_TIME****Name:** IPI7 HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time for pixel Interface 7.**Size:** 32 bits**Offset:** 0x618

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	This field configures the Horizontal Sync Delay period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI7\_ADV\_FEATURES****Name:** IPI7 Advanced Features.**Description:** This register configures advanced features for IPI7 mode.**Size:** 32 bits**Offset:** 0x61c

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
24	ipi_sync_event_mode	R/W	<p>For Camera Timing Mode:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
23:22			<b>Reserved Field:</b> Yes
21	en_embedded	R/W	<p>This register allows the use of embedded packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
20	en_blanking	R/W	<p>This register allows the use of blanking packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
19	en_null	R/W	<p>This register allows the use of null packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
18	en_line_start	R/W	<p>This register allows the use of line start packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
17	en_video	R/W	<p>This register allows the use of video packets for IPI synchronization events.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
16	line_event_selection	R/W	<p>For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	<p>Datatype to overwrite.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	<p>Ignore datatype of the header using the programmed datatype for decoding.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI8\_MODE****Name:** IPI8 Mode.**Description:** This register selects how the IPI interface 8 generates the video frame.**Size:** 32 bits**Offset:** 0x620

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_enable	R/W	<p>This register enables the interface.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
23:17			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
16	ipi_cut_through	R/W	<p>This field indicates cut-through mode state:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (CTINACTIVE): Cut-through mode inactive</li> <li>■ 0x1 (CTACTIVE): Cut-through mode active</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
15:9			<b>Reserved Field:</b> Yes
8	ipi_color_com	R/W	<p>This field indicates if color mode components are delivered as follows:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (COLOR48): 48 bits interface</li> <li>■ 0x1 (COLOR16): 16 bits interface</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:0			<b>Reserved Field:</b> Yes

**IPI8\_VCID****Name:** IPI8 Virtual Channel.**Description:** This register selects the virtual channel processed by IPI8.**Size:** 32 bits**Offset:** 0x624

Bits	Name	Memory Access	Description
31:5			<b>Reserved Field:</b> Yes
4	ipi_vcx_2	R/W	<p>Virtual channel extension extra bit of data to be processed by pixel interface 8</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> (CSI2_HOST_PHY == 2)==1</p>
3:2	ipi_vcx_0_1	R/W	<p>Virtual channel extension of data to be processed by pixel interface 8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

Bits	Name	Memory Access	Description
1:0	ipi_vcidx	R/W	<p>Virtual channel of data to be processed by pixel interface 8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI8\_DATA\_TYPE**

**Name:** IPI8 Data Type.

**Description:** This register selects the data type processed by IPI8.

**Size:** 32 bits

**Offset:** 0x628

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	embedded_data	R/W	<p>For Camera Timing Mode, this bit enables embedded data processing on pixel interface 8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>
7:6			<b>Reserved Field:</b> Yes
5:0	ipi_data_type	R/W	<p>Data type of data to be processed by pixel interface 8.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI8\_MEM\_FLUSH**

**Name:** IPI8 Flush Memory.

**Description:** This register control the flush of IPI8 memory.

**Size:** 32 bits

**Offset:** 0x62c

Bits	Name	Memory Access	Description
31:9			<b>Reserved Field:</b> Yes
8	ipi_auto_flush	R/W	Memory is automatically flushed at each Frame Start.

Bits	Name	Memory Access	Description
			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_flush	R/W	Flush IPI8 memory. This bit is auto clear. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI8\_HSA\_TIME****Name:** IPI8 HSA.**Description:** This register configures the video Horizontal Synchronism Active (HSA) time for pixel Interface 8.**Size:** 32 bits**Offset:** 0x630

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsa_time	R/W	This field configures the Horizontal Synchronism Active period in pixclk cycles. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always

**IPI8\_HBP\_TIME****Name:** IPI8 HBP.**Description:** This register configures the video Horizontal Back Porch (HBP) time for pixel Interface 8.**Size:** 32 bits**Offset:** 0x634

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes

Bits	Name	Memory Access	Description
11:0	ipi_hbp_time	R/W	<p>This field configures the Horizontal Back Porch period in pixclk cycles.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI8\_HSD\_TIME****Name:** IPI8 HSD.**Description:** This register configures the video Horizontal Sync Delay (HSD) time for pixel Interface 8.**Size:** 32 bits**Offset:** 0x638

Bits	Name	Memory Access	Description
31:12			<b>Reserved Field:</b> Yes
11:0	ipi_hsd_time	R/W	<p>This field configures the Horizontal Sync Delay period in pixclk cycles.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p>

**IPI8\_ADV\_FEATURES****Name:** IPI8 Advanced Features.**Description:** This register configures advanced features for IPI8 mode.**Size:** 32 bits**Offset:** 0x63c

Bits	Name	Memory Access	Description
31:25			<b>Reserved Field:</b> Yes
24	ipi_sync_event_mode	R/W	<p>For Camera Timing Mode:</p> <p><b>Values:</b></p> <ul style="list-style-type: none"> <li>■ 0x0 (SYNCEVFSN): Frame Start does not trigger any sync event</li> <li>■ 0x1 (SYNCEVFS): Legacy mode. Frame Start triggers a sync event</li> </ul>

Bits	Name	Memory Access	Description
			<b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
23:22			<b>Reserved Field:</b> Yes
21	en_embedded	R/W	This register allows the use of embedded packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
20	en_blanking	R/W	This register allows the use of blanking packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
19	en_null	R/W	This register allows the use of null packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
18	en_line_start	R/W	This register allows the use of line start packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
17	en_video	R/W	This register allows the use of video packets for IPI synchronization events. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always
16	line_event_selection	R/W	For Camera Timing Mode, this register allows manual selection of the Packet for line delimiter as follows: <b>Values:</b> <ul style="list-style-type: none"> <li>■ 0x0 (EVSELAUTO): Controller selects it automatically</li> <li>■ 0x1 (EVSELPROG): Select packets from list programmed in [17:21]</li> </ul> <b>Value After Reset:</b> 0x0

Bits	Name	Memory Access	Description
			<b>Exists:</b> Always
15:14			<b>Reserved Field:</b> Yes
13:8	ipi_dt	R/W	Datatype to overwrite. <b>Value</b> <b>After Reset:</b> 0x0  <b>Exists:</b> Always
7:1			<b>Reserved Field:</b> Yes
0	ipi_dt_overwrite	R/W	Ignore datatype of the header using the programmed datatype for decoding.  <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always

#### 8.4.3 Combo PHY CSR

##### PPI\_STARTUP\_RW\_COMMON\_DPHY\_0

- **Description:** PWR\_DWN state address configuration
- **Size:** 16 bits
- **Offset:** 0xc00

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0  <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

7:0	PWR_DWN_addr	R/W	<p>Configures behavior of PWR_DWN state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>
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**PPI\_STARTUP\_RW\_COMMON\_DPHY\_1**

- **Description:** BG\_ON state address configuration
- **Size:** 16 bits
- **Offset:** 0xc01

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x0</p>
7:0	BG_ON_addr	R/W	<p>Configures behavior of BG_ON state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x22  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_DPHY\_2**

- **Description:** RCAL state address configuration
- **Size:** 16 bits
- **Offset:** 0xc02

Bits	Name	Memory Access	Description
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15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	RCAL_addr	R/W	<p>Configures behavior of RCAL state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x4</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_DPHY\_3**

- **Description:** PLL\_START state address configuration
- **Size:** 16 bits
- **Offset:** 0xc03

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	PLL_START_addr	R/W	<p>Configures behavior of PLL_START state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x45</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_DPHY\_4**

- **Description:** HS\_DCO\_CAL state address configuration

- **Size:** 16 bits
- **Offset:** 0xc04

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	HS_DCO_CAL_addr	R/W	<p>Configures behavior of HS_DCO_CAL state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x5</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

#### PPI\_STARTUP\_RW\_COMMON\_DPHY\_5

- **Description:** OFFSET\_CAL state address configuration
- **Size:** 16 bits
- **Offset:** 0xc05

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

7:0	OFFSET_CAL_addr	R/W	<p>Configures behavior of OFFSET_CAL state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x6  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>
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**PPI\_STARTUP\_RW\_COMMON\_DPHY\_6**

- **Description:** LP\_DCO\_CAL state address configuration
- **Size:** 16 bits
- **Offset:** 0xc06

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x0</p>
7:0	LP_DCO_CAL_addr	R/W	<p>Configures behavior of LP_DCO_CAL state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x7  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_DPHY\_7**

- **Description:** DPHY\_DDL\_CAL state address configuration
- **Size:** 16 bits
- **Offset:** 0xc07

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	DPHY_DDL_CAL_addr	R/W	<p>Configures behavior of DPHY_DDL_CAL state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x30</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_DPHY\_8**

- **Description:** CPHY\_DDL\_CAL state address configuration
- **Size:** 16 bits
- **Offset:** 0xc08

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	CPHY_DDL_CAL_addr	R/W	<p>Configures behavior of CPHY_DDL_CAL state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x10</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_DPHY\_9**

- **Description:** DESKEW\_1P1 state address configuration
- **Size:** 16 bits
- **Offset:** 0xc09

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	DESKEW_1P1_addr	R/W	<p>Configures behavior of DESKEW_1P1 state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x50</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_DPHY\_A**

- **Description:** HIBERNATE state address configuration
- **Size:** 16 bits
- **Offset:** 0xc0a

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

7:0	HIBERNATE_addr	R/W	<p>Configures behavior of HIBERNATE state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x21  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>
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**PPI\_STARTUP\_RW\_COMMON\_DPHY\_10**

- **Description:** PHY\_READY state address configuration
- **Size:** 16 bits
- **Offset:** 0xc10

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x0</p>
7:0	PHY_READY_addr	R/W	<p>Configures behavior of PHY_READY state. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ [7] stuck: if 1'b1, FSM will stop in this state.</li> <li>■ [6] bypass: if 1'b1, FSM will bypass this state. Must be mutually exclusive with stuck.</li> <li>■ [5] leaving_hibernate: if 1'b1, FSM will run this state when leaving hibernate.</li> <li>■ [4:0] next_state: defines the next state. Please check the table for state codes.</li> </ul> <p><b>Value After Reset:</b> 0x2f  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>

**PPI\_STARTUP\_RW\_COMMON\_STARTUP\_1\_1**

- **Description:** PHY startup FSM configuration
- **Size:** 16 bits
- **Offset:** 0xc11

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11:0	PHY_READY_DLY	R/W	Delay of phy_ready signal from the hard macro to top. Measured in cfg_clk cycles. This field is quasi-static. <b>Value After Reset:</b> 0x96 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**PPI\_STARTUP\_RW\_COMMON\_STARTUP\_1\_2**

- **Description:** PHY startup FSM configuration
- **Size:** 16 bits
- **Offset:** 0xc12

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11:0	TXCLKESC_SWAP_DLY	R/W	Delay of txclkesc_swap signal from the hard macro to top. Measured in cfg_clk cycles. This field is quasi-static. <b>Value After Reset:</b> 0x78 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**PPI\_CALIBCTRL\_RW\_COMMON\_CALIBCTRL\_2\_0**

- **Description:** Power on lane calibration configuration
- **Size:** 16 bits
- **Offset:** 0xc20

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

11	TERMCAL_RECALIBRATION_EN	R/W	Enable to manually allow terminal recalibration. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OFFSETCAL_RECALIBRATION_EN	R/W	Enable to manually allow offset recalibration. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:5	LANE_CALIB_OFFSETCAL_EN	R/W	Calibration enable for all lanes (lane4 down to lane0) This field is quasi-static. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
4:0	LANE_CALIB_OFFSETCAL_LAST	R/W	Indicator of last lane to calibrate (lane4 down to lane0) This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f

**PPI\_CALIBCTRL\_R\_COMMON\_CALIBCTRL\_2\_1**

- **Description:** DDL calibration observability
- **Size:** 16 bits
- **Offset:** 0xc21

Bits	Name	Memory Access	Description
15:0	DDL_COUNTER_TARGET_OBS_LSBs	R	16 LSBs of the counter target calculated during DDL calibration <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**PPI\_CALIBCTRL\_R\_COMMON\_CALIBCTRL\_2\_2**

- **Description:** DDL calibration observability
- **Size:** 16 bits
- **Offset:** 0xc22

Bits	Name	Memory Access	Description
15:4	DDL_COUNTER_MULT_OBS_LSBs	R	12 LSBs of the multiplication calculated during DDL calibration <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

3:0	DDL_COUNTER_TARGET_OBS_MSBs	R	4 MSBs of the counter target calculated during DDL calibration <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
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**PPI\_CALIBCTRL\_R\_COMMON\_CALIBCTRL\_2\_3**

- **Description:** DDL calibration observability
- **Size:** 16 bits
- **Offset:** 0xc23

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	DDL_COUNTER_MULT_OBS_MS_Bs	R	8 MSBs of the multiplication calculated during DDL calibration <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**PPI\_CALIBCTRL\_R\_COMMON\_CALIBCTRL\_2\_4**

- **Description:** DDL calibration observability
- **Size:** 16 bits
- **Offset:** 0xc24

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10:0	DDL_COUNTER_SUM_OBS	R	Result of the sum calculated during DDL calibration <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7ff

**PPI\_CALIBCTRL\_R\_COMMON\_CALIBCTRL\_2\_5**

- **Description:** DDL calibration observability
- **Size:** 16 bits
- **Offset:** 0xc25

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:4	DDL_CAL_STATUS1	R	<p>Status of Lane 1's DDL calibration</p> <ul style="list-style-type: none"> <li>■ Bit 0 : Signals that the calibration has finished, regardless of the result</li> <li>■ Bit 1 : Indicates an error in the calibration (Full bias range was swept with no convergence)</li> <li>■ Bit 2 : Indicates an error in the calibration (osc_clk was detected to be stuck)</li> <li>■ Bit 3 : Final result is outside of the set acceptable range.</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
3:0	DDL_CAL_STATUS0	R	<p>Status of Lane 0's DDL calibration</p> <ul style="list-style-type: none"> <li>■ Bit 0 : Signals that the calibration has finished, regardless of the result</li> <li>■ Bit 1 : Indicates an error in the calibration (Full bias range was swept with no convergence)</li> <li>■ Bit 2 : Indicates an error in the calibration (osc_clk was detected to be stuck)</li> <li>■ Bit 3 : Final result is outside of the set acceptable range.</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

**PPI\_CALIBCTRL\_RW\_COMMON\_BG\_0**

- **Description:** Bandgap configuration
- **Size:** 16 bits
- **Offset:** 0xc26

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

8:0	BG_MAX_COUNTER	R/W	Configures waiting time since the beginning of bandgap state until the jump to the next state. Measured in config clock cycles. This field is quasi-static. <b>Value After Reset:</b> 0x8f <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff
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**PPI\_CALIBCTRL\_RW\_COMMON\_CALIBCTRL\_2\_7**

- **Description:** Power on lane calibration configuration
- **Size:** 16 bits
- **Offset:** 0xc27

Bits	Name	Memory Access	Description
15:5	RESERVED_15_5	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
4:0	STATE_DONE_TIMER_THRES	R/W	Sets the time to move to the next FSM state to allow all blocks to synchronize thier flags appropriately. Measured in config clock cycles. This field is quasi-static. <b>Value After Reset:</b> 0x8 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f

**PPI\_CALIBCTRL\_RW\_ADC\_CFG\_0**

- **Description:** ADC configuration register 0
- **Size:** 16 bits
- **Offset:** 0xc28

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	ADC_ENB	R/W	ADC enable (active high, edge triggered) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**PPI\_CALIBCTRL\_RW\_ADC\_CFG\_1**

- **Description:** ADC configuration register 1
- **Size:** 16 bits

- **Offset:** 0xc29

Bits	Name	Memory Access	Description
15:8	ADC_WAIT_THRESH_T2	R/W	ADC wait threshold timer 2 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	ADC_WAIT_THRESH_T1	R/W	ADC wait threshold timer 1 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

#### PPI\_CALIBCTRL\_R\_ADC\_DEBUG

- **Description:** ADC outputs observability
- **Size:** 16 bits
- **Offset:** 0xc2a

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10	ADC_DONE	R	ADC done flag. This flag is asserted at the end of ADC SAR operation and de-asserted with the rising edge of the adc enable. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:0	CB_ATB_SEL_DAC	R	ADC output word calculated using SAR algorithm <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

#### PPI\_RW\_LPDCOCAL\_TOP\_OVERRIDE

- **Description:** LP-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe00

Bits	Name	Memory Access	Description
15	LPCDCOCAL_I_MAN_TRIGGER	R/W	<p>Enable for triggering new LPDCO calibration. Active on rising edge.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	LPCDCOCAL_I_MAN_CAL_EN	R/W	<p>o_fword and o_fword_latch override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13:7	LPCDCOCAL_I_MAN_FWORD	R/W	<p>o_fword override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f</p>
6	LPCDCOCAL_I_MAN_FWORD_LATCH	R/W	<p>o_fword_latch override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	LPCDCOCAL_I_MAN_LPDCO_PON_EN	R/W	<p>o_lpdcopon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	LPCDCOCAL_I_MAN_LPDCO_PON	R/W	<p>o_lpdcopon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	LPCDCOCAL_I_MAN_LPDCOEN_EN	R/W	<p>o_lpdcoen override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	LPCDCOCAL_I_MAN_LPDCOEN	R/W	<p>o_lpdcoen override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	LPCDCOCAL_I_MAN_LPDCO_CLKEN_EN	R/W	<p>o_lpdcclk_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	LPCDCOCAL_I_MAN_LPDCO_CLKEN	R/W	<p><b>o_lpdcoc_clk_en</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_LPDCOCAL\_TIMEBASE**

- **Description:** LP-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe01

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
9:0	LPCDCOCAL_TIMEBASE	R/W	<p>Timebase configuration required to measure LPDCO clock. Defined in cfg_clk cycles.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3ff</p>

**PPI\_RW\_LPDCOCAL\_NREF**

- **Description:** LP-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe02

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
10:0	LPCDCOCAL_NREF	R/W	<p>Sets LPDCO calibration target: number of expected LPDCO clock ticks observed within measurement window.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7ff</p>

**PPI\_RW\_LPDCOCAL\_NREF\_RANGE**

- **Description:** LP-DCO calibration control
- **Size:** 16 bits

- **Offset:** 0xe03

Bits	Name	Memory Access	Description
15:5	RESERVED_15_5	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
4:0	LPCDCOCAL_NREF_RANGE	R/W	<p>Range around LPCDCOCAL_NREF where calibration is considered successful.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1f</p>

#### PPI\_RW\_LPDCOCAL\_NREF\_TRIGGER\_MAN

- **Description:** LP-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe04

Bits	Name	Memory Access	Description
15:2	RESERVED_15_2	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
1	LPDCOCAL_CMU_REF_TRIGGER_OVR_EN	R/W	<p>LP-DCO clock measurement unit trigger override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	LPDCOCAL_CMU_REF_TRIGGER_OVR_VAL	R/W	<p>LP-DCO clock measurement unit trigger override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

#### PPI\_RW\_LPDCOCAL\_TWAIT\_CONFIG

- **Description:** LP-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe05

Bits	Name	Memory Access	Description

15:9	LPCDCOCAL_TWAIT_PON	R/W	<p>Counter (in cfg_clk cycles) which controls the settling time between enabling the analog circuitry and starting the calibration. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
8:0	LPCDCOCAL_TWAIT_COARSE	R/W	<p>Counter (in cfg_clk cycles) which controls the settling time after changing the coarse setting before performing the next measurement. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0xc8</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1ff</p>

**PPI\_RW\_LPDCOCAL\_VT\_CONFIG**

- **Description:** LP-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe06

Bits	Name	Memory Access	Description
15:7	LPCDCOCAL_TWAIT_FINE	R/W	<p>Counter (in cfg_clk cycles) which controls the settling time after changing the fine setting before performing the next measurement. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0xc8</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1ff</p>
6:2	LPCDCOCAL_VT_NREF_RANGE	R/W	<p>Defines the tolerance which VT tracking mode still considers to be good. Setting will only be updated if measured LP-DCO frequency deviates from interval [NREF - LPCDCOCAL_VT_NREF_RANGE; NREF + LPCDCOCAL_VT_NREF_RANGE]. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1f</p>

1	LPCDCOCAL_USE_IDEAL_NREF	R/W	<p>Selects which reference target to use in VT tracking mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: VT tracking mode uses LPCDCOCAL_NREF as reference target.</li> <li>■ 1'b1: VT tracking mode uses the result from the power on calibration as reference target.</li> </ul> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
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0	LPCDCOCAL_VT_TRACKING_EN	R/W	<p>Enables VT tracking mode where calibration machine will keep monitoring LP-DCO's frequency and adjusting to variations.</p> <p>Active high. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
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**PPI\_R\_LPDCOCAL\_DEBUG\_RB**

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe07

Bits	Name	Memory Access	Description
15	LPDCOCAL_ERROR_VT_RB	R	<p>VT drift calibration error. Occurs when correction reached max/min nfine control word.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	LPDCOCAL_N_MEAS_DONE	R	<p>LPDCO machine CMU indication that measurement is ready</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	LPDCOCAL_CAL_DONE	R	<p>Power-on calibration has successfully finished. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12:11	LPDCOCAL_ERROR_RB	R	<p>Power-on calibration error.</p> <ul style="list-style-type: none"> <li>■ Bit 1 asserts - None of the coarse curves can be selected (hard error).</li> <li>■ Bit 0 asserts - None of the coarse curves can be selected within target range (soft error).</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
10:0	LPDCOCAL_N_MEAS	R	<p>dco_clk counter result of last measurement.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7ff</p>

**PPI\_RW\_LPDCOCAL\_COARSE\_CFG**

- **Description:** LP-DCO calibration control
- **Size:** 16 bits

- **Offset:** 0xe08

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
8:4	SCALE_REF	R/W	Sets the reference point to be used to find the best match from the coarse curves This field is quasi-static. <b>Value After Reset:</b> 0x10 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
3:2	NCOARSE_DIAG	R/W	Selects which coarse curve data is to be observed after LPDCO calibration is completed. Used for debug. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
1:0	NCOARSE_START	R/W	Selects the first coarse curve to be used in the sweep. This field is quasi-static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

#### PPI\_R\_LPDCOCAL\_DEBUG\_COARSE\_RB

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe09

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:6	LPDCOCAL_PON_STATE	R	State of LPDCO pon machine <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
5:2	LPDCOCAL_CAL_COARSE_HIT	R	Indicates in which coarse curves caliobration hit the target <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

Bits	Name	Memory Access	Description
1:0	LPDCOCAL_CAL_BOUND_STATUS	R	Indication of the quality of the calibration result relatively to the target <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

**PPI\_R\_LPDCOCAL\_DEBUG\_COARSE\_MEAS\_0\_RB**

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe0a

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10:0	LPDCOCAL_STORED_MEAS_0	R	Indicates the last measurement of the selected coarse curve <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7ff

**PPI\_R\_LPDCOCAL\_DEBUG\_COARSE\_MEAS\_1\_RB**

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe0b

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10:0	LPDCOCAL_STORED_MEAS_1	R	Indicates the N-1 measurement of the selected coarse curve <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7ff

**PPI\_R\_LPDCOCAL\_DEBUG\_COARSE\_FWORD\_RB**

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits

- **Offset:** 0xe0c

Bits	Name	Memory Access	Description
15:8	LPDCOCAL_STORED_FWORD_1	R	Flag indication of the last point (N-1) of calibration for the selected coarse curve <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	LPDCOCAL_STORED_FWORD_0	R	Flag indication of the last point (N) of calibration for the selected coarse curve <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

#### PPI\_R\_LPDCOCAL\_DEBUG\_MEASURE\_CURR\_ERROR

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe0d

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11:0	LPDCOCAL_MEAS_CURR_ERROR	R	Error value observed along the consecutive measurements <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

#### PPI\_R\_LPDCOCAL\_DEBUG\_MEASURE\_LAST\_ERROR

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe0e

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

14:12	LPDCOCAL_VT_STATE	R	State of VT drift machine <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
11:0	LPDCOCAL_LAST_MEAS_ERROR	R	Saved error value observed along the consecutive measurements <b>Value After Reset:</b> 0x800 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**PPI\_R\_LPDCOCAL\_DEBUG\_VT**

- **Description:** LP-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe0f

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:3	LPDCOCAL_MEAS_ADJ_P0_VT	R	Measured DCO values during VT drift adjustment <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7ff
2	LPDCOCAL_N ABOVE RANGE VT	R	VTdrift machine indicating that we are above defined range <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	LPDCOCAL_N BELOW RANGE VT	R	VTdrift machine indicating that we are below defined range <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LPDCOCAL_N WITHIN RANGE VT	R	VTdrift machine indicating that we are within defined range <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**PPI\_RW\_LB\_TIMEBASE\_CONFIG**

- **Description:** High speed loopback timebase configuration
- **Size:** 16 bits
- **Offset:** 0xe10

Bits	Name	Memory Access	Description
15:0	LOOPBACK_TIMEBASE	R/W	<p>Timebase configuration required to measure HS loopback clock. Defined in cfg_clk cycles.</p> <p><b>Value After Reset:</b> 0x180</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_RW\_LB\_STARTCMU\_CONFIG**

- **Description:** High speed loopack measurement trigger
- **Size:** 16 bits
- **Offset:** 0xe11

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
0	LB_START_CMU	R/W	<p>Trigger to start high speed loopback clock measurement. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_R\_LBPULSE\_COUNTER\_RB**

- **Description:** High speed loopback measurement results
- **Size:** 16 bits
- **Offset:** 0xe12

Bits	Name	Memory Access	Description
15:0	LB_PULSE_COUNTER	R	<p>Measured ticks of high speed loopback clock observed within timebase window.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_R\_LB\_START\_CMU\_RB**

- **Description:** High speed loopback measurement flag
- **Size:** 16 bits
- **Offset:** 0xe13

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	LB_STOP_CMU	R	High speed loopback flag indicating that measurement is completed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**PPI\_RW\_LB\_DPHY\_BURST\_START**

- **Description:** DPHY loopback burst control
- **Size:** 16 bits
- **Offset:** 0xe14

Bits	Name	Memory Access	Description
15:5	RESERVED_15_5	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
4	LBERT_DPHY_TXALTERNATECALHS_DATA	R/W	Initiates the HS-TX alternate calibration training sequence. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	LBERT_DPHY_TXSKEWCALHS_DATA	R/W	Initiates the HS-TX deskew training sequence. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	LBERT_DPHY_TXDATATRANSFERENHS_DATA	R/W	Initiates the HS-TX payload packing. Triggered on all lanes at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
1	LBERT_DPHY_TXREQUESTHS_DATA	R/W	<p>Initiates the HS-TX entry on the data lane. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	LBERT_DPHY_TXREQUESTHS_CLK	R/W	<p>Initiates the HS-TX entry on the clock lane. Used for loopback purposes. Must be set to zero in mission mode. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_LB\_CPHY\_BURST\_START**

- **Description:** CPHY loopback burst control
- **Size:** 16 bits
- **Offset:** 0xe15

Bits	Name	Memory Access	Description
15:2	RESERVED_15_2	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
1	LBERT_CPHY_TXDATATRANSFERENHS_DATA	R/W	<p>Initiates the HS-TX payload packing. Triggered on all lanes at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	LBERT_CPHY_TXREQUESTHS_DATA	R/W	<p>Initiates the HS-TX entry on the data lane. All lanes enter HS at the same time. Used for loopback purposes. Must be set to zero in mission mode. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_DDLCAL\_CFG\_0**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe20

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:0	DDLCAL_TIMEBASE_TARGET	R/W	Timebase for oscillation clock measurement (cfg_clk cycles). Quasi static. <b>Value After Reset:</b> 0x14 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

**PPI\_RW\_DDLCAL\_CFG\_1**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe21

Bits	Name	Memory Access	Description
15:8	DDLCAL_DISABLE_TIME	R/W	Time the DDL is disabled after applying a phase setting (cfg_clk cycles). Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	DDLCAL_MAX_PHASE	R/W	Maximum phase setting for DDL calibration. Quasi static. <b>Value After Reset:</b> 0x40 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**PPI\_RW\_DDLCAL\_CFG\_2**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe22

Bits	Name	Memory Access	Description
15:12	DDLCAL_WAIT	R/W	Wait time between DDL calibrations (in cfg_clk cycles) Quasi static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

Bits	Name	Memory Access	Description
11:10	DDLCAL_TUNE_MODE	R/W	Select phase setting to use during DDL calibration. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9	DDLCAL_UPDATE_SETTINGS	R/W	Flag to update the machine's settings. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	DDLCAL_DDL_DLL	R/W	Select DDL or DLL calibration. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:0	DDLCAL_ENABLE_WAIT	R/W	Time to wait before counting the oscillation clock's ticks after applying a phase setting (cfg_clk cycles). Quasi static. <b>Value After Reset:</b> 0x14 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**PPI\_RW\_DDLCAL\_CFG\_3**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe23

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:0	DDLCAL_COUNTER_REF	R/W	Target number of ticks for the oscillation clock (cfg_clk cycles). Quasi static. <b>Value After Reset:</b> 0x47 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

**PPI\_RW\_DDLCAL\_CFG\_4**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe24

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:0	DDLCAL_STUCK_THRESH	R/W	Minimum number of oscillation clock ticks not to flag stuck condition (cfg_clk cycles). Quasi static. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

**PPI\_RW\_DDLCAL\_CFG\_5**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe25

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:4	DDLCAL_DLL_FBK	R/W	Coarse delay output used as output of DLL. Quasi static. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
3:0	DDLCAL_DDL_COARSE_BANK	R/W	Number of used coarse delay cells. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**PPI\_RW\_DDLCAL\_CFG\_6**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe26

Bits	Name	Memory Access	Description

15:10	DDLCAL_CLEAR_COUNT_THRESH	R/W	Counter threshold for the reset of the oscillation counter of the DDL calibration. (cfg_clk cycles). Quasi static.  <b>Value After Reset:</b> 0x20 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
9:0	DDLCAL_MAX_DIFF	R/W	Maximum difference towards target not to flag an error. Quasi static.  <b>Value After Reset:</b> 0x64 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

**PPI\_RW\_DDLCAL\_CFG\_7**

- **Description:** DDL calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe27

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0X0  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:7	DDLCAL_DECR_WAIT	R/W	Counter threshold for ddl_en deassertion (cfg_clk cycles). Quasi static.  <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
6:0	DDLCAL_START_DELAY	R/W	Counter threshold for initial delay before DDL calibration start. (cfg_clk cycles). Quasi static  <b>Value After Reset:</b> 0x32 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f

**PPI\_R\_DDLCAL\_DEBUG\_0**

- **Description:** DDL calibration observability
- **Size:** 16 bits
- **Offset:** 0xe28

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0X0  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

9:0	DDLCAL_COUNTER0	R	<p>Value of the tick count for phase = 0. For observability purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3ff</p>
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**PPI\_R\_DDLCAL\_DEBUG\_1**

- **Description:** DDL calibration observability
- **Size:** 16 bits
- **Offset:** 0xe29

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
9:0	DDLCAL_COUNTERX	R	<p>Value of the tick count for phase = X. For observability purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3ff</p>

**PPI\_RW\_PARITY\_TEST**

- **Description:** Parity test set and clear control
- **Size:** 16 bits
- **Offset:** 0xe30

Bits	Name	Memory Access	Description
15:2	RESERVED_15_2	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
1	CR_PARITY_TESTSET	R/W	<p>Parity error set. Active high. Set to force parity error to assert.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	CR_PARITY_TESTCLEAR	R/W	<p>Parity error clear. Active high. In the presence of a parity error, output asserts and remains asserted until CR_PARITY_TESTCLEAR is asserted.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_STARTUP\_OVR\_0**

- **Description:** Override control for state in startup FSM
- **Size:** 16 bits
- **Offset:** 0xe31

Bits	Name	Memory Access	Description
15:5	RESERVED_15_5	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
4:0	STARTUP_STATE_OVR_VAL	R/W	<p>Startup FMS state override value</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1f</p>

**PPI\_RW\_STARTUP\_STATE\_OVR\_1**

- **Description:** Override control for state in startup FSM
- **Size:** 16 bits
- **Offset:** 0xe32

Bits	Name	Memory Access	Description
15:3	RESERVED_15_3	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
2:1	TXCLKESC_DRV_CFG	R/W	<p>Escape clock driver configuration</p> <ul style="list-style-type: none"> <li>■ 2'b00: Swap from cfg_clk_div to txclkesc during startup</li> <li>■ 2'b01: Permanently driven with cfg_clk_div</li> <li>■ 2'b10: Permanently driven with txclkesc</li> <li>■ 2'b11: Reserved Value</li> </ul> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
0	STARTUP_STATE_OVR_EN	R/W	<p>Startup FMS state override enable</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_DTB\_SELECTOR**

- **Description:** Selector control for DTB
- **Size:** 16 bits
- **Offset:** 0xe33

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
8	DTB_SOURCE_SELECT	R/W	DTB source selector : soft or hard macro <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:0	DTB_SELECT_ADDR	R/W	DTB selector address for soft macro signals <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**PPI\_RW\_DPHY\_CLK\_SPARE**

- **Description:** DPHY spare registers
- **Size:** 16 bits
- **Offset:** 0xe35

Bits	Name	Memory Access	Description
15:0	DPHY_CLK_LANE_SPARE	R/W	Spare registers for future use <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**PPI\_RW\_COMMON\_CFG**

- **Description:** Common system configurations
- **Size:** 16 bits
- **Offset:** 0xe36

Bits	Name	Memory Access	Description

15:2	RESERVED_15_2	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
1:0	CFG_CLK_DIV_FACTOR	R/W	Selects cfg_clk division factor for txclkesc assignment. Quasi-static. <ul style="list-style-type: none"> <li>■ 2'b00 : No division</li> <li>■ 2'b01 : Factor of 2</li> <li>■ 2'b10 : Factor of 4</li> <li>■ 2'b11 : Factor of 8</li> </ul> <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

**PPI\_RW\_TERMCAL\_CFG\_0**

- **Description:** Termination calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe40

Bits	Name	Memory Access	Description
15:7	RESERVED_15_7	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
6:0	TERMCAL_TIMER	R/W	Period of atb_clk measured in cfg_clk cycles. <b>Value After Reset:</b> 0x13 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f

**PPI\_R\_TERMCAL\_DEBUG\_0**

- **Description:** Termination calibration observability
- **Size:** 16 bits
- **Offset:** 0xe41

Bits	Name	Memory Access	Description
15:3	RESERVED_15_3	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

2	TERMCAL_CALDONE	R	Termination calibration done flag. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	TERMCAL_CAL_ERROR	R	Termination calibration multi-toggle detection. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	TERMCAL_COMP_UNCHANGED	R	Termination calibration error. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**PPI\_RW\_TERMCAL\_CTRL\_0**

- **Description:** Termination calibration controllability
- **Size:** 16 bits
- **Offset:** 0xe42

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
3	TERMCAL_CALDONE_OVR_EN	R/W	termcal_caldone override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	TERMCAL_CALDONE_OVR_VAL	R/W	termcal_caldone override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	TERMCAL_CALDONE_PULSE_O_VR_EN	R/W	termcal_caldone_pulse override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	TERMCAL_CALDONE_PULSE_O_VR_VAL	R/W	termcal_caldone_pulse override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**PPI\_RW\_OFFSETCAL\_CFG\_0**

- **Description:** Offset calibration configurations
- **Size:** 16 bits
- **Offset:** 0xe50

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
5	OFFSETCAL_CALIB_MODE	R/W	<p>Defines the offset calibration mode.</p> <ul style="list-style-type: none"> <li>■ 1'b0 : Outputs default setting when no transition is detected on pre-amplifier.</li> <li>■ 1'b1 : Outputs max or min setting depending on the initial state of the pre-amplifier if no transition is detected.</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4:0	OFFSETCAL_WAIT_THRESH	R/W	<p>Wait threshold of 200ns from the time that the offsetcal setting is changed to the time that the DAC output is sampled. Configured in cfg_clk cycles.</p> <p><b>Value After Reset:</b> 0x4</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1f</p>

**PPI\_R\_OFFSETCAL\_DEBUG\_LANE0**

- **Description:** Offset calibration observability
- **Size:** 16 bits
- **Offset:** 0xe51

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

Bits	Name	Memory Access	Description
7:4	OFFSETCAL_ERRCAL_LEFT	R	<p>Offset calibration error output from dclk lane left. Active high.</p> <ul style="list-style-type: none"> <li>■ 4'b1xxx : Calibration error - An error has been detected</li> <li>■ 4'b1001 : Calibration error - Lines did not toggle</li> <li>■ 4'b1010 : Calibration error - One off the lines didn't toggle</li> <li>■ 4'b1011 : Calibration error - Lines toggle during rampup/down but not during rampdown/up</li> <li>■ 4'b0000 : Calibration ok - Lines have toggled for different calibration words</li> <li>■ 4'b0001 : Calibration ok - Lines have toggled for the same calibration word</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xf</p>
3:0	OFFSETCAL_ERRCAL_RIGHT	R	<p>Offset calibration error output from dclk lane right. Active high.</p> <ul style="list-style-type: none"> <li>■ 4'b1xxx : Calibration error - An error has been detected</li> <li>■ 4'b1001 : Calibration error - Lines did not toggle</li> <li>■ 4'b1010 : Calibration error - One off the lines didn't toggle</li> <li>■ 4'b1011 : Calibration error - Lines toggle during rampup/down but not during rampdown/up</li> <li>■ 4'b0000 : Calibration ok - Lines have toggled for different calibration words</li> <li>■ 4'b0001 : Calibration ok - Lines have toggled for the same calibration word</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xf</p>

**PPI\_R\_OFFSETCAL\_DEBUG\_LANE1**

- **Description:** Offset calibration observability
- **Size:** 16 bits
- **Offset:** 0xe52

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:4	OFFSETCAL_ERRCAL_LEFT	R	<p>Offset calibration error output from dclk lane left. Active high.</p> <ul style="list-style-type: none"> <li>■ 4'b1xxx : Calibration error - An error has been detected</li> <li>■ 4'b1001 : Calibration error - Lines did not toggle</li> <li>■ 4'b1010 : Calibration error - One off the lines didn't toggle</li> <li>■ 4'b1011 : Calibration error - Lines toggle during rampup/down but not during rampdown/up</li> <li>■ 4'b0000 : Calibration ok - Lines have toggled for different calibration words</li> <li>■ 4'b0001 : Calibration ok - Lines have toggled for the same calibration word</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
3:0	OFFSETCAL_ERRCAL_RIGHT	R	<p>Offset calibration error output from dclk lane right. Active high.</p> <ul style="list-style-type: none"> <li>■ 4'b1xxx : Calibration error - An error has been detected</li> <li>■ 4'b1001 : Calibration error - Lines did not toggle</li> <li>■ 4'b1010 : Calibration error - One off the lines didn't toggle</li> <li>■ 4'b1011 : Calibration error - Lines toggle during rampup/down but not during rampdown/up</li> <li>■ 4'b0000 : Calibration ok - Lines have toggled for different calibration words</li> <li>■ 4'b0001 : Calibration ok - Lines have toggled for the same calibration word</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

**PPI\_R\_OFFSETCAL\_DEBUG\_LANE2**

- **Description:** Offset calibration observability
- **Size:** 16 bits
- **Offset:** 0xe53

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:4	OFFSETCAL_ERRCAL_LEFT	R	<p>Offset calibration error output from dclk lane left. Active high.</p> <ul style="list-style-type: none"> <li>■ 4'b1xxx : Calibration error - An error has been detected</li> <li>■ 4'b1001 : Calibration error - Lines did not toggle</li> <li>■ 4'b1010 : Calibration error - One off the lines didn't toggle</li> <li>■ 4'b1011 : Calibration error - Lines toggle during rampup/down but not during rampdown/up</li> <li>■ 4'b0000 : Calibration ok - Lines have toggled for different calibration words</li> <li>■ 4'b0001 : Calibration ok - Lines have toggled for the same calibration word</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
3:0	OFFSETCAL_ERRCAL_RIGHT	R	<p>Offset calibration error output from dclk lane right. Active high.</p> <ul style="list-style-type: none"> <li>■ 4'b1xxx : Calibration error - An error has been detected</li> <li>■ 4'b1001 : Calibration error - Lines did not toggle</li> <li>■ 4'b1010 : Calibration error - One off the lines didn't toggle</li> <li>■ 4'b1011 : Calibration error - Lines toggle during rampup/down but not during rampdown/up</li> <li>■ 4'b0000 : Calibration ok - Lines have toggled for different calibration words</li> <li>■ 4'b0001 : Calibration ok - Lines have toggled for the same calibration word</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

**PPI\_RW\_HSDCOCAL\_CFG\_0**

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe80

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12	HSDCOCAL_ENABLE_OVR_VAL	R/W	calibctrl o_hsdcoCAL_cal_en override value. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	HSDCOCAL_BYPASS_FWORD	R/W	Flag to bypass f_word calibration. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	HSDCOCAL_UPDATE_SETTINGS	R/W	Flag to update the machine's settings. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:0	HSDCOCAL_SELDAC_INIT_POINT	R/W	Configure sel_dac initial point value. This field is quasi-static. <b>Value After Reset:</b> 0x100 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

**PPI\_RW\_HSDCOCAL\_CFG\_1**

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe81

Bits	Name	Memory Access	Description
15:8	HSDCOCAL_WAIT_PON	R/W	Counter (in cfg_clk cycles) which controls the settling time between powering on the analog circuitry (pon) and starting the calibration (enable). This field is quasi-static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HSDCOCAL_WAIT_SELDAC	R/W	Counter (in cfg_clk cycles) which controls the settling time between changing sel_dac configuration and trigger new DCO clock measure. This field is quasi-static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**PPI\_RW\_HSDCOCAL\_CFG\_2**

- **Description:** HS-DCO calibration control

- **Size:** 16 bits
- **Offset:** 0xe82

Bits	Name	Memory Access	Description
15:8	HSDCOCAL_TUNE_CLKDIG_ENABLE_DLY	R/W	<p>Counter (in cfg_clk cycles) which controls the settling time between AFE enable and tune_clkdig_en. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0xc7</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:0	HSDCOCAL_ENABLE_DLY	R/W	<p>Counter (in cfg_clk cycles) which controls the settling time between tune_clkdig_en deassertion and AFE enable deassertion. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

#### PPI\_RW\_HSDCOCAL\_CFG\_3

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe83

Bits	Name	Memory Access	Description
15:8	HSDCOCAL_FWORD_ENABLE_TIME	R/W	<p>Counter (in cfg_clk cycles) which controls the settling time between changing f_word configuration and enable assertion. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:0	HSDCOCAL_FWORD_DISABLE_TIME	R/W	<p>Counter (in cfg_clk cycles) which controls the settling time between enable deassertion and changing f_word configuration. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

#### PPI\_RW\_HSDCOCAL\_CFG\_4

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe84

Bits	Name	Memory Access	Description
15:0	HSDCOCAL_N_REF	R/W	<p>Sets HSDCO calibration target: number of expected HSDCO clock ticks observed within measurement window. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_RW\_HSDCOCAL\_CFG\_5**

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe85

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
8:1	HSDCOCAL_TIMEBASE_TARGET	R/W	<p>Timebase for oscillation clock measurement (cfg_clk cycles). This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x13</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
0	HSDCOCAL_ENABLE_OVR_EN	R/W	<p>calibctrl o_hsdcoCAL_cal_en override enable. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_HSDCOCAL\_CFG\_6**

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe86

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

9:0	HSDCOCAL_SELDAC_UP_LIMIT	R/W	Configure sel_dac upper limit value. This field is quasi-static. <b>Value After Reset:</b> 0x1ff <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff
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**PPI\_RW\_HSDCOCAL\_CFG\_7**

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe87

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:0	HSDCOCAL_SELDAC_DOWN_LI MIT	R/W	Configure sel_dac lower limit value. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

**PPI\_RW\_HSDCOCAL\_CFG\_8**

- **Description:** HS-DCO calibration control
- **Size:** 16 bits
- **Offset:** 0xe88

Bits	Name	Memory Access	Description
15:0	HSDCOCAL_N_REF_RANGE	R/W	Sets HSDCO calibration target frequency range. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**PPI\_R\_HSDCOCAL\_DEBUG\_RB**

- **Description:** HS-DCO calibration observability
- **Size:** 16 bits
- **Offset:** 0xe89

Bits	Name	Memory Access	Description
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15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7	HSDCOCAL_DONE	R	Power-on calibration has successfully finished. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6:4	HSDCOCAL_ERROR	R	Power-on calibration error. Target frequency not reached. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
3:0	HSDCOCAL_STATE	R	Power-on FSM current state. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_ICTRL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_0**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1000

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_RXALTERNATECALHS_D0_OV_R_VAL	R/W	o_rxalternatecalhs_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12:5	O_RXDATAHS_D0_OVR_VAL	R/W	o_rxdatahs_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
4	O_RXWORDCLKHS_D0_OVR_VAL	R/W	o_rxwordclkhs_d0_override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
3	O_RXSKEWCALHS_D0_OVR_VAL	R/W	<p>o_rxskewcalhs_d0_ override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXVALIDHS_D0_OVR_VAL	R/W	<p>o_rxvalidhs_d0_ override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXSYNCHS_D0_OVR_VAL	R/W	<p>o_rxsynchs_d0_ override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXACTIVEHS_D0_OVR_VAL	R/W	<p>o_rxactivehs_d0_ override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG IOCTL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_1**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1001

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
11	O_RXALTERNATECALHS_D0_OVR_EN	R/W	<p>o_rxalternatecalhs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	I_TXDATAHS_D0_OVR_EN	R/W	<p>i_txdatahs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
9	O_TXWORDCLKHS_D0_OVR_EN	R/W	<p>o_txwordclkhs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_TXREADYHS_D0_OVR_EN	R/W	<p>o_txreadyhs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_TXDATATRANSFERENHS_D0_OVR_EN	R/W	<p>i_txdatatransferenhs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_TXREQUESTHS_D0_OVR_EN	R/W	<p>i_txrequesths_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_RXDATAHS_D0_OVR_EN	R/W	<p>o_rxdatahs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	O_RXWORDCLKHS_D0_OVR_EN	R/W	<p>o_rxwordclkhs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	O_RXSKEWCALHS_D0_OVR_EN	R/W	<p>o_rxskewcalhs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXVALIDHS_D0_OVR_EN	R/W	<p>o_rxvalidhs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
1	O_RXSYNCHS_D0_OVR_EN	R/W	<p>o_rxsynchs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXACTIVEHS_D0_OVR_EN	R/W	<p>o_rxactivehs_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_2**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1002

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0X</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	I_TXSKEWCALHS_D0_OVR_VAL	R/W	<p>i_txskewcalhs_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:4	I_TXDATAHS_D0_OVR_VAL	R/W	<p>i_txdatahs_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
3	O_TXWORDCLKHS_D0_OVR_VAL	R/W	<p>o_txwordclkhs_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_TXREADYHS_D0_OVR_VAL	R/W	<p>o_txreadyhs_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
1	I_TXDATATRANSFERENHS_D0_OVR_VAL	R/W	i_txdatatransferenhs_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXREQUESTHS_D0_OVR_VAL	R/W	i_txrequesths_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_3**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1003

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12	I_TXSKEWCALHS_D0_OVR_EN	R/W	i_txskewcalhs_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	I_TXALTERNATECALHS_D0_OVR_EN	R/W	i_txalternatecalhs_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	I_TXDATAESC_D0_OVR_EN	R/W	i_txdataesc_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:6	I_TXTRIGGERESC_D0_OVR_VAL	R/W	i_txtriggeresc_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

Bits	Name	Memory Access	Description
5	O_TXREADYESC_D0_OVR_VAL	R/W	<p>o_txreadyesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TXVALIDDESC_D0_OVR_VAL	R/W	<p>i_txvaliddesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TXULPSESC_D0_OVR_VAL	R/W	<p>i_txulpsesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	I_TXULPSEXIT_D0_OVR_VAL	R/W	<p>i_txulpsexit_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	I_TXLPDTESC_D0_OVR_VAL	R/W	<p>i_txlpdtesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	I_TXREQUESTESC_D0_OVR_VAL	R/W	<p>i_txrequestesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_4**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1004

Bits	Name	Memory Access	Description
15	I_TXALTERNATECALHS_D0_OVR_VAL	R/W	<p>i_txalternatecalhs_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14:7	I_TXDATAESC_D0_OVR_VAL	R/W	<p>i_txdataesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

Bits	Name	Memory Access	Description
6	I_TXTRIGGERESC_D0_OVR_EN	R/W	i_txtriggeresc_d0override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	O_TXREADYESC_D0_OVR_EN	R/W	o_txreadyesc_d0override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	I_TXVALIDDESC_D0_OVR_EN	R/W	i_txvaliddesc_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	I_TXULPSESC_D0_OVR_EN	R/W	i_txulpsesc_d0override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	I_TXULPSEXIT_D0_OVR_EN	R/W	i_txulpsexit_d0override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	I_TXLPDTESC_D0_OVR_EN	R/W	i_txlpdtesc_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXREQUESTESC_D0_OVR_EN	R/W	i_txrequestesc_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_5**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1005

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_D0_OVR_VAL	R/W	<p>o_rxdataesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:4	O_RXTRIGGERESC_D0_OVR_VAL	R/W	<p>o_rxtriggeresc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
3	O_RXVALIDDESC_D0_OVR_VAL	R/W	<p>o_rxvaliddesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXULPSESC_D0_OVR_VAL	R/W	<p>o_rxulpsesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXLPDTESC_D0_OVR_VAL	R/W	<p>o_rxlpdtesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_D0_OVR_VAL	R/W	<p>o_rxclkesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_6**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1006

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0X</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
5	O_RXDATAESC_D0_OVR_EN	R/W	<p>o_rxdataesc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4	O_RXTRIGGERESC_D0_OVR_EN	R/W	<p>o_rxtriggeresc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	O_RXVALIDDESC_D0_OVR_EN	R/W	<p>o_rxvaliddesc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXULPSESC_D0_OVR_EN	R/W	<p>o_rxulpsesc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXLPDTESC_D0_OVR_EN	R/W	<p>o_rxlpdtesc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_D0_OVR_EN	R/W	<p>o_rxclkesc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_7**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1007

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	O_ERRSOTSYNCHS_D0_OVR_V AL	R/W	<p>o_errsotsynchs_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
13	O_ERRSOTHS_D0_OVR_VAL	R/W	<p>o_errsoths_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	O_ERRCONTENTIONLP1_D0_OVR_VAL	R/W	<p>o_errcontentionlp1_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	O_ERRCONTENTIONLP0_D0_OVR_VAL	R/W	<p>o_errcontentionlp0_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	O_ERRCONTROL_D0_OVR_VAL	R/W	<p>o_errcontrol_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	O_ERRSYNCESC_D0_OVR_VAL	R/W	<p>o_errsynceesc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_ERRESC_D0_OVR_VAL	R/W	<p>o_erresc_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCECTXSTOPMODE_D0_OVR_VAL	R/W	<p>i_forcetxstopmode_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCECRXMODE_D0_OVR_VAL	R/W	<p>i_forcerxmode_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_D0_OVR_VAL	R/W	<p>o_direction_d0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4	I_TURNDISABLE_D0_OVR_VAL	R/W	i_turndisable_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	I_TURNREQUEST_D0_OVR_VAL	R/W	i_turnrequest_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	O_ULPSACTIVENOT_D0_OVR_VAL	R/W	o_ulpsactivenot_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	O_STOPSTATE_D0_OVR_VAL	R/W	o_stopstate_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_ENABLE_D0_OVR_VAL	R/W	i_enable_d0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG IOCTL\_RW\_DPHY\_PPI\_LANE0\_OVR\_0\_8**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1008

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14	O_ERRSOTSYNCHS_D0_OVR_EN	R/W	o_errsotsynchs_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13	O_ERRSOTHs_D0_OVR_EN	R/W	o_errsoths_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
12	O_ERRCONTENTIONLP1_D0_OVR_EN	R/W	<p>o_errcontentionlp1_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	O_ERRCONTENTIONLP0_D0_OVR_EN	R/W	<p>o_errcontentionlp0_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	O_ERRCONTROL_D0_OVR_EN	R/W	<p>o_errcontrol_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	O_ERRSYNCESC_D0_OVR_EN	R/W	<p>o_errsyncesc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_ERRESC_D0_OVR_EN	R/W	<p>o_erresc_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCETXSTOPMODE_D0_OVR_EN	R/W	<p>i_forcetxstopmode_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCERXMODE_D0_OVR_EN	R/W	<p>i_forcerxmode_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_D0_OVR_EN	R/W	<p>o_direction_d0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4	I_TURNDISABLE_D0_OVR_EN	R/W	i_turndisable_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	I_TURNREQUEST_D0_OVR_EN	R/W	i_turnrequest_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	O_ULPSACTIVENOT_D0_OVR_EN	R/W	o_ulpsactivenot_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	O_STOPSTATE_D0_OVR_EN	R/W	o_stopstate_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_ENABLE_D0_OVR_EN	R/W	i_enable_d0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE0\_OVR\_0\_9**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1009

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_RXALTERNATECALHS_D0	R	o_rxalternatecalhs_d0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

Bits	Name	Memory Access	Description
12:5	O_RXDATAHS_D0	R	<p>o_rxdatahs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
4	O_RXWORDCLKHS_D0	R	<p>o_rxwordclkhs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	O_RXSKEWCALHS_D0	R	<p>o_rxskewcalhs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXVALIDHS_D0	R	<p>o_rxvalidhs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXSYNCHS_D0	R	<p>o_rxsynchs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXACTIVEHS_D0	R	<p>o_rxactivehs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_DPHY\_PPI\_LANE0\_OVR\_0\_10**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x100a

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	I_TXSKEWCALHS_D0_INT	R	<p>i_txskewcalhs_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	I_TXALTERNATECALHS_D0_INT	R	<p>i_txalternatecalhs_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11:4	I_TXDATAHS_D0_INT	R	<p>i_txdatahs_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
3	O_TXWORDCLKHS_D0	R	<p>o_txwordclkhs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_TXREADYHS_D0	R	<p>o_txreadyhs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	I_TXDATATRANSFERENHS_D0_INT	R	<p>i_txdatatransferenhs_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
0	I_TXREQUESTHS_D0_INT	R	<p>i_txrequesths_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE0\_OVR\_0\_11**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x100b

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
9:6	I_TXTRIGGERESC_D0_INT	R	<p>i_txtriggeresc_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
5	O_TXREADYESC_D0	R	<p>o_txreadyesc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
4	I_TXVALIDDESC_D0_INT	R	<p>i_txvaliddesc_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	I_TXULPSESC_D0_INT	R	<p>i_txulpsesc_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
2	I_TXULPSEXIT_D0_INT	R	<p>i_txulpsexit_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	I_TXLPDTESC_D0_INT	R	<p>i_txlpdtesc_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	I_TXREQUESTESC_D0_INT	R	<p>i_txrequestesc_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE0\_OVR\_0\_12**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x100c

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	I_TXDATAESC_D0_INT	R	<p>i_txdataesc_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE0\_OVR\_0\_13**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x100d

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_D0	R	<p>o_rxdataesc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:4	O_RXTRIGGERESC_D0	R	<p>o_rxtriggeresc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
3	O_RXVALIDDESC_D0	R	<p>o_rxvaliddesc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXULPSESC_D0	R	<p>o_rxulpsesc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXLPDTESC_D0	R	<p>o_rxlpdtesc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXCLKESC_D0	R	<p>o_rxclkesc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_DPHY\_PPI\_LANE0\_OVR\_0\_14**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x100e

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	O_ERRSOTSYNCHS_D0	R	<p>o_errsotsynchs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
13	O_ERRSOTHs_D0	R	<p>o_errsoths_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	O_ERRCONTENTIONLP1_D0	R	<p>o_errcontentionlp1_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11	O_ERRCONTENTIONLP0_D0	R	<p>o_errcontentionlp0_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	O_ERRCONTROL_D0	R	<p>o_errcontrol_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	O_ERRSYNCESC_D0	R	<p>o_errsyncesc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
8	O_ERRESC_D0	R	<p>o_erresc_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7	I_FORCETXSTOPMODE_D0_INT	R	<p>i_forcetxstopmode_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
6	I_FORCERXMODE_D0_INT	R	<p>i_forcerxmode_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
5	O_DIRECTION_D0	R	<p>o_direction_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
4	I_TURNDISABLE_D0_INT	R	<p>i_turndisable_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	I_TURNREQUEST_D0_INT	R	<p>i_turnrequest_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_ULPSACTIVENOT_D0	R	<p>o_ulpsactivenot_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
1	O_STOPSTATE_D0	R	<p>o_stopstate_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	I_ENABLE_D0_INT	R	<p>i_enable_d0_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG IOCTL\_R\_DPHY\_PPI\_LANE0\_OVR\_0\_15**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x100f

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12:5	O_RXDATAHS_D0	R	<p>o_rxdatahs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
4	O_RXWORDCLKHS_D0	R	<p>o_rxwordclkhs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	O_RXSKEWCALHS_D0	R	<p>o_rxskewcalhs_d0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
2	O_RXVALIDHS_D0	R	<p><code>o_rxvalidhs_d0</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXSYNCHS_D0	R	<p><code>o_rxsynchs_d0</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXACTIVEHS_D0	R	<p><code>o_rxactivehs_d0</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_0**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1010

Bits	Name	Memory Access	Description
15:0	O_RXDATAHS_C0_OVR_VAL	R/W	<p><code>o_rxdatahs_c0</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_1**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1011

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

Bits	Name	Memory Access	Description
13	O_RXALPNIBBLE_C0_OVR_EN	R/W	<p>o_rxalpnibble_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12:9	O_RXALPCODE_C0_OVR_VAL	R/W	<p>o_rxalpcode_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
8	O_RXALPVALIDHS_C0_OVR_EN	R/W	<p>o_rxalpvalidhs_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:5	O_RXSYNCTYPEHS_C0_OVR_VAL	R/W	<p>o_rxsynctypehs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
4	O_RXWORDCLKHS_C0_OVR_VAL	R/W	<p>o_rxwordclkhs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	O_RXINVALIDCODEHS_C0_OVR_VAL	R/W	<p>o_rxinvalidcodehs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXVALIDHS_C0_OVR_VAL	R/W	<p>o_rxvalidhs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXSYNCHS_C0_OVR_VAL	R/W	<p>o_rxsynchs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXACTIVEHS_C0_OVR_VAL	R/W	<p>o_rxactivehs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_2**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits

## ■ Offset: 0x1012

Bits	Name	Memory Access	Description
15:13	I_TXSYNCTYPEHS_C0_OVR_VA L	R/W	i_txsynctypehs_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
12	O_RXALPCODE_C0_OVR_EN	R/W	o_rxalpcode_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11:8	O_RXALPNIBBLE_C0_OVR_VAL	R/W	o_rxalpnibble_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7	O_RXALPVALIDHS_C0_OVR_VA L	R/W	o_rxalpvalidhs_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	O_RXDATAHS_C0_OVR_EN	R/W	o_rxdatahs_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	O_RXSYNCTYPEHS_C0_OVR_E N	R/W	o_rxsynctypehs_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	O_RXWORDCLKHS_C0_OVR_EN	R/W	o_rxwordclkhs_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	O_RXINVALIDCODEHS_C0_OVR _EN	R/W	o_rxinvalidcodehs_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
2	O_RXVALIDHS_C0_OVR_EN	R/W	<p><code>o_rxvalidhs_c0</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXSYNCHS_C0_OVR_EN	R/W	<p><code>o_rxsynchs_c0</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXACTIVEHS_C0_OVR_EN	R/W	<p><code>o_rxactivehs_c0</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCRTL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_3**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1013

Bits	Name	Memory Access	Description
15:0	I_TXDATAHS_C0_OVR_VAL	R/W	<p><code>i_txdatahs_c0</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCRTL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_4**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1014

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

Bits	Name	Memory Access	Description
14	O_TXWORDCLKHS_C0_OVR_VAL	R/W	<p>o_txwordclkhs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	O_TXREADYHS_C0_OVR_VAL	R/W	<p>o_txreadyhs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	I_TXDATATRANSFERENHS_C0_OVR_VAL	R/W	<p>i_txdatatransferenhs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	I_TXREQUESTHS_C0_OVR_VAL	R/W	<p>i_txrequesths_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	I_TXDATAESC_C0_OVR_EN	R/W	<p>i_txdataesc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9:6	I_TXTRIGGERESC_C0_OVR_VAL	R/W	<p>i_txtriggeresc_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
5	O_TXREADYESC_C0_OVR_VAL	R/W	<p>o_txreadyesc_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TXVALIDDESC_C0_OVR_VAL	R/W	<p>i_txvaliddesc_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TXULPSESC_C0_OVR_VAL	R/W	<p>i_txulpsesc_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	I_TXULPSEXIT_C0_OVR_VAL	R/W	<p>i_txulpsexit_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
1	I_TXLPDTESC_C0_OVR_VAL	R/W	i_txlpdtesc_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXREQUESTESC_C0_OVR_VAL	R/W	i_txrequestesc_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCtrl\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_5**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1015

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:7	I_TXDATAESC_C0_OVR_VAL	R/W	i_txdataesc_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
6	I_TXTRIGGERESC_C0_OVR_EN	R/W	i_txtriggeresc_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	O_TXREADYESC_C0_OVR_EN	R/W	o_txreadyesc_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	I_TXVALIDDESC_C0_OVR_EN	R/W	i_txvaliddesc_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
3	I_TXULPSESC_C0_OVR_EN	R/W	i_txulpsesc_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	I_TXULPSEXIT_C0_OVR_EN	R/W	i_txulpsexit_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	I_TXLPDTESC_C0_OVR_EN	R/W	i_txlpdtesc_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXREQUESTESC_C0_OVR_EN	R/W	i_txrequestesc_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_6**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1016

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_C0_OVR_VAL	R/W	o_rxdataesc_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:4	O_RXTRIGGERESC_C0_OVR_VAL	R/W	o_rxtriggeresc_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3	O_RXVALIDDESC_C0_OVR_VAL	R/W	o_rxvaliddesc_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
2	O_RXULPSESC_C0_OVR_VAL	R/W	<p><i>o_rxulpsesc_c0</i> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXLPDTESC_C0_OVR_VAL	R/W	<p><i>o_rxlpdtesc_c0</i> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_C0_OVR_VAL	R/W	<p><i>o_rxclkesc_c0</i> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_7**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1017

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	I_TXSYNCTYPEHS_C0_OVR_EN	R/W	<p><i>i_txsynctypehs_c0</i> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	I_TXSENDSYNCHS_C0_OVR_EN	R/W	<p><i>i_txsendsynchs_c0</i> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	I_TXDATAHS_C0_OVR_EN	R/W	<p><i>i_txdatahs_c0</i> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
9	O_TXWORDCLKHS_C0_OVR_EN	R/W	<p>o_txwordclkhs_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_TXREADYHS_C0_OVR_EN	R/W	<p>o_txreadyhs_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_TXDATATRANSFERENHS_C0_OVR_EN	R/W	<p>i_txdatatransferenhs_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_TXREQUESTHS_C0_OVR_EN	R/W	<p>i_txrequesths_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_RXDATAESC_C0_OVR_EN	R/W	<p>o_rxdataesc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	O_RXTRIGGERESC_C0_OVR_E N	R/W	<p>o_rxtriggeresc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	O_RXVALIDDESC_C0_OVR_EN	R/W	<p>o_rxvaliddesc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXULPSESC_C0_OVR_EN	R/W	<p>o_rxulpsesc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
1	O_RXLPDTESC_C0_OVR_EN	R/W	<p>o_rxlpdtesc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_C0_OVR_EN	R/W	<p>o_rxclkesc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE0\_OVR\_1\_8**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1018

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	I_TXSENDSYNCHS_C0_OVR_VAL	R/W	<p>i_txsendsynchs_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	O_ERRSOTHS_C0_OVR_VAL	R/W	<p>o_errsoths_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	O_ERRCONTENTIONLP1_C0_OVR_VAL	R/W	<p>o_errcontentionlp1_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	O_ERRCONTENTIONLP0_C0_OVR_VAL	R/W	<p>o_errcontentionlp0_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
10	O_ERRCONTROL_C0_OVR_VAL	R/W	<p>o_errcontrol_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	O_ERRSYNCESC_C0_OVR_VAL	R/W	<p>o_errsyncesc_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_ERRESC_C0_OVR_VAL	R/W	<p>o_erresc_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCECTXSTOPMODE_C0_OVR_VAL	R/W	<p>i_forcetxstopmode_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCECRXMODE_C0_OVR_VAL	R/W	<p>i_forcerxmode_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_C0_OVR_VAL	R/W	<p>o_direction_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TURNDISABLE_C0_OVR_VAL	R/W	<p>i_turndisable_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TURNREQUEST_C0_OVR_VAL	R/W	<p>i_turnrequest_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_ULPSACTIVENOT_C0_OVR_VAL	R/W	<p>o_ulpsactivenot_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_STOPSTATE_C0_OVR_VAL	R/W	<p>o_stopstate_c0 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	I_ENABLE_C0_OVR_VAL	R/W	i_enable_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IODRIVE\_R\_W\_CPHY\_PPI\_LANE0\_OVR\_1\_9**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1019

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0X0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_ERRSOTHS_C0_OVR_EN	R/W	o_errsoths_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	O_ERRCONTENTIONLP1_C0_OVR_EN	R/W	o_errcontentionlp1_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	O_ERRCONTENTIONLP0_C0_OVR_EN	R/W	o_errcontentionlp0_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	O_ERRCONTROL_C0_OVR_EN	R/W	o_errcontrol_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	O_ERRSYNCESC_C0_OVR_EN	R/W	o_errsyncesc_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
8	O_ERRESC_C0_OVR_EN	R/W	<p>o_erreesc_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCETXSTOPMODE_C0_OVR_EN	R/W	<p>i_forcetxstopmode_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCERXMODE_C0_OVR_EN	R/W	<p>i_forcerxmode_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_C0_OVR_EN	R/W	<p>o_direction_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TURNDISABLE_C0_OVR_EN	R/W	<p>i_turndisable_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TURNREQUEST_C0_OVR_EN	R/W	<p>i_turnrequest_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_ULPSACTIVENOT_C0_OVR_EN	R/W	<p>o_ulpsactivenot_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_STOPSTATE_C0_OVR_EN	R/W	<p>o_stopstate_c0 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	I_ENABLE_C0_OVR_EN	R/W	i_enable_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE0\_OVR\_1\_10**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x101a

Bits	Name	Memory Access	Description
15:0	O_RXDATAHS_C0	R	o_rxdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE0\_OVR\_1\_11**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x101b

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:12	I_TXSYNCTYPEHS_C0_INT	R	i_txsynctypehs_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7 <b>Volatile:</b> true

Bits	Name	Memory Access	Description
11:8	O_RXALPCODE_C0	R	<p>o_rxalpcode_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
7:5	O_RXSYNCTYPEHS_C0	R	<p>o_rxsynctypehs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>
4	O_RXWORDCLKHS_C0	R	<p>o_rxwordclkhs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	O_RXINVALIDCODEHS_C0	R	<p>o_rxinvalidcodehs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXVALIDHS_C0	R	<p>o_rxvalidhs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXSYNCHS_C0	R	<p>o_rxsynchs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXACTIVEHS_C0	R	<p>o_rxactivehs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_CPHY\_PPI\_LANE0\_OVR\_1\_12**

- **Description:** Digital hard macro interface observability

- **Size:** 16 bits
- **Offset:** 0x101c

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	I_TXSENDSYNCHS_C0_INT	R	<p>i_txsendsynchs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12:5	I_TXDATAESC_C0_INT	R	<p>i_txdataesc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
4:1	O_RXALPNIBBLE_C0	R	<p>o_rxalpnibble_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
0	O_RXALPVALIDHS_C0	R	<p>o_rxalpvalidhs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

### CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE0\_OVR\_1\_13

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x101d

Bits	Name	Memory Access	Description

15:0	I_TXDATAHS_C0_INT	R	i_txdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true
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**CORE\_DIG\_IOCtrl\_R\_CPHY\_PPI\_LANE0\_OVR\_1\_14**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x101e

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0X0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_TXWORDCLKHS_C0	R	o_txwordclkhs_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
12	O_TXREADYHS_C0	R	o_txreadyhs_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
11	I_TXDATATRANSFERENHS_C0_INT	R	i_txdatatransferenhs_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
10	I_TXREQUESTHS_C0_INT	R	i_txrequesths_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

Bits	Name	Memory Access	Description
9:6	I_TXTRIGGERESC_C0_INT	R	i_txtriggeresc_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true
5	O_TXREADYESC_C0	R	o_txreadyesc_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
4	I_TXVALIDESC_C0_INT	R	i_txvalidesc_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	I_TXULPSESC_C0_INT	R	i_txulpsesc_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	I_TXULPSEXIT_C0_INT	R	i_txulpsexit_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	I_TXLPDTESC_C0_INT	R	i_txlpdtesc_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	I_TXREQUESTESC_C0_INT	R	i_txrequestesc_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_CPHY\_PPI\_LANE0\_OVR\_1\_15**

- **Description:** Digital hard macro interface observability

- **Size:** 16 bits
- **Offset:** 0x101f

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_C0	R	<p>o_rxdataesc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:4	O_RXTRIGGERESC_C0	R	<p>o_rxtriggeresc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
3	O_RXVALIDDESC_C0	R	<p>o_rxvaliddesc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXULPSESC_C0	R	<p>o_rxulpsesc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXLPDTESC_C0	R	<p>o_rxlpdtesc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXCLKESC_C0	R	<p>o_rxclkesc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

#### CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_2\_0

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits

- **Offset:** 0x1020

Bits	Name	Memory Access	Description
15	OA_LANE0_SHORT_LB_EN	R/W	oa_lane0_short_lb_en bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	I_LANE0_GPIO_IN_OVR_EN	R/W	i_lane0_gpio_in override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13	OA_LANE0_LVDS_OFFSET_EN_OVR_EN	R/W	oa_lane0_lvds_offset_en override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_LANE0_LVDS_HYST_EN_OVR_EN	R/W	oa_lane0_lvds_hyst_en override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11:0	OA_LANE0_SPARE_IN	R/W	Lane 0 input spare bus (bits [11:0]). This signal is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

### CORE\_DIG\_IODEL\_R\_W\_AFE\_LANE0\_CTRL\_2\_1

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1021

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14	OA_LANE0_HSTX_LOWCAP_EN_OVR_EN	R/W	oa_lane0_hstx_lowcap_en override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
13:12	I_LANE0_GPIO_IN_OVR_VAL	R/W	i_lane0_gpio_in_ovr_val override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
11:10	OA_LANE0_GPO_EN	R/W	oa_lane0_gpo_en[0] bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9:8	OA_LANE0_GPI_HYST_EN	R/W	oa_lane0_gpi_hyst_en[0] bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7:6	OA_LANE0_GPI_EN	R/W	oa_lane0_gpi_en[0] bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
5	OA_LANE0_LVDS_OFFSET_EN_OVR_VAL	R/W	oa_lane0_lvds_offset_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE0_LVDS_HYST_EN_OVR_VAL	R/W	oa_lane0_lvds_hyst_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE0_SEL_LVDS_OFF	R/W	oa_lane0_lvds_cmsw_off bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2:1	OA_LANE0_LVDS_CMSW_PROG	R/W	oa_lane0_lvds_cmsw_prog word configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

Bits	Name	Memory Access	Description
0	OA_LANE0_LVDS_EN	R/W	<p>oa_lane0_lvds_en bit configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_2\_2**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1022

Bits	Name	Memory Access	Description
15:7	RESERVED_15_7	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
6	OA_LANE0_HSTX_DIV_EN_OVR_VAL	R/W	<p>oa_lane0_hstx_div_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5:4	OA_LANE0_HSTX_LOWCAP_EN_OVR_VAL	R/W	<p>oa_lane0_hstx_lowcap_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
3	OA_LANE0_HSRX_DPHY_DDL_PON_OVR_VAL	R/W	<p>oa_lane0_hsrx_dphy_ddl_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	OA_LANE0_HSRX_TERM_EN200_OHMS	R/W	<p>Lane 0 HS-RX termination value. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	OA_LANE0_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_cphy_cdr_fbk_fast_lock_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	OA_LANE0_SEL_LANE_CFG	R/W	<p>Lane 0 D-PHY/C-PHY configuration. 1'b0: D-PHY data lane (when phy_mode is 1'b0); C-PHY slave lane (when phy_mode is 1'b1). 1'b1: D-PHY clock lane (when phy_mode is 1'b0); C-PHY master lane (when phy_mode is 1'b1). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_2\_3**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1023

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	OA_LANE0_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_VAL	R/W	<p>oa_lane0_hsrx_cphy_cdr_fbk_fast_lock_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	OA_LANE0_HSRX_DPHY_DDL_EN_OVR_VAL	R/W	<p>oa_lane0_hsrx_dphy_ddl_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_LANE0_HSRX_DPHY_DDL_DCC_EN_OVR_VAL	R/W	<p>oa_lane0_hsrx_dphy_ddl_dcc_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	OA_LANE0_LPTX_DIN_DP_OVR_VAL	R/W	<p>oa_lane0_lptx_din_dp override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
9	OA_LANE0_LPTX_DIN_DN_OVR_VAL	R/W	oa_lane0_lptx_din_dn override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE0_HSTX_SEL_CLKLB	R/W	Lane 0 HS-TX clock source. 1'b0: External PLL clock. 1'b1: Common block internal DCO clock. This signal is quasi-static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:5	OA_LANE0_HSTX_EQA	R/W	Lane 0 HS-TX de-emphasis word (upper-half). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
4	OA_LANE0_HSTX_SEL_PHASE0	R/W	Lane 0 HS-TX clock phase selection. 1'b0: 90 (for D-PHY clock lane configuration), 1'b1: 0 (for both C-PHY and D-PHY data lane configurations). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:2	OA_LANE0_HSTX_BOOST_EN_OVR_VAL	R/W	oa_lane0_hstx_boost_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
1:0	OA_LANE0_HSTX_PON_OVR_VAL	R/W	oa_lane0_hstx_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_2\_4**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1024

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

Bits	Name	Memory Access	Description
11	OA_LANE0_HSRX_DPHY_DDL_D CC_EN_OVR_EN	R/W	oa_lane0_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE0_HSTX_TERM_EN_OV R_EN	R/W	oa_lane0_hstx_term_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:8	OA_LANE0_LPTX_SR_BYPASS_EN	R/W	oa_lane0_lptx_sr_bypass_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7	OA_LANE0_LPTX_DIN_DP_OVR_EN	R/W	oa_lane0_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE0_LPTX_DIN_DN_OVR _EN	R/W	oa_lane0_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	OA_LANE0_HSTX_CLK_OBS_EN	R/W	Lane 0 HS clock pattern driven in the lines (debug feature). Active high. This signal is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4:2	OA_LANE0_HSTX_EQB	R/W	Lane 0 HS-TX de-emphasis word (lower-half). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
1	OA_LANE0_HSTX_BOOST_EN_OVR_EN	R/W	oa_lane0_hstx_boost_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
0	OA_LANE0_HSTX_PON_OVR_E_N	R/W	<p>oa_lane0_hstx_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_2\_5**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1025

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0X0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	OA_LANE0_HSRX_DPHY_DDL_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:10	OA_LANE0_HSTX_TERM_EN_OVR_VAL	R/W	<p>oa_lane0_hstx_term_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
9	OA_LANE0_HSTX_DATA_CA_OVR_EN	R/W	<p>oa_lane0_hstx_data_ca override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE0_HSTX_DATA_BC_OVR_EN	R/W	<p>oa_lane0_hstx_data_ca override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:0	OA_LANE0_HSTX_DATA_AB_DPHY_OVR_VAL	R/W	<p>oa_lane0_hstx_data_ab_dphy override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_2\_6**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1026

Bits	Name	Memory Access	Description
15	OA_LANE0_HSRX_DPHY_DDL_PON_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	OA_LANE0_HSTX_DATA_AB_DPHY_OVR_EN	R/W	<p>oa_lane0_hstx_data_ab_dphy override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13:7	OA_LANE0_HSTX_DATA_CA_OVR_VAL	R/W	<p>oa_lane0_hstx_data_ca override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f</p>
6:0	OA_LANE0_HSTX_DATA_BC_OVR_VAL	R/W	<p>oa_lane0_hstx_data_bc override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_2\_7**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1027

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0X0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

Bits	Name	Memory Access	Description
13	OA_LANE0_HSRX_VCM_DET_SYNC_BYPASS	R/W	<p>Enable vcm detector filter bypass which controls CDR input propagation. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12:10	OA_LANE0_HSRX_CPHY_CDR_FBK_CAP_PROG	R/W	<p>Lane 0 C-PHY low-pass filter bandwidth (symbol rate dependent). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x7</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
9	OA_LANE0_HSRX_CPHY_CDR_FBK_EN_OVR_VAL	R/W	<p>oa_lane0_hsrx_cphy_cdr_fbk_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE0_LPRX_ULP_PON_OVR_EN	R/W	<p>oa_lane0_lprx_ulp_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	OA_LANE0_LPRX_CD_PON_OVR_EN	R/W	<p>oa_lane0_lprx_cd_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE0_LPRX_LP_PON_OVR_EN	R/W	<p>oa_lane0_lprx_lp_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5:4	OA_LANE0_LPTX_PULLDWN_EN_OVR_VAL	R/W	<p>oa_lane0_lptx_pulldwn_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
3:2	OA_LANE0_LPTX_PON_OVR_VAL	R/W	<p>oa_lane0_lptx_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

Bits	Name	Memory Access	Description
1:0	OA_LANE0_LPTX_EN_OVR_VAL	R/W	<p>oa_lane0_lptx_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

**CORE\_DIG IOCTL\_RW\_AFE\_LANE0\_CTRL\_2\_8**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1028

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	OA_LANE0_HSRX_CDPHY_SEL_FAST	R/W	<p>Lane 0 HS-RX DDL delay cell strength. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_LANE0_HSRX_CPHY_DELAY_OVR_EN	R/W	<p>oa_lane0_hsrx_cphy_delay override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	OA_LANE0_HSRX_CPHY_MASK_CHANGE_OVR_VAL	R/W	<p>oa_lane0_hsrx_cphy_mask_change override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	OA_LANE0_HSRX_CPHY_CDR_FBK_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_cphy_cdr_fbk_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE0_LPTX_PULLDWN_EN_OVR_EN	R/W	<p>oa_lane0_lptx_pulldwn_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
7	OA_LANE0_LPTX_PON_OVR_EN	R/W	oa_lane0_lptx_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE0_LPTX_EN_OVR_EN	R/W	oa_lane0_lptx_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5:4	OA_LANE0_LPRX_ULP_PON_OVR_VAL	R/W	oa_lane0_lprx_ulp_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3:2	OA_LANE0_LPRX_CD_PON_OVR_VAL	R/W	oa_lane0_lprx_cd_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
1:0	OA_LANE0_LPRX_LP_PON_OVR_VAL	R/W	oa_lane0_lprx_lp_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_2\_9**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1029

Bits	Name	Memory Access	Description
15:12	OA_LANE0_HSRX_CPHY_DELAY_OVR_VAL	R/W	oa_lane0_hsrx_cphy_delay override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
11:9	OA_LANE0_HSRX_CPHY_CDR_DIV	R/W	Lane 0 C-PHY oscillation clock divider (for calibration). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x5 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

Bits	Name	Memory Access	Description
8	OA_LANE0_HSRX_SEL_GATED_POLARITY	R/W	<p>Lane &lt;0&gt; deserializer output polarity (D-PHY related). Active high. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:5	OA_LANE0_HSRX_HS_CLK_DIV	R/W	<p>Lane 0 D-PHY DDR clock lane divider (data rate dependent). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x7</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
4:3	OA_LANE0_HSRX_GMODE	R/W	<p>Lane 0 HS-RX preamplifier bandwidth configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
2:0	OA_LANE0_HSRX_EQUALIZER	R/W	<p>Lane 0 HS-RX preamplifier equalizer bitword configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_2\_10**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x102a

Bits	Name	Memory Access	Description
15	OA_LANE0_HSTX_DIV_EN_OVR_EN	R/W	<p>oa_lane0_hstx_div_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	OA_LANE0_HSRX_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
13	OA_LANE0_HSRX_PON_OVR_EN	R/W	<p>oa_lane0_hsrx_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	OA_LANE0_HSRX_CPHY_MASK_CHANGE_OVR_EN	R/W	<p>oa_lane0_hsrx_cphy_mask_change override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_LANE0_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_VAL	R/W	<p>oa_lane0_hsrx_cphy_alp_det_left_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	OA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_VAL	R/W	<p>oa_lane0_hsrx_cphy_alp_det_right_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	OA_LANE0_HSRX_VCM_DET_OUT_EN_OVR_VAL	R/W	<p>oa_lane0_hsrx_vcm_det_out_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE0_HSRX_VCM_DET_PON_OVR_VAL	R/W	<p>oa_lane0_hsrx_vcm_det_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	OA_LANE0_HSRX_OFFCAL_OBS_EN_OVR_VAL	R/W	<p>oa_lane0_hsrx_offcal_obs_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE0_HSRX_DESERIALIZE_R_DIV_EN_OVR_VAL	R/W	<p>oa_lane0_hsrx_deserializer_div_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
5	OA_LANE0_HSRX_DESERIALIZE_R_DATA_EN_OVR_VAL	R/W	oa_lane0_hsrx_deserializer_data_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE0_HSRX_DESERIALIZE_R_EN_OVR_VAL	R/W	oa_lane0_hsrx_deserializer_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE0_HSRX_HS_CLK_DIV_EN_OVR_VAL	R/W	oa_lane0_hsrx_hs_clk_div_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_LANE0_HSRX_DPHY_CLK_C_HANNEL_PULL_EN	R/W	Lane 0 D-PHY clock channel pull-up/pull-down enable. Active high. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE0_HSRX_TERM_LEFT_EN_OVR_VAL	R/W	oa_lane0_hsrx_term_left_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE0_HSRX_TERM_RIGHT_EN_OVR_VAL	R/W	oa_lane0_hsrx_term_right_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_2\_11**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x102b

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

Bits	Name	Memory Access	Description
14:13	OA_LANE0_HSRX_EN_OVR_VAL	R/W	oa_lane0_hsrx_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
12:11	OA_LANE0_HSRX_PON_OVR_VAL	R/W	oa_lane0_hsrx_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
10	OA_LANE0_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_EN	R/W	oa_lane0_hsrx_cphy_alp_det_left_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_EN	R/W	oa_lane0_hsrx_cphy_alp_det_right_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE0_HSRX_VCM_DET_OUT_EN_OVR_EN	R/W	oa_lane0_hsrx_vcm_det_out_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_LANE0_HSRX_VCM_DET_PON_OVR_EN	R/W	oa_lane0_hsrx_vcm_det_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE0_HSRX_OFFCAL_OBS_EN_OVR_EN	R/W	oa_lane0_hsrx_offcal_obs_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	OA_LANE0_HSRX_DESERIALIZE_R_DIV_EN_OVR_EN	R/W	oa_lane0_hsrx_deserializer_div_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE0_HSRX_DESERIALIZE_R_DATA_EN_OVR_EN	R/W	oa_lane0_hsrx_deserializer_data_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
3	OA_LANE0_HSRX_DESERIALIZE_R_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_deserializer_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	OA_LANE0_HSRX_HS_CLK_DIV_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_hs_clk_div_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	OA_LANE0_HSRX_TERM_LEFT_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_term_left_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	OA_LANE0_HSRX_TERM_RIGHT_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_term_right_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_2\_12**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x102c

Bits	Name	Memory Access	Description
15	OA_LANE0_HSRX_CPHY_SR_BY_PASS_Z	R/W	<p>Enable for the slew rate control latch bypass inside CDR. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14:13	OA_LANE0_HSRX_CPHY_FINE_RANGE	R/W	<p>Delay line fine delay cell setting for DDL. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
12:10	OA_LANE0_HSRX_DPHY_DDL_D IV	R/W	<p>Lane 0 HS-RX DDL oscillation clock divider. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

Bits	Name	Memory Access	Description
9	OA_LANE0_HSRX_DPHY_DATA_DELAY_OVR_EN	R/W	oa_lane0_hsrx_dphy_data_delay override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:5	OA_LANE0_HSRX_DPHY_DDL_VT_COMP_BIAS	R/W	Reserved. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
4	OA_LANE0_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_VAL	R/W	oa_lane0_hsrx_dphy_preamble_cal_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE0_HSRX_DPHY_DLL_EN_OVR_VAL	R/W	oa_lane0_hsrx_dphy_dll_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_LANE0_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_phase_change override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE0_HSRX_DPHY_DDL_BYPASS_EN_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_bypass_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE0_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_bias_bypass_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_2\_13**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x102d

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	OA_LANE0_HSRX_DPHY_DLL_F_BK_OVR_EN	R/W	oa_lane0_hsrx_dphy_dll_fbk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_LANE0_HSRX_DPHY_DLL_TUNE_MODE_OVR_EN	R/W	oa_lane0_hsrx_dphy_ddl_tune_mode override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	OA_LANE0_HSRX_DPHY_DLL_COARSE_BANK_OVR_EN	R/W	oa_lane0_hsrx_dphy_ddl_coarse_bank override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE0_HSRX_DPHY_DLL_BIAS_OVR_EN	R/W	oa_lane0_hsrx_dphy_ddl_bias override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:6	OA_LANE0_HSRX_DPHY_DATA_DELAY_OVR_VAL	R/W	oa_lane0_hsrx_dphy_data_delay override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
5	OA_LANE0_HSRX_DPHY_DLL_VT_COMP_EN	R/W	Reserved. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE0_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_EN	R/W	oa_lane0_hsrx_dphy_preamble_cal_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE0_HSRX_DPHY_DLL_EN_OVR_EN	R/W	oa_lane0_hsrx_dphy_dll_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
2	OA_LANE0_HSRX_DPHY_DDL_P HASE_CHANGE_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_phase_change override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	OA_LANE0_HSRX_DPHY_DDL_B YPASS_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_bypass_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	OA_LANE0_HSRX_DPHY_DDL_B IAS_BYPASS_EN_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_bias_bypass_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_2\_14**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x102e

Bits	Name	Memory Access	Description
15:10	OA_LANE0_HSRX_DPHY_DLL_F BK_OVR_VAL	R/W	<p>oa_lane0_hsrx_dphy_dll_fbk override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3f</p>
9:8	OA_LANE0_HSRX_DPHY_DLL_T UNE_MODE_OVR_VAL	R/W	<p>oa_lane0_hsrx_dphy_ddl_tune_mode override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
7:4	OA_LANE0_HSRX_DPHY_DLL_C OARSE_BANK_OVR_VAL	R/W	<p>oa_lane0_hsrx_dphy_ddl_coarse_bank override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
3:0	OA_LANE0_HSRX_DPHY_DLL_B IAS_OVR_VAL	R/W	<p>oa_lane0_hsrx_dphy_ddl_bias override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_2\_15**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x102f

Bits	Name	Memory Access	Description
15:11	OA_LANE0_ATB_SW	R/W	<p>Lane 0 analog test bus signal selection. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1f</p>
10	OA_LANE0_HSRX_MODE_OVR_EN	R/W	<p>oa_lane0_hsrx_mode override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	OA_LANE0_HSRX_DPHY_DDL_P HASE_LEFT_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_phase_left override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE0_HSRX_DPHY_DDL_P HASE_MID_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_phase_mid override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	OA_LANE0_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_EN	R/W	<p>oa_lane0_hsrx_dphy_ddl_phase_right override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE0_HSRX_OFFCAL_LEF T_OVR_EN	R/W	<p>oa_lane0_hsrx_offcal_left override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	OA_LANE0_HSRX_OFFCAL_RIG HT_OVR_EN	R/W	<p>oa_lane0_hsrx_offcal_right override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4:3	OA_LANE0_HSRX_DPHY_CLK_C HANNEL	R/W	Lane 0 D-PHY HS-RX clock channel selection. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
2:0	OA_LANE0_HSRX_DPHY_DLL_C P_PROG	R/W	Lane 0 D-PHY HS-RX DLL charge pump gain configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_IOCTL\_RW\_AFE\_LANE0\_CTRL\_3\_0**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1030

Bits	Name	Memory Access	Description
15:8	OA_LANE0_HSRX_OFFCAL_LEFT_OVR_VAL	R/W	oa_lane0_hsrx_offcal_left override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	OA_LANE0_HSRX_OFFCAL_RIGHT_OVR_VAL	R/W	oa_lane0_hsrx_offcal_right override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_IOCTL\_RW\_AFE\_LANE0\_CTRL\_3\_1**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1031

Bits	Name	Memory Access	Description
15:8	OA_LANE0_HSRX_DPHY_DDL_PHASE_MID_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_phase_mid (bits [7:0]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

7:0	OA_LANE0_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_phase_right (bits [7:0]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_3\_2**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1032

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:11	OA_LANE0_HSRX_MODE_OVR_VAL	R/W	oa_lane0_hsrx_mode override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
10	OA_LANE0_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_phase_right (bit [8]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE0_HSRX_DPHY_DDL_P HASE_MID_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_phase_mid (bit [8]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:0	OA_LANE0_HSRX_DPHY_DDL_P HASE_LEFT_OVR_VAL	R/W	oa_lane0_hsrx_dphy_ddl_phase_left override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_3\_3**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1033

Bits	Name	Memory Access	Description
15:8	IA_LANE0_HSRX_DATA_BC_MID_OVR_VAL	R/W	<p>ia_lane0_hsrx_data_bc_mid override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:0	IA_LANE0_HSRX_DATA_AB_LEFT_OVR_VAL	R/W	<p>ia_lane0_hsrx_data_ab_left override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_3\_4**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1034

Bits	Name	Memory Access	Description
15	IA_LANE0_HSRX_OUT_CAL_RIGHT_P_OVR_VAL	R/W	<p>ia_lane0_hsrx_out_cal_right_p override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	IA_LANE0_HSRX_OUT_CAL_RIGHT_N_OVR_VAL	R/W	<p>ia_lane0_hsrx_out_cal_right_n override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	IA_LANE0_HSRX_OUT_CAL_LEFT_P_OVR_VAL	R/W	<p>ia_lane0_hsrx_out_cal_left_p override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	IA_LANE0_HSRX_OUT_CAL_LEFT_N_OVR_VAL	R/W	<p>ia_lane0_hsrx_out_cal_left_n override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	IA_LANE0_HSRX_VCM_DET_OUT_OVR_VAL	R/W	<p>ia_lane0_hsrx_vcm_det_out override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
10	IA_LANE0_HSTX_WORD_CLK_O_VR_VAL	R/W	<p>ia_lane0_hstx_word_clk override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	IA_LANE0_HSRX_HS_CLK_DIV_OUT_OVR_VAL	R/W	<p>ia_lane0_hsrx_hs_clk_div_out override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	IA_LANE0_HSRX_WORD_CLK_O_VR_VAL	R/W	<p>ia_lane0_hsrx_word_clk override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:0	IA_LANE0_HSRX_DATA_CA_RIGHT_OVR_VAL	R/W	<p>ia_lane0_hsrx_data_ca_right override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_3\_5**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1035

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	IA_LANE0_HSRX_CPHY_CDR_OSC_CLK_OVR_EN	R/W	<p>ia_lane0_hsrx_cphy_cdr_osc_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	IA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_EN	R/W	<p>ia_lane0_hsrx_cphy_alp_det_right_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
12	IA_LANE0_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_EN	R/W	<p>ia_lane0_hsrx_cphy_alp_det_left_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	IA_LANE0_HSRX_DPHY_DDL_OSC_CLK_OVR_EN	R/W	<p>ia_lane0_hsrx_dphy_ddl_osc_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	IA_LANE0_HSRX_OUT_CAL_RIGHT_P_OVR_EN	R/W	<p>ia_lane0_hsrx_out_cal_right_p override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	IA_LANE0_HSRX_OUT_CAL_RIGHT_N_OVR_EN	R/W	<p>ia_lane0_hsrx_out_cal_right_n override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	IA_LANE0_HSRX_OUT_CAL_LEFT_P_OVR_EN	R/W	<p>ia_lane0_hsrx_out_cal_left_p override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	IA_LANE0_HSRX_OUT_CAL_LEFT_N_OVR_EN	R/W	<p>ia_lane0_hsrx_out_cal_left_n override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	IA_LANE0_HSRX_VCM_DET_OUTPUT_OVR_EN	R/W	<p>ia_lane0_hsrx_vcm_det_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	IA_LANE0_HSTX_WORD_CLK_OUTPUT_OVR_EN	R/W	<p>ia_lane0_hstx_word_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4	IA_LANE0_HSRX_HS_CLK_DIV_OUT_OVR_EN	R/W	<p>ia_lane0_hsrx_hs_clk_div_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	IA_LANE0_HSRX_WORD_CLK_OVR_EN	R/W	<p>ia_lane0_hsrx_word_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	IA_LANE0_HSRX_DATA_CA_RIGHT_OVR_EN	R/W	<p>ia_lane0_hsrx_data_ca_right override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	IA_LANE0_HSRX_DATA_BC_MID_OVR_EN	R/W	<p>ia_lane0_hsrx_data_bc_mid override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	IA_LANE0_HSRX_DATA_AB_LEFT_OVR_EN	R/W	<p>ia_lane0_hsrx_data_ab_left override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE0\_CTRL\_3\_6**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits
- **Offset:** 0x1036

Bits	Name	Memory Access	Description
15:14	O_LANE0_GPIO_OUT_OVR_VAL	R/W	<p>o_lane0_gpio_out_ovr_val override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
13:12	IA_LANE0_GPI_OUT_OVR_VAL	R/W	<p>ia_lane0_gpi_out_ovr_val override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

Bits	Name	Memory Access	Description
11:10	IA_LANE0_SPARE_OUT_OVR_VAL	R/W	ia_lane0_spare_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9:8	IA_LANE0_LPRX_DOUTULP_OVR_VAL	R/W	ia_lane0_lprx_doutulp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7:6	IA_LANE0_LPRX_DOUTLP_OVR_VAL	R/W	ia_lane0_lprx_doutlp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
5:4	IA_LANE0_LPRX_DOUTCD_OVR_VAL	R/W	ia_lane0_lprx_doutcd override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3	IA_LANE0_HSRX_CPHY_CDR_OSC_CLK_OVR_VAL	R/W	ia_lane0_hsrx_cphy_cdr_osc_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_VAL	R/W	ia_lane0_hsrx_cphy_alp_det_right_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_LANE0_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_VAL	R/W	ia_lane0_hsrx_cphy_alp_det_left_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	IA_LANE0_HSRX_DPHY_DDL_OSC_CLK_OVR_VAL	R/W	ia_lane0_hsrx_dphy_ddl_osc_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE0\_CTRL\_3\_7**

- **Description:** Analog macro lane 0 control
- **Size:** 16 bits

- **Offset:** 0x1037

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
5	O_LANE0_GPIO_OUT_OVR_EN	R/W	o_lane0_gpio_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	IA_LANE0_GPI_OUT_OVR_EN	R/W	ia_lane0_gpi_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	IA_LANE0_SPARE_OUT_OVR_E N	R/W	ia_lane0_spare_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_LANE0_LPRX_DOUTULP_OV R_EN	R/W	ia_lane0_lprx_doutulp override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_LANE0_LPRX_DOUTLP_OVR_EN	R/W	ia_lane0_lprx_doutlp override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	IA_LANE0_LPRX_DOUTCD_OVR _EN	R/W	ia_lane0_lprx_doutcd override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

### CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_3\_8

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x1038

Bits	Name	Memory Access	Description
15:12	OA_LANE0_HSRX_CPHY_DELAY	R	<p>oa_lane0_hsrx_cphy_delay multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
11	OA_LANE0_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN	R	<p>oa_lane0_hsrx_cphy_cdr_fbk_fast_lock_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	OA_LANE0_HSRX_DPHY_DDL_E_N	R	<p>oa_lane0_hsrx_dphy_ddl_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	OA_LANE0_HSRX_DPHY_DDL_DCC_EN	R	<p>oa_lane0_hsrx_dphy_ddl_dcc_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
8	OA_LANE0_LPTX_DIN_DP	R	<p>oa_lane0_lptx_din_dp multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7	OA_LANE0_LPTX_DIN_DN	R	<p>oa_lane0_lptx_din_dn multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
6:5	OA_LANE0_HSTX_LOWCAP_EN	R	<p>oa_lane0_hstx_lowcap_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
4	OA_LANE0_HSRX_DPHY_DDL_P_ON	R	<p>oa_lane0_hsrx_dphy_ddl_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3:2	OA_LANE0_HSTX_BOOST_EN	R	<p>oa_lane0_hstx_boost_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
1:0	OA_LANE0_HSTX_PON	R	<p>oa_lane0_hstx_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE0\_CTRL\_3\_9**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x1039

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
10	OA_LANE0_HSTX_DIV_EN	R	<p>oa_lane0_hstx_div_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9:8	OA_LANE0_HSTX_TERM_EN	R	<p>oa_lane0_hstx_term_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
7:0	OA_LANE0_HSTX_DATA_AB_DP HY	R	<p>oa_lane0_hstx_data_ab_dphy multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE0\_CTRL\_3\_10**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x103a

Bits	Name	Memory Access	Description
15:14	I_LANE0_GPIO_IN	R	<p>i_lane0_gpio_in[0] multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
13:7	OA_LANE0_HSTX_DATA_CA	R	<p>oa_lane0_hstx_data_ca multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f      <b>Volatile:</b> true</p>
6:0	OA_LANE0_HSTX_DATA_BC	R	<p>oa_lane0_hstx_data_bc multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f      <b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE0\_CTRL\_3\_11**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x103b

Bits	Name	Memory Access	Description
15:14	O_LANE0_GPIO_OUT	R	<p>oa_lane0_gpio_out multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
13	OA_LANE0_HSRX_CPHY_MASK_CHANGE	R	<p>oa_lane0_hsrx_cphy_mask_change multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	OA_LANE0_HSRX_CPHY_CDR_FBK_EN	R	<p>oa_lane0_hsrx_cphy_cdr_fbk_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11:10	OA_LANE0_LPRX_ULP_PON	R	<p>oa_lane0_lprx_ulp_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
9:8	OA_LANE0_LPRX_CD_PON	R	<p>oa_lane0_lprx_cd_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
7:6	OA_LANE0_LPRX_LP_PON	R	<p>oa_lane0_lprx_lp_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
5:4	OA_LANE0_LPTX_PULLDWN_EN	R	<p>oa_lane0_lptx_pulldwn_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
3:2	OA_LANE0_LPTX_PON	R	<p>oa_lane0_lptx_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
1:0	OA_LANE0_LPTX_EN	R	<p>oa_lane0_lptx_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_3\_12**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x103c

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14:13	OA_LANE0_HSRX_EN	R	<p>oa_lane0_hsrx_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
12:11	OA_LANE0_HSRX_PON	R	<p>oa_lane0_hsrx_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
10	OA_LANE0_HSRX_CPHY_ALP_DET_LEFT_PON	R	<p>oa_lane0_hsrx_cphy_alp_det_left_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
9	OA_LANE0_HSRX_CPHY_ALP_DETECT_RIGHT_PON	R	<p>oa_lane0_hsrx_cphy_alp_det_right_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
8	OA_LANE0_HSRX_VCM_DET_OUTPUT_EN	R	<p>oa_lane0_hsrx_vcm_det_out_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7	OA_LANE0_HSRX_VCM_DET_PON	R	<p>oa_lane0_hsrx_vcm_det_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
6	OA_LANE0_HSRX_OFFCAL_OBS_EN	R	<p>oa_lane0_hsrx_offcal_obs_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
5	OA_LANE0_HSRX_DESERIALIZE_R_DIV_EN	R	<p>oa_lane0_hsrx_deserializer_div_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
4	OA_LANE0_HSRX_DESERIALIZE_R_DATA_EN	R	<p>oa_lane0_hsrx_deserializer_data_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	OA_LANE0_HSRX_DESERIALIZE_R_EN	R	<p>oa_lane0_hsrx_deserializer_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
2	OA_LANE0_HSRX_HS_CLK_DIV_EN	R	<p>oa_lane0_hsrx_hs_clk_div_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	OA_LANE0_HSRX_TERM_LEFT_EN	R	<p>oa_lane0_hsrx_term_left_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	OA_LANE0_HSRX_TERM_RIGHT_EN	R	<p>oa_lane0_hsrx_term_right_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_3\_13**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x103d

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
8:5	OA_LANE0_HSRX_DPHY_DATA_DELAY	R	<p>oa_lane0_hsrx_dphy_data_delay multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
4	OA_LANE0_HSRX_DPHY_PREAMBLE_CAL_EN	R	<p>oa_lane0_hsrx_dphy_preamble_cal_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
3	OA_LANE0_HSRX_DPHY_DLL_E_N	R	<p>oa_lane0_hsrx_dphy_dll_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	OA_LANE0_HSRX_DPHY_DDL_P HASE_CHANGE	R	<p>oa_lane0_hsrx_dphy_ddl_phase_change multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	OA_LANE0_HSRX_DPHY_DDL_B YPASS_EN	R	<p>oa_lane0_hsrx_dphy_ddl_bypass_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	OA_LANE0_HSRX_DPHY_DDL_B IAS_BYPASS_EN	R	<p>oa_lane0_hsrx_dphy_ddl_bias_bypass_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_3\_14**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x103e

Bits	Name	Memory Access	Description
15:10	OA_LANE0_HSRX_DPHY_DLL_F_BK	R	<p>oa_lane0_hsrx_dphy_dll_fbk multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3f</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
9:8	OA_LANE0_HSRX_DPHY_DDL_TUNE_MODE	R	<p>oa_lane0_hsrx_dphy_ddl_tune_mode multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
7:4	OA_LANE0_HSRX_DPHY_DDL_COARSE_BANK	R	<p>oa_lane0_hsrx_dphy_ddl_coarse_bank multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
3:0	OA_LANE0_HSRX_DPHY_DDL_BIAS	R	<p>oa_lane0_hsrx_dphy_ddl_bias multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE0\_CTRL\_3\_15**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x103f

Bits	Name	Memory Access	Description
15:8	OA_LANE0_HSRX_OFFCAL_LEFT	R	<p>oa_lane0_hsrx_offcal_left multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:0	OA_LANE0_HSRX_OFFCAL_RIGHT	R	<p>oa_lane0_hsrx_offcal_right multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE0\_CTRL\_4\_0**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x1040

Bits	Name	Memory Access	Description
15:8	OA_LANE0_HSRX_DPHY_DDL_P HASE_MID	R	<p>oa_lane0_hsrx_dphy_ddl_phase_mid (bits [7:0]) multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:0	OA_LANE0_HSRX_DPHY_DDL_P HASE_RIGHT	R	<p>oa_lane0_hsrx_dphy_ddl_phase_right (bits [7:0]) multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_4\_1**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x1041

Bits	Name	Memory Access	Description
15	OA_LANE0_LVDS_OFFSET_EN	R	<p>oa_lane0_lvds_offset_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
14	OA_LANE0_LVDS_HYST_EN	R	<p>oa_lane0_lvds_hyst_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
13:11	OA_LANE0_HSRX_MODE	R	<p>oa_lane0_hsrx_mode multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
10	OA_LANE0_HSRX_DPHY_DDL_P HASE_RIGHT	R	<p>oa_lane0_hsrx_dphy_ddl_phase_right (bit [8]) multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	OA_LANE0_HSRX_DPHY_DDL_P HASE_MID	R	<p>oa_lane0_hsrx_dphy_ddl_phase_mid (bit [8]) multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
8:0	OA_LANE0_HSRX_DPHY_DDL_P HASE_LEFT	R	<p>oa_lane0_hsrx_dphy_ddl_phase_left multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1ff   <b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_4\_2**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x1042

Bits	Name	Memory Access	Description
15:8	IA_LANE0_HSRX_DATA_BC_MID _INT	R	<p>ia_lane0_hsrx_data_bc_mid multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:0	IA_LANE0_HSRX_DATA_AB_LEFT _INT	R	<p>ia_lane0_hsrx_data_ab_left multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_4\_3**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x1043

Bits	Name	Memory Access	Description
15	IA_LANE0_HSRX_OUT_CAL_RIGHT_P_INT	R	<p>ia_lane0_hsrx_out_cal_right_p multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
14	IA_LANE0_HSRX_OUT_CAL_RIGHT_N_INT	R	<p>ia_lane0_hsrx_out_cal_right_n multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
13	IA_LANE0_HSRX_OUT_CAL_LEFT_P_INT	R	<p>ia_lane0_hsrx_out_cal_left_p multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	IA_LANE0_HSRX_OUT_CAL_LEFT_N_INT	R	<p>ia_lane0_hsrx_out_cal_left_n multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11	IA_LANE0_HSRX_VCM_DET_OUTPUT_INT	R	<p>ia_lane0_hsrx_vcm_det_out multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	IA_LANE0_HSTX_WORD_CLK_IN_T	R	<p>ia_lane0_hstx_word_clk multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	IA_LANE0_HSRX_HS_CLK_DIV_OUT_INT	R	<p>ia_lane0_hsrx_hs_clk_div_out multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
8	IA_LANE0_HSRX_WORD_CLK_INT	R	<p>ia_lane0_hsrx_word_clk multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7:0	IA_LANE0_HSRX_DATA_CA_RIGHT_INT	R	<p>ia_lane0_hsrx_data_ca_right multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE0\_CTRL\_4\_4**

- **Description:** Analog macro lane 0 observability
- **Size:** 16 bits
- **Offset:** 0x1044

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13:12	IA_LANE0_GPI_OUT	R	<p>ia_lane0_gpi_out[0] multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
11:10	IA_LANE0_SPARE_OUT_INT	R	<p>ia_lane0_spare_out multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
9:8	IA_LANE0_LPRX_DOUTULP_INT	R	<p>ia_lane0_lprx_doutulp multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
7:6	IA_LANE0_LPRX_DOUTLP_INT	R	<p>ia_lane0_lprx_doutlp multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
5:4	IA_LANE0_LPRX_DOUTCD_INT	R	<p>ia_lane0_lprx_doutcd multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
3	IA_LANE0_HSRX_CPHY_CDR_OSC_CLK_INT	R	<p>ia_lane0_hsrx_cphy_cdr_osc_clk multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	IA_LANE0_HSRX_CPHY_ALP_DET_RIGHT_OUT_INT	R	<p>ia_lane0_hsrx_cphy_alp_det_right_out multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	IA_LANE0_HSRX_CPHY_ALP_DET_LEFT_OUT_INT	R	<p>ia_lane0_hsrx_cphy_alp_det_left_out multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	IA_LANE0_HSRX_DPHY_DDL_OSC_CLK_INT	R	<p>ia_lane0_hsrx_dphy_ddl_osc_clk multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_CPHY\_PPI\_LANE0\_OVR\_5\_0**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1050

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	O_ERRSOTHS_C0	R	<p>o_errsoths_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	O_ERRCONTENTIONLP1_C0	R	<p>o_errcontentionlp1_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11	O_ERRCONTENTIONLP0_C0	R	<p>o_errcontentionlp0_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	O_ERRCONTROL_C0	R	<p>o_errcontrol_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	O_ERRSYNCESC_C0	R	<p>o_errsyncesc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
8	O_ERRESC_C0	R	<p>o_erresc_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
7	I_FORCETXSTOPMODE_C0_INT	R	i_forcetxstopmode_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
6	I_FORCERXMODE_C0_INT	R	i_forcerxmode_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
5	O_DIRECTION_C0	R	o_direction_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
4	I_TURNDISABLE_C0_INT	R	i_turndisable_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	I_TURNREQUEST_C0_INT	R	i_turnrequest_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	O_ULPSACTIVENOT_C0	R	o_ulpsactivenot_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	O_STOPSTATE_C0	R	o_stopstate_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

Bits	Name	Memory Access	Description
0	I_ENABLE_C0_INT	R	i_enable_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_R\_CPHY\_PPI\_LANE0\_OVR\_5\_1**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1051

Bits	Name	Memory Access	Description
15:0	O_RXDATAHS_C0	R	o_rxdatahs_c0 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_RW\_CPHY\_PPI\_LANE0\_OVR\_5\_2**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1052

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:10	I_ALPWAKESTATE_C0_OVR_VAL	R/W	i_alpwakestate_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
9:6	I_TXALPNIBBLE_C0_OVR_VAL	R/W	i_txalpnibble_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

Bits	Name	Memory Access	Description
5:2	I_TXALPCODE_C0_OVR_VAL	R/W	i_txalpcode_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
1:0	I_TXSENDALPHS_C0_OVR_VAL	R/W	i_txsendalphs_c0 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE0\_OVR\_5\_3**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1053

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
3	I_ALPWAKESTATE_C0_OVR_EN	R/W	i_alpwakestate_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	I_TXALPNIBBLE_C0_OVR_EN	R/W	i_txalpnibble_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	I_TXALPCODE_C0_OVR_EN	R/W	i_txalpcode_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXSENDALPHS_C0_OVR_EN	R/W	i_txsendalphs_c0 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE0\_OVR\_5\_4**

- **Description:** Digital hard macro interface observability

- **Size:** 16 bits
- **Offset:** 0x1054

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12:10	I_ALPWAKESTATE_C0_INT	R	<p>i_alpwakestate_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>
9:6	I_TXALPNIBBLE_C0_INT	R	<p>i_txalpnibble_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
5:2	I_TXALPCODE_C0_INT	R	<p>i_txalpcode_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
1:0	I_TXSENDALPHS_C0_INT	R	<p>i_txsendalphs_c0 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

## CORE\_DIG\_RW\_TRI00\_0

- **Description:** Configurations for Trio 0
- **Size:** 16 bits
- **Offset:** 0x1080

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11:9	POST_RECEIVED_RESET_THRESH	R/W	Counter for resetting the post detected flag. In word_clk cycles. Quasi static. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
8:6	DESERIALIZER_DIV_EN_DELAY_DEASS_THRESH	R/W	Counter for deassertion of deserializer_div_en after deassertion of deserializer_data_en. In dco_clk cycles. Quasi Static. 0 is a forbidden value. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
5:3	DESERIALIZER_DIV_EN_DELAY_THRESH	R/W	Counter for deserializer_div_en delay. In dco_clk cycles. Quasi static. 0 is a forbidden value. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
2:0	DESERIALIZER_DATA_EN_DELAY_THRESH	R/W	Counter for deserializer_data_en delay. In dco_clk cycles. Quasi static. 0 is a forbidden value. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

### CORE\_DIG\_RW\_TRI00\_1

- **Description:** Configurations for Trio 0
- **Size:** 16 bits
- **Offset:** 0x1081

Bits	Name	Memory Access	Description
15:0	POST_DET_DELAY_THRESH	R/W	Counter for deassertion of deserializer_data_en after Post2 reception. In dco_clk cycles. Quasi static. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

### CORE\_DIG\_RW\_TRI00\_2

- **Description:** Configurations for Trio 0
- **Size:** 16 bits
- **Offset:** 0x1082

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	DESERIALIZER_EN_DELAY_DEASS_THRESH	R/W	Counter for deassertion of deserializer_en after deassertion of deserializer_data_en. In dco_clk cycles. Quasi Static. 0 is a forbidden value. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_ICTRL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_0**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1200

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_RXALTERNATECALHS_D1_OVR_VAL	R/W	o_rxalternatecalhs_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12:5	O_RXDATAHS_D1_OVR_VAL	R/W	o_rxdatahs_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
4	O_RXWORDCLKHS_D1_OVR_VAL	R/W	o_rxwordclkhs_d1_override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	O_RXSKEWCALHS_D1_OVR_VAL	R/W	o_rxskewcalhs_d1_override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
2	O_RXVALIDHS_D1_OVR_VAL	R/W	<p><b>o_rxvalidhs_d1_</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXSYNCHS_D1_OVR_VAL	R/W	<p><b>o_rxsynchs_d1_</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXACTIVEHS_D1_OVR_VAL	R/W	<p><b>o_rxactivehs_d1_</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_1**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1201

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
11	O_RXALTERNATECALHS_D1_OVR_EN	R/W	<p><b>o_rxalternatecalhs_d1</b> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	I_TXDATAHS_D1_OVR_EN	R/W	<p><b>i_txdatahs_d1</b> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	O_TXWORDCLKHS_D1_OVR_EN	R/W	<p><b>o_txwordclkhs_d1</b> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
8	O_TXREADYHS_D1_OVR_EN	R/W	<p><code>o_txreadyhs_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_TXDATATRANSFERENHS_D1_OVR_EN	R/W	<p><code>i_txdatatransferenhs_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_TXREQUESTHS_D1_OVR_EN	R/W	<p><code>i_txrequesths_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_RXDATAHS_D1_OVR_EN	R/W	<p><code>o_rxdatahs_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	O_RXWORDCLKHS_D1_OVR_EN	R/W	<p><code>o_rxwordclkhs_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	O_RXSKEWCALHS_D1_OVR_EN	R/W	<p><code>o_rxskewcalhs_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXVALIDHS_D1_OVR_EN	R/W	<p><code>o_rxvalidhs_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXSYNCHS_D1_OVR_EN	R/W	<p><code>o_rxsynchs_d1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	O_RXACTIVEHS_D1_OVR_EN	R/W	<p>o_rxactivehs_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCRTL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_2**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1202

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0X</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	I_TXSKEWCALHS_D1_OVR_VAL	R/W	<p>i_txskewcalhs_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:4	I_TXDATAHS_D1_OVR_VAL	R/W	<p>i_txdatahs_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
3	O_TXWORDCLKHS_D1_OVR_VAL	R/W	<p>o_txwordclkhs_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_TXREADYHS_D1_OVR_VAL	R/W	<p>o_txreadyhs_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	I_TXDATATRANSFERENHS_D1_OVR_VAL	R/W	<p>i_txdatatransferenhs_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	I_TXREQUESTHS_D1_OVR_VAL	R/W	<p>i_txrequesths_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCRTL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_3**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1203

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0X0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	I_TXSKEWCALHS_D1_OVR_EN	R/W	<p>i_txskewcalhs_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	I_TXALTERNATECALHS_D1_OVR_EN	R/W	<p>i_txalternatecalhs_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	I_TXDATAESC_D1_OVR_EN	R/W	<p>i_txdataesc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9:6	I_TXTRIGGERESC_D1_OVR_VAL	R/W	<p>i_txtriggeresc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
5	O_TXREADYESC_D1_OVR_VAL	R/W	<p>o_txreadyesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TXVALIDDESC_D1_OVR_VAL	R/W	<p>i_txvaliddesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TXULPSESC_D1_OVR_VAL	R/W	<p>i_txulpsesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
2	I_TXULPSEXIT_D1_OVR_VAL	R/W	i_txulpsexit_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	I_TXLPDTESC_D1_OVR_VAL	R/W	i_txlpdtesc_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXREQUESTESC_D1_OVR_VAL	R/W	i_txrequestesc_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_4**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1204

Bits	Name	Memory Access	Description
15	I_TXALTERNATECALHS_D1_OVR_VAL	R/W	i_txalternatecalhs_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14:7	I_TXDATAESC_D1_OVR_VAL	R/W	i_txdataesc_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
6	I_TXTRIGGERESC_D1_OVR_EN	R/W	i_txtriggeresc_d1override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	O_TXREADYESC_D1_OVR_EN	R/W	o_txreadyesc_d1override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
4	I_TXVALIDDESC_D1_OVR_EN	R/W	i_txvaliddesc_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	I_TXULPSESC_D1_OVR_EN	R/W	i_txulpsesc_d1override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	I_TXULPSEXIT_D1_OVR_EN	R/W	i_txulpsexit_d1override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	I_TXLPDTESC_D1_OVR_EN	R/W	i_txlpdtesc_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXREQUESTESC_D1_OVR_EN	R/W	i_txrequestesc_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_5**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1205

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_D1_OVR_VAL	R/W	o_rxdataesc_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:4	O_RXTRIGGERESC_D1_OVR_VAL	R/W	o_rxtriggeresc_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

Bits	Name	Memory Access	Description
3	O_RXVALIDDESC_D1_OVR_VAL	R/W	<p>o_rxvaliddesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXULPSESC_D1_OVR_VAL	R/W	<p>o_rxulpsesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXLPDTESC_D1_OVR_VAL	R/W	<p>o_rxlpdtesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_D1_OVR_VAL	R/W	<p>o_rxclkesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCtrl\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_6**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1206

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0X</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
5	O_RXDATAESC_D1_OVR_EN	R/W	<p>o_rxdataesc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	O_RXTRIGGERESC_D1_OVR_E_N	R/W	<p>o_rxtriggeresc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
3	O_RXVALIDDESC_D1_OVR_EN	R/W	<p>o_rxvaliddesc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXULPSESC_D1_OVR_EN	R/W	<p>o_rxulpsesc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXLPDTESC_D1_OVR_EN	R/W	<p>o_rxlpdtesc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_D1_OVR_EN	R/W	<p>o_rxclkesc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_7**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1207

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	O_ERRSOTSYNCHS_D1_OVR_VAL	R/W	<p>o_errsotsynchs_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	O_ERRSOTHS_D1_OVR_VAL	R/W	<p>o_errsoths_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
12	O_ERRCONTENTIONLP1_D1_OVR_VAL	R/W	<p>o_errcontentionlp1_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	O_ERRCONTENTIONLP0_D1_OVR_VAL	R/W	<p>o_errcontentionlp0_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	O_ERRCONTROL_D1_OVR_VAL	R/W	<p>o_errcontrol_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	O_ERRSYNCESC_D1_OVR_VAL	R/W	<p>o_errsyncesc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_ERRESC_D1_OVR_VAL	R/W	<p>o_erresc_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCE_TXSTOPMODE_D1_OVR_VAL	R/W	<p>i_forcetxstopmode_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCE_RXMODE_D1_OVR_VAL	R/W	<p>i_forcerxmode_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_D1_OVR_VAL	R/W	<p>o_direction_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TURNDISABLE_D1_OVR_VAL	R/W	<p>i_turndisable_d1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
3	I_TURNREQUEST_D1_OVR_VAL	R/W	i_turnrequest_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	O_ULPSACTIVENOT_D1_OVR_VAL	R/W	o_ulpsactivenot_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	O_STOPSTATE_D1_OVR_VAL	R/W	o_stopstate_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_ENABLE_D1_OVR_VAL	R/W	i_enable_d1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG IOCTL\_RW\_DPHY\_PPI\_LANE1\_OVR\_0\_8**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1208

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14	O_ERRSOTSYNCHS_D1_OVR_EN	R/W	o_errsotsynchs_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13	O_ERRSOTHs_D1_OVR_EN	R/W	o_errsoths_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
12	O_ERRCONTENTIONLP1_D1_OVR_EN	R/W	<p>o_errcontentionlp1_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	O_ERRCONTENTIONLP0_D1_OVR_EN	R/W	<p>o_errcontentionlp0_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	O_ERRCONTROL_D1_OVR_EN	R/W	<p>o_errcontrol_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	O_ERRSYNCESC_D1_OVR_EN	R/W	<p>o_errsyncesc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_ERRESC_D1_OVR_EN	R/W	<p>o_erresc_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCETXSTOPMODE_D1_OVR_EN	R/W	<p>i_forcetxstopmode_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCERXMODE_D1_OVR_EN	R/W	<p>i_forcerxmode_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_D1_OVR_EN	R/W	<p>o_direction_d1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4	I_TURNDISABLE_D1_OVR_EN	R/W	i_turndisable_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	I_TURNREQUEST_D1_OVR_EN	R/W	i_turnrequest_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	O_ULPSACTIVENOT_D1_OVR_EN	R/W	o_ulpsactivenot_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	O_STOPSTATE_D1_OVR_EN	R/W	o_stopstate_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_ENABLE_D1_OVR_EN	R/W	i_enable_d1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE1\_OVR\_0\_9**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1209

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_RXALTERNATECALHS_D1	R	o_rxalternatecalhs_d1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

Bits	Name	Memory Access	Description
12:5	O_RXDATAHS_D1	R	<p>o_rxdatahs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
4	O_RXWORDCLKHS_D1	R	<p>o_rxwordclkhs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	O_RXSKEWCALHS_D1	R	<p>o_rxskewcalhs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXVALIDHS_D1	R	<p>o_rxvalidhs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXSYNCHS_D1	R	<p>o_rxsynchs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXACTIVEHS_D1	R	<p>o_rxactivehs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_DPHY\_PPI\_LANE1\_OVR\_0\_10**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x120a

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	I_TXSKEWCALHS_D1_INT	R	<p>i_txskewcalhs_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	I_TXALTERNATECALHS_D1_INT	R	<p>i_txalternatecalhs_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11:4	I_TXDATAHS_D1_INT	R	<p>i_txdatahs_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
3	O_TXWORDCLKHS_D1	R	<p>o_txwordclkhs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_TXREADYHS_D1	R	<p>o_txreadyhs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	I_TXDATATRANSFERENHS_D1_INT	R	<p>i_txdatatransferenhs_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
0	I_TXREQUESTHS_D1_INT	R	<p>i_txrequesths_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE1\_OVR\_0\_11**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x120b

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
9:6	I_TXTRIGGERESC_D1_INT	R	<p>i_txtriggeresc_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
5	O_TXREADYESC_D1	R	<p>o_txreadyesc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
4	I_TXVALIDDESC_D1_INT	R	<p>i_txvaliddesc_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	I_TXULPSESC_D1_INT	R	<p>i_txulpsesc_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
2	I_TXULPSEXIT_D1_INT	R	i_txulpsexit_d1_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	I_TXLPDTESC_D1_INT	R	i_txlpdtesc_d1_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	I_TXREQUESTESC_D1_INT	R	i_txrequestesc_d1_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE1\_OVR\_0\_12**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x120c

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	I_TXDATAESC_D1_INT	R	i_txdataesc_d1_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_LANE1\_OVR\_0\_13**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x120d

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_D1	R	<p>o_rxdataesc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:4	O_RXTRIGGERESC_D1	R	<p>o_rxtriggeresc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
3	O_RXVALIDDESC_D1	R	<p>o_rxvaliddesc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXULPSESC_D1	R	<p>o_rxulpsesc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXLPDTESC_D1	R	<p>o_rxlpdtesc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXCLKESC_D1	R	<p>o_rxclkesc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_DPHY\_PPI\_LANE1\_OVR\_0\_14**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x120e

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	O_ERRSOTSYNCHS_D1	R	<p>o_errsotsynchs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
13	O_ERRSOTHs_D1	R	<p>o_errsoths_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	O_ERRCONTENTIONLP1_D1	R	<p>o_errcontentionlp1_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11	O_ERRCONTENTIONLP0_D1	R	<p>o_errcontentionlp0_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	O_ERRCONTROL_D1	R	<p>o_errcontrol_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	O_ERRSYNCESC_D1	R	<p>o_errsyncesc_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
8	O_ERRESC_D1	R	<p><code>o_erresc_d1</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7	I_FORCETXSTOPMODE_D1_INT	R	<p><code>i_forcetxstopmode_d1_int</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
6	I_FORCERXMODE_D1_INT	R	<p><code>i_forcerxmode_d1_int</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
5	O_DIRECTION_D1	R	<p><code>o_direction_d1</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
4	I_TURNDISABLE_D1_INT	R	<p><code>i_turndisable_d1_int</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	I_TURNREQUEST_D1_INT	R	<p><code>i_turnrequest_d1_int</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_ULPSACTIVENOT_D1	R	<p><code>o_ulpsactivenot_d1</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
1	O_STOPSTATE_D1	R	<p>o_stopstate_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	I_ENABLE_D1_INT	R	<p>i_enable_d1_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG IOCTL\_R\_DPHY\_PPI\_LANE1\_OVR\_0\_15**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x120f

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12:5	O_RXDATAHS_D1	R	<p>o_rxdatahs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
4	O_RXWORDCLKHS_D1	R	<p>o_rxwordclkhs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	O_RXSKEWCALHS_D1	R	<p>o_rxskewcalhs_d1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
2	O_RXVALIDHS_D1	R	<p><code>o_rxvalidhs_d1</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXSYNCHS_D1	R	<p><code>o_rxsynchs_d1</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXACTIVEHS_D1	R	<p><code>o_rxactivehs_d1</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_0**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1210

Bits	Name	Memory Access	Description
15:0	O_RXDATAHS_C1_OVR_VAL	R/W	<p><code>o_rxdatahs_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_1**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1211

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

Bits	Name	Memory Access	Description
13	O_RXALPNIBBLE_C1_OVR_EN	R/W	<p>o_rxalpnibble_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12:9	O_RXALPCODE_C1_OVR_VAL	R/W	<p>o_rxalpcode_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
8	O_RXALPVALIDHS_C1_OVR_EN	R/W	<p>o_rxalpvalidhs_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:5	O_RXSYNCTYPEHS_C1_OVR_VAL	R/W	<p>o_rxsynctypehs_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
4	O_RXWORDCLKHS_C1_OVR_VAL	R/W	<p>o_rxwordclkhs_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	O_RXINVALIDCODEHS_C1_OVR_VAL	R/W	<p>o_rxinvalidcodehs_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXVALIDHS_C1_OVR_VAL	R/W	<p>o_rxvalidhs_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXSYNCHS_C1_OVR_VAL	R/W	<p>o_rxsynchs_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXACTIVEHS_C1_OVR_VAL	R/W	<p>o_rxactivehs_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_2**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits

## ■ Offset: 0x1212

Bits	Name	Memory Access	Description
15:13	I_TXSYNCTYPEHS_C1_OVR_VA L	R/W	i_txsynctypehs_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
12	O_RXALPCODE_C1_OVR_EN	R/W	o_rxalpcode_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11:8	O_RXALPNIBBLE_C1_OVR_VAL	R/W	o_rxalpnibble_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7	O_RXALPVALIDHS_C1_OVR_VA L	R/W	o_rxalpvalidhs_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	O_RXDATAHS_C1_OVR_EN	R/W	o_rxdatahs_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	O_RXSYNCTYPEHS_C1_OVR_E N	R/W	o_rxsynctypehs_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	O_RXWORDCLKHS_C1_OVR_EN	R/W	o_rxwordclkhs_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	O_RXINVALIDCODEHS_C1_OVR _EN	R/W	o_rxinvalidcodehs_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
2	O_RXVALIDHS_C1_OVR_EN	R/W	<p><code>o_rxvalidhs_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXSYNCHS_C1_OVR_EN	R/W	<p><code>o_rxsynchs_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXACTIVEHS_C1_OVR_EN	R/W	<p><code>o_rxactivehs_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_3**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1213

Bits	Name	Memory Access	Description
15:0	I_TXDATAHS_C1_OVR_VAL	R/W	<p><code>i_txdatahs_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_4**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1214

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

Bits	Name	Memory Access	Description
14	O_TXWORDCLKHS_C1_OVR_VAL	R/W	<p><code>o_txwordclkhs_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	O_TXREADYHS_C1_OVR_VAL	R/W	<p><code>o_txreadyhs_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	I_TXDATATRANSFERNHS_C1_OVR_VAL	R/W	<p><code>i_txdatatransfernhs_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	I_TXREQUESTHS_C1_OVR_VAL	R/W	<p><code>i_txrequesths_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	I_TXDATAESC_C1_OVR_EN	R/W	<p><code>i_txdataesc_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9:6	I_TXTRIGGERESC_C1_OVR_VAL	R/W	<p><code>i_txtriggeresc_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
5	O_TXREADYESC_C1_OVR_VAL	R/W	<p><code>o_txreadyesc_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TXVALIDDESC_C1_OVR_VAL	R/W	<p><code>i_txvaliddesc_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TXULPSESC_C1_OVR_VAL	R/W	<p><code>i_txulpsesc_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	I_TXULPSEXIT_C1_OVR_VAL	R/W	<p><code>i_txulpsexit_c1</code> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
1	I_TXLPDTESC_C1_OVR_VAL	R/W	i_txlpdtesc_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

0	I_TXREQUESTESC_C1_OVR_VAL	R/W	i_txrequestesc_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG\_ICTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_5**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1215

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:7	I_TXDATAESC_C1_OVR_VAL	R/W	i_txdataesc_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
6	I_TXTRIGGERESC_C1_OVR_EN	R/W	i_txtriggeresc_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	O_TXREADYESC_C1_OVR_EN	R/W	o_txreadyesc_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	I_TXVALIDDESC_C1_OVR_EN	R/W	i_txvaliddesc_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
3	I_TXULPSESC_C1_OVR_EN	R/W	i_txulpsesc_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	I_TXULPSEXIT_C1_OVR_EN	R/W	i_txulpsexit_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	I_TXLPDTESC_C1_OVR_EN	R/W	i_txlpdtesc_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXREQUESTESC_C1_OVR_EN	R/W	i_txrequestesc_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_6**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1216

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_C1_OVR_VAL	R/W	o_rxdataesc_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:4	O_RXTRIGGERESC_C1_OVR_VAL	R/W	o_rxtriggeresc_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3	O_RXVALIDDESC_C1_OVR_VAL	R/W	o_rxvaliddesc_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
2	O_RXULPSESC_C1_OVR_VAL	R/W	<p><i>o_rxulpsesc_c1</i> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_RXLPDTESC_C1_OVR_VAL	R/W	<p><i>o_rxlpdtesc_c1</i> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_C1_OVR_VAL	R/W	<p><i>o_rxclkesc_c1</i> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_7**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1217

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	I_TXSYNCTYPEHS_C1_OVR_EN	R/W	<p><i>i_txsynctypehs_c1</i> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	I_TXSENDSYNCHS_C1_OVR_EN	R/W	<p><i>i_txsendsynchs_c1</i> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	I_TXDATAHS_C1_OVR_EN	R/W	<p><i>i_txdatahs_c1</i> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
9	O_TXWORDCLKHS_C1_OVR_EN	R/W	<p>o_txwordclkhs_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_TXREADYHS_C1_OVR_EN	R/W	<p>o_txreadyhs_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_TXDATATRANSFERENHS_C1_OVR_EN	R/W	<p>i_txdatatransferenhs_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_TXREQUESTHS_C1_OVR_EN	R/W	<p>i_txrequesths_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_RXDATAESC_C1_OVR_EN	R/W	<p>o_rxdataesc_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	O_RXTRIGGERESC_C1_OVR_E N	R/W	<p>o_rxtriggeresc_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	O_RXVALIDDESC_C1_OVR_EN	R/W	<p>o_rxvaliddesc_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_RXULPSESC_C1_OVR_EN	R/W	<p>o_rxulpsesc_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
1	O_RXLPDTESC_C1_OVR_EN	R/W	<p>o_rxlpdtesc_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	O_RXCLKESC_C1_OVR_EN	R/W	<p>o_rxclkesc_c1 override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_8**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1218

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	I_TXSENDSYNCHS_C1_OVR_VAL	R/W	<p>i_txsendsynchs_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	O_ERRSOTHS_C1_OVR_VAL	R/W	<p>o_errsoths_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	O_ERRCONTENTIONLP1_C1_OVR_VAL	R/W	<p>o_errcontentionlp1_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	O_ERRCONTENTIONLP0_C1_OVR_VAL	R/W	<p>o_errcontentionlp0_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
10	O_ERRCONTROL_C1_OVR_VAL	R/W	<p>o_errcontrol_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	O_ERRSYNCESC_C1_OVR_VAL	R/W	<p>o_errsyncesc_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	O_ERRESC_C1_OVR_VAL	R/W	<p>o_erresc_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCECTXSTOPMODE_C1_OVR_VAL	R/W	<p>i_forcetxstopmode_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCECRXMODE_C1_OVR_VAL	R/W	<p>i_forcerxmode_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_C1_OVR_VAL	R/W	<p>o_direction_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TURNDISABLE_C1_OVR_VAL	R/W	<p>i_turndisable_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TURNREQUEST_C1_OVR_VAL	R/W	<p>i_turnrequest_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_ULPSACTIVENOT_C1_OVR_VAL	R/W	<p>o_ulpsactivenot_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_STOPSTATE_C1_OVR_VAL	R/W	<p>o_stopstate_c1 override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	I_ENABLE_C1_OVR_VAL	R/W	i_enable_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG IOCTL\_RW\_CPHY\_PPI\_LANE1\_OVR\_1\_9**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1219

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_ERRSOTHS_C1_OVR_EN	R/W	o_errsoths_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	O_ERRCONTENTIONLP1_C1_OVR_EN	R/W	o_errcontentionlp1_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	O_ERRCONTENTIONLP0_C1_OVR_EN	R/W	o_errcontentionlp0_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	O_ERRCONTROL_C1_OVR_EN	R/W	o_errcontrol_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	O_ERRSYNCESC_C1_OVR_EN	R/W	o_errsyncesc_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
8	O_ERRESC_C1_OVR_EN	R/W	<p><code>o_erresc_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	I_FORCETXSTOPMODE_C1_OVR_EN	R/W	<p><code>i_forcetxstopmode_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	I_FORCERXMODE_C1_OVR_EN	R/W	<p><code>i_forcerxmode_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	O_DIRECTION_C1_OVR_EN	R/W	<p><code>o_direction_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_TURNDISABLE_C1_OVR_EN	R/W	<p><code>i_turndisable_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_TURNREQUEST_C1_OVR_EN	R/W	<p><code>i_turnrequest_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_ULPSACTIVENOT_C1_OVR_EN	R/W	<p><code>o_ulpsactivenot_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	O_STOPSTATE_C1_OVR_EN	R/W	<p><code>o_stopstate_c1</code> override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	I_ENABLE_C1_OVR_EN	R/W	i_enable_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE1\_OVR\_1\_10**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x121a

Bits	Name	Memory Access	Description
15:0	O_RXDATAHS_C1	R	o_rxdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE1\_OVR\_1\_11**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x121b

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:12	I_TXSYNCTYPEHS_C1_INT	R	i_txsynctypehs_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7 <b>Volatile:</b> true

Bits	Name	Memory Access	Description
11:8	O_RXALPCODE_C1	R	<p>o_rxalpcode_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
7:5	O_RXSYNCTYPEHS_C1	R	<p>o_rxsynctypehs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>
4	O_RXWORDCLKHS_C1	R	<p>o_rxwordclkhs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3	O_RXINVALIDCODEHS_C1	R	<p>o_rxinvalidcodehs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXVALIDHS_C1	R	<p>o_rxvalidhs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXSYNCHS_C1	R	<p>o_rxsynchs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXACTIVEHS_C1	R	<p>o_rxactivehs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_ICTRL\_R\_CPHY\_PPI\_LANE1\_OVR\_1\_12**

- **Description:** Digital hard macro interface observability

- **Size:** 16 bits
- **Offset:** 0x121c

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	I_TXSENDSYNCHS_C1_INT	R	<p>i_txsendsynchs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12:5	I_TXDATAESC_C1_INT	R	<p>i_txdataesc_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
4:1	O_RXALPNIBBLE_C1	R	<p>o_rxalpnibble_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
0	O_RXALPVALIDHS_C1	R	<p>o_rxalpvalidhs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

### CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE1\_OVR\_1\_13

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x121d

Bits	Name	Memory Access	Description

15:0	I_TXDATAHS_C1_INT	R	i_txdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true
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**CORE\_DIG\_IOCRTL\_R\_CPHY\_PPI\_LANE1\_OVR\_1\_14**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x121e

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_TXWORDCLKHS_C1	R	o_txwordclkhs_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
12	O_TXREADYHS_C1	R	o_txreadyhs_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

11	I_TXDATATRANSFERENHS_C1_INT	R	i_txdatatransferenhs_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
10	I_TXREQUESTHS_C1_INT	R	i_txrequesths_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

9:6	I_TXTRIGGERESC_C1_INT	R	i_txtriggeresc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true
5	O_TXREADYESC_C1	R	o_txreadyesc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
4	I_TXVALIDESC_C1_INT	R	i_txvalidesc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	I_TXULPSESC_C1_INT	R	i_txulpsesc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	I_TXULPSEXIT_C1_INT	R	i_txulpsexit_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	I_TXLPDTESC_C1_INT	R	i_txlpdtesc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	I_TXREQUESTESC_C1_INT	R	i_txrequestesc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE1\_OVR\_1\_15**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits

- **Offset:** 0x121f

Bits	Name	Memory Access	Description
15:8	O_RXDATAESC_C1	R	<p>o_rxdataesc_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:4	O_RXTRIGGERESC_C1	R	<p>o_rxtriggeresc_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
3	O_RXVALIDDESC_C1	R	<p>o_rxvaliddesc_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
2	O_RXULPSESC_C1	R	<p>o_rxulpsesc_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
1	O_RXLPDTESC_C1	R	<p>o_rxlpdtesc_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	O_RXCLKESC_C1	R	<p>o_rxclkesc_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

#### CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_0

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1220

Bits	Name	Memory Access	Description
15	OA_LANE1_SHORT_LB_EN	R/W	oa_lane1_short_lb_en bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	I_LANE1_GPIO_IN_OVR_EN	R/W	i_lane1_gpio_in override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13	OA_LANE1_LVDS_OFFSET_EN_OVR_EN	R/W	oa_lane1_lvds_offset_en override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_LANE1_LVDS_HYST_EN_OVR_EN	R/W	oa_lane1_lvds_hyst_en override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11:0	OA_LANE1_SPARE_IN	R/W	Lane 1 input spare bus (bits [11:0]). This signal is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE1\_CTRL\_2\_1**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1221

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14	OA_LANE1_HSTX_LOWCAP_EN_OVR_EN	R/W	oa_lane1_hstx_lowcap_en override enable. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
13:12	I_LANE1_GPIO_IN_OVR_VAL	R/W	i_lane1_gpio_in_ovr_val override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
11:10	OA_LANE1_GPO_EN	R/W	oa_lane1_gpo_en[0] bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9:8	OA_LANE1_GPI_HYST_EN	R/W	oa_lane1_gpi_hyst_en[0] bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7:6	OA_LANE1_GPI_EN	R/W	oa_lane1_gpi_en[0] bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
5	OA_LANE1_LVDS_OFFSET_EN_OVR_VAL	R/W	oa_lane1_lvds_offset_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE1_LVDS_HYST_EN_OVR_VAL	R/W	oa_lane1_lvds_hyst_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE1_SEL_LVDS_OFF	R/W	oa_lane1_lvds_cmsw_off bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2:1	OA_LANE1_LVDS_CMSW_PROG	R/W	oa_lane1_lvds_cmsw_prog word configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

Bits	Name	Memory Access	Description
0	OA_LANE1_LVDS_EN	R/W	<p>oa_lane1_lvds_en bit configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE1\_CTRL\_2\_2**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1222

Bits	Name	Memory Access	Description
15:7	RESERVED_15_7	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
6	OA_LANE1_HSTX_DIV_EN_OVR_VAL	R/W	<p>oa_lane1_hstx_div_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5:4	OA_LANE1_HSTX_LOWCAP_EN_OVR_VAL	R/W	<p>oa_lane1_hstx_lowcap_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
3	OA_LANE1_HSRX_DPHY_DDL_PON_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_ddl_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	OA_LANE1_HSRX_TERM_EN200_OHMS	R/W	<p>Lane 1 HS-RX termination value. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	OA_LANE1_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_cphy_cdr_fbk_fast_lock_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
0	OA_LANE1_SEL_LANE_CFG	R/W	<p>Lane 1 D-PHY/C-PHY configuration. 1'b0: D-PHY data lane (when phy_mode is 1'b0); C-PHY slave lane (when phy_mode is 1'b1). 1'b1: D-PHY clock lane (when phy_mode is 1'b0); C-PHY master lane (when phy_mode is 1'b1). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE1\_CTRL\_2\_3**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1223

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	OA_LANE1_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_cphy_cdr_fbk_fast_lock_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	OA_LANE1_HSRX_DPHY_DDL_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_ddl_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_LANE1_HSRX_DPHY_DDL_DCC_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_ddl_dcc_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	OA_LANE1_LPTX_DIN_DP_OVR_VAL	R/W	<p>oa_lane1_lptx_din_dp override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
9	OA_LANE1_LPTX_DIN_DN_OVR_VAL	R/W	oa_lane1_lptx_din_dn override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE1_HSTX_SEL_CLKLB	R/W	Lane 1 HS-TX clock source. 1'b0: External PLL clock. 1'b1: Common block internal DCO clock. This signal is quasi-static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:5	OA_LANE1_HSTX_EQA	R/W	Lane 1 HS-TX de-emphasis word (upper-half). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
4	OA_LANE1_HSTX_SEL_PHASE0	R/W	Lane 1 HS-TX clock phase selection. 1'b0: 90 (for D-PHY clock lane configuration), 1'b1: 0 (for both C-PHY and D-PHY data lane configurations). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:2	OA_LANE1_HSTX_BOOST_EN_OVR_VAL	R/W	oa_lane1_hstx_boost_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
1:0	OA_LANE1_HSTX_PON_OVR_VAL	R/W	oa_lane1_hstx_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

**CORE\_DIG\_IOCtrl\_Rw\_AFE\_LANE1\_CTRL\_2\_4**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1224

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

Bits	Name	Memory Access	Description
11	OA_LANE1_HSRX_DPHY_DDL_D CC_EN_OVR_EN	R/W	oa_lane1_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE1_HSTX_TERM_EN_OV R_EN	R/W	oa_lane1_hstx_term_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:8	OA_LANE1_LPTX_SR_BYPASS_EN	R/W	oa_lane1_lptx_sr_bypass_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7	OA_LANE1_LPTX_DIN_DP_OVR_EN	R/W	oa_lane1_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE1_LPTX_DIN_DN_OVR _EN	R/W	oa_lane1_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	OA_LANE1_HSTX_CLK_OBS_EN	R/W	Lane 1 HS clock pattern driven in the lines (debug feature). Active high. This signal is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4:2	OA_LANE1_HSTX_EQB	R/W	Lane 1 HS-TX de-emphasis word (lower-half). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
1	OA_LANE1_HSTX_BOOST_EN_OVR_EN	R/W	oa_lane1_hstx_boost_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
0	OA_LANE1_HSTX_PON_OVR_E_N	R/W	<p>oa_lane1_hstx_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE1\_CTRL\_2\_5**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1225

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0X0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	OA_LANE1_HSRX_DPHY_DDL_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_ddl_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:10	OA_LANE1_HSTX_TERM_EN_OVR_VAL	R/W	<p>oa_lane1_hstx_term_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
9	OA_LANE1_HSTX_DATA_CA_OVR_EN	R/W	<p>oa_lane1_hstx_data_ca override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE1_HSTX_DATA_BC_OVR_EN	R/W	<p>oa_lane1_hstx_data_ca override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:0	OA_LANE1_HSTX_DATA_AB_DPHY_OVR_VAL	R/W	<p>oa_lane1_hstx_data_ab_dphy override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_6**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1226

Bits	Name	Memory Access	Description
15	OA_LANE1_HSRX_DPHY_DDL_PON_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_ddl_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	OA_LANE1_HSTX_DATA_AB_DPHY_OVR_EN	R/W	<p>oa_lane1_hstx_data_ab_dphy override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13:7	OA_LANE1_HSTX_DATA_CA_OVR_VAL	R/W	<p>oa_lane1_hstx_data_ca override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f</p>
6:0	OA_LANE1_HSTX_DATA_BC_OVR_VAL	R/W	<p>oa_lane1_hstx_data_bc override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_7**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1227

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0X0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

Bits	Name	Memory Access	Description
13	OA_LANE1_HSRX_VCM_DET_SYNC_BYPASS	R/W	<p>Enable vcm detector filter bypass which controls CDR input propagation. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12:10	OA_LANE1_HSRX_CPHY_CDR_FBK_CAP_PROG	R/W	<p>Lane 1 C-PHY low-pass filter bandwidth (symbol rate dependent). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x7</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
9	OA_LANE1_HSRX_CPHY_CDR_FBK_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_cphy_cdr_fbk_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE1_LPRX_ULP_PON_OVR_EN	R/W	<p>oa_lane1_lprx_ulp_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	OA_LANE1_LPRX_CD_PON_OVR_EN	R/W	<p>oa_lane1_lprx_cd_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE1_LPRX_LP_PON_OVR_EN	R/W	<p>oa_lane1_lprx_lp_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5:4	OA_LANE1_LPTX_PULLDWN_EN_OVR_VAL	R/W	<p>oa_lane1_lptx_pulldwn_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
3:2	OA_LANE1_LPTX_PON_OVR_VAL	R/W	<p>oa_lane1_lptx_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

Bits	Name	Memory Access	Description
1:0	OA_LANE1_LPTX_EN_OVR_VAL	R/W	<p>oa_lane1_lptx_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

**CORE\_DIG IOCTL\_RW\_AFE\_LANE1\_CTRL\_2\_8**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1228

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12	OA_LANE1_HSRX_CDPHY_SEL_FAST	R/W	<p>Lane 1 HS-RX DDL delay cell strength. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_LANE1_HSRX_CPHY_DELAY_OVR_EN	R/W	<p>oa_lane1_hsrx_cphy_delay override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	OA_LANE1_HSRX_CPHY_MASK_CHANGE_OVR_VAL	R/W	<p>oa_lane1_hsrx_cphy_mask_change override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	OA_LANE1_HSRX_CPHY_CDR_FBK_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_cphy_cdr_fbk_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE1_LPTX_PULLDWN_EN_OVR_EN	R/W	<p>oa_lane1_lptx_pulldwn_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
7	OA_LANE1_LPTX_PON_OVR_EN	R/W	<p>oa_lane1_lptx_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE1_LPTX_EN_OVR_EN	R/W	<p>oa_lane1_lptx_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5:4	OA_LANE1_LPRX_ULP_PON_OVR_VAL	R/W	<p>oa_lane1_lprx_ulp_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
3:2	OA_LANE1_LPRX_CD_PON_OVR_VAL	R/W	<p>oa_lane1_lprx_cd_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
1:0	OA_LANE1_LPRX_LP_PON_OVR_VAL	R/W	<p>oa_lane1_lprx_lp_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_9**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1229

Bits	Name	Memory Access	Description
15:12	OA_LANE1_HSRX_CPHY_DELAY_OVR_VAL	R/W	<p>oa_lane1_hsrx_cphy_delay override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
11:9	OA_LANE1_HSRX_CPHY_CDR_DIV	R/W	<p>Lane 1 C-PHY oscillation clock divider (for calibration). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x5</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

Bits	Name	Memory Access	Description
8	OA_LANE1_HSRX_SEL_GATED_POLARITY	R/W	<p>Lane &lt;0&gt; deserializer output polarity (D-PHY related). Active high. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:5	OA_LANE1_HSRX_HS_CLK_DIV	R/W	<p>Lane 1 D-PHY DDR clock lane divider (data rate dependent). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x7</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
4:3	OA_LANE1_HSRX_GMODE	R/W	<p>Lane 1 HS-RX preamplifier bandwidth configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
2:0	OA_LANE1_HSRX_EQUALIZER	R/W	<p>Lane 1 HS-RX preamplifier equalizer bitword configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_10**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x122a

Bits	Name	Memory Access	Description
15	OA_LANE1_HSTX_DIV_EN_OVR_EN	R/W	<p>oa_lane1_hstx_div_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	OA_LANE1_HSRX_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
13	OA_LANE1_HSRX_PON_OVR_EN	R/W	<p>oa_lane1_hsrx_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	OA_LANE1_HSRX_CPHY_MASK_CHANGE_OVR_EN	R/W	<p>oa_lane1_hsrx_cphy_mask_change override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_LANE1_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_VAL	R/W	<p>oa_lane1_hsrx_cphy_alp_det_left_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	OA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_VAL	R/W	<p>oa_lane1_hsrx_cphy_alp_det_right_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	OA_LANE1_HSRX_VCM_DET_OUT_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_vcm_det_out_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE1_HSRX_VCM_DET_PON_OVR_VAL	R/W	<p>oa_lane1_hsrx_vcm_det_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	OA_LANE1_HSRX_OFFCAL_OBS_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_offcal_obs_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE1_HSRX_DESERIALIZE_R_DIV_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_deserializer_div_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
5	OA_LANE1_HSRX_DESERIALIZE_R_DATA_EN_OVR_VAL	R/W	oa_lane1_hsrx_deserializer_data_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE1_HSRX_DESERIALIZE_R_EN_OVR_VAL	R/W	oa_lane1_hsrx_deserializer_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE1_HSRX_HS_CLK_DIV_EN_OVR_VAL	R/W	oa_lane1_hsrx_hs_clk_div_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_LANE1_HSRX_DPHY_CLK_C_HANNEL_PULL_EN	R/W	Lane 1 D-PHY clock channel pull-up/pull-down enable. Active high. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE1_HSRX_TERM_LEFT_EN_OVR_VAL	R/W	oa_lane1_hsrx_term_left_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE1_HSRX_TERM_RIGHT_EN_OVR_VAL	R/W	oa_lane1_hsrx_term_right_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE1\_CTRL\_2\_11**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x122b

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

Bits	Name	Memory Access	Description
14:13	OA_LANE1_HSRX_EN_OVR_VAL	R/W	oa_lane1_hsrx_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
12:11	OA_LANE1_HSRX_PON_OVR_V AL	R/W	oa_lane1_hsrx_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
10	OA_LANE1_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_EN	R/W	oa_lane1_hsrx_cphy_alp_det_left_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_EN	R/W	oa_lane1_hsrx_cphy_alp_det_right_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE1_HSRX_VCM_DET_OUT_EN_OVR_EN	R/W	oa_lane1_hsrx_vcm_det_out_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_LANE1_HSRX_VCM_DET_PON_OVR_EN	R/W	oa_lane1_hsrx_vcm_det_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE1_HSRX_OFFCAL_OBS_EN_OVR_EN	R/W	oa_lane1_hsrx_offcal_obs_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	OA_LANE1_HSRX_DESERIALIZE_R_DIV_EN_OVR_EN	R/W	oa_lane1_hsrx_deserializer_div_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE1_HSRX_DESERIALIZE_R_DATA_EN_OVR_EN	R/W	oa_lane1_hsrx_deserializer_data_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
3	OA_LANE1_HSRX_DESERIALIZE_R_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_deserializer_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	OA_LANE1_HSRX_HS_CLK_DIV_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_hs_clk_div_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	OA_LANE1_HSRX_TERM_LEFT_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_term_left_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	OA_LANE1_HSRX_TERM_RIGHT_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_term_right_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_12**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x122c

Bits	Name	Memory Access	Description
15	OA_LANE1_HSRX_CPHY_SR_BY_PASS_Z	R/W	<p>Enable for the slew rate control latch bypass inside CDR. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14:13	OA_LANE1_HSRX_CPHY_FINE_RANGE	R/W	<p>Delay line fine delay cell setting for DDL. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
12:10	OA_LANE1_HSRX_DPHY_DDL_D IV	R/W	<p>Lane 1 HS-RX DDL oscillation clock divider. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

Bits	Name	Memory Access	Description
9	OA_LANE1_HSRX_DPHY_DATA_DELAY_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_data_delay override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8:5	OA_LANE1_HSRX_DPHY_DDL_VT_COMP_BIAS	R/W	<p>Reserved.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
4	OA_LANE1_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_preamble_cal_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	OA_LANE1_HSRX_DPHY_DLL_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_dll_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	OA_LANE1_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_ddl_phase_change override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	OA_LANE1_HSRX_DPHY_DDL_BYPASS_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_ddl_bypass_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	OA_LANE1_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_ddl_bias_bypass_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE1\_CTRL\_2\_13**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x122d

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	OA_LANE1_HSRX_DPHY_DLL_F_BK_OVR_EN	R/W	oa_lane1_hsrx_dphy_dll_fbk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_LANE1_HSRX_DPHY_DLL_TUNE_MODE_OVR_EN	R/W	oa_lane1_hsrx_dphy_ddl_tune_mode override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	OA_LANE1_HSRX_DPHY_DLL_COARSE_BANK_OVR_EN	R/W	oa_lane1_hsrx_dphy_ddl_coarse_bank override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE1_HSRX_DPHY_DLL_BIAS_OVR_EN	R/W	oa_lane1_hsrx_dphy_ddl_bias override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:6	OA_LANE1_HSRX_DPHY_DATA_DELAY_OVR_VAL	R/W	oa_lane1_hsrx_dphy_data_delay override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
5	OA_LANE1_HSRX_DPHY_DLL_VT_COMP_EN	R/W	Reserved. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE1_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_EN	R/W	oa_lane1_hsrx_dphy_preamble_cal_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE1_HSRX_DPHY_DLL_EN_OVR_EN	R/W	oa_lane1_hsrx_dphy_dll_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
2	OA_LANE1_HSRX_DPHY_DLL_P HASE_CHANGE_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_dll_phase_change override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	OA_LANE1_HSRX_DPHY_DLL_B YPASS_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_dll_bypass_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	OA_LANE1_HSRX_DPHY_DLL_B IAS_BYPASS_EN_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_dll_bias_bypass_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_14**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x122e

Bits	Name	Memory Access	Description
15:10	OA_LANE1_HSRX_DPHY_DLL_F BK_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_dll_fbk override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3f</p>
9:8	OA_LANE1_HSRX_DPHY_DLL_T UNE_MODE_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_dll_tune_mode override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
7:4	OA_LANE1_HSRX_DPHY_DLL_C OARSE_BANK_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_dll_coarse_bank override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
3:0	OA_LANE1_HSRX_DPHY_DLL_B IAS_OVR_VAL	R/W	<p>oa_lane1_hsrx_dphy_dll_bias override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_2\_15**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x122f

Bits	Name	Memory Access	Description
15:11	OA_LANE1_ATB_SW	R/W	<p>Lane 1 analog test bus signal selection. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1f</p>
10	OA_LANE1_HSRX_MODE_OVR_EN	R/W	<p>oa_lane1_hsrx_mode override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	OA_LANE1_HSRX_DPHY_DDL_P HASE_LEFT_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_ddl_phase_left override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE1_HSRX_DPHY_DDL_P HASE_MID_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_ddl_phase_mid override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	OA_LANE1_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_EN	R/W	<p>oa_lane1_hsrx_dphy_ddl_phase_right override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE1_HSRX_OFFCAL_LEF T_OVR_EN	R/W	<p>oa_lane1_hsrx_offcal_left override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	OA_LANE1_HSRX_OFFCAL_RIG HT_OVR_EN	R/W	<p>oa_lane1_hsrx_offcal_right override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4:3	OA_LANE1_HSRX_DPHY_CLK_C HANNEL	R/W	Lane 1 D-PHY HS-RX clock channel selection. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
2:0	OA_LANE1_HSRX_DPHY_DLL_C P_PROG	R/W	Lane 1 D-PHY HS-RX DLL charge pump gain configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_IOCTL\_RW\_AFE\_LANE1\_CTRL\_3\_0**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1230

Bits	Name	Memory Access	Description
15:8	OA_LANE1_HSRX_OFFCAL_LEFT_OVR_VAL	R/W	oa_lane1_hsrx_offcal_left override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	OA_LANE1_HSRX_OFFCAL_RIGHT_OVR_VAL	R/W	oa_lane1_hsrx_offcal_right override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_IOCTL\_RW\_AFE\_LANE1\_CTRL\_3\_1**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1231

Bits	Name	Memory Access	Description
15:8	OA_LANE1_HSRX_DPHY_DDL_PHASE_MID_OVR_VAL	R/W	oa_lane1_hsrx_dphy_ddl_phase_mid (bits [7:0]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

7:0	OA_LANE1_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_VAL	R/W	oa_lane1_hsrx_dphy_ddl_phase_right (bits [7:0]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_3\_2**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1232

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:11	OA_LANE1_HSRX_MODE_OVR_VAL	R/W	oa_lane1_hsrx_mode override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
10	OA_LANE1_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_VAL	R/W	oa_lane1_hsrx_dphy_ddl_phase_right (bit [8]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE1_HSRX_DPHY_DDL_P HASE_MID_OVR_VAL	R/W	oa_lane1_hsrx_dphy_ddl_phase_mid (bit [8]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:0	OA_LANE1_HSRX_DPHY_DDL_P HASE_LEFT_OVR_VAL	R/W	oa_lane1_hsrx_dphy_ddl_phase_left override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_3\_3**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1233

Bits	Name	Memory Access	Description
15:8	IA_LANE1_HSRX_DATA_BC_MID_OVR_VAL	R/W	<p>ia_lane1_hsrx_data_bc_mid override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:0	IA_LANE1_HSRX_DATA_AB_LEFT_OVR_VAL	R/W	<p>ia_lane1_hsrx_data_ab_left override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_3\_4**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1234

Bits	Name	Memory Access	Description
15	IA_LANE1_HSRX_OUT_CAL_RIGHT_P_OVR_VAL	R/W	<p>ia_lane1_hsrx_out_cal_right_p override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	IA_LANE1_HSRX_OUT_CAL_RIGHT_N_OVR_VAL	R/W	<p>ia_lane1_hsrx_out_cal_right_n override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	IA_LANE1_HSRX_OUT_CAL_LEFT_P_OVR_VAL	R/W	<p>ia_lane1_hsrx_out_cal_left_p override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	IA_LANE1_HSRX_OUT_CAL_LEFT_N_OVR_VAL	R/W	<p>ia_lane1_hsrx_out_cal_left_n override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	IA_LANE1_HSRX_VCM_DET_OUTPUT_OVR_VAL	R/W	<p>ia_lane1_hsrx_vcm_det_out override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
10	IA_LANE1_HSTX_WORD_CLK_OVR_VAL	R/W	<p>ia_lane1_hstx_word_clk override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	IA_LANE1_HSRX_HS_CLK_DIV_OUT_OVR_VAL	R/W	<p>ia_lane1_hsrx_hs_clk_div_out override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	IA_LANE1_HSRX_WORD_CLK_OVR_VAL	R/W	<p>ia_lane1_hsrx_word_clk override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:0	IA_LANE1_HSRX_DATA_CA_RIGHT_OVR_VAL	R/W	<p>ia_lane1_hsrx_data_ca_right override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_3\_5**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1235

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	IA_LANE1_HSRX_CPHY_CDR_OSC_CLK_OVR_EN	R/W	<p>ia_lane1_hsrx_cphy_cdr_osc_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	IA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_EN	R/W	<p>ia_lane1_hsrx_cphy_alp_det_right_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
12	IA_LANE1_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_EN	R/W	<p>ia_lane1_hsrx_cphy_alp_det_left_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	IA_LANE1_HSRX_DPHY_DDL_OSC_CLK_OVR_EN	R/W	<p>ia_lane1_hsrx_dphy_ddl_osc_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	IA_LANE1_HSRX_OUT_CAL_RIGHT_P_OVR_EN	R/W	<p>ia_lane1_hsrx_out_cal_right_p override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	IA_LANE1_HSRX_OUT_CAL_RIGHT_N_OVR_EN	R/W	<p>ia_lane1_hsrx_out_cal_right_n override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	IA_LANE1_HSRX_OUT_CAL_LEFT_P_OVR_EN	R/W	<p>ia_lane1_hsrx_out_cal_left_p override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	IA_LANE1_HSRX_OUT_CAL_LEFT_N_OVR_EN	R/W	<p>ia_lane1_hsrx_out_cal_left_n override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	IA_LANE1_HSRX_VCM_DET_OUTPUT_OVR_EN	R/W	<p>ia_lane1_hsrx_vcm_det_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	IA_LANE1_HSTX_WORD_CLK_OUTPUT_OVR_EN	R/W	<p>ia_lane1_hstx_word_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
4	IA_LANE1_HSRX_HS_CLK_DIV_OUT_OVR_EN	R/W	<p>ia_lane1_hsrx_hs_clk_div_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	IA_LANE1_HSRX_WORD_CLK_OVR_EN	R/W	<p>ia_lane1_hsrx_word_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	IA_LANE1_HSRX_DATA_CA_RIGHT_OVR_EN	R/W	<p>ia_lane1_hsrx_data_ca_right override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	IA_LANE1_HSRX_DATA_BC_MID_OVR_EN	R/W	<p>ia_lane1_hsrx_data_bc_mid override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	IA_LANE1_HSRX_DATA_AB_LEFT_OVR_EN	R/W	<p>ia_lane1_hsrx_data_ab_left override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_3\_6**

- **Description:** Analog macro lane 1 control
- **Size:** 16 bits
- **Offset:** 0x1236

Bits	Name	Memory Access	Description
15:14	O_LANE1_GPIO_OUT_OVR_VAL	R/W	<p>o_lane1_gpio_out_ovr_val override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
13:12	IA_LANE1_GPI_OUT_OVR_VAL	R/W	<p>ia_lane1_gpi_out_ovr_val override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

Bits	Name	Memory Access	Description
11:10	IA_LANE1_SPARE_OUT_OVR_VAL	R/W	ia_lane1_spare_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9:8	IA_LANE1_LPRX_DOUTULP_OVR_VAL	R/W	ia_lane1_lprx_doutulp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7:6	IA_LANE1_LPRX_DOUTLP_OVR_VAL	R/W	ia_lane1_lprx_doutlp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
5:4	IA_LANE1_LPRX_DOUTCD_OVR_VAL	R/W	ia_lane1_lprx_doutcd override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3	IA_LANE1_HSRX_CPHY_CDR_OSC_CLK_OVR_VAL	R/W	ia_lane1_hsrx_cphy_cdr_osc_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_LANE1_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_VAL	R/W	ia_lane1_hsrx_cphy_alp_det_right_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_LANE1_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_VAL	R/W	ia_lane1_hsrx_cphy_alp_det_left_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

0	IA_LANE1_HSRX_DPHY_DDL_OSC_CLK_OVR_VAL	R/W	ia_lane1_hsrx_dphy_ddl_osc_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE1\_CTRL\_3\_7**

- **Description:** Analog macro lane 1 control

- **Size:** 16 bits
- **Offset:** 0x1237

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
5	O_LANE1_GPIO_OUT_OVR_EN	R/W	o_lane1_gpio_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	IA_LANE1_GPI_OUT_OVR_EN	R/W	ia_lane1_gpi_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	IA_LANE1_SPARE_OUT_OVR_EN	R/W	ia_lane1_spare_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_LANE1_LPRX_DOUTULP_OVR_EN	R/W	ia_lane1_lprx_doutulp override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_LANE1_LPRX_DOUTLP_OVR_EN	R/W	ia_lane1_lprx_doutlp override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	IA_LANE1_LPRX_DOUTCD_OVR_EN	R/W	ia_lane1_lprx_doutcd override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

### CORE\_DIG\_IOTCTRL\_R\_AFE\_LANE1\_CTRL\_3\_8

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x1238

Bits	Name	Memory Access	Description
15:12	OA_LANE1_HSRX_CPHY_DELAY	R	<p>oa_lane1_hsrx_cphy_delay multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
11	OA_LANE1_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN	R	<p>oa_lane1_hsrx_cphy_cdr_fbk_fast_lock_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	OA_LANE1_HSRX_DPHY_DDL_E_N	R	<p>oa_lane1_hsrx_dphy_ddl_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	OA_LANE1_HSRX_DPHY_DDL_DCC_EN	R	<p>oa_lane1_hsrx_dphy_ddl_dcc_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
8	OA_LANE1_LPTX_DIN_DP	R	<p>oa_lane1_lptx_din_dp multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7	OA_LANE1_LPTX_DIN_DN	R	<p>oa_lane1_lptx_din_dn multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
6:5	OA_LANE1_HSTX_LOWCAP_EN	R	<p>oa_lane1_hstx_lowcap_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

Bits	Name	Memory Access	Description
4	OA_LANE1_HSRX_DPHY_DDL_PON	R	<p>oa_lane1_hsrx_dphy_ddl_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
3:2	OA_LANE1_HSTX_BOOST_EN	R	<p>oa_lane1_hstx_boost_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
1:0	OA_LANE1_HSTX_PON	R	<p>oa_lane1_hstx_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE1\_CTRL\_3\_9**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x1239

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
10	OA_LANE1_HSTX_DIV_EN	R	<p>oa_lane1_hstx_div_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9:8	OA_LANE1_HSTX_TERM_EN	R	<p>oa_lane1_hstx_term_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

7:0	OA_LANE1_HSTX_DATA_AB_DP HY	R	<p>oa_lane1_hstx_data_ab_dphy multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
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**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE1\_CTRL\_3\_10**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x123a

Bits	Name	Memory Access	Description
15:14	I_LANE1_GPIO_IN	R	<p>i_lane1_gpio_in[0] multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
13:7	OA_LANE1_HSTX_DATA_CA	R	<p>oa_lane1_hstx_data_ca multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f      <b>Volatile:</b> true</p>
6:0	OA_LANE1_HSTX_DATA_BC	R	<p>oa_lane1_hstx_data_bc multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f      <b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE1\_CTRL\_3\_11**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x123b

Bits	Name	Memory Access	Description
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15:14	O_LANE1_GPIO_OUT	R	oa_lane1_gpio_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
13	OA_LANE1_HSRX_CPHY_MASK_CHANGE	R	oa_lane1_hsrx_cphy_mask_change multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

12	OA_LANE1_HSRX_CPHY_CDR_FBK_EN	R	oa_lane1_hsrx_cphy_cdr_fbk_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
11:10	OA_LANE1_LPRX_ULP_PON	R	oa_lane1_lprx_ulp_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
9:8	OA_LANE1_LPRX_CD_PON	R	oa_lane1_lprx_cd_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
7:6	OA_LANE1_LPRX_LP_PON	R	oa_lane1_lprx_lp_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
5:4	OA_LANE1_LPTX_PULLDWN_EN	R	oa_lane1_lptx_pulldwn_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

3:2	OA_LANE1_LPTX_PON	R	oa_lane1_lptx_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
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1:0	OA_LANE1_LPTX_EN	R	oa_lane1_lptx_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
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**CORE\_DIG\_ICTRL\_R\_AFE\_LANE1\_CTRL\_3\_12**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x123c

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:13	OA_LANE1_HSRX_EN	R	oa_lane1_hsrx_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

12:11	OA_LANE1_HSRX_PON	R	oa_lane1_hsrx_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
10	OA_LANE1_HSRX_CPHY_ALP_DET_LEFT_PON	R	oa_lane1_hsrx_cphy_alp_det_left_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

9	OA_LANE1_HSRX_CPHY_ALP_DETECT_RIGHT_PON	R	oa_lane1_hsrx_cphy_alp_det_right_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
8	OA_LANE1_HSRX_VCM_DET_OUTPUT_EN	R	oa_lane1_hsrx_vcm_det_out_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
7	OA_LANE1_HSRX_VCM_DET_PON	R	oa_lane1_hsrx_vcm_det_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
6	OA_LANE1_HSRX_OFFCAL_OBS_EN	R	oa_lane1_hsrx_offcal_obs_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

5	OA_LANE1_HSRX_DESERIALIZE_R_DIV_EN	R	oa_lane1_hsrx_deserializer_div_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
4	OA_LANE1_HSRX_DESERIALIZE_R_DATA_EN	R	oa_lane1_hsrx_deserializer_data_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	OA_LANE1_HSRX_DESERIALIZE_R_EN	R	oa_lane1_hsrx_deserializer_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

2	OA_LANE1_HSRX_HS_CLK_DIV_EN	R	oa_lane1_hsrx_hs_clk_div_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	OA_LANE1_HSRX_TERM_LEFT_EN	R	oa_lane1_hsrx_term_left_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	OA_LANE1_HSRX_TERM_RIGHT_EN	R	oa_lane1_hsrx_term_right_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE1\_CTRL\_3\_13**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x123d

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
8:5	OA_LANE1_HSRX_DPHY_DATA_DELAY	R	oa_lane1_hsrx_dphy_data_delay multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true

4	OA_LANE1_HSRX_DPHY_PREAMBLE_CAL_EN	R	oa_lane1_hsrx_dphy_preamble_cal_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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3	OA_LANE1_HSRX_DPHY_DLL_E_N	R	oa_lane1_hsrx_dphy_dll_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	OA_LANE1_HSRX_DPHY_DLL_P_HASE_CHANGE	R	oa_lane1_hsrx_dphy_ddl_phase_change multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	OA_LANE1_HSRX_DPHY_DLL_BYPASS_EN	R	oa_lane1_hsrx_dphy_ddl_bypass_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	OA_LANE1_HSRX_DPHY_DLL_BIAS_BYPASS_EN	R	oa_lane1_hsrx_dphy_ddl_bias_bypass_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE1\_CTRL\_3\_14**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x123e

Bits	Name	Memory Access	Description
15:10	OA_LANE1_HSRX_DPHY_DLL_F_BK	R	oa_lane1_hsrx_dphy_dll_fbk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f <b>Volatile:</b> true
9:8	OA_LANE1_HSRX_DPHY_DLL_TUNE_MODE	R	oa_lane1_hsrx_dphy_ddl_tune_mode multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

Bits	Name	Memory Access	Description
7:4	OA_LANE1_HSRX_DPHY_DDL_C OARSE_BANK	R	oa_lane1_hsrx_dphy_ddl_coarse_bank multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true
3:0	OA_LANE1_HSRX_DPHY_DDL_B IAS	R	oa_lane1_hsrx_dphy_ddl_bias multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE1\_CTRL\_3\_15**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x123f

Bits	Name	Memory Access	Description
15:8	OA_LANE1_HSRX_OFFCAL_LEFT	R	oa_lane1_hsrx_offcal_left multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
7:0	OA_LANE1_HSRX_OFFCAL_RIGHT	R	oa_lane1_hsrx_offcal_right multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE1\_CTRL\_4\_0**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x1240

Bits	Name	Memory Access	Description

15:8	OA_LANE1_HSRX_DPHY_DDL_P HASE_MID	R	oa_lane1_hsrx_dphy_ddl_phase_mid (bits [7:0]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
7:0	OA_LANE1_HSRX_DPHY_DDL_P HASE_RIGHT	R	oa_lane1_hsrx_dphy_ddl_phase_right (bits [7:0]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE1\_CTRL\_4\_1**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x1241

Bits	Name	Memory Access	Description
15	OA_LANE1_LVDS_OFFSET_EN	R	oa_lane1_lvds_offset_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
14	OA_LANE1_LVDS_HYST_EN	R	oa_lane1_lvds_hyst_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

13:11	OA_LANE1_HSRX_MODE	R	oa_lane1_hsrx_mode multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7 <b>Volatile:</b> true
10	OA_LANE1_HSRX_DPHY_DDL_P HASE_RIGHT	R	oa_lane1_hsrx_dphy_ddl_phase_right (bit [8]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

9	OA_LANE1_HSRX_DPHY_DDL_P HASE_MID	R	oa_lane1_hsrx_dphy_ddl_phase_mid (bit [8]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
8:0	OA_LANE1_HSRX_DPHY_DDL_P HASE_LEFT	R	oa_lane1_hsrx_dphy_ddl_phase_left multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_R\_AFE\_LANE1\_CTRL\_4\_2**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x1242

Bits	Name	Memory Access	Description
15:8	IA_LANE1_HSRX_DATA_BC_MID _INT	R	ia_lane1_hsrx_data_bc_mid multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
7:0	IA_LANE1_HSRX_DATA_AB_LEFT _INT	R	ia_lane1_hsrx_data_ab_left multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_R\_AFE\_LANE1\_CTRL\_4\_3**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x1243

Bits	Name	Memory Access	Description

15	IA_LANE1_HSRX_OUT_CAL_RIGHT_P_INT	R	ia_lane1_hsrx_out_cal_right_p multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
14	IA_LANE1_HSRX_OUT_CAL_RIGHT_N_INT	R	ia_lane1_hsrx_out_cal_right_n multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

13	IA_LANE1_HSRX_OUT_CAL_LEFT_P_INT	R	ia_lane1_hsrx_out_cal_left_p multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
12	IA_LANE1_HSRX_OUT_CAL_LEFT_N_INT	R	ia_lane1_hsrx_out_cal_left_n multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
11	IA_LANE1_HSRX_VCM_DET_OUT_INT	R	ia_lane1_hsrx_vcm_det_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
10	IA_LANE1_HSTX_WORD_CLK_IN_T	R	ia_lane1_hstx_word_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
9	IA_LANE1_HSRX_HS_CLK_DIV_OUT_INT	R	ia_lane1_hsrx_hs_clk_div_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

8	IA_LANE1_HSRX_WORD_CLK_I NT	R	ia_lane1_hsrx_word_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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7:0	IA_LANE1_HSRX_DATA_CA_RIG HT_INT	R	ia_lane1_hsrx_data_ca_right multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
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**CORE\_DIG IOCTL\_R\_AFE\_LANE1\_CTRL\_4\_4**

- **Description:** Analog macro lane 1 observability
- **Size:** 16 bits
- **Offset:** 0x1244

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:12	IA_LANE1_GPI_OUT	R	ia_lane1_gpi_out[0] multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

11:10	IA_LANE1_SPARE_OUT_INT	R	ia_lane1_spare_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
9:8	IA_LANE1_LPRX_DOUTULP_INT	R	ia_lane1_lprx_doutulp multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

7:6	IA_LANE1_LPRX_DOUTLP_INT	R	ia_lane1_lprx_doutlp multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
5:4	IA_LANE1_LPRX_DOUTCD_INT	R	ia_lane1_lprx_doutcd multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
3	IA_LANE1_HSRX_CPHY_CDR_OSC_CLK_INT	R	ia_lane1_hsrx_cphy_cdr_osc_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	IA_LANE1_HSRX_CPHY_ALP_DETECT_RIGHT_OUT_INT	R	ia_lane1_hsrx_cphy_alp_det_right_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	IA_LANE1_HSRX_CPHY_ALP_DETECT_LEFT_OUT_INT	R	ia_lane1_hsrx_cphy_alp_det_left_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	IA_LANE1_HSRX_DPHY_DDL_OSC_CLK_INT	R	ia_lane1_hsrx_dphy_ddl_osc_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE1\_OVR\_5\_0**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1250

Bits	Name	Memory Access	Description

15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13	O_ERRSOTHS_C1	R	o_errsoths_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
12	O_ERRCONTENTIONLP1_C1	R	o_errcontentionlp1_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

11	O_ERRCONTENTIONLP0_C1	R	o_errcontentionlp0_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
10	O_ERRCONTROL_C1	R	o_errcontrol_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
9	O_ERRSYNCESC_C1	R	o_errsyncesc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
8	O_ERRESC_C1	R	o_erresc_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

7	I_FORCETXSTOPMODE_C1_INT	R	i_forcetxstopmode_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
6	I_FORCERXMODE_C1_INT	R	i_forcerxmode_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

5	O_DIRECTION_C1	R	o_direction_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
4	I_TURNDISABLE_C1_INT	R	i_turndisable_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	I_TURNREQUEST_C1_INT	R	i_turnrequest_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	O_ULPSACTIVENOT_C1	R	o_ulpsactivenot_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	O_STOPSTATE_C1	R	o_stopstate_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

0	I_ENABLE_C1_INT	R	i_enable_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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**CORE\_DIG\_IOCTRL\_R\_CPHY\_PPI\_LANE1\_OVR\_5\_1**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1251

Bits	Name	Memory Access	Description
15:0	O_RXDATAHS_C1	R	o_rxdatahs_c1 override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_5\_2**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1252

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0X0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:10	I_ALPWAKESTATE_C1_OVR_VAL	R/W	i_alpwakestate_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
9:6	I_TXALPNIBBLE_C1_OVR_VAL	R/W	i_txalpnibble_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

5:2	I_TXALPCODE_C1_OVR_VAL	R/W	i_txalpcode_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
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1:0	I_TXSENDALPHS_C1_OVR_VAL	R/W	i_txsendalphs_c1 override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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**CORE\_DIG\_ICTRL\_RW\_CPHY\_PPI\_LANE1\_OVR\_5\_3**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1253

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	Reserved for Future use and actual reset value is 0X0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
3	I_ALPWAKESTATE_C1_OVR_EN	R/W	i_alpwakestate_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	I_TXALPNIBBLE_C1_OVR_EN	R/W	i_txalpnibble_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

1	I_TXALPCODE_C1_OVR_EN	R/W	i_txalpcode_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	I_TXSENDALPHS_C1_OVR_EN	R/W	i_txsendalphs_c1 override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCRTL\_R\_CPHY\_PPI\_LANE1\_OVR\_5\_4**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1254

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
12:10	I_ALPWAKESTATE_C1_INT	R	<p>i_alpwakestate_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>
9:6	I_TXALPNIBBLE_C1_INT	R	<p>i_txalpnibble_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>

5:2	I_TXALPCODE_C1_INT	R	<p>i_txalpcode_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
1:0	I_TXSENDALPHS_C1_INT	R	<p>i_txsendalphs_c1 override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_RW\_TRI01\_0**

- **Description:** Configurations for Trio 1
- **Size:** 16 bits
- **Offset:** 0x1280

Bits	Name	Memory Access	Description

15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11:9	POST_RECEIVED_RESET_THRESHOLD	R/W	Counter for resetting the post detected flag. In word_clk cycles. Quasi static. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

8:6	DESERIALIZER_DIV_EN_DELAY_DEASS_THRESH	R/W	Counter for deassertion of deserializer_div_en after deassertion of deserializer_data_en. In dco_clk cycles. Quasi Static. 0 is a forbidden value. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
5:3	DESERIALIZER_DIV_EN_DELAY_THRESH	R/W	Counter for deserializer_div_en delay. In dco_clk cycles. Quasi static. 0 is a forbidden value. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
2:0	DESERIALIZER_DATA_EN_DELAY_THRESH	R/W	Counter for deserializer_data_en delay. In dco_clk cycles. Quasi static. 0 is a forbidden value. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

### CORE\_DIG\_RW\_TRI01\_1

- **Description:** Configurations for Trio 1
- **Size:** 16 bits
- **Offset:** 0x1281

Bits	Name	Memory Access	Description
15:0	POST_DET_DELAY_THRESH	R/W	Counter for deassertion of deserializer_data_en after Post2 reception. In dco_clk cycles. Quasi static. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

### CORE\_DIG\_RW\_TRI01\_2

- **Description:** Configurations for Trio 1
- **Size:** 16 bits
- **Offset:** 0x1282

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	DESERIALIZER_EN_DELAY_DEASSER-TION_SS_THRESH	R/W	<p>Counter for deassertion of deserializer_en after deassertion of deserializer_data_en. In dco_clk cycles. Quasi Static. 0 is a forbidden value.</p> <p><b>Value After Reset:</b> 0xa</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_2\_0**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1420

Bits	Name	Memory Access	Description
15	OA_LANE2_SHORT_LB_EN	R/W	<p>oa_lane2_short_lb_en bit configuration.This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	I_LANE2_GPIO_IN_OVR_EN	R/W	<p>i_lane2_gpio_in override enable. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	OA_LANE2_LVDS_OFFSET_EN_OVR_EN	R/W	<p>oa_lane2_lvds_offset_en override enable. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

12	OA_LANE2_LVDS_HYST_EN_OVR_EN	R/W	<p>oa_lane2_lvds_hyst_en override enable. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:0	OA_LANE2_SPARE_IN	R/W	<p>Lane 2 input spare bus (bits [11:0]). This signal is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCRTL\_RW\_AFE\_LANE2\_CTRL\_2\_1**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1421

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	OA_LANE2_HSTX_LOWCAP_EN_OVR_EN	R/W	<p>oa_lane2_hstx_lowcap_en override enable. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13:12	I_LANE2_GPIO_IN_OVR_VAL	R/W	<p>i_lane2_gpio_in_ovr_val override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

11:10	OA_LANE2_GPO_EN	R/W	<p>oa_lane2_gpo_en[0] bit configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
9:8	OA_LANE2_GPI_HYST_EN	R/W	<p>oa_lane2_gpi_hyst_en[0] bit configuration. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
7:6	OA_LANE2_GPI_EN	R/W	<p>oa_lane2_gpi_en[0] bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
5	OA_LANE2_LVDS_OFFSET_EN_OVR_VAL	R/W	<p>oa_lane2_lvds_offset_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

4	OA_LANE2_LVDS_HYST_EN_OV_R_VAL	R/W	oa_lane2_lvds_hyst_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE2_SEL_LVDS_OFF	R/W	oa_lane2_lvds_cmsw_off bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2:1	OA_LANE2_LVDS_CMSW_PROG	R/W	oa_lane2_lvds_cmsw_prog word configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
0	OA_LANE2_LVDS_EN	R/W	oa_lane2_lvds_en bit configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_2**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1422

Bits	Name	Memory Access	Description
15:7	RESERVED_15_7	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

6	OA_LANE2_HSTX_DIV_EN_OVR_VAL	R/W	oa_lane2_hstx_div_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5:4	OA_LANE2_HSTX_LOWCAP_EN_OVR_VAL	R/W	oa_lane2_hstx_lowcap_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

3	OA_LANE2_HSRX_DPHY_DDL_PON_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_LANE2_HSRX_TERM_EN200_OHMS	R/W	Lane 2 HS-RX termination value. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE2_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_EN	R/W	oa_lane2_hsrx_cphy_cdr_fbk_fast_lock_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE2_SEL_LANE_CFG	R/W	Lane 2 D-PHY/C-PHY configuration. 1'b0: D-PHY data lane (when phy_mode is 1'b0); C-PHY slave lane (when phy_mode is 1'b1). 1'b1: D-PHY clock lane (when phy_mode is 1'b0); C-PHY master lane (when phy_mode is 1'b1). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_2\_3**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1423

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

13	OA_LANE2_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_OVR_VAL	R/W	oa_lane2_hsrx_cphy_cdr_fbk_fast_lock_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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12	OA_LANE2_HSRX_DPHY_DDL_EN_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	OA_LANE2_HSRX_DPHY_DDL_DCC_EN_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_dcc_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE2_LPTX_DIN_DP_OVR_VAL	R/W	oa_lane2_lptx_din_dp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE2_LPTX_DIN_DN_OVR_VAL	R/W	oa_lane2_lptx_din_dn override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE2_HSTX_SEL_CLKLB	R/W	Lane 2 HS-TX clock source. 1'b0: External PLL clock. 1'b1: Common block internal DCO clock. This signal is quasi-static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:5	OA_LANE2_HSTX_EQA	R/W	Lane 2 HS-TX de-emphasis word (upper-half). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

4	OA_LANE2_HSTX_SEL_PHASE0	R/W	Lane 2 HS-TX clock phase selection. 1'b0: 90 (for D-PHY clock lane configuration). 1'b1: 0 (for both C-PHY and D-PHY data lane configurations). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:2	OA_LANE2_HSTX_BOOST_EN_OVR_VAL	R/W	oa_lane2_hstx_boost_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

1:0	OA_LANE2_HSTX_PON_OVR_VA_L	R/W	oa_lane2_hstx_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_4**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1424

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11	OA_LANE2_HSRX_DPHY_DDL_DCC_EN_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

10	OA_LANE2_HSTX_TERM_EN_OVR_EN	R/W	oa_lane2_hstx_term_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:8	OA_LANE2_LPTX_SR_BYPASS_EN	R/W	oa_lane2_lptx_sr_bypass_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7	OA_LANE2_LPTX_DIN_DP_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE2_LPTX_DIN_DN_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_dcc_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

5	OA_LANE2_HSTX_CLK_OBS_EN	R/W	Lane 2 HS clock pattern driven in the lines (debug feature). Active high. This signal is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4:2	OA_LANE2_HSTX_EQB	R/W	Lane 2 HS-TX de-emphasis word (lower-half). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
1	OA_LANE2_HSTX_BOOST_EN_OVR_EN	R/W	oa_lane2_hstx_boost_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE2_HSTX_PON_OVR_EN	R/W	oa_lane2_hstx_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_5**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1425

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12	OA_LANE2_HSRX_DPHY_DDL_EN_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

11:10	OA_LANE2_HSTX_TERM_EN_OVR_VAL	R/W	oa_lane2_hstx_term_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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9	OA_LANE2_HSTX_DATA_CA_OV_R_EN	R/W	oa_lane2_hstx_data_ca override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE2_HSTX_DATA_BC_OV_R_EN	R/W	oa_lane2_hstx_data_ca override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:0	OA_LANE2_HSTX_DATA_AB_DPHY_OVR_VAL	R/W	oa_lane2_hstx_data_ab_dphy override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_2\_6**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1426

Bits	Name	Memory Access	Description
15	OA_LANE2_HSRX_DPHY_DDL_PON_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	OA_LANE2_HSTX_DATA_AB_DPHY_OVR_EN	R/W	oa_lane2_hstx_data_ab_dphy override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13:7	OA_LANE2_HSTX_DATA_CA_OV_R_VAL	R/W	oa_lane2_hstx_data_ca override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f
6:0	OA_LANE2_HSTX_DATA_BC_OV_R_VAL	R/W	oa_lane2_hstx_data_bc override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f

**CORE\_DIG\_IOCRTL\_RW\_AFE\_LANE2\_CTRL\_2\_7**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1427

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	OA_LANE2_HSRX_VCM_DET_SYNC_BYPASS	R/W	<p>Enable vcm detector filter bypass which controls CDR input propagation. This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

12:10	OA_LANE2_HSRX_CPHY_CDR_FBK_CAP_PROG	R/W	<p>Lane 2 C-PHY low-pass filter bandwidth (symbol rate dependent). This signal is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x7</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
9	OA_LANE2_HSRX_CPHY_CDR_FBK_EN_OVR_VAL	R/W	<p>oa_lane2_hsrx_cphy_cdr_fbk_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_LANE2_LPRX_ULP_PON_OVR_EN	R/W	<p>oa_lane2_lprx_ulp_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	OA_LANE2_LPRX_CD_PON_OVR_EN	R/W	<p>oa_lane2_lprx_cd_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	OA_LANE2_LPRX_LP_PON_OVR_EN	R/W	<p>oa_lane2_lprx_lp_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

5:4	OA_LANE2_LPTX_PULLDWN_EN_OVR_VAL	R/W	oa_lane2_lptx_pulldwn_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3:2	OA_LANE2_LPTX_PON_OVR_VAL	R/W	oa_lane2_lptx_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
1:0	OA_LANE2_LPTX_EN_OVR_VAL	R/W	oa_lane2_lptx_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_2\_8**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1428

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12	OA_LANE2_HSRX_CDPHY_SEL_FAST	R/W	Lane 2 HS-RX DDL delay cell strength. Please check table for more details. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

11	OA_LANE2_HSRX_CPHY_DELAY_OVR_EN	R/W	oa_lane2_hsrx_cphy_delay override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE2_HSRX_CPHY_MASK_CHANGE_OVR_VAL	R/W	oa_lane2_hsrx_cphy_mask_change override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

9	OA_LANE2_HSRX_CPHY_CDR_FBK_EN_OVR_EN	R/W	oa_lane2_hsrx_cphy_cdr_fbk_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE2_LPTX_PULLDWN_EN_OVR_EN	R/W	oa_lane2_lptx_pulldwn_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_LANE2_LPTX_PON_OVR_EN	R/W	oa_lane2_lptx_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE2_LPTX_EN_OVR_EN	R/W	oa_lane2_lptx_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5:4	OA_LANE2_LPRX_ULP_PON_OVR_VAL	R/W	oa_lane2_lprx_ulp_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3:2	OA_LANE2_LPRX_CD_PON_OVR_VAL	R/W	oa_lane2_lprx_cd_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

1:0	OA_LANE2_LPRX_LP_PON_OVR_VAL	R/W	oa_lane2_lprx_lp_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_9**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1429

Bits	Name	Memory Access	Description
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15:12	OA_LANE2_HSRX_CPHY_DELAY_OVR_VAL	R/W	oa_lane2_hsrx_cphy_delay override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
11:9	OA_LANE2_HSRX_CPHY_CDR_DIV	R/W	Lane 2 C-PHY oscillation clock divider (for calibration). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x5 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

8	OA_LANE2_HSRX_SEL_GATED_POLARITY	R/W	Lane <0> deserializer output polarity (D-PHY related). Active high. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:5	OA_LANE2_HSRX_HS_CLK_DIV	R/W	Lane 2 D-PHY DDR clock lane divider (data rate dependent). This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
4:3	OA_LANE2_HSRX_GMODE	R/W	Lane 2 HS-RX preamplifier bandwidth configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
2:0	OA_LANE2_HSRX_EQUALIZER	R/W	Lane 2 HS-RX preamplifier equalizer bitword configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_10**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x142a

Bits	Name	Memory Access	Description
15	OA_LANE2_HSTX_DIV_EN_OVR_EN	R/W	oa_lane2_hstx_div_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

14	OA_LANE2_HSRX_EN_OVR_EN	R/W	oa_lane2_hsrx_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13	OA_LANE2_HSRX_PON_OVR_EN	R/W	oa_lane2_hsrx_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_LANE2_HSRX_CPHY_MASK_CHANGE_OVR_EN	R/W	oa_lane2_hsrx_cphy_mask_change override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	OA_LANE2_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_VAL	R/W	oa_lane2_hsrx_cphy_alp_det_left_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_VAL	R/W	oa_lane2_hsrx_cphy_alp_det_right_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE2_HSRX_VCM_DET_OUT_EN_OVR_VAL	R/W	oa_lane2_hsrx_vcm_det_out_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE2_HSRX_VCM_DET_PON_OVR_VAL	R/W	oa_lane2_hsrx_vcm_det_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_LANE2_HSRX_OFFCAL_OBS_EN_OVR_VAL	R/W	oa_lane2_hsrx_offcal_obs_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE2_HSRX_DESERIALIZE_R_DIV_EN_OVR_VAL	R/W	oa_lane2_hsrx_deserializer_div_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

5	OA_LANE2_HSRX_DESERIALIZE_R_DATA_EN_OVR_VAL	R/W	oa_lane2_hsrx_deserializer_data_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE2_HSRX_DESERIALIZE_R_EN_OVR_VAL	R/W	oa_lane2_hsrx_deserializer_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE2_HSRX_HS_CLK_DIV_EN_OVR_VAL	R/W	oa_lane2_hsrx_hs_clk_div_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_LANE2_HSRX_DPHY_CLK_C_HANNEL_PULL_EN	R/W	Lane 2 D-PHY clock channel pull-up/pull-down enable. Active high. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE2_HSRX_TERM_LEFT_EN_OVR_VAL	R/W	oa_lane2_hsrx_term_left_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE2_HSRX_TERM_RIGHT_EN_OVR_VAL	R/W	oa_lane2_hsrx_term_right_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_2\_11**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x142b

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

14:13	OA_LANE2_HSRX_EN_OVR_VAL	R/W	oa_lane2_hsrx_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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12:11	OA_LANE2_HSRX_PON_OVR_VAL	R/W	oa_lane2_hsrx_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
10	OA_LANE2_HSRX_CPHY_ALP_DET_LEFT_PON_OVR_EN	R/W	oa_lane2_hsrx_cphy_alp_det_left_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_PON_OVR_EN	R/W	oa_lane2_hsrx_cphy_alp_det_right_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE2_HSRX_VCM_DET_OUT_EN_OVR_EN	R/W	oa_lane2_hsrx_vcm_det_out_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_LANE2_HSRX_VCM_DET_PON_OVR_EN	R/W	oa_lane2_hsrx_vcm_det_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE2_HSRX_OFFCAL_OBS_EN_OVR_EN	R/W	oa_lane2_hsrx_offcal_obs_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	OA_LANE2_HSRX_DESERIALIZE_R_DIV_EN_OVR_EN	R/W	oa_lane2_hsrx_deserializer_div_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE2_HSRX_DESERIALIZE_R_DATA_EN_OVR_EN	R/W	oa_lane2_hsrx_deserializer_data_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

3	OA_LANE2_HSRX_DESERIALIZE_R_EN_OVR_EN	R/W	oa_lane2_hsrx_deserializer_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_LANE2_HSRX_HS_CLK_DIV_EN_OVR_EN	R/W	oa_lane2_hsrx_hs_clk_div_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE2_HSRX_TERM_LEFT_EN_OVR_EN	R/W	oa_lane2_hsrx_term_left_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE2_HSRX_TERM_RIGHT_EN_OVR_EN	R/W	oa_lane2_hsrx_term_right_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_12**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x142c

Bits	Name	Memory Access	Description
15	OA_LANE2_HSRX_CPHY_SR_BY_PASS_Z	R/W	Enable for the slew rate control latch bypass inside CDR. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14:13	OA_LANE2_HSRX_CPHY_FINE_RANGE	R/W	Delay line fine delay cell setting for DDL. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
12:10	OA_LANE2_HSRX_DPHY_DDL_D IV	R/W	Lane 2 HS-RX DDL oscillation clock divider. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

9	OA_LANE2_HSRX_DPHY_DATA_DELAY_OVR_EN	R/W	oa_lane2_hsrx_dphy_data_delay override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:5	OA_LANE2_HSRX_DPHY_DDL_VT_COMP_BIAS	R/W	Reserved. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
4	OA_LANE2_HSRX_DPHY_PREAMBLE_CAL_EN_OVR_VAL	R/W	oa_lane2_hsrx_dphy_preamble_cal_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE2_HSRX_DPHY_DLL_EN_OVR_VAL	R/W	oa_lane2_hsrx_dphy_dll_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_LANE2_HSRX_DPHY_DDL_PHASE_CHANGE_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_phase_change override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE2_HSRX_DPHY_DDL_BYPASS_EN_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_bypass_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

0	OA_LANE2_HSRX_DPHY_DDL_BIAS_BYPASS_EN_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_bias_bypass_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_13**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x142d

Bits	Name	Memory Access	Description
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15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
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13	OA_LANE2_HSRX_DPHY_DLL_F BK_OVR_EN	R/W	oa_lane2_hsrx_dphy_dll_fbk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_LANE2_HSRX_DPHY_DDL_T UNE_MODE_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_tune_mode override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	OA_LANE2_HSRX_DPHY_DDL_C OARSE_BANK_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_coarse_bank override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_LANE2_HSRX_DPHY_DDL_B IAS_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_bias override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:6	OA_LANE2_HSRX_DPHY_DATA_ DELAY_OVR_VAL	R/W	oa_lane2_hsrx_dphy_data_delay override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
5	OA_LANE2_HSRX_DPHY_DDL_V T_COMP_EN	R/W	Reserved. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_LANE2_HSRX_DPHY_PREA MBLE_CAL_EN_OVR_EN	R/W	oa_lane2_hsrx_dphy_preamble_cal_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_LANE2_HSRX_DPHY_DLL_E N_OVR_EN	R/W	oa_lane2_hsrx_dphy_dll_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

2	OA_LANE2_HSRX_DPHY_DLL_P HASE_CHANGE_OVR_EN	R/W	oa_lane2_hsrx_dphy_dll_phase_change override enable. Active high. Used for debug purposes.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_LANE2_HSRX_DPHY_DLL_B YPASS_EN_OVR_EN	R/W	oa_lane2_hsrx_dphy_dll_bypass_en override enable. Active high. Used for debug purposes.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_LANE2_HSRX_DPHY_DLL_B IAS_BYPASS_EN_OVR_EN	R/W	oa_lane2_hsrx_dphy_dll_bias_bypass_en override enable. Active high. Used for debug purposes.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_2\_14**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x142e

Bits	Name	Memory Access	Description
15:10	OA_LANE2_HSRX_DPHY_DLL_F BK_OVR_VAL	R/W	oa_lane2_hsrx_dphy_dll_fbk override value. Used for debug purposes.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f

Bits	Name	Memory Access	Description
9:8	OA_LANE2_HSRX_DPHY_DLL_T UNE_MODE_OVR_VAL	R/W	oa_lane2_hsrx_dphy_dll_tune_mode override value. Used for debug purposes.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7:4	OA_LANE2_HSRX_DPHY_DLL_C OARSE_BANK_OVR_VAL	R/W	oa_lane2_hsrx_dphy_dll_coarse_bank override value. Used for debug purposes.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

3:0	OA_LANE2_HSRX_DPHY_DDL_BIAS_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_bias override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
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**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_2\_15**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x142f

Bits	Name	Memory Access	Description
15:11	OA_LANE2_ATB_SW	R/W	Lane 2 analog test bus signal selection. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
10	OA_LANE2_HSRX_MODE_OVR_EN	R/W	oa_lane2_hsrx_mode override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

9	OA_LANE2_HSRX_DPHY_DDL_PHASE_LEFT_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_phase_left override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_LANE2_HSRX_DPHY_DDL_PHASE_MID_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_phase_mid override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_LANE2_HSRX_DPHY_DDL_PHASE_RIGHT_OVR_EN	R/W	oa_lane2_hsrx_dphy_ddl_phase_right override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_LANE2_HSRX_OFFCAL_LEFT_OVR_EN	R/W	oa_lane2_hsrx_offcal_left override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

5	OA_LANE2_HSRX_OFFCAL_RIG HT_OVR_EN	R/W	oa_lane2_hsrx_offcal_right override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4:3	OA_LANE2_HSRX_DPHY_CLK_C HANNEL	R/W	Lane 2 D-PHY HS-RX clock channel selection. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
2:0	OA_LANE2_HSRX_DPHY_DLL_C P_PROG	R/W	Lane 2 D-PHY HS-RX DLL charge pump gain configuration. This signal is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_3\_0**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1430

Bits	Name	Memory Access	Description
15:8	OA_LANE2_HSRX_OFFCAL_LEFT_OVR_VAL	R/W	oa_lane2_hsrx_offcal_left override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	OA_LANE2_HSRX_OFFCAL_RIGHT_OVR_VAL	R/W	oa_lane2_hsrx_offcal_right override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_3\_1**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1431

Bits	Name	Memory Access	Description

15:8	OA_LANE2_HSRX_DPHY_DDL_P HASE_MID_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_phase_mid (bits [7:0]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	OA_LANE2_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_phase_right (bits [7:0]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_3\_2**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1432

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0X0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:11	OA_LANE2_HSRX_MODE_OVR_VAL	R/W	oa_lane2_hsrx_mode override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
10	OA_LANE2_HSRX_DPHY_DDL_P HASE_RIGHT_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_phase_right (bit [8]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_LANE2_HSRX_DPHY_DDL_P HASE_MID_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_phase_mid (bit [8]) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:0	OA_LANE2_HSRX_DPHY_DDL_P HASE_LEFT_OVR_VAL	R/W	oa_lane2_hsrx_dphy_ddl_phase_left override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_3\_3**

- **Description:** Analog macro lane 2 control

- **Size:** 16 bits
- **Offset:** 0x1433

Bits	Name	Memory Access	Description
15:8	IA_LANE2_HSRX_DATA_BC_MID_OVR_VAL	R/W	<p>ia_lane2_hsrx_data_bc_mid override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:0	IA_LANE2_HSRX_DATA_AB_LEFT_OVR_VAL	R/W	<p>ia_lane2_hsrx_data_ab_left override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

#### CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_3\_4

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1434

Bits	Name	Memory Access	Description
15	IA_LANE2_HSRX_OUT_CAL_RIGHT_P_OVR_VAL	R/W	<p>ia_lane2_hsrx_out_cal_right_p override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	IA_LANE2_HSRX_OUT_CAL_RIGHT_N_OVR_VAL	R/W	<p>ia_lane2_hsrx_out_cal_right_n override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	IA_LANE2_HSRX_OUT_CAL_LEFT_P_OVR_VAL	R/W	<p>ia_lane2_hsrx_out_cal_left_p override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	IA_LANE2_HSRX_OUT_CAL_LEFT_N_OVR_VAL	R/W	<p>ia_lane2_hsrx_out_cal_left_n override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

11	IA_LANE2_HSRX_VCM_DET_OUT_OVR_VAL	R/W	ia_lane2_hsrx_vcm_det_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	IA_LANE2_HSTX_WORD_CLK_OVR_VAL	R/W	ia_lane2_hstx_word_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	IA_LANE2_HSRX_HS_CLK_DIV_OUT_OVR_VAL	R/W	ia_lane2_hsrx_hs_clk_div_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	IA_LANE2_HSRX_WORD_CLK_OVR_VAL	R/W	ia_lane2_hsrx_word_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:0	IA_LANE2_HSRX_DATA_CA_RIGHT_OVR_VAL	R/W	ia_lane2_hsrx_data_ca_right override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_3\_5**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1435

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14	IA_LANE2_HSRX_CPHY_CDR_OSC_CLK_OVR_EN	R/W	ia_lane2_hsrx_cphy_cdr_osc_clk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
13	IA_LANE2_HSRX_CPHY_ALP_DETECT_RIGHT_OUT_OVR_EN	R/W	<p>ia_lane2_hsrx_cphy_alp_det_right_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	IA_LANE2_HSRX_CPHY_ALP_DETECT_LEFT_OUT_OVR_EN	R/W	<p>ia_lane2_hsrx_cphy_alp_det_left_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	IA_LANE2_HSRX_DPHY_DDL_OVERRIDE_SC_CLK_OVR_EN	R/W	<p>ia_lane2_hsrx_dphy_ddl_osc_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	IA_LANE2_HSRX_OUT_CAL_RIGHT_P_OVR_EN	R/W	<p>ia_lane2_hsrx_out_cal_right_p override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	IA_LANE2_HSRX_OUT_CAL_RIGHT_N_OVR_EN	R/W	<p>ia_lane2_hsrx_out_cal_right_n override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	IA_LANE2_HSRX_OUT_CAL_LEFT_P_OVR_EN	R/W	<p>ia_lane2_hsrx_out_cal_left_p override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	IA_LANE2_HSRX_OUT_CAL_LEFT_N_OVR_EN	R/W	<p>ia_lane2_hsrx_out_cal_left_n override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	IA_LANE2_HSRX_VCM_DET_OUTPUT_OVR_EN	R/W	<p>ia_lane2_hsrx_vcm_det_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

Bits	Name	Memory Access	Description
5	IA_LANE2_HSTX_WORD_CLK_O_VR_EN	R/W	ia_lane2_hstx_word_clk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	IA_LANE2_HSRX_HS_CLK_DIV_OUT_OVR_EN	R/W	ia_lane2_hsrx_hs_clk_div_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	IA_LANE2_HSRX_WORD_CLK_O_VR_EN	R/W	ia_lane2_hsrx_word_clk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_LANE2_HSRX_DATA_CA_RIGHT_OVR_EN	R/W	ia_lane2_hsrx_data_ca_right override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_LANE2_HSRX_DATA_BC_MID_OVR_EN	R/W	ia_lane2_hsrx_data_bc_mid override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	IA_LANE2_HSRX_DATA_AB_LEFT_OVR_EN	R/W	ia_lane2_hsrx_data_ab_left override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_LANE2\_CTRL\_3\_6**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1436

Bits	Name	Memory Access	Description
15:14	O_LANE2_GPIO_OUT_OVR_VAL	R/W	o_lane2_gpio_out_ovr_val override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

Bits	Name	Memory Access	Description
13:12	IA_LANE2_GPI_OUT_OVR_VAL	R/W	ia_lane2_gpi_out_ovr_val override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
11:10	IA_LANE2_SPARE_OUT_OVR_VAL	R/W	ia_lane2_spare_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9:8	IA_LANE2_LPRX_DOUTULP_OVR_VAL	R/W	ia_lane2_lprx_doutulp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
7:6	IA_LANE2_LPRX_DOUTLP_OVR_VAL	R/W	ia_lane2_lprx_doutlp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
5:4	IA_LANE2_LPRX_DOUTCD_OVR_VAL	R/W	ia_lane2_lprx_doutcd override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3	IA_LANE2_HSRX_CPHY_CDR_OSC_CLK_OVR_VAL	R/W	ia_lane2_hsrx_cphy_cdr_osc_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_OUT_OVR_VAL	R/W	ia_lane2_hsrx_cphy_alp_det_right_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_LANE2_HSRX_CPHY_ALP_DET_LEFT_OUT_OVR_VAL	R/W	ia_lane2_hsrx_cphy_alp_det_left_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	IA_LANE2_HSRX_DPHY_DDL_OSC_CLK_OVR_VAL	R/W	ia_lane2_hsrx_dphy_ddl_osc_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCTRL\_RW\_AFE\_LANE2\_CTRL\_3\_7**

- **Description:** Analog macro lane 2 control
- **Size:** 16 bits
- **Offset:** 0x1437

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
5	O_LANE2_GPIO_OUT_OVR_EN	R/W	<p>o_lane2_gpio_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	IA_LANE2_GPI_OUT_OVR_EN	R/W	<p>ia_lane2_gpi_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

3	IA_LANE2_SPARE_OUT_OVR_E_N	R/W	<p>ia_lane2_spare_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	IA_LANE2_LPRX_DOUTULP_OVR_EN	R/W	<p>ia_lane2_lprx_doutulp override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	IA_LANE2_LPRX_DOUTLP_OVR_EN	R/W	<p>ia_lane2_lprx_doutlp override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	IA_LANE2_LPRX_DOUTCD_OVR_EN	R/W	<p>ia_lane2_lprx_doutcd override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE2\_CTRL\_3\_8**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x1438

Bits	Name	Memory Access	Description
15:12	OA_LANE2_HSRX_CPHY_DELAY	R	<p>oa_lane2_hsrx_cphy_delay multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>

11	OA_LANE2_HSRX_CPHY_CDR_FBK_FAST_LOCK_EN	R	<p>oa_lane2_hsrx_cphy_cdr_fbk_fast_lock_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	OA_LANE2_HSRX_DPHY_DDL_E_N	R	<p>oa_lane2_hsrx_dphy_ddl_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
9	OA_LANE2_HSRX_DPHY_DDL_DCC_EN	R	<p>oa_lane2_hsrx_dphy_ddl_dcc_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
8	OA_LANE2_LPTX_DIN_DP	R	<p>oa_lane2_lptx_din_dp multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7	OA_LANE2_LPTX_DIN_DN	R	<p>oa_lane2_lptx_din_dn multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

6:5	OA_LANE2_HSTX_LOWCAP_EN	R	oa_lane2_hstx_lowcap_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
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4	OA_LANE2_HSRX_DPHY_DDL_PON	R	oa_lane2_hsrx_dphy_ddl_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3:2	OA_LANE2_HSTX_BOOST_EN	R	oa_lane2_hstx_boost_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
1:0	OA_LANE2_HSTX_PON	R	oa_lane2_hstx_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_AFE\_LANE2\_CTRL\_3\_9**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x1439

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10	OA_LANE2_HSTX_DIV_EN	R	oa_lane2_hstx_div_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

9:8	OA_LANE2_HSTX_TERM_EN	R	oa_lane2_hstx_term_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
7:0	OA_LANE2_HSTX_DATA_AB_DP HY	R	oa_lane2_hstx_data_ab_dphy multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_R\_AFE\_LANE2\_CTRL\_3\_10**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x143a

Bits	Name	Memory Access	Description
15:14	I_LANE2_GPIO_IN	R	i_lane2_gpio_in[0] multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
13:7	OA_LANE2_HSTX_DATA_CA	R	oa_lane2_hstx_data_ca multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f <b>Volatile:</b> true
6:0	OA_LANE2_HSTX_DATA_BC	R	oa_lane2_hstx_data_bc multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_R\_AFE\_LANE2\_CTRL\_3\_11**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x143b

Bits	Name	Memory Access	Description
15:14	O_LANE2_GPIO_OUT	R	<p>oa_lane2_gpio_out multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
13	OA_LANE2_HSRX_CPHY_MASK_CHANGE	R	<p>oa_lane2_hsrx_cphy_mask_change multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
12	OA_LANE2_HSRX_CPHY_CDR_FBK_EN	R	<p>oa_lane2_hsrx_cphy_cdr_fbk_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
11:10	OA_LANE2_LPRX_ULP_PON	R	<p>oa_lane2_lprx_ulp_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
9:8	OA_LANE2_LPRX_CD_PON	R	<p>oa_lane2_lprx_cd_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
7:6	OA_LANE2_LPRX_LP_PON	R	<p>oa_lane2_lprx_lp_pon multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
5:4	OA_LANE2_LPTX_PULLDWN_EN	R	<p>oa_lane2_lptx_pulldwn_en multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>

3:2	OA_LANE2_LPTX_PON	R	oa_lane2_lptx_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
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1:0	OA_LANE2_LPTX_EN	R	oa_lane2_lptx_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
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**CORE\_DIG IOCTL\_R\_AFE\_LANE2\_CTRL\_3\_12**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x143c

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:13	OA_LANE2_HSRX_EN	R	oa_lane2_hsrx_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

12:11	OA_LANE2_HSRX_PON	R	oa_lane2_hsrx_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
10	OA_LANE2_HSRX_CPHY_ALP_DET_LEFT_PON	R	oa_lane2_hsrx_cphy_alp_det_left_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

9	OA_LANE2_HSRX_CPHY_ALP_DETECT_RIGHT_PON	R	oa_lane2_hsrx_cphy_alp_det_right_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
8	OA_LANE2_HSRX_VCM_DET_OUTPUT_EN	R	oa_lane2_hsrx_vcm_det_out_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
7	OA_LANE2_HSRX_VCM_DET_PON	R	oa_lane2_hsrx_vcm_det_pon multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
6	OA_LANE2_HSRX_OFFCAL_OBS_EN	R	oa_lane2_hsrx_offcal_obs_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

5	OA_LANE2_HSRX_DESERIALIZE_R_DIV_EN	R	oa_lane2_hsrx_deserializer_div_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
4	OA_LANE2_HSRX_DESERIALIZE_R_DATA_EN	R	oa_lane2_hsrx_deserializer_data_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	OA_LANE2_HSRX_DESERIALIZE_R_EN	R	oa_lane2_hsrx_deserializer_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

2	OA_LANE2_HSRX_HS_CLK_DIV_EN	R	oa_lane2_hsrx_hs_clk_div_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	OA_LANE2_HSRX_TERM_LEFT_EN	R	oa_lane2_hsrx_term_left_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	OA_LANE2_HSRX_TERM_RIGHT_EN	R	oa_lane2_hsrx_term_right_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE2\_CTRL\_3\_13**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x143d

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
8:5	OA_LANE2_HSRX_DPHY_DATA_DELAY	R	oa_lane2_hsrx_dphy_data_delay multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true

4	OA_LANE2_HSRX_DPHY_PREAMBLE_CAL_EN	R	oa_lane2_hsrx_dphy_preamble_cal_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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3	OA_LANE2_HSRX_DPHY_DLL_E_N	R	oa_lane2_hsrx_dphy_dll_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	OA_LANE2_HSRX_DPHY_DLL_P_HASE_CHANGE	R	oa_lane2_hsrx_dphy_ddl_phase_change multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	OA_LANE2_HSRX_DPHY_DLL_BYPASS_EN	R	oa_lane2_hsrx_dphy_ddl_bypass_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	OA_LANE2_HSRX_DPHY_DLL_BIAS_BYPASS_EN	R	oa_lane2_hsrx_dphy_ddl_bias_bypass_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG IOCTL\_R\_AFE\_LANE2\_CTRL\_3\_14**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x143e

Bits	Name	Memory Access	Description
15:10	OA_LANE2_HSRX_DPHY_DLL_F_BK	R	oa_lane2_hsrx_dphy_dll_fbk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f <b>Volatile:</b> true
9:8	OA_LANE2_HSRX_DPHY_DLL_TUNE_MODE	R	oa_lane2_hsrx_dphy_ddl_tune_mode multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

7:4	OA_LANE2_HSRX_DPHY_DDL_C OARSE_BANK	R	oa_lane2_hsrx_dphy_ddl_coarse_bank multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true
3:0	OA_LANE2_HSRX_DPHY_DDL_B IAS	R	oa_lane2_hsrx_dphy_ddl_bias multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE2\_CTRL\_3\_15**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x143f

Bits	Name	Memory Access	Description
15:8	OA_LANE2_HSRX_OFFCAL_LEFT	R	oa_lane2_hsrx_offcal_left multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
7:0	OA_LANE2_HSRX_OFFCAL_RIGHT	R	oa_lane2_hsrx_offcal_right multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE2\_CTRL\_4\_0**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x1440

Bits	Name	Memory Access	Description

15:8	OA_LANE2_HSRX_DPHY_DDL_P HASE_MID	R	oa_lane2_hsrx_dphy_ddl_phase_mid (bits [7:0]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
7:0	OA_LANE2_HSRX_DPHY_DDL_P HASE_RIGHT	R	oa_lane2_hsrx_dphy_ddl_phase_right (bits [7:0]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_LANE2\_CTRL\_4\_1**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x1441

Bits	Name	Memory Access	Description
15	OA_LANE2_LVDS_OFFSET_EN	R	oa_lane2_lvds_offset_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
14	OA_LANE2_LVDS_HYST_EN	R	oa_lane2_lvds_hyst_en multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

13:11	OA_LANE2_HSRX_MODE	R	oa_lane2_hsrx_mode multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7 <b>Volatile:</b> true
10	OA_LANE2_HSRX_DPHY_DDL_P HASE_RIGHT	R	oa_lane2_hsrx_dphy_ddl_phase_right (bit [8]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

9	OA_LANE2_HSRX_DPHY_DDL_P HASE_MID	R	oa_lane2_hsrx_dphy_ddl_phase_mid (bit [8]) multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
8:0	OA_LANE2_HSRX_DPHY_DDL_P HASE_LEFT	R	oa_lane2_hsrx_dphy_ddl_phase_left multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_R\_AFE\_LANE2\_CTRL\_4\_2**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x1442

Bits	Name	Memory Access	Description
15:8	IA_LANE2_HSRX_DATA_BC_MID _INT	R	ia_lane2_hsrx_data_bc_mid multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
7:0	IA_LANE2_HSRX_DATA_AB_LEF T_INT	R	ia_lane2_hsrx_data_ab_left multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true

**CORE\_DIG\_IOCtrl\_R\_AFE\_LANE2\_CTRL\_4\_3**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x1443

Bits	Name	Memory Access	Description

15	IA_LANE2_HSRX_OUT_CAL_RIGHT_P_INT	R	ia_lane2_hsrx_out_cal_right_p multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
14	IA_LANE2_HSRX_OUT_CAL_RIGHT_N_INT	R	ia_lane2_hsrx_out_cal_right_n multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

13	IA_LANE2_HSRX_OUT_CAL_LEFT_P_INT	R	ia_lane2_hsrx_out_cal_left_p multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
12	IA_LANE2_HSRX_OUT_CAL_LEFT_N_INT	R	ia_lane2_hsrx_out_cal_left_n multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
11	IA_LANE2_HSRX_VCM_DET_OUT_INT	R	ia_lane2_hsrx_vcm_det_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
10	IA_LANE2_HSTX_WORD_CLK_IN_T	R	ia_lane2_hstx_word_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
9	IA_LANE2_HSRX_HS_CLK_DIV_OUT_INT	R	ia_lane2_hsrx_hs_clk_div_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

8	IA_LANE2_HSRX_WORD_CLK_INT	R	ia_lane2_hsrx_word_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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7:0	IA_LANE2_HSRX_DATA_CA_RIGHT_INT	R	ia_lane2_hsrx_data_ca_right multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff <b>Volatile:</b> true
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**CORE\_DIG IOCTL\_R\_AFE\_LANE2\_CTRL\_4\_4**

- **Description:** Analog macro lane 2 observability
- **Size:** 16 bits
- **Offset:** 0x1444

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:12	IA_LANE2_GPI_OUT	R	ia_lane2_gpi_out[0] multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

11:10	IA_LANE2_SPARE_OUT_INT	R	ia_lane2_spare_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
9:8	IA_LANE2_LPRX_DOUTULP_INT	R	ia_lane2_lprx_doutulp multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true

7:6	IA_LANE2_LPRX_DOUTLP_INT	R	ia_lane2_lprx_doutlp multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
5:4	IA_LANE2_LPRX_DOUTCD_INT	R	ia_lane2_lprx_doutcd multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
3	IA_LANE2_HSRX_CPHY_CDR_OSC_CLK_INT	R	ia_lane2_hsrx_cphy_cdr_osc_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	IA_LANE2_HSRX_CPHY_ALP_DET_RIGHT_OUT_INT	R	ia_lane2_hsrx_cphy_alp_det_right_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

1	IA_LANE2_HSRX_CPHY_ALP_DET_LEFT_OUT_INT	R	ia_lane2_hsrx_cphy_alp_det_left_out multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	IA_LANE2_HSRX_DPHY_DDL_OSC_CLK_INT	R	ia_lane2_hsrx_dphy_ddl_osc_clk multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_RW\_DPHY\_PPI\_CLK\_OVR\_0\_0**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1a00

Bits	Name	Memory Access	Description

15	I_DPHY_RX_CLK_AG_OVR_EN	R/W	i_dphy_rx_clk_ag override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14:12	I_DPHY_RX_CLK_AG_OVR_VAL	R/W	i_dphy_rx_clk_ag override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
11	O_TXHSIDLECLKREADYHS_OVR_VAL	R/W	o_txhsidleclkreadyhs override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

10	I_TXHSIDLECLKHS_OVR_VAL	R/W	i_txhsidleclkhs override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	I_TXULPSEXIT_DCK_OVR_VAL	R/W	i_txulpsexit_dck override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	I_TXULPSCLK_DCK_OVR_VAL	R/W	i_txulpsclk_dck override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	I_FORCERXMODE_DCK_OVR_VAL	R/W	i_forcerxmode_dck override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	I_FORCESTOPMODE_DCK_OVR_VAL	R/W	i_forcestopmode_dck override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	I_TXREQUESTHS_DCK_OVR_VAL	R/W	i_txrequesths_dck override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	O_RXCLKACTIVEHS_DCK_OVR_VAL	R/W	o_rxclkactivehs_dck override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

3	O_RXULPSCLKNOT_DCK_OVR_VAL	R/W	<p>o_rxulpsclknot_dck override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	O_ULPSACTIVENOT_DCK_OVR_VAL	R/W	<p>o_ulpsactivenot_dck override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

1	O_STOPSTATE_DCK_OVR_VAL	R/W	<p>o_stopstate_dck override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	I_ENABLE_DCK_OVR_VAL	R/W	<p>i_enable_dck override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

#### CORE\_DIG IOCTL\_RW\_DPHY\_PPI\_CLK\_OVR\_0\_1

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1a01

Bits	Name	Memory Access	Description
15	O_DPHY_RX_CLK_AG_OVR_EN	R/W	<p>o_dphy_rx_clk_ag override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14:12	O_DPHY_RX_CLK_AG_OVR_VAL	R/W	<p>o_dphy_rx_clk_ag override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
11	O_TXHSIDLECLKREADYHS_OVR_EN	R/W	<p>o_txhsidleclkreadyhs override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

10	I_TXHSIDLECLKHS_OVR_EN	R/W	i_txhsidleclkhs override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	I_TXULPSEXIT_DCK_OVR_EN	R/W	i_txulpsexit_dck override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	I_TXULPSCLK_DCK_OVR_EN	R/W	i_txulpsclk_dck override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	I_FORCERXMODE_DCK_OVR_EN	R/W	i_forceremode_dck override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	I_FORCETXSTOPMODE_DCK_OVR_EN	R/W	i_forcestopmode_dck override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	I_TXREQUESTHS_DCK_OVR_EN	R/W	i_txrequesths_dck override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	O_RXCLKACTIVEHS_DCK_OVR_EN	R/W	o_rxclkactivehs_ride enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	O_RXULPSCLKNOT_DCK_OVR_EN	R/W	o_rxulpsclknot_dck override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

2	O_ULPSACTIVENOT_DCK_OVR_EN	R/W	o_ulpsactivenot_dck override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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1	O_STOPSTATE_DCK_OVR_EN	R/W	<p>o_stopstate_dck override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	I_ENABLE_DCK_OVR_EN	R/W	<p>i_enable_dck override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_CLK\_OVR\_0\_2**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1a02

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
11	O_TXHSIDLECLKREADYHS_INT	R	<p>o_txhsidleclkreadyhs override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
10	I_TXHSIDLECLKHS_INT	R	<p>i_txhsidleclkhs override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

9	I_TXULPSEXIT_DCK_INT	R	<p>i_txulpsexit_dck override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
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8	I_TXULPSCLK_DCK_INT	R	i_txulpsclk_dck override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
7	I_FORCERXMODE_DCK_INT	R	i_forcerxmode_dck override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
6	I_FORCETXSTOPMODE_DCK_IN T	R	i_force(txstopmode_dck) override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
5	I_TXREQUESTHS_DCK	R	i_txrequesths_dck override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
4	O_RXCLKACTIVEHS_DCK_INT	R	o_rxclkactivehs_dck_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

3	O_RXULPSCLKNOT_DCK	R	o_rxulpsclknot_dck override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	O_ULPSACTIVENOT_DCK	R	o_ulpsactivenot_dck override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

1	O_STOPSTATE_DCK	R	<p><code>o_stopstate_dck</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
0	I_ENABLE_DCK_INT	R	<p><code>i_enable_dck_int</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_DPHY\_PPI\_CLK\_OVR\_0\_3**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1a03

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
5:3	O_DPHY_RX_CLK_AG_INT	R	<p><code>o_dphy_rx_clk_ag</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>
2:0	I_DPHY_RX_CLK_AG_INT	R	<p><code>i_dphy_rx_clk_ag</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_RW\_COMMON\_PPI\_OVR\_0\_0**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c00

Bits	Name	Memory Access	Description

15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11	I_RX_TX_N_OVR_VAL	R/W	i_rx_tx_n override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	O_PHY_CALIB_OUT_OVR_EN	R/W	o_phy_calib_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

9	I_PHY_CALIB_IN_OVR_EN	R/W	i_phy_calib_in override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	I_PHY_STATE_OVR_EN	R/W	i_phy_state override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	O_MON_OUT_VALID_OVR_VAL	R/W	o_mon_out_valid override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	O_OCLA_CLK_OVR_VAL	R/W	o_ocla_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	I_TEST_STOP_CLK_EN_OVR_VAL	R/W	i_test_stop_clk_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	I_CONT_EN_OVR_VAL	R/W	i_cont_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	I_PHY_MODE_OVR_VAL	R/W	i_phy_mode override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

2	I_RST_N_OVR_VAL	R/W	i_rst_n override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	I_TXCLKESC_OVR_VAL	R/W	i_txclkesc override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

0	I_CFG_CLK_OVR_VAL	R/W	i_cfg_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG IOCTL\_RW\_COMMON\_PPI\_OVR\_0\_1**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c01

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11	I_RX_TX_N_OVR_EN	R/W	i_rx_tx_n override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	O_DTB_OUT_OVR_EN	R/W	o_dtb_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

9	O_CONT_DATA_OVR_EN	R/W	o_cont_data override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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8	O_MON_OUT_OVR_EN	R/W	<p>o_mon_out override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7	O_MON_OUT_VALID_OVR_EN	R/W	<p>o_mon_out_valid override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	O_OCLA_CLK_OVR_EN	R/W	<p>o_ocla_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
5	I_TEST_STOP_CLK_EN_OVR_EN	R/W	<p>i_test_stop_clk_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	I_CONT_EN_OVR_EN	R/W	<p>i_cont_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3	I_PHY_MODE_OVR_EN	R/W	<p>i_phy_mode override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	I_RST_N_OVR_EN	R/W	<p>i_rst_n override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

1	I_TXCLKESC_OVR_EN	R/W	<p>i_txclkesc override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	I_CFG_CLK_OVR_EN	R/W	<p>i_cfg_clk override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_IOCTRL\_RW\_COMMON\_PPI\_OVR\_0\_2**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c02

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11:5	O_CONT_DATA_OVR_VAL	R/W	o_cont_data override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f
4:0	I_PHY_STATE_OVR_VAL	R/W	i_phy_state override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f

**CORE\_DIG\_IOCTRL\_RW\_COMMON\_PPI\_OVR\_0\_3**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c03

Bits	Name	Memory Access	Description
15:0	I_PHY_CALIB_IN_OVR_VAL	R/W	i_phy_calib_in[15:0] override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_IOCTRL\_RW\_COMMON\_PPI\_OVR\_0\_4**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c04

Bits	Name	Memory Access	Description

15:0	I_PHY_CALIB_IN_OVR_VAL	R/W	i_phy_calib_in[31:16] override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**CORE\_DIG\_IODELAY\_RW\_COMMON\_PPI\_OVR\_0\_5**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c05

Bits	Name	Memory Access	Description
15:8	O_DTB_OUT_OVR_VAL	R/W	o_phy_calib_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	I_PHY_CALIB_IN_OVR_VAL	R/W	i_phy_calib_in[39:32] override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_IODELAY\_RW\_COMMON\_PPI\_OVR\_0\_6**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c06

Bits	Name	Memory Access	Description
15:0	O_PHY_CALIB_OUT_OVR_VAL	R/W	o_phy_calib_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_IODELAY\_RW\_COMMON\_PPI\_OVR\_0\_7**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c07

Bits	Name	Memory Access	Description
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15:0	O_MON_OUT_OVR_VAL	R/W	<p><b>o_mon_out[15:0]</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>
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**CORE\_DIG\_IOCTRL\_RW\_COMMON\_PPI\_OVR\_0\_8**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c08

Bits	Name	Memory Access	Description
15:0	O_MON_OUT_OVR_VAL	R/W	<p><b>o_mon_out[31:16]</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCTRL\_RW\_COMMON\_PPI\_OVR\_0\_9**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c09

Bits	Name	Memory Access	Description
15:0	O_MON_OUT_OVR_VAL	R/W	<p><b>o_mon_out[47:32]</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCTRL\_RW\_COMMON\_PPI\_OVR\_0\_10**

- **Description:** Digital hard macro interface override
- **Size:** 16 bits
- **Offset:** 0x1c0a

Bits	Name	Memory Access	Description
15:0	O_MON_OUT_OVR_VAL	R/W	<p><b>o_mon_out[63:48]</b> override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_0\_11**

- **Description:** Digital hard macro interface observability

- **Size:** 16 bits
- **Offset:** 0x1c0b

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
8	I_RX_TX_N	R	<p>i_rx_tx_n override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
7	O_MON_OUT_VALID	R	<p>o_mon_out_valid override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

6	O_OCLA_CLK	R	<p>o_ocla_clk override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
5	I_TEST_STOP_CLK_EN_INT	R	<p>i_test_stop_clk_en override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
4	I_CONT_EN_INT	R	<p>i_cont_en override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>

3	I_PHY_MODE_INT	R	i_phy_mode override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	I_RST_N_INT	R	i_rst_n override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	I_TXCLKESC_INT	R	i_txclkesc override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

0	I_CFG_CLK_INT	R	i_cfg_clk override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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**CORE\_DIG\_IODEV\_R\_COMMON\_PPI\_OVR\_0\_12**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c0c

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11:5	O_CONT_DATA	R	o_cont_data override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f <b>Volatile:</b> true

4:0	I_PHY_STATE_INT	R	i_phy_state override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f <b>Volatile:</b> true
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**CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_0\_13**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c0d

Bits	Name	Memory Access	Description
15:0	I_PHY_CALIB_IN_INT	R	i_phy_calib_in override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_0\_14**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c0e

Bits	Name	Memory Access	Description
15:0	I_PHY_CALIB_IN_INT	R	i_phy_calib_in override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff <b>Volatile:</b> true

**CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_0\_15**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c0f

Bits	Name	Memory Access	Description

15:8	O_DTB_OUT	R	<p><code>o_dtb_out</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>
7:0	I_PHY_CALIB_IN_INT	R	<p><code>i_phy_calib_in</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_1\_0**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c10

Bits	Name	Memory Access	Description
15:0	O_PHY_CALIB_OUT	R	<p><code>o_phy_calib_out</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_1\_1**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c11

Bits	Name	Memory Access	Description
15:0	O_MON_OUT	R	<p><code>o_mon_out</code> override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p> <p><b>Volatile:</b> true</p>

**CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_1\_2**

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits

- **Offset:** 0x1c12

Bits	Name	Memory Access	Description
15:0	O_MON_OUT	R	<p>o_mon_out override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b></p> <p>0xffff <b>Volatile:</b> true</p>

#### CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_1\_3

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c13

Bits	Name	Memory Access	Description
15:0	O_MON_OUT	R	<p>o_mon_out override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b></p> <p>0xffff <b>Volatile:</b> true</p>

#### CORE\_DIG\_IOCTRL\_R\_COMMON\_PPI\_OVR\_1\_4

- **Description:** Digital hard macro interface observability
- **Size:** 16 bits
- **Offset:** 0x1c14

Bits	Name	Memory Access	Description
15:0	O_MON_OUT	R	<p>o_mon_out override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b></p> <p>0xffff <b>Volatile:</b> true</p>

#### CORE\_DIG\_IOCTRL\_RW\_AFE\_CB\_CTRL\_2\_0

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c20

Bits	Name	Memory Access	Description
15	OA_CB_HSTXLB_DCO_CLK90_EN_OVR_VAL	R/W	<p>oa_cb_hstxlb_dco_clk90_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	OA_CB_ATB_SEL_DAC_OVR_EN	R/W	<p>oa_cb_atb_sel_dac override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

13	OA_CB_VPCLK_REG_PON_OVR_VAL	R/W	<p>oa_cb_vpclk_reg_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	OA_CB_AMP1200_PON_OVR_VAL	R/W	<p>oa_cb_amp1200_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_CB_IBIAS_PON_OVR_VAL	R/W	<p>oa_cb_ibias_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10	OA_CB_HSTX_VCOMM_REG_PON_OVR_VAL	R/W	<p>oa_cb_hstx_vcomm_reg_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	OA_CB_ATB_COMP_PON_OVR_VAL	R/W	<p>oa_cb_atb_comp_pon override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	OA_CB_CAL_DOWN_EN_OVR_VAL	R/W	<p>oa_cb_cal_down_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

7	OA_CB_CAL_UP_EN_OVR_VAL	R/W	oa_cb_cal_up_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	OA_CB_CAL_PON_OVR_VAL	R/W	oa_cb_cal_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

5	OA_CB_BG_PON_OVR_VAL	R/W	oa_cb_bg_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_CB_PON_OVR_VAL	R/W	oa_cb_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_CB_CHOP_CLK_EN_OVR_VAL	R/W	oa_cb_chop_clk_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_CB_CHOP_CLK_OVR_VAL	R/W	oa_cb_chop_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_CB_ATB_CLK_OVR_VAL	R/W	oa_cb_atb_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_SEL_CPHY_DPHY_OVR_VAL	R/W	oa_sel_cphy_dphy override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ICTRL\_RW\_AFE\_CB\_CTRL\_2\_1**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c21

Bits	Name	Memory Access	Description
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15	OA_CB_HSTXLB_DCO_CLK0_EN_OVR_VAL	R/W	oa_cb_hstxlb_dco_clk0_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	OA_CB_ATB_SEL_OVR_EN	R/W	oa_cb_atb_sel override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13	OA_CB_VPCLK_REG_PON_OVR_EN	R/W	oa_cb_vpclk_reg_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_CB_AMP1200_PON_OVR_EN	R/W	oa_cb_amp1200_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	OA_CB_IBIAS_PON_OVR_EN	R/W	oa_cb_ibias_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	OA_CB_HSTX_VCOMM_REG_PON_OVR_EN	R/W	oa_cb_hstx_vcomm_reg_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_CB_ATB_COMP_PON_OVR_EN	R/W	oa_cb_atb_comp_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_CB_CAL_DOWN_EN_OVR_EN	R/W	oa_cb_cal_down_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_CB_CAL_UP_EN_OVR_EN	R/W	oa_cb_cal_up_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

6	OA_CB_CAL_PON_OVR_EN	R/W	oa_cb_cal_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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5	OA_CB_BG_PON_OVR_EN	R/W	oa_cb_bg_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	OA_CB_PON_OVR_EN	R/W	oa_cb_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	OA_CB_CHOP_CLK_EN_OVR_EN	R/W	oa_cb_chop_clk_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_CB_CHOP_CLK_OVR_EN	R/W	oa_cb_chop_clk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_CB_ATB_CLK_OVR_EN	R/W	oa_cb_atb_clk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_SEL_CPHY_DPHY_OVR_EN	R/W	oa_sel_cphy_dphy override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IODEV\_R\_W\_AFE\_CB\_CTRL\_2\_2**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c22

Bits	Name	Memory Access	Description
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15	OA_CB_PLL_BUSTIEZ	R/W	Enable for grounding PLL input phases (0 and 90). Active low. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	OA_CB_ATB_PROBE_VBE_EN	R/W	Enable to perform temperature measurement through ATB. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13	OA_CB_ATB_PROBE_BOOST_E_N	R/W	Enable to use boost vctrl as input for ATB comparator. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

12	OA_CB_ATB_EXT_CON	R/W	Enable allowing to directly connect ATB line to ATB pin. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11:10	OA_CB_ATB_SEL_OVR_VAL	R/W	oa_cb_atb_sel override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9:0	OA_CB_ATB_SEL_DAC_OVR_VAL	R/W	oa_cb_atb_sel_dac override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff

**CORE\_DIG\_ICTRL\_RW\_AFE\_CB\_CTRL\_2\_3**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c23

Bits	Name	Memory Access	Description
15	OA_CB_HSTX_VCOMM_REG_ST_BON	R/W	Enable of internal stability loop for HS-TX vcomm regulator. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

14:12	OA_CB_HSTX_BOOST_PROG	R/W	HSTX boost current programmability. Check table for more details. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
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11:10	OA_CB_HSTXLB_DCO_SEL_DIV	R/W	Divider configuration used in the generation of HSTX loopback phases (0 and 90). <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9	OA_CB_HSTXLB_DCO_CLK90_EN_OVR_EN	R/W	oa_cb_hstxlb_dco_clk90_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_CB_HSTXLB_DCO_CLK0_EN_OVR_EN	R/W	oa_cb_hstxlb_dco_clk0_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	OA_CB_SEL_HSTXLB_DCO_VREF	R/W	Source of reference used in HSTX loopback DCO. 0 : mpill_vref ; 1 : ATB DAC <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6:4	OA_CB_SEL_MPILL_REG_VREF	R/W	Programmable voltage reference for MPILL regulator. Check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
3:1	OA_SEL_LPTX_PROG	R/W	LP-TX bias current programmability. Check table for more details. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
0	OA_CB_SEL_LPTX_VREF	R/W	Programmability for LP-TX driver amplitude. 0 : 1200mV ; 1 : 1100mV. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCtrl\_RW\_AFE\_CB\_CTRL\_2\_4**

- **Description:** Analog macro common block control
- **Size:** 16 bits

- **Offset:** 0x1c24

Bits	Name	Memory Access	Description
15	OA_CB_CAL_SINK_EN_OVR_VA L	R/W	<p>oa_cb_cal_sink_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	OA_CB_VCOMM_UNTERM_MOD E	R/W	<p>Selector control for unterminated mode. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13:11	OA_CB_SEL_VCOMM_PROG	R/W	<p>Programmability of HS-TX driver amplitude.</p> <p><b>Value After Reset:</b> 0x4</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

10:9	OA_CB_SEL_HSRX_CM_DET_V REF	R/W	<p>Programmability of used reference voltage in common mode detector. Check table for more details.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
8:6	OA_CB_SEL_TRI02_ALP_VREF	R/W	<p>ALP pause wake up detector sign and offset magnitude control for trio2. Check table for more details.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
5:3	OA_CB_SEL_TRI01_ALP_VREF	R/W	<p>ALP pause wake up detector sign and offset magnitude control for trio1. Check table for more details.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
2:0	OA_CB_SEL_TRI00_ALP_VREF	R/W	<p>ALP pause wake up detector sign and offset magnitude control for trio0. Check table for more details.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

## CORE\_DIG\_ICTRL\_RW\_AFE\_CB\_CTRL\_2\_5

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c25

Bits	Name	Memory Access	Description
15	OA_CB_CAL_SINK_EN_OVR_EN	R/W	oa_cb_cal_sink_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	OA_CB_SEL_EXT_INT_CHOP_C_LK	R/W	Source selector for chop clock used under bandgap circuit : 0 - internal clock from dco; 1 - external clock from cb_refclk <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13:12	OA_CB_DSK_CLK_CHANNEL	R/W	Programmability for D-PHY Internal deskew clock channel. Check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

11:10	OA_CB_VPCLK_REG_MODE	R/W	Vpclk regulator mode.. Check table for more details. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9	OA_CB_REXT_IOCNT_EN_OVR_VAL	R/W	oa_cb_rext_iocnt_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_CB_SEL_450HM_500HM	R/W	Programmability of tuning resistance used in calibration: 0- 50 ohms; 1- 45 ohms <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:4	OA_SETR_CALIB_VT	R/W	Vt drift control for termination. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	OA_CB_SPARE_IN	R/W	Spare pins reserved for analog macro common block control <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_IOCTRL\_RW\_AFE\_CB\_CTRL\_2\_6**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c26

Bits	Name	Memory Access	Description
15	OA_CB_REXT_IOCNT_EN_OVR_EN	R/W	<p>oa_cb_rext_iocnt_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
14	OA_CB_HSTXLB_DCO_TUNECLKDIG_EN_OVR_EN	R/W	<p>oa_cb_hstxlb_dco_tune_clkdig_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

13	OA_CB_HSTXLB_DCO_EN_OVR_EN	R/W	<p>oa_cb_hstxlb_dco_en override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	OA_CB_HSTXLB_DCO_PON_OVR_EN	R/W	<p>oa_cb_hstxlb_dco_pon override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11	OA_CB_HSTXLB_DCO_FWORD_OVR_EN	R/W	<p>oa_cb_hstxlb_dco_fword override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
10:4	OA_CB_LP_DCO_FWORD_OVR_VAL	R/W	<p>oa_cb_lp_dco_fword override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7f</p>
3	OA_CB_LP_DCO_FWORD_CHANGE_OVR_VAL	R/W	<p>oa_cb_lp_dco_fword_change override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	OA_CB_LP_DCO_CLK_EN_OVR_VAL	R/W	<p>oa_cb_lp_dco_clk_en override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

1	OA_CB_LP_DCO_EN_OVR_VAL	R/W	oa_cb_lp_dco_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_CB_LP_DCO_PON_OVR_VAL	R/W	oa_cb_lp_dco_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG IOCTL\_RW\_AFE\_CB\_CTRL\_2\_7**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c27

Bits	Name	Memory Access	Description
15	OA_CB_DSK_CLK_MODE_OVR_EN	R/W	oa_cb_dsk_clk_mode override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	OA_SETRB_OVR_EN	R/W	oa_setrb override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13	OA_SETRA_OVR_EN	R/W	oa_setra override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	OA_SETR_CALIB_OVR_EN	R/W	oa_setr_calib override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
11	OA_SETR_OVR_EN	R/W	oa_setr override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

10	OA_CB_HSTXLB_DCO_TUNE_C_LKDIG_EN_OVR_VAL	R/W	oa_cb_hstxlb_dco_tune_clkdig_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	OA_CB_HSTXLB_DCO_EN_OVR_VAL	R/W	oa_cb_hstxlb_dco_en override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	OA_CB_HSTXLB_DCO_PON_OVR_VAL	R/W	oa_cb_hstxlb_dco_pon override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:5	OA_CB_HSTXLB_DCO_FWORD_OVR_VAL	R/W	oa_cb_hstxlb_dco_fword override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
4	OA_CB_LP_DCO_FWORD_OVR_EN	R/W	oa_cb_lp_dco_fword override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

3	OA_CB_LP_DCO_FWORD_CHANGE_OVR_EN	R/W	oa_cb_lp_dco_fword_change override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	OA_CB_LP_DCO_CLK_EN_OVR_EN	R/W	oa_cb_lp_dco_clk_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	OA_CB_LP_DCO_EN_OVR_EN	R/W	oa_cb_lp_dco_en override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	OA_CB_LP_DCO_PON_OVR_EN	R/W	oa_cb_lp_dco_pon override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IOCtrl\_Rw\_AFE\_CB\_CTRL\_2\_8**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c28

Bits	Name	Memory Access	Description
15:14	OA_CB_DSK_CLK_MODE_OVR_VAL	R/W	oa_cb_dsk_clk_mode override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
13:11	OA_SETRB_OVR_VAL	R/W	oa_setrb override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
10:8	OA_SETRA_OVR_VAL	R/W	oa_setra override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

7:4	OA_SETR_CALIB_OVR_VAL	R/W	oa_setr_calib override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	OA_SETR_OVR_VAL	R/W	oa_setr override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_IOCtrl\_Rw\_AFE\_CB\_CTRL\_2\_9**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c29

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

9:6	IA_CB_SPARE_OUT_OVR_VAL	R/W	ia_cb_spare_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
5	IA_CB_REXT_IOCNT_OVR_VAL	R/W	ia_cb_rext_iocnt override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	IA_CB_LP_DCO_CLK_OVR_VAL	R/W	ia_cb_lp_dco_clk override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

3	IA_CB_HSTXLB_CLKDIG_OVR_VAL	R/W	ia_cb_hstxlb_clkdig override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_CB_DET_VPH_OVR_VAL	R/W	ia_cb_det_vph override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_CB_DET_VP_OVR_VAL	R/W	ia_cb_det_vp override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	IA_CB_ATB_COMP_OUT_OVR_VAL	R/W	ia_cb_atb_comp_out override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG IOCTL\_RW\_AFE\_CB\_CTRL\_2\_10**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c2a

Bits	Name	Memory Access	Description
15:7	RESERVED_15_7	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

6	IA_CB_SPARE_OUT_OVR_EN	R/W	ia_cb_spare_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	IA_CB_REXT_IOCONT_OVR_EN	R/W	ia_cb_rext_iocont override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

4	IA_CB_LP_DCO_CLK_OVR_EN	R/W	ia_cb_lp_dco_clk override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	IA_CB_HSTXLB_CLKDIG_OVR_EN	R/W	ia_cb_hstxlb_clkdig override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	IA_CB_DET_VPH_OVR_EN	R/W	ia_cb_det_vph override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	IA_CB_DET_VP_OVR_EN	R/W	ia_cb_det_vp override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	IA_CB_ATB_COMP_OUT_OVR_EN	R/W	ia_cb_atb_comp_out override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_IODEV\_R\_W\_AFE\_CB\_CTRL\_2\_11**

- **Description:** Analog macro common block control
- **Size:** 16 bits
- **Offset:** 0x1c2b

Bits	Name	Memory Access	Description
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15:3	RESERVED_15_3	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
2:0	OA_CB_VP2_PROG	R/W	Programmability for the reference voltage used for biasing. Check table for more details. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_IOCTRL\_R\_AFE\_CB\_CTRL\_2\_12**

- **Description:** Analog macro common block observability
- **Size:** 16 bits
- **Offset:** 0x1c2c

Bits	Name	Memory Access	Description
15	OA_CB_REXT_IOCNT_EN	R	oa_cb_rext_iocnt_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
14	OA_CB_HSTXLB_DCO_CLK90_E_N	R	oa_cb_hstxlb_dco_clk90_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
13	OA_CB_VPCLK_REG_PON	R	oa_cb_vpclk_reg_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

12	OA_CB_AMP1200_PON	R	oa_cb_amp1200_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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11	OA_CB_IBIAS_PON	R	oa_cb_ibias_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
10	OA_CB_HSTX_VCOMM_REG_P ON	R	oa_cb_hstx_vcomm_reg_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
9	OA_CB_ATB_COMP_PON	R	oa_cb_atb_comp_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
8	OA_CB_CAL_DOWN_EN	R	oa_cb_cal_down_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
7	OA_CB_CAL_UP_EN	R	oa_cb_cal_up_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

6	OA_CB_CAL_PON	R	oa_cb_cal_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
5	OA_CB_BG_PON	R	oa_cb_bg_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

4	OA_CB_PON	R	oa_cb_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	OA_CB_CHOP_CLK_EN	R	oa_cb_chop_clk_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	OA_CB_CHOP_CLK	R	oa_cb_chop_clk override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	OA_CB_ATB_CLK	R	oa_cb_atb_clk override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

0	OA_SEL_CPHY_DPHY	R	oa_sel_cphy_dphy override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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**CORE\_DIG\_IOCTRL\_R\_AFE\_CB\_CTRL\_2\_13**

- **Description:** Analog macro common block observability
- **Size:** 16 bits
- **Offset:** 0x1c2d

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

14	OA_CB_HSTXLB_DCO_TUNE_C_LKDIG_EN	R	oa_cb_hstxlb_dco_tune_clkdig_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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13	OA_CB_HSTXLB_DCO_CLK0_EN	R	oa_cb_hstxlb_dco_clk0_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
12	OA_CB_CAL_SINK_EN	R	oa_cb_cal_sink_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
11:10	OA_CB_ATB_SEL	R	oa_cb_atb_sel override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3 <b>Volatile:</b> true
9:0	OA_CB_ATB_SEL_DAC	R	oa_cb_atb_sel_dac override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3ff <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_CB\_CTRL\_2\_14**

- **Description:** Analog macro common block observability
- **Size:** 16 bits
- **Offset:** 0x1c2e

Bits	Name	Memory Access	Description
15	OA_CB_HSTXLB_DCO_EN	R	oa_cb_hstxlb_dco_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

14	OA_CB_HSTXLB_DCO_PON	R	oa_cb_hstxlb_dco_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
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13:11	OA_CB_HSTXLB_DCO_FWORD	R	oa_cb_hstxlb_dco_fword override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7 <b>Volatile:</b> true
10:4	OA_CB_LP_DCO_FWORD	R	oa_cb_lp_dco_fword override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f <b>Volatile:</b> true
3	OA_CB_LP_DCO_FWORD_CHANGE	R	oa_cb_lp_dco_fword_change override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	OA_CB_LP_DCO_CLK_EN	R	oa_cb_lp_dco_clk_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	OA_CB_LP_DCO_EN	R	oa_cb_lp_dco_en override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
0	OA_CB_LP_DCO_PON	R	oa_cb_lp_dco_pon override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

**CORE\_DIG\_ICTRL\_R\_AFE\_CB\_CTRL\_2\_15**

- **Description:** Analog macro common block observability

- **Size:** 16 bits
- **Offset:** 0x1c2f

Bits	Name	Memory Access	Description
15:14	OA_CB_DSK_CLK_MODE	R	<p>oa_cb_dsk_clk_mode override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p> <p><b>Volatile:</b> true</p>
13:11	OA_SETRB	R	<p>oa_setrb override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>
10:8	OA_SETRA	R	<p>oa_setra override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p> <p><b>Volatile:</b> true</p>

7:4	OA_SETR_CALIB	R	<p>oa_setr_calib override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>
3:0	OA_SETR	R	<p>oa_setr override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p> <p><b>Volatile:</b> true</p>

### CORE\_DIG\_IOCTRL\_R\_AFE\_CB\_CTRL\_3\_0

- **Description:** Analog macro common block observability
- **Size:** 16 bits
- **Offset:** 0x1c30

Bits	Name	Memory Access	Description
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15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:6	IA_CB_SPARE_OUT_INT	R	ia_cb_spare_out_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf <b>Volatile:</b> true
5	IA_CB_REXT_IOCONT_INT	R	ia_cb_rext_iocont_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

4	IA_CB_LP_DCO_CLK_INT	R	ia_cb_lp_dco_clk_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
3	IA_CB_HSTXLB_CLKDIG_INT	R	ia_cb_hstxlb_clkdig_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
2	IA_CB_DET_VPH_INT	R	ia_cb_det_vph_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true
1	IA_CB_DET_VP_INT	R	ia_cb_det_vp_int override multiplexer output. Used for debug purposes. (volatile) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1 <b>Volatile:</b> true

0	IA_CB_ATB_COMP_OUT_INT	R	<p>ia_cb_atb_comp_out_int override multiplexer output. Used for debug purposes. (volatile)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p> <p><b>Volatile:</b> true</p>
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**CORE\_DIG\_RW\_COMMON\_0**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c40

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13:2	HSRX_DPHY_DLL_EN_DLY	R/W	<p>DPHY HSRX DLL enable delay. In dco clock cycles. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>
1	DPHY_RX_CLK_AG_EN	R/W	<p>DPHY RX Aggregation feature enable. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	DPHY_PREAMBLE_EN_REG	R/W	<p>DPHY preamble support enable.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_RW\_COMMON\_1**

- **Description:** OCLA Interface
- **Size:** 16 bits
- **Offset:** 0x1c41

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

5:0	OCLA_DATA_SEL	R/W	All clock domains data enables <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
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**CORE\_DIG\_RW\_COMMON\_2**

- **Description:** OCLA Interface
- **Size:** 16 bits
- **Offset:** 0x1c42

Bits	Name	Memory Access	Description
15:5	RESERVED_15_5	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
4:0	OCLA_DATA_SEL	R/W	All clock domains data enables <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f

**CORE\_DIG\_RW\_COMMON\_3**

- **Description:** OCLA Interface
- **Size:** 16 bits
- **Offset:** 0x1c43

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
5:0	OCLA_CLK_SEL	R/W	All clock domains clock enables <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f

**CORE\_DIG\_RW\_COMMON\_4**

- **Description:** OCLA Interface
- **Size:** 16 bits
- **Offset:** 0x1c44

Bits	Name	Memory Access	Description
15:5	RESERVED_15_5	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
4:0	OCLA_CLK_SEL	R/W	All clock domains clock enables <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f

**CORE\_DIG\_RW\_COMMON\_5**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c45

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:12	WORD_CLK_SEL_CLANE	R/W	CPHY HS-TX word clock common source <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
11:10	WORD_CLK_SEL_DLANE	R/W	DPHY HS-TX word clock common source <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
9	HSRX_DPHY_DLL_EN_DRV	R/W	hsrx_dphy_dll_en data lanes driver (0->clock,1->data) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

8:1	DTB_SELECT	R/W	dtb output mux selector. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
0	INPUT_SAMPLING_REG	R/W	Enables input sampling of AFE data. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_RW\_COMMON\_6**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c46

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
5:3	DESERIALIZER_EN_DEASS_CO UNT_THRESH_D	R/W	<p>Counter for deassertion of deserializer_en of dphy lanes. In dco_clk cycles. Quasi static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

2:0	DESERIALIZER_DIV_EN_DELAY _THRESH_D	R/W	<p>Counter for assertion of deserializer_div_en of dphy lanes. In dco_clk cycles. Quasi static. 0 is a forbidden value.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
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**CORE\_DIG\_RW\_COMMON\_7**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c47

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
5:4	LANE2_HSRX_WORD_CLK_SEL _GATING_REG	R/W	<p>Analog lane 2 word clock gating configuration. Quasi static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
3:2	LANE1_HSRX_WORD_CLK_SEL _GATING_REG	R/W	<p>Analog lane 1 word clock gating configuration. Quasi static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

1:0	LANE0_HSRX_WORD_CLK_SEL_GATING_REG	R/W	Analog lane 0 word clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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**CORE\_DIG\_RW\_COMMON\_8**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c48

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
5	LANE2_HSRX_WORD_CLK_GATING_OVR_VAL	R/W	Analog lane 2 word clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	LANE2_HSRX_WORD_CLK_GATING_OVR_EN	R/W	Analog lane 2 word clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

3	LANE1_HSRX_WORD_CLK_GATING_OVR_VAL	R/W	Analog lane 1 word clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	LANE1_HSRX_WORD_CLK_GATING_OVR_EN	R/W	Analog lane 1 word clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	LANE0_HSRX_WORD_CLK_GATING_OVR_VAL	R/W	Analog lane 0 word clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LANE0_HSRX_WORD_CLK_GATING_OVR_EN	R/W	Analog lane 0 word clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_RW\_COMMON\_9**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c49

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
8	LPRX_DOUTLP_SYNC_SEL	R/W	<p>Select lprx_doutlp synchronization (LP-DCO clock). Active high. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
7:6	HSTXLB_DCO_CLK_SEL_GATIN_G_REG	R/W	<p>HSTXLB DCO clock gating configuration. Quasi static.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

5	HSTXLB_DCO_CLK_GATING_OVR_VAL	R/W	<p>HSTXLB DCO clock gating override value. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	HSTXLB_DCO_CLK_GATING_OVR_EN	R/W	<p>HSTXLB DCO clock gating override enable. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3:2	LP_DCO_CLK_SEL_GATING_REG	R/W	<p>LP DCO clock gating configuration. Quasi static.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
1	LP_DCO_CLK_GATING_OVR_VAL	R/W	<p>LP DCO clock gating override value. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
0	LP_DCO_CLK_GATING_OVR_EN	R/W	<p>LP DCO clock gating override enable. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_RW\_COMMON\_10**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c4a

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
3:2	LANE2_CDROSC_CLK_SEL_GATING_REG	R/W	<p>CDR-OSC lane 2 clock gating configuration. Quasi static.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
1:0	LANE0_CDROSC_CLK_SEL_GATING_REG	R/W	<p>CDR-OSC lane 0 clock gating configuration. Quasi static.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>

**CORE\_DIG\_RW\_COMMON\_11**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c4b

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
3	LANE2_CDROSC_CLK_GATING_OVR_VAL	R/W	<p>CDR-OSC lane 2 clock gating override value. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
2	LANE2_CDROSC_CLK_GATING_OVR_EN	R/W	<p>CDR-OSC lane 2 clock gating override enable. Quasi static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

1	LANE0_CDROSC_CLK_GATING_OVR_VAL	R/W	CDR-OSC lane 0 clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LANE0_CDROSC_CLK_GATING_OVR_EN	R/W	CDR-OSC lane 0 clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_RW\_COMMON\_12**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c4c

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
5:4	LANE2_DDL_OSC_SEL_GATING_REG	R/W	Analog lane 2 ddl osc clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3:2	LANE1_DDL_OSC_SEL_GATING_REG	R/W	Analog lane 1 ddl osc clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
1:0	LANE0_DDL_OSC_SEL_GATING_REG	R/W	Analog lane 0 ddl osc clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

1:0	LANE0_DDL_OSC_SEL_GATING_REG	R/W	Analog lane 0 ddl osc clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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**CORE\_DIG\_RW\_COMMON\_13**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c4d

Bits	Name	Memory Access	Description

15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
5	LANE2_DDL_OSC_GATING_OVR_VAL	R/W	Analog lane 2 ddl osc clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	LANE2_DDL_OSC_GATING_OVR_EN	R/W	Analog lane 2 ddl osc clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

3	LANE1_DDL_OSC_GATING_OVR_VAL	R/W	Analog lane 1 ddl osc clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	LANE1_DDL_OSC_GATING_OVR_EN	R/W	Analog lane 1 ddl osc clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	LANE0_DDL_OSC_GATING_OVR_VAL	R/W	Analog lane 0 ddl osc clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LANE0_DDL_OSC_GATING_OVR_EN	R/W	Analog lane 0 ddl osc clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_RW\_COMMON\_14**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c4e

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

5:4	LANE2_HSTX_WORD_CLK_SEL_GATING_REG	R/W	Analog lane 2 Tx word clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
3:2	LANE1_HSTX_WORD_CLK_SEL_GATING_REG	R/W	Analog lane 1 Tx word clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3

1:0	LANE0_HSTX_WORD_CLK_SEL_GATING_REG	R/W	Analog lane 0 Tx word clock gating configuration. Quasi static. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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**CORE\_DIG\_RW\_COMMON\_15**

- **Description:** Common configuration
- **Size:** 16 bits
- **Offset:** 0x1c4f

Bits	Name	Memory Access	Description
15:6	RESERVED_15_6	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
5	LANE2_HSTX_WORD_CLK_GATING_OVR_VAL	R/W	Analog lane 2 Tx word clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

4	LANE2_HSTX_WORD_CLK_GATING_OVR_EN	R/W	Analog lane 2 Tx word clock gating override enable. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	LANE1_HSTX_WORD_CLK_GATING_OVR_VAL	R/W	Analog lane 1 Tx word clock gating override value. Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

2	LANE1_HSTX_WORD_CLK_GATING_OVR_EN	R/W	Analog lane 1 Tx word clock gating override enable. Quasi static.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	LANE0_HSTX_WORD_CLK_GATING_OVR_VAL	R/W	Analog lane 0 Tx word clock gating override value. Quasi static.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LANE0_HSTX_WORD_CLK_GATING_OVR_EN	R/W	Analog lane 0 Tx word clock gating override enable. Quasi static.  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_ANACTRL\_RW\_COMMON\_ANACTRL\_0**

- **Description:** Power on analog control configuration
- **Size:** 16 bits
- **Offset:** 0x1cf0

Bits	Name	Memory Access	Description
15:14	CB_CHOP_CLK_DIV_SEL	R/W	Select division factor for cb_chop_clk. This field is quasi-static. -2'd0: Division by 1 -2'd1: Division by 2 -2'd2: Division by 4 -2'd3: Not used  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
13:8	CB_LP_DCO_CLK_EN_DLY	R/W	Configurable delay from cb_lp_dco_pon to cb_lp_dco_clk_en. Measured in Config clock cycles. This field is quasi-static.  <b>Value After Reset:</b> 0x1b <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
7:2	CB_LP_DCO_EN_DLY	R/W	Configurable delay from cb_lp_dco_pon to cb_lp_dco_en. Measured in Config clock cycles. This field is quasi-static.  <b>Value After Reset:</b> 0x1b <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f

1:0	CB_DSK_CLK_MODE_CFG	R/W	Configuration of internal deskew clock source mode. This field is quasi-static.  <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
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**CORE\_DIG\_ANACTRL\_RW\_COMMON\_ANACTRL\_1**

- **Description:** Power on analog control configuration
- **Size:** 16 bits
- **Offset:** 0x1cf1

Bits	Name	Memory Access	Description
15:9	RESERVED_15_9	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
8:6	HSRX_DLY	R/W	<p>Configurable delay from all lane?_hsrx_pon to all lane?_hsrx_*. Measured in Config clock cycles. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
5:0	CB_LP_DCO_CLK_EN_DLY	R/W	<p>Configurable delay from cb_lp_dco_pon to cb_lp_dco_fword_change. Measured in Config clock cycles. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x1b</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3f</p>

**CORE\_DIG\_ANACTRL\_RW\_COMMON\_ANACTRL\_2**

- **Description:** Power on analog control configuration
- **Size:** 16 bits
- **Offset:** 0x1cf2

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
13	GLOBAL_ULPS_OVR_VAL	R/W	<p>Global ULPS override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	GLOBAL_ULPS_OVR_EN	R/W	<p>Global ULPS override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

11:8	CB_HSTXLB_DCO_TUNE_CLKDI_G_EN_DLY	R/W	Configurable delay from cb_hstxlb_dco_pon to cb_hstxlb_dco_tune_clkdig_en. Measured in Config clock cycles. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7:4	CB_HSTXLB_DCO_CLK_EN_DLY	R/W	Configurable delay from cb_hstxlb_dco_pon to cb_hstxlb_dco_clk0/90_en. Measured in Config clock cycles. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	CB_HSTXLB_DCO_EN_DLY	R/W	Configurable delay from cb_hstxlb_dco_pon to cb_hstxlb_dco_en delay. Measured in Config clock cycles. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_ANACTRL\_RW\_COMMON\_ANACTRL\_3**

- **Description:** Power on analog control configuration
- **Size:** 16 bits
- **Offset:** 0x1cf3

Bits	Name	Memory Access	Description
15:8	HIBERNATE_DLY	R/W	Configurable delay for the deassertion of the clock gating signals in hibernate mode. Measured in Config clock cycles. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HSTX_DIV_EN_CNTR_DLY	R/W	Configurable delay from PHY_READY to hstx_div_en. Measured in Config clock cycles. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_COMMON\_RW\_DESKEW\_FINE\_MEM**

- **Description:** DPHY deskew fine FSM state jumps programmability
- **Size:** 16 bits
- **Offset:** 0x1ff0

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10	DESKEW_FINE_MEM_WR_EN	R/W	FSM programming write enable. Writes the content DESKEW_FINE_MEM_VALUE into address DESKEW_FINE_MEM_ADDR. Active high. Set to 1'b0 to allow observability of memory content without re-programming. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9:3	DESKEW_FINE_MEM_ADDR	R/W	Selects state address. Must be set to allow observability. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7f

2:0	DESKEW_FINE_MEM_VALUE	R/W	Selects state value. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
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**CORE\_DIG\_COMMON\_R DESKEW\_FINE\_MEM**

- **Description:** DPHY deskew fine FSM state jumps observability
- **Size:** 16 bits
- **Offset:** 0x1ff1

Bits	Name	Memory Access	Description
15:3	RESERVED_15_3	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
2:0	DESKEW_FINE_MEM_VALUE	R	Memory contents of position defined by field DESKEW_FINE_MEM_ADDR. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**PPI\_RW\_DPHY\_LANE0\_LBERT\_0**

- **Description:** DPHY loopback control
- **Size:** 16 bits

- **Offset:** 0x2000

Bits	Name	Memory Access	Description
15	LBERT_PM_DATA_SWAP	R/W	<p>Controls lane mux to choose normal or swapped data (actual reset value is 0xX)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	LBERT_PG_ERROR_INJECTION	R/W	<p>Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

13	LBERT_PG_START_OVR_EN	R/W	<p>Pattern generator start override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	LBERT_PG_START_OVR_VAL	R/W	<p>Pattern generator start override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:8	LBERT_PG_MODE	R/W	<p>Pattern generator mode. This bus is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern generator disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p><b>reserved Value</b></p> <p><b>After Reset:</b> 0x0</p>

			<b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	R/W	Pattern matcher error counter sampling override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	R/W	Pattern matcher error counter sampling override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

5	LBERT_PM_START_OVR_EN	R/W	Pattern matcher start override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	LBERT_PM_START_OVR_VAL	R/W	Pattern matcher start override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

3:0	LBERT_PM_MODE	R/W	<p>Pattern matcher mode. This bus is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern matcher disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p>reserved <b>Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
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**PPI\_RW\_DPHY\_LANE0\_LBERT\_1**

- **Description:** DPHY loopback control
- **Size:** 16 bits
- **Offset:** 0x2001

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	LBERT_PG_USER_PATTERN	R/W	<p>Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_R\_DPHY\_LANE0\_LBERT\_0**

- **Description:** DPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x2002

Bits	Name	Memory Access	Description
15:0	LBERT_PM_ERROR_COUNTER	R	<p>Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_R\_DPHY\_LANE0\_LBERT\_1**

- **Description:** DPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x2003

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
0	LBERT_PG_ENABLED	R	<p>Pattern generator enable observability. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_DPHY\_LANE0\_SPARE**

- **Description:** DPHY spare registers
- **Size:** 16 bits
- **Offset:** 0x2004

Bits	Name	Memory Access	Description
15:0	DPHY_LANE_0_SPARE	R/W	<p>Spare registers for future use</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_RW\_DPHY\_LANE1\_LBERT\_0**

- **Description:** DPHY loopback control
- **Size:** 16 bits
- **Offset:** 0x2200

Bits	Name	Memory Access	Description
15	LBERT_PM_DATA_SWAP	R/W	<p>Controls lane mux to choose normal or swapped data (actual reset value is 0xX)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	LBERT_PG_ERROR_INJECTION	R/W	<p>Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

13	LBERT_PG_START_OVR_EN	R/W	<p>Pattern generator start override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	LBERT_PG_START_OVR_VAL	R/W	<p>Pattern generator start override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:8	LBERT_PG_MODE	R/W	<p>Pattern generator mode. This bus is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern generator disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p><b>reserved Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	R/W	Pattern matcher error counter sampling override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	R/W	Pattern matcher error counter sampling override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

5	LBERT_PM_START_OVR_EN	R/W	Pattern matcher start override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	LBERT_PM_START_OVR_VAL	R/W	Pattern matcher start override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:0	LBERT_PM_MODE	R/W	<p>Pattern matcher mode. This bus is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern matcher disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p>reserved Value</p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

**PPI\_R\_DPHY\_LANE1\_LBERT\_1**

- **Description:** DPHY loopback control
- **Size:** 16 bits
- **Offset:** 0x2201

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	LBERT_PG_USER_PATTERN	R/W	<p>Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_R\_DPHY\_LANE1\_LBERT\_0**

- **Description:** DPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x2202

Bits	Name	Memory Access	Description
15:0	LBERT_PM_ERROR_COUNTER	R	<p>Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_R\_DPHY\_LANE1\_LBERT\_1**

- **Description:** DPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x2203

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

0	LBERT_PG_ENABLED	R	Pattern generator enable observability. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**PPI\_RW\_DPHY\_LANE1\_SPARE**

- **Description:** DPHY spare registers
- **Size:** 16 bits
- **Offset:** 0x2204

Bits	Name	Memory Access	Description
15:0	DPHY_LANE_1_SPARE	R/W	Spare registers for future use <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_CFG\_0**

- **Description:** DPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x3000

Bits	Name	Memory Access	Description
15:3	RESERVED_15_3	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
2	LOOPBACK_MODE_EN	R/W	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
1	CFG_0_HS_PIN_SWAP_REG	R/W	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

0	CFG_0_LP_PIN_SWAP_REG	R/W	<p>Swap dp and dn lines. Applies to low power mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
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**CORE\_DIG\_DLANE\_0\_RW\_CFG\_1**

- **Description:** DPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x3001

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x0</p>
3	CFG_1_SOT_DETECTION_REG	R/W	<p>Selects whether start of transmission (SoT) soft error is flagged. Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
2	CFG_1_DESKEW_SUPPORTED_REG	R/W	<p>Selects whether deskew bursts (DPHY specification 1.2 and above) with 16'hFFFF sync headers are supported. Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>

1	CFG_1_BACKWARDS_DESKEW_REG	R/W	<p>Enables internal skew calibration for DPHY1.1 modes. Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
0	CFG_1_PREAMBLE_EN_REG	R/W	<p>Enables support of data burst with preamble (DPHY specification 2.0 and above). Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_DLANE\_0\_RW\_CFG\_2**

- **Description:** DPHY lane configuration
- **Size:** 16 bits

- **Offset:** 0x3002

Bits	Name	Memory Access	Description
15:0	CFG_2_SPARE	R/W	Spare registers for future use. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

### CORE\_DIG\_DLANE\_0\_RW\_LP\_0

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3040

Bits	Name	Memory Access	Description
15:12	LP_0_ITMINRX_REG	R/W	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
11:8	LP_0_TTAGO_REG	R/W	BTA timing control. Defines the time that the transmitter drives LP00 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7:4	LP_0_TTASURE_REG	R/W	BTA timing control. Defines the time that the new transmitter waits, after the LP10 state before driving LP00. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

3:0	LP_0_TTAGET_REG	R/W	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE <b>Value After Reset:</b> 0xc <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
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### CORE\_DIG\_DLANE\_0\_RW\_LP\_1

- **Description:** Low power subsystem parameters control

- **Size:** 16 bits
- **Offset:** 0x3041

Bits	Name	Memory Access	Description
15:8	LP_1_LPTX_PON_TIMER_REG	R/W	<p>LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x80</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:0	LP_1_ERRCONTENTION_THRES_REG	R/W	<p>Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x10</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

#### CORE\_DIG\_DLANE\_0\_RW\_LP\_2

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3042

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
0	LP_2_FILTER_INPUT_SAMPLING_REG	R/W	<p>LPRX filter input data sampling</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

#### CORE\_DIG\_DLANE\_0\_R\_LP\_0

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x3050

Bits	Name	Memory Access	Description

15:2	RESERVED_15_2	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
1	LP_0_RXHSRQST	R	Signal which indicates that the HS entry transition LP11 -> LP01 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LP_0_HSACTIVERX	R	Signal which indicates that the HS entry transition LP01 -> LP00 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_DLANE\_0\_R\_LP\_1**

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x3051

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:8	LP_1_STATE_LPTX	R	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
7:4	LP_1_STATE_LPRX	R	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	LP_1_STATE_BTA	R	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_0\_R\_HS\_TX\_0**

- **Description:** High speed TX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3070

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:4	STATE_DCO_DHSTX	R	HS-TX DCO clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	STATE_DHSTX	R	HS-TX word clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_0**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3080

Bits	Name	Memory Access	Description
15:8	HS_RX_0_THSSETTLE_REG	R/W	DPHY Ths-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the HS data path. <b>Value After Reset:</b> 0x9 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_0_TCLKSETTLE_REG	R/W	DPHY Tclk-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the reception logic <b>Value After Reset:</b> 0x1d <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_1**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits

- **Offset:** 0x3081

Bits	Name	Memory Access	Description
15:8	HS_RX_1_FILTER_SIZE_SKEWCAL_REG	R/W	Skew calibration algorithm filter size (word_clk cycles). Corresponds to the number of samples used to assess the quality of a phase setting. <b>Value After Reset:</b> 0x40 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_1_FILTER_SIZE_DESKEW_REG	R/W	Deskew algorithm filter size (word clock cycles). Corresponds to the number of samples used to assess the quality of a phase setting. <b>Value After Reset:</b> 0x10 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

### CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_2

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3082

Bits	Name	Memory Access	Description
15	HS_RX_2_IGNORE_ALTERNCAL_REG	R/W	Signal used to ignore alternate calibration patterns. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	HS_RX_2_UPDATE_SETTINGS_SKEWCAL_REG	R/W	Signal used to update the skew calibration algorithm's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13	HS_RX_2_UPDATE_SETTINGS_DESKEW_REG	R/W	Signal used to update the deskew algorithm's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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12:9	HS_RX_2_WINDOW_SIZE_DESK_EW_REG	R/W	Used by the deskew algorithm; Consists of the number of consecutive good settings needed to detect the left edge. Used to prevent false edge detection (word clock cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
8	HS_RX_2_RECAL_SKEWCAL_R_EG	R/W	Signal used to trigger a skew recalibration. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	HS_RX_2_POLARITY_SKEWCAL_REG	R/W	Inverts the data from the AFE's polarity during skew calibration. (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6:5	HS_RX_2_JUMP2STEPS_SKEWCAL_REG	R/W	How many phase settings to jump after detecting the edge during skew calibration algorithm <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
4:3	HS_RX_2_LATENCY_SKEWCAL_REG	R/W	Number of cycles to wait for to account for the AFE's latency during skew calibration (word clock cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
2:0	HS_RX_2_LATENCY_DESKEW_R_EG	R/W	Number of cycles to wait for to account for the AFE's latency during deskew (word clock cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_3**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3083

Bits	Name	Memory Access	Description
15	HS_RX_3_ROUNDUP_DESKEW_REG	R/W	Selects whether to average the final calibration result up (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

14:12	HS_RX_3_SHRINK_STEP_DESK EW_REG	R/W	Shrink step size for fine calibration of the deskew algorithm. In phase steps. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
11:9	HS_RX_3_SHIFT_STEP_DESKE W_REG	R/W	Shift step size for fine calibration of the deskew algorithm. In phase steps. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

8:3	HS_RX_3_FJUMP_DESKEW_RE G	R/W	After detecting the left edge this bus selects how many phases to jump during the deskew algorithm. In phase steps. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
2:0	HS_RX_3_STEP_SIZE_DESKEW _REG	R/W	Size of the deskew algorithm's phase settings step. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_4**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3084

Bits	Name	Memory Access	Description
15:0	HS_RX_4_MAX_ITERATIONS_DE SKEW_REG	R/W	Maximum number of iterations of the deskew algorithm (word_clk cycles) <b>Value After Reset:</b> 0x96 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_5**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3085

Bits	Name	Memory Access	Description

15:8	HS_RX_5_DDL_MID_INIT_REG	R/W	Initial DDL setting for the mid pointer of the deskew algorithm <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_5_DDL_LEFT_INIT_REG	R/W	Initial DDL setting for the left pointer of the deskew algorithm <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_6**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3086

Bits	Name	Memory Access	Description
15:8	HS_RX_6_MIN_EYE_OPENING_DESKEW_REG	R/W	Minimum eye opening after deskew algorithm is complete not to flag an error. Used to obtain error information. (in DDL steps) <b>Value After Reset:</b> 0x2d <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_6_DDL_RIGHT_INIT_REG	R/W	Initial DDL setting for the right pointer of the deskew algorithm <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_7**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3087

Bits	Name	Memory Access	Description
15	HS_RX_7_SELECT_ALTERNATE_ALGO_REG	R/W	Selects which algorithm is triggered by the alternate calibration pattern. <ul style="list-style-type: none"> <li>■ 1'b0 - Triggers coarse calibration</li> <li>■ 1'b1 - Triggers fine calibration</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

14	HS_RX_7_DESKEW_REARM_INI_TIAL_REG	R/W	<p>Allows running an initial calibration after a previous successful one when in automatic mode. This feature shall be used in continuous clock mode.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	HS_RX_7_DESKEW_AUTO_ALGO_SEL_REG	R/W	<p>Select manual or automatic deskew algorithm selection.</p> <ul style="list-style-type: none"> <li>■ 1'b0 - Manual control of the algorithm. HS_RX_7_INI-TIAL_CALIBRATION_REG selects whether to run an initial calibration or a fine calibration.</li> <li>■ 1'b1 - Automatic control of the algorithm. After the first successful initial calibration always run a fine one.</li> </ul> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12:11	HS_RX_7_DESKEW_CNF_REG	R/W	<p>Deskew pattern length configuration for aligner's pattern search. Used for debug purposes. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 2'b00 - Minimum deskew pattern length of 10 bits</li> <li>■ 2'b01 - Minimum deskew pattern length of 12 bits</li> <li>■ 2'b10 - Minimum deskew pattern length of 14 bits</li> <li>■ 2'b11 - Minimum deskew pattern length of 16 bits (default)</li> </ul> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
10	HS_RX_7_THSEXIT_MIN_REG	R/W	<p>Controls lane aligner. Used for lower bitrates if bursts received have minimum Ths-exit. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	HS_RX_7_INITIAL_CALIBRATION_REG	R/W	<p>Select deskew initial calibration (Active high) If 0 triggers a periodic calibration.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	HS_RX_7_INVORDER_RX_REG	R/W	<p>Signal used to invert MSB to LSB reception order (Active high). This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

7:0	HS_RX_7_TCLKMISS_REG	R/W	Tclkmiss timer counter (dco_clk cycles). Defines the minimum time with absence of clock before flagging clock miss. This field is quasi-static. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_8**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3088

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9	HS_ALIGN_BYPASS_REG	R/W	Bypasses alignment and sync detection. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:1	HS_RX_8_START_DELAY_REG	R/W	Selects an initial delay for the deskew algorithm (word_clk cycles) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

0	HS_RX_8_FILTER_DITHERING_EN_REG	R/W	Enable dithering to the deskew algorithm's filter size (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG\_DLANE\_0\_RW\_HS\_RX\_9**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3089

Bits	Name	Memory Access	Description
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15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	HS_RX_9_PHASE_BOUND_REG	R/W	Maximum phase allowed during Deskew algorithm <b>Value After Reset:</b> 0xff <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_0\_R\_HS\_RX\_0**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3090

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:2	DESKEW_CAL_STATUS	R	Bus with status information of the deskew algorithm. <ul style="list-style-type: none"> <li>■ [0] - signals that the deskew algorithm has finished;</li> <li>■ [1] - signals that an initial calibration has finished successfully;</li> <li>■ [2] - signals that an initial calibration has finished with an unsatisfactory eye size;</li> <li>■ [3] - signals that an initial calibration has failed;</li> <li>■ [4] - signals that a fine calibration has finished with convergence;</li> <li>■ [5] - signals that a fine calibration ran out of time but found a new best setting;</li> <li>■ [6] - signals that a fine calibration ran out of time with no best setting;</li> <li>■ [7] - signals that during either calibration the phase setting went out of bounds.</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

1	DESKEWCALFAILED	R	Signals a skew calibration with errors (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	DESKEWCALDONE	R	Signals that the skew calibration has completed. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_DLANE\_0\_R\_HS\_RX\_1**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3091

Bits	Name	Memory Access	Description
15:0	DESKEWCALTIME	R	Bus containing information on how many cycles the deskew calibration took (word_clk cycles) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_R\_HS\_RX\_2**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3092

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	DESKEW_STATE	R	Deskew algorithm FSM's state <b>Value After Reset:</b> 0xa0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_0\_R\_HS\_RX\_3**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3093

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11	DESKEW_ALL_DIFF	R	Result of the deskew algorithm three pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	DESKEW_FAILED_RIGHT	R	Result of the deskew algorithm right pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	DESKEW_FAILED_LEFT	R	Result of the deskew algorithm left pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

8:5	DESKEW_CURR_ACTION	R	Deskew algorithm current action <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
4	DESKEW_PREV_RESULT	R	Deskew algorithm previous action's result <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:0	DESKEW_PREV_ACTION	R	Deskew algorithm previous action <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_0\_R\_HS\_RX\_4**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3094

Bits	Name	Memory Access	Description

15:8	EDGE2POINTER_SKEWCAL	R	Skewcal algorithm's second edge <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	EDGE1POINTER_SKEWCAL	R	Skewcal algorithm's first edge <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_0**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3100

Bits	Name	Memory Access	Description
15:0	HS_TX_0_THSTRAIL_REG	R/W	Tclk-trail/Ths-trail setting (word clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x9 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_1**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3101

Bits	Name	Memory Access	Description
15:0	HS_TX_1_THSZERO_REG	R/W	Tclk-zero/Ths-zero setting (word clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x20 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_2**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3102

Bits	Name	Memory Access	Description

15:0	HS_TX_2_TCLKPRE_REG	R/W	Tclk-pre setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_3**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3103

Bits	Name	Memory Access	Description
15	HS_TX_3_PIN_SWAP_REG	R/W	Swap dp and dn lines. Applies to high speed mode. This field is quasi-static. <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	HS_TX_3_HSDIRECT_REG	R/W	Reserved. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13:10	HS_TX_3_STATE_OVR_REG	R/W	HS-TX FSM state (word clock) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

9	HS_TX_3_STATE_OVR_EN_REG	R/W	HS-TX FSM state (word clock) override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	HS_TX_3_INVORDER_TX_REG	R/W	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

7:0	HS_TX_3_TLPTXOVERLAP_REG	R/W	LP-TX/HS-TX drivers enable overlap (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_4**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3104

Bits	Name	Memory Access	Description
15:0	HS_TX_4_TLPX_DCO_REG	R/W	Tlp value (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_5**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3105

Bits	Name	Memory Access	Description
15:0	HS_TX_5_THSTRAIL_DCO_REG	R/W	Tclk-trail/Ths-trail value (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_6**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3106

Bits	Name	Memory Access	Description

15:0	HS_TX_6_TLP11END_DCO_REG	R/W	HS2LP final LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_7**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3107

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:10	HS_TX_7_STATE_DCO_OVR_VA_L_REG	R/W	HS-TX FSM state (DCO clock) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
9	HS_TX_7_STATE_DCO_OVR_EN_REG	R/W	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

8:0	HS_TX_7_ALTCALSEED_REG	R/W	Alternate calibration PRBS seed. Used for debug purposes. <b>Value After Reset:</b> 0xff <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff
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**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_8**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3108

Bits	Name	Memory Access	Description
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15:0	HS_TX_8_TCLKPOST_REG	R/W	Tclk-post setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x1c <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_9**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3109

Bits	Name	Memory Access	Description
15:0	HS_TX_9_THSPRPR_DCO_REG	R/W	Tclk-prepare/Ths-prepare setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_10**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x310a

Bits	Name	Memory Access	Description
15:0	HS_TX_10_TLP11INIT_DCO_REG	R/W	LP2HS initial LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_11**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x310b

Bits	Name	Memory Access	Description
15:0	HS_TX_11_TPREAMBLE_REG	R/W	Reserved. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_0\_RW\_HS\_TX\_12**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x310c

Bits	Name	Memory Access	Description
15:0	HS_TX_12_THSEXIT_DCO_REG	R/W	<p>Ths-exit setting (DCO clock cycles). This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x14</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_DLANE\_1\_RW\_CFG\_0**

- **Description:** DPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x3200

Bits	Name	Memory Access	Description
15:3	RESERVED_15_3	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
2	LOOPBACK_MODE_EN	R/W	<p>Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	CFG_0_HS_PIN_SWAP_REG	R/W	<p>Swap dp and dn lines. Applies to high speed mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

0	CFG_0_LP_PIN_SWAP_REG	R/W	<p>Swap dp and dn lines. Applies to low power mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
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**CORE\_DIG\_DLANE\_1\_RW\_CFG\_1**

- **Description:** DPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x3201

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x0</p>
3	CFG_1_SOT_DETECTION_REG	R/W	<p>Selects whether start of transmission (SoT) soft error is flagged. Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
2	CFG_1_DESKEW_SUPPORTED_REG	R/W	<p>Selects whether deskew bursts (DPHY specification 1.2 and above) with 16'hFFFF sync headers are supported. Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>

1	CFG_1_BACKWARDS_DESKEW_REG	R/W	<p>Enables internal skew calibration for DPHY1.1 modes. Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
0	CFG_1_PREAMBLE_EN_REG	R/W	<p>Enables support of data burst with preamble (DPHY specification 2.0 and above). Active high.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_DLANE\_1\_RW\_CFG\_2**

- **Description:** DPHY lane configuration
- **Size:** 16 bits

- **Offset:** 0x3202

Bits	Name	Memory Access	Description
15:0	CFG_2_SPARE	R/W	Spare registers for future use. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

### CORE\_DIG\_DLANE\_1\_RW\_LP\_0

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3240

Bits	Name	Memory Access	Description
15:12	LP_0_ITMINRX_REG	R/W	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
11:8	LP_0_TTAGO_REG	R/W	BTA timing control. Defines the time that the transmitter drives LP00 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7:4	LP_0_TTASURE_REG	R/W	BTA timing control. Defines the time that the new transmitter waits, after the LP10 state before driving LP00. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

3:0	LP_0_TTAGET_REG	R/W	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE <b>Value After Reset:</b> 0xc <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
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### CORE\_DIG\_DLANE\_1\_RW\_LP\_1

- **Description:** Low power subsystem parameters control

- **Size:** 16 bits
- **Offset:** 0x3241

Bits	Name	Memory Access	Description
15:8	LP_1_LPTX_PON_TIMER_REG	R/W	<p>LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x80</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>
7:0	LP_1_ERRCONTENTION_THRES_REG	R/W	<p>Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x10</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

#### CORE\_DIG\_DLANE\_1\_RW\_LP\_2

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3242

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
0	LP_2_FILTER_INPUT_SAMPLING_REG	R/W	<p>LPRX filter input data sampling</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

#### CORE\_DIG\_DLANE\_1\_R\_LP\_0

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x3250

Bits	Name	Memory Access	Description

15:2	RESERVED_15_2	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
1	LP_0_RXHSRQST	R	Signal which indicates that the HS entry transition LP11 -> LP01 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LP_0_HSACTIVERX	R	Signal which indicates that the HS entry transition LP01 -> LP00 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_DLANE\_1\_R\_LP\_1**

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x3251

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:8	LP_1_STATE_LPTX	R	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
7:4	LP_1_STATE_LPRX	R	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	LP_1_STATE_BTA	R	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_1\_R\_HS\_TX\_0**

- **Description:** High speed TX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3270

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:4	STATE_DCO_DHSTX	R	HS-TX DCO clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	STATE_DHSTX	R	HS-TX word clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_0**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3280

Bits	Name	Memory Access	Description
15:8	HS_RX_0_THSSETTLE_REG	R/W	DPHY Ths-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the HS data path. <b>Value After Reset:</b> 0x9 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_0_TCLKSETTLE_REG	R/W	DPHY Tclk-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the reception logic <b>Value After Reset:</b> 0x1d <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_1**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits

- **Offset:** 0x3281

Bits	Name	Memory Access	Description
15:8	HS_RX_1_FILTER_SIZE_SKEWCAL_REG	R/W	Skew calibration algorithm filter size (word_clk cycles). Corresponds to the number of samples used to assess the quality of a phase setting. <b>Value After Reset:</b> 0x40 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_1_FILTER_SIZE_DESKEW_REG	R/W	Deskew algorithm filter size (word clock cycles). Corresponds to the number of samples used to assess the quality of a phase setting. <b>Value After Reset:</b> 0x10 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

### CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_2

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3282

Bits	Name	Memory Access	Description
15	HS_RX_2_IGNORE_ALTERNCAL_REG	R/W	Signal used to ignore alternate calibration patterns. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	HS_RX_2_UPDATE_SETTINGS_SKEWCAL_REG	R/W	Signal used to update the skew calibration algorithm's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13	HS_RX_2_UPDATE_SETTINGS_DESKEW_REG	R/W	Signal used to update the deskew algorithm's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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12:9	HS_RX_2_WINDOW_SIZE_DESK_EW_REG	R/W	Used by the deskew algorithm; Consists of the number of consecutive good settings needed to detect the left edge. Used to prevent false edge detection (word clock cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
8	HS_RX_2_RECAL_SKEWCAL_R_EG	R/W	Signal used to trigger a skew recalibration. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	HS_RX_2_POLARITY_SKEWCAL_REG	R/W	Inverts the data from the AFE's polarity during skew calibration. (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6:5	HS_RX_2_JUMP2STEPS_SKEWCAL_REG	R/W	How many phase settings to jump after detecting the edge during skew calibration algorithm <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
4:3	HS_RX_2_LATENCY_SKEWCAL_REG	R/W	Number of cycles to wait for to account for the AFE's latency during skew calibration (word clock cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
2:0	HS_RX_2_LATENCY_DESKEW_R_EG	R/W	Number of cycles to wait for to account for the AFE's latency during deskew (word clock cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_3**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3283

Bits	Name	Memory Access	Description
15	HS_RX_3_ROUNDUP_DESKEW_REG	R/W	Selects whether to average the final calibration result up (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

14:12	HS_RX_3_SHRINK_STEP_DESK EW_REG	R/W	Shrink step size for fine calibration of the deskew algorithm. In phase steps. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
11:9	HS_RX_3_SHIFT_STEP_DESKE W_REG	R/W	Shift step size for fine calibration of the deskew algorithm. In phase steps. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

8:3	HS_RX_3_FJUMP_DESKEW_RE G	R/W	After detecting the left edge this bus selects how many phases to jump during the deskew algorithm. In phase steps. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
2:0	HS_RX_3_STEP_SIZE_DESKEW _REG	R/W	Size of the deskew algorithm's phase settings step. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_4**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3284

Bits	Name	Memory Access	Description
15:0	HS_RX_4_MAX_ITERATIONS_DE SKEW_REG	R/W	Maximum number of iterations of the deskew algorithm (word_clk cycles) <b>Value After Reset:</b> 0x96 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_5**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3285

Bits	Name	Memory Access	Description

15:8	HS_RX_5_DDL_MID_INIT_REG	R/W	Initial DDL setting for the mid pointer of the deskew algorithm <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_5_DDL_LEFT_INIT_REG	R/W	Initial DDL setting for the left pointer of the deskew algorithm <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_6**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3286

Bits	Name	Memory Access	Description
15:8	HS_RX_6_MIN_EYE_OPENING_DESKEW_REG	R/W	Minimum eye opening after deskew algorithm is complete not to flag an error. Used to obtain error information. (in DDL steps) <b>Value After Reset:</b> 0x2d <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_6_DDL_RIGHT_INIT_REG	R/W	Initial DDL setting for the right pointer of the deskew algorithm <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_7**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3287

Bits	Name	Memory Access	Description
15	HS_RX_7_SELECT_ALTERNATE_ALGO_REG	R/W	Selects which algorithm is triggered by the alternate calibration pattern. <ul style="list-style-type: none"> <li>■ 1'b0 - Triggers coarse calibration</li> <li>■ 1'b1 - Triggers fine calibration</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

14	HS_RX_7_DESKEW_REARM_INI_TIAL_REG	R/W	<p>Allows running an initial calibration after a previous successful one when in automatic mode. This feature shall be used in continuous clock mode.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
13	HS_RX_7_DESKEW_AUTO_ALGO_SEL_REG	R/W	<p>Select manual or automatic deskew algorithm selection.</p> <ul style="list-style-type: none"> <li>■ 1'b0 - Manual control of the algorithm. HS_RX_7_INI-TIAL_CALIBRATION_REG selects whether to run an initial calibration or a fine calibration.</li> <li>■ 1'b1 - Automatic control of the algorithm. After the first successful initial calibration always run a fine one.</li> </ul> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12:11	HS_RX_7_DESKEW_CNF_REG	R/W	<p>Deskew pattern length configuration for aligner's pattern search. Used for debug purposes. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 2'b00 - Minimum deskew pattern length of 10 bits</li> <li>■ 2'b01 - Minimum deskew pattern length of 12 bits</li> <li>■ 2'b10 - Minimum deskew pattern length of 14 bits</li> <li>■ 2'b11 - Minimum deskew pattern length of 16 bits (default)</li> </ul> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3</p>
10	HS_RX_7_THSEXIT_MIN_REG	R/W	<p>Controls lane aligner. Used for lower bitrates if bursts received have minimum Ths-exit. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
9	HS_RX_7_INITIAL_CALIBRATION_REG	R/W	<p>Select deskew initial calibration (Active high) If 0 triggers a periodic calibration.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
8	HS_RX_7_INVORDER_RX_REG	R/W	<p>Signal used to invert MSB to LSB reception order (Active high). This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

7:0	HS_RX_7_TCLKMISS_REG	R/W	Tclkmiss timer counter (dco_clk cycles). Defines the minimum time with absence of clock before flagging clock miss. This field is quasi-static. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_8**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3288

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9	HS_ALIGN_BYPASS_REG	R/W	Bypasses alignment and sync detection. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:1	HS_RX_8_START_DELAY_REG	R/W	Selects an initial delay for the deskew algorithm (word_clk cycles) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

0	HS_RX_8_FILTER_DITHERING_EN_REG	R/W	Enable dithering to the deskew algorithm's filter size (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG\_DLANE\_1\_RW\_HS\_RX\_9**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3289

Bits	Name	Memory Access	Description
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15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	HS_RX_9_PHASE_BOUND_REG	R/W	Maximum phase allowed during Deskew algorithm <b>Value After Reset:</b> 0xff <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_1\_R\_HS\_RX\_0**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3290

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:2	DESKEW_CAL_STATUS	R	Bus with status information of the deskew algorithm. <ul style="list-style-type: none"> <li>■ [0] - signals that the deskew algorithm has finished;</li> <li>■ [1] - signals that an initial calibration has finished successfully;</li> <li>■ [2] - signals that an initial calibration has finished with an unsatisfactory eye size;</li> <li>■ [3] - signals that an initial calibration has failed;</li> <li>■ [4] - signals that a fine calibration has finished with convergence;</li> <li>■ [5] - signals that a fine calibration ran out of time but found a new best setting;</li> <li>■ [6] - signals that a fine calibration ran out of time with no best setting;</li> <li>■ [7] - signals that during either calibration the phase setting went out of bounds.</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

1	DESKEWCALFAILED	R	Signals a skew calibration with errors (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	DESKEWCALDONE	R	Signals that the skew calibration has completed. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_DLANE\_1\_R\_HS\_RX\_1**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3291

Bits	Name	Memory Access	Description
15:0	DESKEWCALTIME	R	Bus containing information on how many cycles the deskew calibration took (word_clk cycles) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_R\_HS\_RX\_2**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3292

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	DESKEW_STATE	R	Deskew algorithm FSM's state <b>Value After Reset:</b> 0xa0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_1\_R\_HS\_RX\_3**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3293

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11	DESKEW_ALL_DIFF	R	Result of the deskew algorithm three pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	DESKEW_FAILED_RIGHT	R	Result of the deskew algorithm right pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	DESKEW_FAILED_LEFT	R	Result of the deskew algorithm left pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

8:5	DESKEW_CURR_ACTION	R	Deskew algorithm current action <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
4	DESKEW_PREV_RESULT	R	Deskew algorithm previous action's result <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:0	DESKEW_PREV_ACTION	R	Deskew algorithm previous action <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_1\_R\_HS\_RX\_4**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3294

Bits	Name	Memory Access	Description
15:8	EDGE2POINTER_SKEWCAL	R	Skewcal algorithm's second edge <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

7:0	EDGE1POINTER_SKEWCAL	R	Skewcal algorithm's first edge <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_0**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3300

Bits	Name	Memory Access	Description
15:0	HS_TX_0_THSTRAIL_REG	R/W	Tclk-trail/Ths-trail setting (word clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x9 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_1**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3301

Bits	Name	Memory Access	Description
15:0	HS_TX_1_THSZERO_REG	R/W	Tclk-zero/Ths-zero setting (word clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x20 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_2**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3302

Bits	Name	Memory Access	Description
15:0	HS_TX_2_TCLKPRE_REG	R/W	Tclk-pre setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_3**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3303

Bits	Name	Memory Access	Description
15	HS_TX_3_PIN_SWAP_REG	R/W	<p>Swap dp and dn lines. Applies to high speed mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
14	HS_TX_3_HSDIRECT_REG	R/W	<p>Reserved.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
13:10	HS_TX_3_STATE_OVR_REG	R/W	<p>HS-TX FSM state (word clock) override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xf</p>

9	HS_TX_3_STATE_OVR_EN_REG	R/W	<p>HS-TX FSM state (word clock) override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
8	HS_TX_3_INVORDER_TX_REG	R/W	<p>Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
7:0	HS_TX_3_TLPTXOVERLAP_REG	R/W	<p>LP-TX/HS-TX drivers enable overlap (DCO clock cycles). This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x6  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_4**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3304

Bits	Name	Memory Access	Description
15:0	HS_TX_4_TLPX_DCO_REG	R/W	Tlpx value (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_5**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3305

Bits	Name	Memory Access	Description
15:0	HS_TX_5_THSTRAIL_DCO_REG	R/W	Tclk-trail/Ths-trail value (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_6**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3306

Bits	Name	Memory Access	Description
15:0	HS_TX_6_TLP11END_DCO_REG	R/W	HS2LP final LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_7**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3307

Bits	Name	Memory Access	Description

15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:10	HS_TX_7_STATE_DCO_OVR_VA_L_REG	R/W	HS-TX FSM state (DCO clock) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
9	HS_TX_7_STATE_DCO_OVR_EN_REG	R/W	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:0	HS_TX_7_ALTCALSEED_REG	R/W	Alternate calibration PRBS seed. Used for debug purposes. <b>Value After Reset:</b> 0xff <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_8**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3308

Bits	Name	Memory Access	Description
15:0	HS_TX_8_TCLKPOST_REG	R/W	Tclk-post setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x1c <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_9**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3309

Bits	Name	Memory Access	Description

15:0	HS_TX_9_THSPRPR_DCO_REG	R/W	Tclk-prepare/Ths-prepare setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_10**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x330a

Bits	Name	Memory Access	Description
15:0	HS_TX_10_TLP11INIT_DCO_REG	R/W	LP2HS initial LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_11**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x330b

Bits	Name	Memory Access	Description
15:0	HS_TX_11_TPREAMBLE_REG	R/W	Reserved. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_1\_RW\_HS\_TX\_12**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x330c

Bits	Name	Memory Access	Description
15:0	HS_TX_12_THSEXIT_DCO_REG	R/W	Ths-exit setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x14 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_CFG\_0**

- **Description:** DPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x3800

Bits	Name	Memory Access	Description
15:3	RESERVED_15_3	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
2	LOOPBACK_MODE_EN	R/W	<p>Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
1	CFG_0_HS_PIN_SWAP_REG	R/W	<p>Swap dp and dn lines. Applies to high speed mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

0	CFG_0_LP_PIN_SWAP_REG	R/W	<p>Swap dp and dn lines. Applies to low power mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
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**CORE\_DIG\_DLANE\_CLK\_RW\_CFG\_1**

- **Description:** DPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x3801

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

3	CFG_1_SOT_DETECTION_REG	R/W	Selects whether start of transmission (SoT) soft error is flagged. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2	CFG_1_DESKEW_SUPPORTED_REG	R/W	Selects whether deskew bursts (DPHY specification 1.2 and above) with 16'hFFFF sync headers are supported. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

1	CFG_1_BACKWARDS_DESKEW_REG	R/W	Enables internal skew calibration for DPHY1.1 modes. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	CFG_1_PREAMBLE_EN_REG	R/W	Enables support of data burst with preamble (DPHY specification 2.0 and above). Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_DLANE\_CLK\_RW\_CFG\_2**

- **Description:** DPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x3802

Bits	Name	Memory Access	Description
15:0	CFG_2_SPARE	R/W	Spare registers for future use. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_LP\_0**

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3840

Bits	Name	Memory Access	Description

15:12	LP_0_ITMINRX_REG	R/W	LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static. <b>Value After Reset:</b> 0x4 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
11:8	LP_0_TTAGO_REG	R/W	BTA timing control. Defines the time that the transmitter drives LP00 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7:4	LP_0_TTASURE_REG	R/W	BTA timing control. Defines the time that the new transmitter waits, after the LP10 state before driving LP00. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	LP_0_TTAGET_REG	R/W	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE <b>Value After Reset:</b> 0xc <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_CLK\_RW\_LP\_1**

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3841

Bits	Name	Memory Access	Description
15:8	LP_1_LPTX_PON_TIMER_REG	R/W	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static. <b>Value After Reset:</b> 0x80 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

7:0	LP_1_ERRCONTENTION_THRES_REG	R/W	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static. <b>Value After Reset:</b> 0x10 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_DLANE\_CLK\_RW\_LP\_2**

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3842

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	LP_2_FILTER_INPUT_SAMPLING_REG	R/W	LPRX filter input data sampling <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_DLANE\_CLK\_R\_LP\_0**

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x3850

Bits	Name	Memory Access	Description
15:2	RESERVED_15_2	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
1	LP_0_RXHSRQST	R	Signal which indicates that the HS entry transition LP11 -> LP01 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LP_0_HSACTIVERX	R	Signal which indicates that the HS entry transition LP01 -> LP00 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_DLANE\_CLK\_R\_LP\_1**

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x3851

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:8	LP_1_STATE_LPTX	R	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
7:4	LP_1_STATE_LPRX	R	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	LP_1_STATE_BTA	R	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_CLK\_R\_HS\_TX\_0**

- **Description:** High speed TX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3870

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

7:4	STATE_DCO_DHSTX	R	HS-TX DCO clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	STATE_DHSTX	R	HS-TX word clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_0**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3880

Bits	Name	Memory Access	Description
15:8	HS_RX_0_THSSETTLE_REG	R/W	DPHY Ths-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the HS data path. <b>Value After Reset:</b> 0x9 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_0_TCLKSETTLE_REG	R/W	DPHY Tclk-settle timer counter (dco_clk cycles). Defines the time interval between the detection of the LP01 -> LP00 transition and the enabling of the reception logic <b>Value After Reset:</b> 0x1d <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_1**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3881

Bits	Name	Memory Access	Description
15:8	HS_RX_1_FILTER_SIZE_SKEWCAL_REG	R/W	Skew calibration algorithm filter size (word_clk cycles). Corresponds to the number of samples used to assess the quality of a phase setting. <b>Value After Reset:</b> 0x40 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

7:0	HS_RX_1_FILTER_SIZE_DESKE_W_REG	R/W	Deskew algorithm filter size (word clock cycles). Corresponds to the number of samples used to assess the quality of a phase setting. <b>Value After Reset:</b> 0x10 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_2**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3882

Bits	Name	Memory Access	Description
15	HS_RX_2_IGNORE_ALTERNCAL_REG	R/W	Signal used to ignore alternate calibration patterns. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	HS_RX_2_UPDATE_SETTINGS_SKEWCAL_REG	R/W	Signal used to update the skew calibration algorithm's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13	HS_RX_2_UPDATE_SETTINGS_DESKEW_REG	R/W	Signal used to update the deskew algorithm's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12:9	HS_RX_2_WINDOW_SIZE_DESK_EW_REG	R/W	Used by the deskew algorithm; Consists of the number of consecutive good settings needed to detect the left edge. Used to prevent false edge detection (word clock cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
8	HS_RX_2_RECAL_SKWCAL_REG	R/W	Signal used to trigger a skew recalibration. (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	HS_RX_2_POLARITY_SKWCAL_REG	R/W	Inverts the data from the AFE's polarity during skew calibration. (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

6:5	HS_RX_2_JUMP2STEPS_SKEW_CAL_REG	R/W	How many phase settings to jump after detecting the edge during skew calibration algorithm  <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
4:3	HS_RX_2_LATENCY_SKEWCAL_REG	R/W	Number of cycles to wait for to account for the AFE's latency during skew calibration (word clock cycles)  <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3
2:0	HS_RX_2_LATENCY_DESKEW_REG	R/W	Number of cycles to wait for to account for the AFE's latency during deskew (word clock cycles)  <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_3**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3883

Bits	Name	Memory Access	Description
15	HS_RX_3_ROUNDUP_DESKEW_REG	R/W	Selects whether to average the final calibration result up (Active high)  <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14:12	HS_RX_3_SHRINK_STEP_DESK_EW_REG	R/W	Shrink step size for fine calibration of the deskew algorithm. In phase steps.  <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
11:9	HS_RX_3_SHIFT_STEP_DESK_EW_REG	R/W	Shift step size for fine calibration of the deskew algorithm. In phase steps.  <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

8:3	HS_RX_3_FJUMP_DESKEW_REG	R/W	After detecting the left edge this bus selects how many phases to jump during the deskew algorithm. In phase steps.  <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f
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2:0	HS_RX_3_STEP_SIZE_DESKEW_REG	R/W	Size of the deskew algorithm's phase settings step. <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
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**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_4**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3884

Bits	Name	Memory Access	Description
15:0	HS_RX_4_MAX_ITERATIONS_DESKW_REG	R/W	Maximum number of iterations of the deskew algorithm (word_clk cycles) <b>Value After Reset:</b> 0x96 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_5**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3885

Bits	Name	Memory Access	Description
15:8	HS_RX_5_DDL_MID_INIT_REG	R/W	Initial DDL setting for the mid pointer of the deskew algorithm <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_5_DDL_LEFT_INIT_REG	R/W	Initial DDL setting for the left pointer of the deskew algorithm <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_6**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3886

Bits	Name	Memory Access	Description
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15:8	HS_RX_6_MIN_EYE_OPENING_DESKW_REG	R/W	Minimum eye opening after deskew algorithm is complete not to flag an error. Used to obtain error information. (in DDL steps) <b>Value After Reset:</b> 0x2d <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	HS_RX_6_DDL_RIGHT_INIT_REG	R/W	Initial DDL setting for the right pointer of the deskew algorithm <b>Value After Reset:</b> 0x2 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_7**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3887

Bits	Name	Memory Access	Description
15	HS_RX_7_SELECT_ALTERNATE_ALGO_REG	R/W	Selects which algorithm is triggered by the alternate calibration pattern. <ul style="list-style-type: none"> <li>■ 1'b0 - Triggers coarse calibration</li> <li>■ 1'b1 - Triggers fine calibration</li> </ul> <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
14	HS_RX_7_DESKW_REARM_INITIAL_REG	R/W	Allows running an initial calibration after a previous successful one when in automatic mode. This feature shall be used in continuous clock mode. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13	HS_RX_7_DESKW_AUTO_ALG_O_SEL_REG	R/W	Select manual or automatic deskew algorithm selection. <ul style="list-style-type: none"> <li>■ 1'b0 - Manual control of the algorithm. HS_RX_7_INITIAL_CALIBRATION_REG selects whether to run an initial calibration or a fine calibration.</li> <li>■ 1'b1 - Automatic control of the algorithm. After the first successful initial calibration always run a fine one.</li> </ul> <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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12:11	HS_RX_7_DESKEW_CNF_REG	R/W	<p>Deskew pattern length configuration for aligner's pattern search. Used for debug purposes. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 2'b00 - Minimum deskew pattern length of 10 bits</li> <li>■ 2'b01 - Minimum deskew pattern length of 12 bits</li> <li>■ 2'b10 - Minimum deskew pattern length of 14 bits</li> <li>■ 2'b11 - Minimum deskew pattern length of 16 bits (default)</li> </ul> <p><b>Value After Reset:</b> 0x3  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x3</p>
10	HS_RX_7_THSEXIT_MIN_REG	R/W	<p>Controls lane aligner. Used for lower bitrates if bursts received have minimum Ths-exit. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
9	HS_RX_7_INITIAL_CALIBRATION_REG	R/W	<p>Select deskew initial calibration (Active high) If 0 triggers a periodic calibration.</p> <p><b>Value After Reset:</b> 0x1  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
8	HS_RX_7_INVORDER_RX_REG	R/W	<p>Signal used to invert MSB to LSB reception order (Active high). This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x1  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
7:0	HS_RX_7_TCLKMISS_REG	R/W	<p>Tclkmiss timer counter (dco_clk cycles). Defines the minimum time with absence of clock before flagging clock miss. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x6  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_8**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3888

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	<p>Reserved for Future use and actual reset value is 0X</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x0</p>

9	HS_ALIGN_BYPASS_REG	R/W	Bypasses alignment and sync detection. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8:1	HS_RX_8_START_DELAY_REG	R/W	Selects an initial delay for the deskew algorithm (word_clk cycles) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

0	HS_RX_8_FILTER_DITHERING_EN_REG	R/W	Enable dithering to the deskew algorithm's filter size (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_RX\_9**

- **Description:** High speed RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3889

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	HS_RX_9_PHASE_BOUND_REG	R/W	Maximum phase allowed during Deskew algorithm <b>Value After Reset:</b> 0xff <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_CLK\_R\_HS\_RX\_0**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3890

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

9:2	DESKEW_CAL_STATUS	R	<p>Bus with status information of the deskew algorithm.</p> <ul style="list-style-type: none"> <li>■ [0] - signals that the deskew algorithm has finished;</li> <li>■ [1] - signals that an initial calibration has finished success- fully;</li> <li>■ [2] - signals that an initial calibration has finished with an unsatisfactory eye size;</li> <li>■ [3] - signals that an initial calibration has failed;</li> <li>■ [4] - signals that a fine calibration has finished with conver- gence;</li> <li>■ [5] - signals that a fine calibration ran out of time but found a new best setting;</li> <li>■ [6] - signals that a fine calibration ran out of time with no best setting;</li> <li>■ [7] - signals that during either calibration the phase setting went out of bounds.</li> </ul> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xff</p>
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1	DESKEWCALFAILED	R	<p>Signals a skew calibration with errors (Active high)</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>
0	DESKEWCALDONE	R	<p>Signals that the skew calibration has completed. (Active high)</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_DLANE\_CLK\_R\_HS\_RX\_1**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3891

Bits	Name	Memory Access	Description
15:0	DESKEWCALTIME	R	<p>Bus containing information on how many cycles the deskew calibration took (word_clk cycles)</p> <p><b>Value After Reset:</b> 0x0  <b>Exists:</b> Always  <b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_DLANE\_CLK\_R\_HS\_RX\_2**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3892

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	DESKEW_STATE	R	Deskew algorithm FSM's state <b>Value After Reset:</b> 0xa0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_CLK\_R\_HS\_RX\_3**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3893

Bits	Name	Memory Access	Description
15:12	RESERVED_15_12	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
11	DESKEW_ALL_DIFF	R	Result of the deskew algorithm three pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
10	DESKEW_FAILED_RIGHT	R	Result of the deskew algorithm right pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	DESKEW_FAILED_LEFT	R	Result of the deskew algorithm left pointers' comparison <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

8:5	DESKEW_CURR_ACTION	R	Deskew algorithm current action <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
4	DESKEW_PREV_RESULT	R	Deskew algorithm previous action's result <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:0	DESKEW_PREV_ACTION	R	Deskew algorithm previous action <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_DLANE\_CLK\_R\_HS\_RX\_4**

- **Description:** High speed RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x3894

Bits	Name	Memory Access	Description
15:8	EDGE2POINTER_SKEWCAL	R	Skewcal algorithm's second edge <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	EDGE1POINTER_SKEWCAL	R	Skewcal algorithm's first edge <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_0**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3900

Bits	Name	Memory Access	Description
15:0	HS_TX_0_THSTRAIL_REG	R/W	Tclk-trail/Ths-trail setting (word clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x9 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_1**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3901

Bits	Name	Memory Access	Description
15:0	HS_TX_1_THSZERO_REG	R/W	<p>Tclk-zero/Ths-zero setting (word clock cycles). This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x20</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_2**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3902

Bits	Name	Memory Access	Description
15:0	HS_TX_2_TCLKPRE_REG	R/W	<p>Tclk-pre setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_3**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3903

Bits	Name	Memory Access	Description
15	HS_TX_3_PIN_SWAP_REG	R/W	<p>Swap dp and dn lines. Applies to high speed mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 1'b0: positive on dp / negative on dn;</li> <li>■ 1'b1: positive on dn / negative on dp;</li> </ul> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

14	HS_TX_3_HSDIRECT_REG	R/W	Reserved. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
13:10	HS_TX_3_STATE_OVR_REG	R/W	HS-TX FSM state (word clock) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

9	HS_TX_3_STATE_OVR_EN_REG	R/W	HS-TX FSM state (word clock) override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	HS_TX_3_INVORDER_TX_REG	R/W	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:0	HS_TX_3_TLPTXOVERLAP_REG	R/W	LP-TX/HS-TX drivers enable overlap (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

#### CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_4

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3904

Bits	Name	Memory Access	Description
15:0	HS_TX_4_TLPX_DCO_REG	R/W	Tlp value (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

#### CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_5

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3905

Bits	Name	Memory Access	Description
15:0	HS_TX_5_THSTRAIL_DCO_REG	R/W	Tclk-trail/Ths-trail value (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x7 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_6**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3906

Bits	Name	Memory Access	Description
15:0	HS_TX_6_TLP11END_DCO_REG	R/W	HS2LP final LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_7**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3907

Bits	Name	Memory Access	Description
15:14	RESERVED_15_14	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
13:10	HS_TX_7_STATE_DCO_OVR_VA_L_REG	R/W	HS-TX FSM state (DCO clock) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
9	HS_TX_7_STATE_DCO_OVR_EN_REG	R/W	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

8:0	HS_TX_7_ALTCALSEED_REG	R/W	Alternate calibration PRBS seed. Used for debug purposes. <b>Value After Reset:</b> 0xff <b>Exists:</b> Always <b>Reset Mask:</b> 0x1ff
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**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_8**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3908

Bits	Name	Memory Access	Description
15:0	HS_TX_8_TCLKPOST_REG	R/W	Tclk-post setting (word clock cycles). Clock lane related. This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x1c <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_9**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x3909

Bits	Name	Memory Access	Description
15:0	HS_TX_9_THSPRPR_DCO_REG	R/W	Tclk-prepare/Ths-prepare setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_10**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x390a

Bits	Name	Memory Access	Description
15:0	HS_TX_10_TLP11INIT_DCO_REG	R/W	LP2HS initial LP11 setting (DCO clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0xa <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_11**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x390b

Bits	Name	Memory Access	Description
15:0	HS_TX_11_TPREAMBLE_REG	R/W	<p>Reserved.</p> <p><b>Value After Reset:</b> 0x7</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_DLANE\_CLK\_RW\_HS\_TX\_12**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x390c

Bits	Name	Memory Access	Description
15:0	HS_TX_12_THSEXIT_DCO_REG	R/W	<p>Ths-exit setting (DCO clock cycles). This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x14</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_RW\_CPHY\_TRIO0\_LBERT\_0**

- **Description:** CPHY loopback control
- **Size:** 16 bits
- **Offset:** 0x4000

Bits	Name	Memory Access	Description
15	LBERT_PM_DATA_SWAP	R/W	<p>Controls trio mux to choose normal or swapped data (actual reset value is 0xX)</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14	LBERT_PG_ERROR_INJECTION	R/W	<p>Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

13	LBERT_PG_START_OVR_EN	R/W	<p>Pattern generator start override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
12	LBERT_PG_START_OVR_VAL	R/W	<p>Pattern generator start override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
11:8	LBERT_PG_MODE	R/W	<p>Pattern generator mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern generator disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p><b>reserved Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	R/W	<p>Pattern matcher error counter sampling override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	R/W	<p>Pattern matcher error counter sampling override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

5	LBERT_PM_START_OVR_EN	R/W	<p>Pattern matcher start override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	LBERT_PM_START_OVR_VAL	R/W	<p>Pattern matcher start override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
3:0	LBERT_PM_MODE	R/W	<p>Pattern matcher mode. This bus is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern matcher disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p><b>reserved Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

**PPI\_RW\_CPHY\_TRI00\_LBERT\_1**

- **Description:** CPHY loopback control
- **Size:** 16 bits
- **Offset:** 0x4001

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>

7:0	LBERT_PG_USER_PATTERN	R/W	Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
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**PPI\_R\_CPHY\_TRIO0\_LBERT\_0**

- **Description:** CPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x4002

Bits	Name	Memory Access	Description
15:0	LBERT_PM_ERROR_COUNTER	R	Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER. <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**PPI\_R\_CPHY\_TRIO0\_LBERT\_1**

- **Description:** CPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x4003

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	LBERT_PG_ENABLED	R	Pattern generator enable observability. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**PPI\_RW\_CPHY\_TRIO0\_SPARE**

- **Description:** CPHY spare registers
- **Size:** 16 bits
- **Offset:** 0x4004

Bits	Name	Memory Access	Description
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15:0	CPHY_TRI00_SPARE	R/W	Spare registers for future use <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**PPI\_RW\_CPHY\_TRI01\_LBERT\_0**

- **Description:** CPHY loopback control
- **Size:** 16 bits
- **Offset:** 0x4200

Bits	Name	Memory Access	Description
15	LBERT_PM_DATA_SWAP	R/W	Controls trio mux to choose normal or swapped data (actual reset value is 0xX) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14	LBERT_PG_ERROR_INJECTION	R/W	Injects 1 bit error on output pattern. Active high. Each rising edge inserts 1 error. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

13	LBERT_PG_START_OVR_EN	R/W	Pattern generator start override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
12	LBERT_PG_START_OVR_VAL	R/W	Pattern generator start override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

11:8	LBERT_PG_MODE	R/W	<p>Pattern generator mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern generator disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p><b>reserved Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
7	LBERT_PM_SAMPLE_COUNTER_OVR_EN	R/W	<p>Pattern matcher error counter sampling override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
6	LBERT_PM_SAMPLE_COUNTER_OVR_VAL	R/W	<p>Pattern matcher error counter sampling override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

5	LBERT_PM_START_OVR_EN	R/W	<p>Pattern matcher start override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>
4	LBERT_PM_START_OVR_VAL	R/W	<p>Pattern matcher start override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

3:0	LBERT_PM_MODE	R/W	<p>Pattern matcher mode. This bus is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 4'b0000: pattern matcher disabled</li> <li>■ 4'b0001: PRBS31 (<math>x^{31} + x^{28} + 1</math>)</li> <li>■ 4'b0010: PRBS23 (<math>x^{23} + x^{18} + 1</math>)</li> <li>■ 4'b0011: PRBS23 (<math>x^{23} + x^{21} + x^{16} + x^8 + x^5 + x^2 + 1</math>)</li> <li>■ 4'b0100: PRBS16 (<math>x^{16} + x^5 + x^4 + x^3 + 1</math>)</li> <li>■ 4'b0101: PRBS15 (<math>x^{15} + x^{14} + 1</math>)</li> <li>■ 4'b0110: PRBS11 (<math>x^{11} + x^9 + 1</math>)</li> <li>■ 4'b0111: PRBS9 (<math>x^9 + x^5 + 1</math>)</li> <li>■ 4'b1000: PRBS7 (<math>x^7 + x^6 + 1</math>)</li> <li>■ 4'b1001: Custom 8 bit pattern</li> <li>■ 4'b1010: DC balanced custom 8 bit pattern (pat[7:0], ~pat[7:0])</li> <li>■ all others</li> </ul> <p>reserved <b>Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
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**PPI\_RW\_CPHY\_TRI01\_LBERT\_1**

- **Description:** CPHY loopback control
- **Size:** 16 bits
- **Offset:** 0x4201

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	LBERT_PG_USER_PATTERN	R/W	<p>Custom 8 bit pattern. Requires LBERT_PG_MODE to be set to 4'b1001 or 4'b1010. This bus is quasi-static.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

**PPI\_R\_CPHY\_TRI01\_LBERT\_0**

- **Description:** CPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x4202

Bits	Name	Memory Access	Description
15:0	LBERT_PM_ERROR_COUNTER	R	<p>Pattern matcher error counter. Readouts are valid after a rising edge on LBERT_PM_SAMPLE_COUNTER.</p> <p><b>Value After Reset:</b> 0x1</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**PPI\_R\_CPHY\_TRI01\_LBERT\_1**

- **Description:** CPHY loopback observability
- **Size:** 16 bits
- **Offset:** 0x4203

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
0	LBERT_PG_ENABLED	R	<p>Pattern generator enable observability. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**PPI\_RW\_CPHY\_TRI01\_SPARE**

- **Description:** CPHY spare registers
- **Size:** 16 bits
- **Offset:** 0x4204

Bits	Name	Memory Access	Description
15:0	CPHY_TRI01_SPARE	R/W	<p>Spare registers for future use</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_0\_RW\_CFG\_0**

- **Description:** CPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x5000

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10	LOOPBACK_MODE_EN	R/W	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	CFG_0_SWAP_ENCODE_REG	R/W	Order of encoding LSB to MSB or MSB to LSB <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

8	CFG_0_ALP_ENABLE_REG	R/W	Enable ALP mode <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	CFG_0_HS_SYNC_DET_SWAP_REG	R/W	Sync detector swap control <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	CFG_0_HS_ALIGNER_SWAP_REG	R/W	Aligner output swap control <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
5	CFG_0_HS_DECODE_SWAP_REG	R/W	Decoder swap control : looks from MSB to LSB when decoding <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	CFG_0_HS_ORDER_SWAP_REG	R/W	Deserializer MSB to LSB swap control <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	CFG_0_HS_PIN_SWAP_REG	R/W	Select the three lines' order in high speed mode <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

2:0	CFG_0_LP_PIN_SWAP_REG	R/W	<p>Swap a, b and c lines. Applies to low power mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 3'b000: TX ABC connected to RX ABC</li> <li>■ 3'b001: TX ABC connected to RX CBA</li> <li>■ 3'b010: TX ABC connected to RX ACB</li> <li>■ 3'b011: TX ABC connected to RX BCA</li> <li>■ 3'b100: TX ABC connected to RX BAC</li> <li>■ 3'b101: TX ABC connected to RX CAB</li> <li>■ all others</li> </ul> <p><b>reserved Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
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**CORE\_DIG\_CLANE\_0\_RW\_CFG\_2**

- **Description:** CPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x5002

Bits	Name	Memory Access	Description
15:0	CFG_2_SPARE	R/W	<p>Spare registers for future use. <b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_0\_RW\_LP\_0**

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5040

Bits	Name	Memory Access	Description
15:12	LP_0_ITMINRX_REG	R/W	<p>LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x4</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

11:8	LP_0_TTAGO_REG	R/W	BTA timing control. Defines the time that the transmitter drives LP000 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.  <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
7:4	LP_0_TTASURE_REG	R/W	BTA timing control. Defines the time that the new transmitter waits, after the LP100 state before driving LP000. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.  <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

3:0	LP_0_TTAGET_REG	R/W	BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE  <b>Value After Reset:</b> 0xc <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
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### CORE\_DIG\_CLANE\_0\_RW\_LP\_1

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5041

Bits	Name	Memory Access	Description
15:8	LP_1_LPTX_PON_TIMER_REG	R/W	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static.  <b>Value After Reset:</b> 0x80 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	LP_1_ERRCONTENTION_THRES_REG	R/W	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static.  <b>Value After Reset:</b> 0x10 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

### CORE\_DIG\_CLANE\_0\_RW\_LP\_2

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits

- **Offset:** 0x5042

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	LP_2_FILTER_INPUT_SAMPLING_REG	R/W	LPRX filter input data sampling <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

### CORE\_DIG\_CLANE\_0\_R\_LP\_0

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x5050

Bits	Name	Memory Access	Description
15:2	RESERVED_15_2	R	Reserved for Future use and actual reset value is 0X <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
1	LP_0_RXHSRQST	R	Signal which indicates that the HS entry transition LP111 -> LP001 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LP_0_HSACTIVERX	R	Signal which indicates that the HS entry transition LP001 -> LP000 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

### CORE\_DIG\_CLANE\_0\_R\_LP\_1

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x5051

Bits	Name	Memory Access	Description

15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:8	LP_1_STATE_LPTX	R	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
7:4	LP_1_STATE_LPRX	R	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	LP_1_STATE_BTA	R	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_CLANE\_0\_RW\_HS\_RX\_0**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5080

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:7	HSRX_CPHY_CDR_FBK_EN_DLY_REG	R/W	Timer counter after which hsrx_cphy_cdr_fbk_en is asserted (word_clk cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

6:2	HSACTIVERX_DLY_REG	R/W	Timer counter after which hsactiverx is asserted (DCO clock cycles) <b>Value After Reset:</b> 0x5 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
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1	HS_RX_0_HS_CDR_FEEDBACK_ENABLED_REG	R/W	Signal which indicates whether the feedback loop is enabled. (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	HS_RX_0_HS_CDR_UPDATE_SETTINGS_REG	R/W	Signal used to update the CDR calibration machine's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_CLANE\_0\_RW\_HS\_RX\_1**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5081

Bits	Name	Memory Access	Description
15:0	HS_RX_1_HS_CDR_TIMEBASE_TARGET_REG	R/W	Timebase for the oscillation clock's tick count (cfg_clk cycles) <b>Value After Reset:</b> 0x14 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_0\_RW\_HS\_RX\_2**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5082

Bits	Name	Memory Access	Description
15:0	HS_RX_2_HS_CDR_COARSE_TARGET_REG	R/W	Target for the oscillation clock's tick count (osc_clk cycles) <b>Value After Reset:</b> 0x14 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_0\_RW\_HS\_RX\_3**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5083

Bits	Name	Memory Access	Description

15:7	RESERVED_15_7	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
6:1	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_DLY_REG	R/W	Timer counter after which hsrxCphy_cdr_fbk_fast_lock_en is asserted (word clock cycles) <b>Value After Reset:</b> 0x3f <b>Exists:</b> Always <b>Reset Mask:</b> 0x3f

0	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_REG	R/W	C-PHY CDR delay mask LPF bandwidth extension. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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**CORE\_DIG\_CLANE\_0\_RW\_HS\_RX\_4**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5084

Bits	Name	Memory Access	Description
15:4	RESERVED_15_4	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
3:0	HS_RX_3_HS_CDR_COARSE_OBS_SEL_REG	R/W	Selector to define setting for which to read CDR cycle count results <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_CLANE\_0\_RW\_HS\_RX\_5**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5085

Bits	Name	Memory Access	Description
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15:0	HS_RX_5_HS_CDR_INIT_WAIT_TARGET_REG	R/W	Counter target for initial CDR delay. (Cfg_clk cycles). Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**CORE\_DIG\_CLANE\_0\_RW\_HS\_RX\_6**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5086

Bits	Name	Memory Access	Description
15:0	HS_RX_6_HS_CDR_STUCK_THR_ESH_REG	R/W	Minimum tick count not to flag a stuck condition (Osc_clk cycles). Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_0\_R\_RX\_0**

- **Description:** HSRX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5090

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0X0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	O_CDR_CALDONE	R	Signal that flags the completion of a CDR calibration (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_CLANE\_0\_R\_RX\_1**

- **Description:** HSRX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5091

Bits	Name	Memory Access	Description
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15:0	COARSE_DIF_TARGET	R	Difference between the oscillation clock's tick count towards the selected target <b>Value After Reset:</b> 0xffff <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff
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**CORE\_DIG\_CLANE\_0\_R\_TX\_0**

- **Description:** HSTX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5092

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:4	STATE_DCO_CHSTX	R	HS-TX DCO clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	STATE_CHSTX	R	HS-TX word clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_CLANE\_0\_R\_RX\_2**

- **Description:** HS RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5093

Bits	Name	Memory Access	Description
15:0	CR_COARSE_VALUE_OBS	R	CDR clock cycles measured for setting defined in cdr_coarse_obs_sel_reg <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_0\_R\_RX\_3**

- **Description:** HS RX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5094

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	CR_CDR_STATUS_OBS	R	CDR calibration status flag <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_0**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5100

Bits	Name	Memory Access	Description
15:0	HS_TX_0_THSEXIT_DCO_REG	R/W	Ths-exit setting (dco_clk cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x14 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_1**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5101

Bits	Name	Memory Access	Description
15:0	HS_TX_1_TPOST_REG	R/W	T3-post setting (word clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_2**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5102

Bits	Name	Memory Access	Description
15:0	HS_TX_2_TCALPREAMBLE_REG	R/W	T3-calpreamble setting (word clock cycles). This field is quasi-static. Please check table for more details. <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_3**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5103

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:11	HS_TX_3_STATE_DCO_OVR_VA_L_REG	R/W	HS-TX FSM state (DCO clock) override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
10	HS_TX_3_STATE_DCO_VR_EN_REG	R/W	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

9	HS_TX_3_INVORDER_REG	R/W	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	HS_TX_3_HSDIRECT_REG	R/W	Reserved <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

7:5	HS_TX_3_BURST_TYPE_REG	R/W	<p>Select burst to transmit type.</p> <ul style="list-style-type: none"> <li>■ 000 For normal burst</li> <li>■ 001 for normal burst with programmable sequence</li> <li>■ 010 for calibration</li> </ul> <p><b>burst Value After</b></p> <p><b>Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7</p>
4	HS_TX_3_STATE_OVR_EN_REG	R/W	<p>state override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always <b>Reset Mask:</b> 0x1</p>
3:0	HS_TX_3_STATE_OVR_REG	R/W	<p>state override enable. Active high. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always <b>Reset Mask:</b> 0xf</p>

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_4**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5104

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always <b>Reset Mask:</b> 0x0</p>
14:12	HS_TX_4_PROGSEQSYMB4_REG	R/W	<p>Symbol 4 of the programmable sequence</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always <b>Reset Mask:</b> 0x7</p>
11:9	HS_TX_4_PROGSEQSYMB3_REG	R/W	<p>Symbol 3 of the programmable sequence</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always <b>Reset Mask:</b> 0x7</p>
8:6	HS_TX_4_PROGSEQSYMB2_REG	R/W	<p>Symbol 2 of the programmable sequence</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always <b>Reset Mask:</b> 0x7</p>

5:3	HS_TX_4_PROGSEQSYMB1_REG	R/W	Symbol 1 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
2:0	HS_TX_4_PROGSEQSYMB0_REG	R/W	Symbol 0 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_5**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5105

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:12	HS_TX_5_PROGSEQSYMB9_REG	R/W	Symbol 9 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
11:9	HS_TX_5_PROGSEQSYMB8_REG	R/W	Symbol 8 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
8:6	HS_TX_5_PROGSEQSYMB7_REG	R/W	Symbol 7 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
5:3	HS_TX_5_PROGSEQSYMB6_REG	R/W	Symbol 6 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
2:0	HS_TX_5_PROGSEQSYMB5_REG	R/W	Symbol 5 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_6**

- **Description:** High speed TX subsystem parameters control

- **Size:** 16 bits
- **Offset:** 0x5106

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14:12	HS_TX_6_PIN_SWAP_REG	R/W	<p>Swap ABC lines. Applies to high speed mode. This field is quasi-static.</p> <ul style="list-style-type: none"> <li>■ 3'b000: TX ABC connected to RX ABC</li> <li>■ 3'b001: TX ABC connected to RX CBA</li> <li>■ 3'b010: TX ABC connected to RX ACB</li> <li>■ 3'b011: TX ABC connected to RX BCA</li> <li>■ 3'b100: TX ABC connected to RX BAC</li> <li>■ 3'b101: TX ABC connected to RX CAB</li> <li>■ all others</li> </ul> <p>reserved <b>Value</b></p> <p><b>After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
11:9	HS_TX_6_PROGSEQSYMB13_R EG	R/W	<p>Symbol 13 of the programmable sequence</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
8:6	HS_TX_6_PROGSEQSYMB12_R EG	R/W	<p>Symbol 12 of the programmable sequence</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
5:3	HS_TX_6_PROGSEQSYMB11_R EG	R/W	<p>Symbol 11 of the programmable sequence</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>
2:0	HS_TX_6_PROGSEQSYMB10_R EG	R/W	<p>Symbol 10 of the programmable sequence</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x7</p>

### CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_7

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits

- **Offset:** 0x5107

Bits	Name	Memory Access	Description
15:0	HS_TX_7_T3PRPR_DCO_REG	R/W	<p>Timer counter for T3prepare (DCO clock cycles). Defines the time to wait after driving LP000 to the lines before turning on the HS logic</p> <p><b>Value After Reset:</b> 0xd</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

#### CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_8

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5108

Bits	Name	Memory Access	Description
15:0	HS_TX_8_TLP11END_DCO_REG	R/W	<p>Final time to drive LP111 to the lines (after HS-leave) (DCO clock cycles)</p> <p><b>Value After Reset:</b> 0xa</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

#### CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_9

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5109

Bits	Name	Memory Access	Description
15:0	HS_TX_9_T3POST_DCO_REG	R/W	<p>Timer counter for T3post (DCO clock cycles). Defines how long to keep the HS logic on before moving to LP111</p> <p><b>Value After Reset:</b> 0x6</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

#### CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_10

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x510a

Bits	Name	Memory Access	Description
15:0	HS_TX_10_TPREBEGIN_REG	R/W	<p>Timer counter for Treamble begin (word_clk cycles). Defines the time to drive the preamble pattern to the lines before sending the programmable sequence (if applicable).</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_11**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x510b

Bits	Name	Memory Access	Description
15:0	HS_TX_11_TLPX_DCO_REG	R/W	<p>Timer counter for TlpX (DCO clock cycles). Defines the time to drive LP001 to the lines.</p> <p><b>Value After Reset:</b> 0xa</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_12**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x510c

Bits	Name	Memory Access	Description
15:0	HS_TX_12_TLP11INIT_DCO_REG	R/W	<p>Initial time to drive LP111 to the lines (before HS-entry) (DCO clock cycles)</p> <p><b>Value After Reset:</b> 0xa</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_0\_RW\_HS\_TX\_13**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x510d

Bits	Name	Memory Access	Description

15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:0	HS_TX_13_TLPTXOVERLAP_REG	R/W	Counter to define the time the LPTX driver overlaps the HSTX driver. (dco_clk cycles). This field is quasi-static. <b>Value After Reset:</b> 0x6 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_CLANE\_1\_RW\_CFG\_0**

- **Description:** CPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x5200

Bits	Name	Memory Access	Description
15:11	RESERVED_15_11	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
10	LOOPBACK_MODE_EN	R/W	Primes the lane in loopback mode by enabling the LP-TX and LP-RX at the same time. Active high. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
9	CFG_0_SWAP_ENCODE_REG	R/W	Order of encoding LSB to MSB or MSB to LSB <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	CFG_0_ALP_ENABLE_REG	R/W	Enable ALP mode <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7	CFG_0_HS_SYNC_DET_SWAP_REG	R/W	Sync detector swap control <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
6	CFG_0_HS_ALIGNER_SWAP_REG	R/W	Aligner output swap control <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

Bits	Name	Memory Access	Description
5	CFG_0_HS_DECODE_SWAP_REG	R/W	Decoder swap control : looks from MSB to LSB when decoding <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
4	CFG_0_HS_ORDER_SWAP_REG	R/W	Deserializer MSB to LSB swap control <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3	CFG_0_HS_PIN_SWAP_REG	R/W	Select the three lines' order in high speed mode <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
2:0	CFG_0_LP_PIN_SWAP_REG	R/W	Swap a, b and c lines. Applies to low power mode. This field is quasi-static. <ul style="list-style-type: none"> <li>■ 3'b000: TX ABC connected to RX ABC</li> <li>■ 3'b001: TX ABC connected to RX CBA</li> <li>■ 3'b010: TX ABC connected to RX ACB</li> <li>■ 3'b011: TX ABC connected to RX BCA</li> <li>■ 3'b100: TX ABC connected to RX BAC</li> <li>■ 3'b101: TX ABC connected to RX CAB</li> <li>■ all others</li> </ul> <b>reserved Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_CLANE\_1\_RW\_CFG\_2**

- **Description:** CPHY lane configuration
- **Size:** 16 bits
- **Offset:** 0x5202

Bits	Name	Memory Access	Description
15:0	CFG_2_SPARE	R/W	Spare registers for future use. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_1\_RW\_LP\_0**

- **Description:** Low power subsystem parameters control

- **Size:** 16 bits
- **Offset:** 0x5240

Bits	Name	Memory Access	Description
15:12	LP_0_ITMINRX_REG	R/W	<p>LP-RX pulse filter width (in dco_clk cycles). Used to reject pulses smaller than the desired size. This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x4</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
11:8	LP_0_TTAGO_REG	R/W	<p>BTA timing control. Defines the time that the transmitter drives LP000 before releasing control of the lines. Tta-go timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x6</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
7:4	LP_0_TTASURE_REG	R/W	<p>BTA timing control. Defines the time that the new transmitter waits, after the LP100 state before driving LP000. Tta-sure timer counter (resolution of 1/2 txclkesc period). This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

3:0	LP_0_TTAGET_REG	R/W	<p>BTA timing control. Defines the time that the new transmitter drives LP000 after taking control of the lines. Tta-get timer counter (resolution of 1/2 txclkesc period). This field is quasi-static. Effective timer size is LP_0_TTAGET - LP_0_TTASURE</p> <p><b>Value After Reset:</b> 0xc</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>
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### CORE\_DIG\_CLANE\_1\_RW\_LP\_1

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5241

Bits	Name	Memory Access	Description
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15:8	LP_1_LPTX_PON_TIMER_REG	R/W	LP-TX power on timer (in txclkesc cycles). Defines the time when switching from the ULP pull down back to the LP-TX driver. This field is quasi-static. <b>Value After Reset:</b> 0x80 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff
7:0	LP_1_ERRCONTENTION_THRES_REG	R/W	Error contention detection filter size (in dco_clk cycles). Defines the time that the system tolerates contention before asserting errcontentionlp* flags. This field is quasi-static. <b>Value After Reset:</b> 0x10 <b>Exists:</b> Always <b>Reset Mask:</b> 0xff

**CORE\_DIG\_CLANE\_1\_RW\_LP\_2**

- **Description:** Low power subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5242

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	LP_2_FILTER_INPUT_SAMPLING_REG	R/W	LPRX filter input data sampling <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_CLANE\_1\_R\_LP\_0**

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x5250

Bits	Name	Memory Access	Description
15:2	RESERVED_15_2	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0

1	LP_0_RXHSRQST	R	Signal which indicates that the HS entry transition LP111 -> LP001 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	LP_0_HSACTIVERX	R	Signal which indicates that the HS entry transition LP001 -> LP000 has been observed. Active high. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_CLANE\_1\_R\_LP\_1**

- **Description:** Low power subsystem status
- **Size:** 16 bits
- **Offset:** 0x5251

Bits	Name	Memory Access	Description
15:13	RESERVED_15_13	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
12:8	LP_1_STATE_LPTX	R	LP-TX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
7:4	LP_1_STATE_LPRX	R	LP-RX FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	LP_1_STATE_BTA	R	BTA FSM state variable observability. CDC can prevent full observability of all states. Available through OCLA in proper synchronous fashion. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_CLANE\_1\_RW\_HS\_RX\_0**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5280

Bits	Name	Memory Access	Description
15:10	RESERVED_15_10	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
9:7	HSRX_CPHY_CDR_FBK_EN_DLY_REG	R/W	Timer counter after which hsrx_cphy_cdr_fbk_en is asserted (word_clk cycles) <b>Value After Reset:</b> 0x3 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

6:2	HSACTIVERX_DLY_REG	R/W	Timer counter after which hsactiverx is asserted (DCO clock cycles) <b>Value After Reset:</b> 0x5 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1f
1	HS_RX_0_HS_CDR_FEEDBACK_ENABLED_REG	R/W	Signal which indicates whether the feedback loop is enabled. (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
0	HS_RX_0_HS_CDR_UPDATE_SETTINGS_REG	R/W	Signal used to update the CDR calibration machine's settings (Active high) <b>Value After Reset:</b> 0x1 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

### CORE\_DIG\_CLANE\_1\_RW\_HS\_RX\_1

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5281

Bits	Name	Memory Access	Description
15:0	HS_RX_1_HS_CDR_TIMEBASE_TARGET_REG	R/W	Timebase for the oscillation clock's tick count (cfg_clk cycles) <b>Value After Reset:</b> 0x14 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

### CORE\_DIG\_CLANE\_1\_RW\_HS\_RX\_2

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits

- **Offset:** 0x5282

Bits	Name	Memory Access	Description
15:0	HS_RX_2_HS_CDR_COARSE_TARGET_REG	R/W	<p>Target for the oscillation clock's tick count (osc_clk cycles)</p> <p><b>Value After Reset:</b> 0x14</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

### CORE\_DIG\_CLANE\_1\_RW\_HS\_RX\_3

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5283

Bits	Name	Memory Access	Description
15:7	RESERVED_15_7	R	<p>Reserved for Future use and actual reset value is 0X0</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
6:1	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_DLY_REG	R/W	<p>Timer counter after which hsrxCphy_cdr_fbk_fast_lock_en is asserted (word clock cycles)</p> <p><b>Value After Reset:</b> 0x3f</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x3f</p>

Bits	Name	Memory Access	Description
0	HSRX_CPHY_CDR_FBK_FAST_LOCK_EN_REG	R/W	<p>C-PHY CDR delay mask LPF bandwidth extension. Active high.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

### CORE\_DIG\_CLANE\_1\_RW\_HS\_RX\_4

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5284

Bits	Name	Memory Access	Description

15:4	RESERVED_15_4	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
3:0	HS_RX_3_HS_CDR_COARSE_O BS_SEL_REG	R/W	Selector to define setting for which to read CDR cycle count results <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_CLANE\_1\_RW\_HS\_RX\_5**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5285

Bits	Name	Memory Access	Description
15:0	HS_RX_5_HS_CDR_INIT_WAIT_TARGET_REG	R/W	Counter target for initial CDR delay. (Cfg_clk cycles). Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_1\_RW\_HS\_RX\_6**

- **Description:** CPHY HS RX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5286

Bits	Name	Memory Access	Description
15:0	HS_RX_6_HS_CDR_STUCK_THR_ESH_REG	R/W	Minimum tick count not to flag a stuck condition (Osc_clk cycles). Quasi static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_1\_R\_RX\_0**

- **Description:** HSRX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5290

Bits	Name	Memory Access	Description

15:1	RESERVED_15_1	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
0	O_CDR_CALDONE	R	Signal that flags the completion of a CDR calibration (Active high) <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1

**CORE\_DIG\_CLANE\_1\_R\_RX\_1**

- **Description:** HSRX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5291

Bits	Name	Memory Access	Description
15:0	COARSE_DIF_TARGET	R	Difference between the oscillation clock's tick count towards the selected target <b>Value After Reset:</b> 0xffff <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_1\_R\_TX\_0**

- **Description:** HSTX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5292

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
7:4	STATE_DCO_CHSTX	R	HS-TX DCO clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf
3:0	STATE_CHSTX	R	HS-TX word clock FSM state <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_CLANE\_1\_R\_RX\_2**

- **Description:** HSRX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5293

Bits	Name	Memory Access	Description
15:0	CR_COARSE_VALUE_OBS	R	<p>CDR clock cycles measured for setting defined in cdr_coarse_obs_sel_reg</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_1\_R\_RX\_3**

- **Description:** HSRX subsystem status
- **Size:** 16 bits
- **Offset:** 0x5294

Bits	Name	Memory Access	Description
15:1	RESERVED_15_1	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
0	CR_CDR_STATUS_OBS	R	<p>CDR calibration status flag</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x1</p>

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_0**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5300

Bits	Name	Memory Access	Description
15:0	HS_TX_0_THSEXIT_DCO_REG	R/W	<p>Ths-exit setting (dco_clk cycles). This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x14</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_1**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5301

Bits	Name	Memory Access	Description
15:0	HS_TX_1_TPOST_REG	R/W	<p>T3-post setting (word clock cycles). This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_2**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5302

Bits	Name	Memory Access	Description
15:0	HS_TX_2_TCALPREAMBLE_REG	R/W	<p>T3-calpreamble setting (word clock cycles). This field is quasi-static. Please check table for more details.</p> <p><b>Value After Reset:</b> 0x3</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_3**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5303

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	<p>Reserved for Future use and actual reset value is 0xX</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
14:11	HS_TX_3_STATE_DCO_OVR_VA_L_REG	R/W	<p>HS-TX FSM state (DCO clock) override value. Used for debug purposes.</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xf</p>

10	HS_TX_3_STATE_DCO_VR_EN_REG	R/W	HS-TX FSM state (DCO clock) override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
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9	HS_TX_3_INVORDER_REG	R/W	Invert TX data's MSB to LSB transmission order. Active high. This field is quasi-static. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
8	HS_TX_3_HSDIRECT_REG	R/W	Reserved <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
7:5	HS_TX_3_BURST_TYPE_REG	R/W	Select burst to transmit type. <ul style="list-style-type: none"><li>■ 000 For normal burst</li><li>■ 001 for normal burst with programmable sequence</li><li>■ 010 for calibration</li></ul> burst <b>Value After</b> <b>Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
4	HS_TX_3_STATE_OVR_EN_REG	R/W	state override value. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x1
3:0	HS_TX_3_STATE_OVR_REG	R/W	state override enable. Active high. Used for debug purposes. <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0xf

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_4**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5304

Bits	Name	Memory Access	Description
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15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:12	HS_TX_4_PROGSEQSYMB4_REG	R/W	Symbol 4 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
11:9	HS_TX_4_PROGSEQSYMB3_REG	R/W	Symbol 3 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
8:6	HS_TX_4_PROGSEQSYMB2_REG	R/W	Symbol 2 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

5:3	HS_TX_4_PROGSEQSYMB1_REG	R/W	Symbol 1 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
2:0	HS_TX_4_PROGSEQSYMB0_REG	R/W	Symbol 0 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_5**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5305

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0xX <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:12	HS_TX_5_PROGSEQSYMB9_REG	R/W	Symbol 9 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

11:9	HS_TX_5_PROGSEQSYMB8_REG	R/W	Symbol 8 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
8:6	HS_TX_5_PROGSEQSYMB7_REG	R/W	Symbol 7 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

5:3	HS_TX_5_PROGSEQSYMB6_REG	R/W	Symbol 6 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
2:0	HS_TX_5_PROGSEQSYMB5_REG	R/W	Symbol 5 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_6**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5306

Bits	Name	Memory Access	Description
15	RESERVED_15_15	R	Reserved for Future use and actual reset value is 0X0 <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x0
14:12	HS_TX_6_PIN_SWAP_REG	R/W	Swap ABC lines. Applies to high speed mode. This field is quasi-static. <ul style="list-style-type: none"> <li>■ 3'b000: TX ABC connected to RX ABC</li> <li>■ 3'b001: TX ABC connected to RX CBA</li> <li>■ 3'b010: TX ABC connected to RX ACB</li> <li>■ 3'b011: TX ABC connected to RX BCA</li> <li>■ 3'b100: TX ABC connected to RX BAC</li> <li>■ 3'b101: TX ABC connected to RX CAB</li> <li>■ all others</li> </ul> <b>reserved Value</b> <b>After Reset:</b> 0x0 <b>Exists:</b> Always

			<b>Reset Mask:</b> 0x7
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11:9	HS_TX_6_PROGSEQSYMB13_R EG	R/W	Symbol 13 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
8:6	HS_TX_6_PROGSEQSYMB12_R EG	R/W	Symbol 12 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
5:3	HS_TX_6_PROGSEQSYMB11_R EG	R/W	Symbol 11 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7
2:0	HS_TX_6_PROGSEQSYMB10_R EG	R/W	Symbol 10 of the programmable sequence <b>Value After Reset:</b> 0x0 <b>Exists:</b> Always <b>Reset Mask:</b> 0x7

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_7**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5307

Bits	Name	Memory Access	Description
15:0	HS_TX_7_T3PRPR_DCO_REG	R/W	Timer counter for T3prepare (DCO clock cycles). Defines the time to wait after driving LP000 to the lines before turning on the HS logic <b>Value After Reset:</b> 0xd <b>Exists:</b> Always <b>Reset Mask:</b> 0xffff

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_8**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5308

Bits	Name	Memory Access	Description
15:0	HS_TX_8_TLP11END_DCO_REG	R/W	<p>Final time to drive LP111 to the lines (after HS-leave) (DCO clock cycles)</p> <p><b>Value After Reset:</b> 0xa</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_9**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x5309

Bits	Name	Memory Access	Description
15:0	HS_TX_9_T3POST_DCO_REG	R/W	<p>Timer counter for T3post (DCO clock cycles). Defines how long to keep the HS logic on before moving to LP111</p> <p><b>Value After Reset:</b> 0x6</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_10**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x530a

Bits	Name	Memory Access	Description
15:0	HS_TX_10_TPREGBEGIN_REG	R/W	<p>Timer counter for Tpreamble begin (word_clk cycles). Defines the time to drive the preamble pattern to the lines before sending the programmable sequence (if applicable).</p> <p><b>Value After Reset:</b> 0x2</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

**CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_11**

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits

- **Offset:** 0x530b

Bits	Name	Memory Access	Description
15:0	HS_TX_11_TLPX_DCO_REG	R/W	<p>Timer counter for Tlp1x (DCO clock cycles). Defines the time to drive LP001 to the lines.</p> <p><b>Value After Reset:</b> 0xa</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

#### CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_12

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x530c

Bits	Name	Memory Access	Description
15:0	HS_TX_12_TLP11INIT_DCO_REG	R/W	<p>Initial time to drive LP111 to the lines (before HS-entry) (DCO clock cycles)</p> <p><b>Value After Reset:</b> 0xa</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xffff</p>

#### CORE\_DIG\_CLANE\_1\_RW\_HS\_TX\_13

- **Description:** High speed TX subsystem parameters control
- **Size:** 16 bits
- **Offset:** 0x530d

Bits	Name	Memory Access	Description
15:8	RESERVED_15_8	R	<p>Reserved for Future use and actual reset value is 0X</p> <p><b>Value After Reset:</b> 0x0</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0x0</p>
7:0	HS_TX_13_TLPTXOVERLAP_REG	R/W	<p>Counter to define the time the LPTX driver overlaps the HSTX driver. (dco_clk cycles). This field is quasi-static.</p> <p><b>Value After Reset:</b> 0x6</p> <p><b>Exists:</b> Always</p> <p><b>Reset Mask:</b> 0xff</p>

#### 8.4.4 VICAP CSR

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
COMMON_	16'h00			Reserved	

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
SET	00	RW	1'b0	debug_en	Pass through all of the data as embedded data
		RW	1'b0	cap_en	Enable the protocol analysis and output dvp data
		RW	1'b0	rgb_yuv_map	YUV 422 or RGB pixel(2 or 3 words) map to same Lane. 0:distributed to any Lanes; 1:converge on one same Lane.
		RW	3'b0	I_bit	The word length, pixel length. 3'b000: 8bit/word; 3'b001: 10bit/word; 3'b010: 12bit/word; 3'b011: 14bit/word; 3'b100: 16bit/word;
		RW	1'b0	bit_reorder	Reverse the effective bit order based on I_bit pixel length.
		RW	1'b1	ail_msb	AIL MSB/LSB, 0: LSB; 1: MSB.
				Reserved	
		RW	1'b0	yuv422_en	Enable YUV422 format, 2 word per pixel.
				Reserved	
		RW	1'b0	resid_out_en	output received line even if current frame incomplete(for streaming-s mode, none of frame head).
		RW	1'b0	hdr_padd_mode	The padding line detect mode: 0:use start line number(HDR_frm*_start) to detect, 1.use fixed pix value(HDR_padding_pix) detect for padding line.
		RW	1'b0	crop_en	Crop enable
		RW	1'b0	combo_mode	Mode select 0: HiSPi mode, 1: SLVS and SUB-LVDS mode.
		RW	2'b0	phy_num	PHY number of sensor: 2'b00: 1 PHY, 2'b01: 2 PHY, 2'b10: 4 PHY, 2'b11: 8 PHY. Note: Please refer to the sensor's TX PHY info.

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
		RW	2'b0	lane_num	Lane number per PHY of sensor: 2'b00: 1 Lane/PHY, 2'b01: 2 Lane/PHY, 2'b10: 4 Lane/PHY, 2'b11: 8 Lane/PHY. Note: Please refer to the sensor's TX PHY info.
		RW	2'b0	hdr_mode	HDR mode: 2'b00: linear mode single frame, 2'b01: 2 HDR frame, 2'b10: 3 HDR frame, 2'b11: reserved.
		RW	6'b100 100	frm_id	Frame ID: [5:4]: HDR frame-3 ID, [3:2]: HDR frame-2 ID, [1:0]: HDR frame-1 or linear mode single frame ID,
PIC_RES	16'h00 04	RW	16'd64 0	pic_width	Effective pixel width
		RW	16'd48 0	pic_height	Effective pixel height
HDR_ARG1	16'h00 08	RW	16'b0	frm_height	frame height, per frame, contain padding line.
		RW	16'h04	hdr_padd_pix	Value of HDR frame padding line.
HDR_ARG2	16'h00 0C	RW	16'b0	hdr_frm2_star t	HDR second frame start line number.
		RW	16'b0	hdr_frm3_star t	HDR third frame start line number.
CROP_X	16'h00 10	RW	16'b0	pix_crop_x1	Start point of the crop line. 0<x1<x2<width Even number is better.
		RW	16'b0	pix_crop_x2	End point of the crop line. 0<x1<x2<width Even number is better.
CROP_Y	16'h00 14	RW	16'b0	pix_crop_y1	Start line of the crop zone. 0<y1<y2<height Even number is better.
		RW	16'b0	pix_crop_y2	End line of the crop zone. 0<y1<y2<height Even number is better.

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
SC1	16'h00 18	RW	16'b0	sc_w1	<p>Sync Code word1, maybe            HiSPI ActiveStart-SP8 SOF word 1            HiSPI Packetized-SP SOF word 4            HiSPI Streaming-SP SOF word 4            SLVS HDR mode 1 frame 1, SOF word4            SLVS HDR mode 2/3 frame 1, SAV(Valid) word 4            SLVS single frame mode SOF/SAV(Valid) word 4            Note: Unused bit must be set to 0</p>
				sc_w2	<p>Sync Code word2, maybe            HiSPI ActiveStart-SP8 SOF word 2            HiSPI Packetized-SP SOL word 4            HiSPI Streaming-SP SOL word 4            HiSPI Streaming-S SOL word 4            SLVS HDR mode 1 frame 2, SOF word4            SLVS HDR mode 2/3 frame 2, SAV(Valid) word 4            Note: Unused bit must be set to 0</p>
SC2	16'H00 1c	RW	16'b0	sc_w3	<p>Sync Code word3, maybe            HiSPI ActiveStart-SP8 SOF word 3            HiSPI Packetized-SP EOF word 4            SLVS HDR mode 1 frame 3, SOF word4            SLVS HDR mode 2/3 frame 3, SAV(Valid) word 4            Note: Unused bit must be set to 0</p>
				sc_w4	<p>Sync Code word4, maybe            HiSPI ActiveStart-SP8 SOF word 4            HiSPI Packetized-SP EOL word 4            SLVS HDR mode 1 frame 1, SOL word4            SLVS HDR mode 3 frame 1, SAV(Valid) word 5            SLVS single frame mode SAV(Valid) word 5            SLVS single frame mode SOL word4            Note: Unused bit must be set to 0</p>
SC3	16'h00 20	RW	16'b0	sc_w5	<p>Sync Code word5, maybe            HiSPI ActiveStart-SP8 SOF word 5            HiSPI Streaming-SP SOV word 4            HiSPI Streaming-S SOV word 4            SLVS HDR mode 1 frame 2, SOL word4            SLVS HDR mode 3 frame 2, SAV(Valid) word 5            Note: Unused bit must be set to 0</p>

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
		RW	16'b0	sc_w6	Sync Code word6, maybe HiSPi ActiveStart-SP8 SOF word 6 SLVS HDR mode 1 frame 3, SOL word4 SLVS HDR mode 3 frame 3, SAV(Valid) word 5 Note: Unused bit must be set to 0
SC4	16'h00 24	RW	16'b0	sc_w7	Sync Code word7, maybe HiSPi ActiveStart-SP8 SOF word 7 SLVS HDR mode 1 frame 1, EOF word4 SLVS HDR mode 2/3 frame 1, EAV(Valid) word 4 SLVS single frame mode EOF/EAV(Valid) word 4 Note: Unused bit must be set to 0
		RW	16'b0	sc_w8	Sync Code word8, maybe HiSPi ActiveStart-SP8 SOF word 8 SLVS HDR mode 1 frame 2, EOF word4 SLVS HDR mode 2/3 frame 2, EAV(Valid) word 4 Note: Unused bit must be set to 0
		RW	16'b0	sc_w9	Sync Code word9, maybe HiSPi ActiveStart-SP8 SOL word 1 SLVS HDR mode 1 frame 3, EOF word4 SLVS HDR mode 2/3 frame 3, EAV(Valid) word 4 Note: Unused bit must be set to 0
SC5	16'h00 28	RW	16'b0	sc_w10	Sync Code word10, maybe HiSPi ActiveStart-SP8 SOL word 2 SLVS HDR mode 1 frame 1, EOL word4 SLVS HDR mode 2/3 frame 1, EAV(Valid) word 5 Note: Unused bit must be set to 0
		RW	16'b0	sc_w11	Sync Code word11, maybe HiSPi ActiveStart-SP8 SOL word 3 SLVS HDR mode 1 frame 2, EOL word4 SLVS HDR mode 2/3 frame 2, EAV(Valid) word 5 Note: Unused bit must be set to 0
SC6	16'h00 2c	RW	16'b0	sc_w12	Sync Code word12, maybe HiSPi ActiveStart-SP8 SOL word 4 SLVS HDR mode 1 frame 3, EOL word4 SLVS HDR mode 3 frame 3, EAV(Valid) word 5

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
					Note: Unused bit must be set to 0
SC7	16'h00 30	RW	16'b0	sc_w13	Sync Code word13, maybe HiSPi ActiveStart-SP8 SOL word 5 SLVS HDR mode 2/3 SAV(Invalid) word 4 SLVS single frame mode SAV(Invalid) word 4 Note: Unused bit must be set to 0
		RW	16'b0	sc_w14	Sync Code word14, maybe HiSPi ActiveStart-SP8 SOL word 6 SLVS HDR mode 2/3 EAV(Invalid) word 4 SLVS single frame mode EAV(Invalid) word 4 Note: Unused bit must be set to 0
SC8	16'h00 34	RW	16'b0	sc_w15	Sync Code word15, maybe HiSPi ActiveStart-SP8 SOL word 7 SLVS HDR mode 3 SAV(Invalid) word 5 Note: Unused bit must be set to 0
		RW	16'b0	sc_w16	Sync Code word16, maybe HiSPi ActiveStart-SP8 SOL word 8 SLVS HDR mode 3 EAV(Invalid) word 5 Note: Unused bit must be set to 0
SLVS_ARG	16'h00 3C			Reserved	
		RW	1'b0	slvs_map	Sync Code mapping when SLVS or SUB-LVDSmode 0:Sync Code duplication copies a word to every Lanes. 1:Sync Code striped across the data Lanes within each PHY.
		RW	1'b0	slvs_5word	SLVS or SUB-LVDS Sync Code word length config 0:Sync Code 4 words. 1:Sync Code 5 words.
		RW	1'b0	slvs_mode	SLVS or SUB-LVDS Sync Code mode config 0:SLVS and SUB-LVDS use SAV(valid and invalid) and EAV(valid and invalid) as Sync Code. 1:SLVS and SUB-LVDS use SOF, SOL, EOF and EOL Sync Code as Sync Code.

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
				Reserved	
		RW	3'b0	info_line_en	Has info line each frame(max 3 HDR frame) when SLVS or SUB-LVDS mode
				Reserved	
		RW	3'b0	ob_line_en	Has OB line each frame(max 3 HDR frame) when SLVS or SUB-LVDS mode
		RW	8'b0	info_line_num	Number of info line when SLVS or SUB-LVDS mode
		RW	8'b0	ob_line_num	Number of OB line when SLVS or SUB-LVDS mode
HISPI_ARG	16'h00 40			Reserved	
		RW	1'b0	flr_en	Has FLR word or not.
		RW	1'b0	crc_en	Has CRC word or not.
		RW	4'b0	hispi_mode	[0]: Packetized-SP mode, [1]: Streaming-SP mode, [2]: Streaming-S mode, [3]: ActiveStart-SP8 mode.
				Reserved	
ANLYS_ST ATE	16'h00 44	RO	4'b0	hispi_state	HiSPI fsm state for debug
		RO	4'b0	slvs_state	SLVS fsm state for debug
				Reserved	
		RO	2'b0	crop_state	CROP fsm state for debug
IRQ_EN	16'h00 48			Reserved	
		RW	4'b0	irq_en	Interrupt enable [3]: PHY unlocked interrupt enable, [2]: Start Sync Code error interrupt enable, [1]: End Sync Code error interrupt enable, [0]: Frame end interrupt enable.
				Reserved	
IRQ_STAT E	16'h00 4C			Reserved	
		RW1C	1'b0	irq_phy_unlock	PHY unlocked.
		RW1C	1'b0	irq_so_err	Interrupt status of Start Sync Code error.
		RW1C	1'b0	irq_eo_err	Interrupt status of End Sync Code error interrupt status.
		RW1C	1'b0	irq_frm_end	Interrupt status of Frame end interrupt status.
phy_ctrl_cf g0	16'h00 80	RW	16'b0	sync_mode1_l ane0_0	stream-s mode sync word0 of lane0
		RW	16'b0	sync_mode1_l ane0_1	stream-s mode sync word1 of lane0
phy_ctrl_cf g1	16'h00 84	RW	16'b0	sync_mode1_l ane1_0	stream-s mode sync word0 of lane1
		RW	16'b0	sync_mode1_l	stream-s mode sync word1 of lane1

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
				ane1_1	
phy_ctrl_cf_g2	16'h0088	RW	16'b0	sync_mode1_lane2_0	stream-s mode sync word0 of lane2
		RW	16'b0	sync_mode1_lane2_1	stream-s mode sync word1 of lane2
phy_ctrl_cf_g3	16'h008c	RW	16'b0	sync_mode1_lane3_0	stream-s mode sync word0 of lane3
		RW	16'b0	sync_mode1_lane3_1	stream-s mode sync word1 of lane3
phy_ctrl_cf_g4	16'h0090	RW	16'b0	sync_mode1_lane4_0	stream-s mode sync word0 of lane4
		RW	16'b0	sync_mode1_lane4_1	stream-s mode sync word1 of lane4
phy_ctrl_cf_g5	16'h0094	RW	16'b0	sync_mode1_lane5_0	stream-s mode sync word0 of lane5
		RW	16'b0	sync_mode1_lane5_1	stream-s mode sync word1 of lane5
phy_ctrl_cf_g6	16'h0098	RW	16'b0	sync_mode1_lane6_0	stream-s mode sync word0 of lane6
		RW	16'b0	sync_mode1_lane6_1	stream-s mode sync word1 of lane6
phy_ctrl_cf_g7	16'h009c	RW	16'b0	sync_mode1_lane7_0	stream-s mode sync word0 of lane7
		RW	16'b0	sync_mode1_lane7_1	stream-s mode sync word1 of lane7
phy_ctrl_cf_g8	16'h00a0	RW	1'b0	vin_transfer_lsbs	phy layer data transfer first [0] : MSB [1] : LSB
				Reserved	
		RW	1'b1	vin_soft_rstn	phy layer software reset,active low
		RW	1'b1	vin_unlock_rstn_fifo	word unlock signal reset aysnc fifo enable,active high
		RW	8'h00	vin_lane_en	phy layer 8 lane enable per bit, active high
		RW	1'b0	vin_sync_lsb	phy layer Sync Code transfer first [0] : MSB [1] : LSB
		RW	7'h7f	vin_sync_unlock_ck_num	sync word unlock when continue detect lane number sync word error
		RW	4'h4	vin_sync_line_num	sync word lock when continue detect lane number sync word
		RW	4'ha	vin_afifo_rths	async fifo always empty waterline
phy_ctrl_cf_g9	16'h00a4	RW	10'h16	vin_cycle_range	sync word offset of between two lane
		RW	6'h20	vin_afifo_thsh	async fifo always full waterline
		RW	8'h00	vin_sync_mod_e1	which lane support stream_s mode

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
		RW	4'hf	vin_sync_unlock_num	the line number of sync code error results unlock.
				Reserved	
		RW	2'h0	vin_sync_mod_e1_skew	stream_s mode lane to lane deskew
		RW	1'b0	vin_tp_en	test pattern_enable, active high
phy_ctrl_cfg10	16'h00a8	RW	32'h9f600	vin_lock_time	time out trigger unlock during lock, two fram at 640x480
test_patter_n_cfg0	16'h00ac	RW	16'h0	tp_oneline_num	cycle number of oneline
		RW	16'h0	tp_line_data_num	active pixel cycle number of oneline
test_patter_n_cfg1	16'h00b0	RW	16'h0	tp_line_num	line number of one frame
		RW	16'h0	tp_line_valid_num	active line number of one frame
test_patter_n_cfg2	16'h00b4	RW	8'h0	tp_red_data	test pattern pixel red data
		RW	8'h0	tp_green_data	test pattern pixel green data
		RW	8'h0	tp_blue_data	test pattern pixel blue data
		RW	8'h0	tp_idle_data	test pattern idle data
phy_status0	16'h00b8			Reserved	
		RO	1'b0	vin_sync_lock	phy layer sync lock flag
snapshot_mode	16'h00c0			Reserved	
		RW	1'b0	snapshot_mode	hispi and lvds snapshot mode enable
PHYC_SC0_0	16'h0050	RW	16'hfffff	phyc_sc1_0	Snapshot Mode Snapshot mode hdr0 sync code num1 Stream Mode Stream mode sync code 1st word(L-bit), normally it will be L bit 1
		RW	16'h0000	phyc_sc2_0	Snapshot Mode Snapshot mode hdr0 sync code num2 Stream Mode Stream mode sync code 2nd word(L-bit), normally it will be L bit 0
PHYC_SC0_1	16'h0054	RW	16'h0000	phyc_sc3_0	Snapshot Mode Snapshot mode hdr0 sync code num3 Stream Mode Stream mode sync code 3rd word(L-bit), normally it will be L bit 0
		RW	16'h0000	phyc_sc4_0	snapshot mode hdr0 sync code num4
PHYC_SC0_2	16'h0058	RW	16'h0000	phyc_sc5_0	snapshot mode hdr0 sync code num5
		RW	16'h0000	phyc_sc6_0	snapshot mode hdr0 sync code num6

REG NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	DESCRIPTION
PHYC_SC0_3	16'h005c	RW	16'h0000	phyc_sc7_0	snapshot mode hdr0 sync code num7
		RW	16'h0000	phyc_sc8_0	snapshot mode hdr0 sync code num8
PHYC_SC1_0	16'h0060	RW	16'hfffff	phyc_sc1_1	snapshot mode hdr1 sync code num1
		RW	16'h0000	phyc_sc2_1	snapshot mode hdr1 sync code num2
PHYC_SC1_1	16'h0064	RW	16'h0000	phyc_sc3_1	snapshot mode hdr1 sync code num3
		RW	16'h0000	phyc_sc4_1	snapshot mode hdr1 sync code num4
PHYC_SC1_2	16'h0068	RW	16'h0000	phyc_sc5_1	snapshot mode hdr1 sync code num5
		RW	16'h0000	phyc_sc6_1	snapshot mode hdr1 sync code num6
PHYC_SC1_3	16'h006c	RW	16'h0000	phyc_sc7_1	snapshot mode hdr1 sync code num7
		RW	16'h0000	phyc_sc8_1	snapshot mode hdr1 sync code num8
PHYC_SC2_0	16'h0070	RW	16'hfffff	phyc_sc1_2	snapshot mode hdr2 sync code num1
		RW	16'h0000	phyc_sc2_2	snapshot mode hdr2 sync code num2
PHYC_SC2_1	16'h0074	RW	16'h0000	phyc_sc3_2	snapshot mode hdr2 sync code num3
		RW	16'h0000	phyc_sc4_2	snapshot mode hdr2 sync code num4
PHYC_SC2_2	16'h0078	RW	16'h0000	phyc_sc5_2	snapshot mode hdr2 sync code num5
		RW	16'h0000	phyc_sc6_2	snapshot mode hdr2 sync code num6
PHYC_SC2_3	16'h007c	RW	16'h0000	phyc_sc7_2	snapshot mode hdr2 sync code num7
		RW	16'h0000	phyc_sc8_2	snapshot mode hdr2 sync code num8
soft_rstn	16'h00c4			reserved	
		RW	1'b1	vicap_sw_rstn	Vicap soft reset, low active

#### 8.4.5 DVP2AXI CSR

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
vi_dvp2_axi_ctrl_0	16'h0000	RW	4'h0	dvp3_shift_num	dvp3 pixel data bit shift number
		RW	4'h0	dvp2_shift_num	dvp2 pixel data bit shift number
		RW	4'h0	dvp1_shift_num	dvp1 pixel data bit shift number
		RW	4'h0	dvp0_shift_num	dvp0 pixel data bit shift number
		RW	1'b0	Reserved	
		RO	1'b0	axi_soft_rstn_done	

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
vi_dvp2 axi_ctrl 1	16'h00 04	RW	6'h0	dvp_data_shift	dvp0~dvp5 data shift 0: left shift 1: right shift
		RW	1'h0	axi_burst_len	axi burst length 0: length eq 16 1: length eq 8
		RW	1'h1	dvp2axi_soft_rstn	dvp2axi module soft reset,low active
		RW	6'h0	dvp_chn_en	dvp channel enable
		RW	2'h0	io_dvp_mux	dvp0\dvp1 IO input sel 0:sel dvp0/dvp1 1: sel IO dvp0/dvp1
		RW	5'h8	dvp1_pixel_width	dvp1 pixel data bit width
		RW	5'h8	dvp0_pixel_width	dvp0 pixel data bit width
		RW	2'h0	dvp5_pixel_mode	dvp5 pixel mode 00: 1 pixel weight per cycle 01: 2 pixel weight per cycle 10: 3 pixel weight per cycle 11: reserved
		RW	2'h0	dvp4_pixel_mode	dvp4 pixel mode 00: 1 pixel weight per cycle 01: 2 pixel weight per cycle 10: 3 pixel weight per cycle 11: reserved
		RW	2'h0	dvp3_pixel_mode	dvp3 pixel mode 00: 1 pixel weight per cycle 01: 2 pixel weight per cycle 10: 3 pixel weight per cycle 11: reserved
		RW	2'h0	dvp2_pixel_mode	dvp2 pixel mode 00: 1 pixel weight per cycle 01: 2 pixel weight per cycle 10: 3 pixel weight per cycle 11: reserved
		RW	2'h0	dvp1_pixel_mode	dvp1 pixel mode 00: 1 pixel weight per cycle 01: 2 pixel weight per cycle 10: 3 pixel weight per cycle 11: reserved
		RW	2'h0	dvp0_pixel_mode	dvp0 pixel mode 00: 1 pixel weight per cycle 01: 2 pixel weight per cycle 10: 3 pixel weight per cycle 11: reserved
		RW	4'h0	dvp5_shift_num	dvp5 pixel data bit shift number
		RW	4'h0	dvp4_shift_num	dvp4 pixel data bit shift number

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
vi_dvp2_axi_ctrl_2	16'h0008	RW	8'hf	axi_outstanding	axi outstanding number
		RW	4'h0	axi_mstr_wqos_cfg	axi wqos configure
		RW	5'h8	dvp5_pixel_width	dvp5 pixel data bit width
		RW	5'h8	dvp4_pixel_width	dvp4 pixel data bit width
		RW	5'h8	dvp3_pixel_width	dvp3 pixel data bit width
		RW	5'h8	dvp2_pixel_width	dvp2 pixel data bit width
vi_dvp2_axi_ctrl_3	16'h000c	RW	16'h280	dvp0_vs_num	dvp0 pixel data line number per frame
		RW	16'h1e0	dvp0_hs_num	dvp0 pixel data cycle number per line
vi_dvp2_axi_ctrl_4	16'h0010	RW	16'h280	dvp1_vs_num	dvp1 pixel data line number per frame
		RW	16'h1e0	dvp1_hs_num	dvp1 pixel data cycle number per line
vi_dvp2_axi_ctrl_5	16'h0014	RW	16'h280	dvp2_vs_num	dvp2 pixel data line number per frame
		RW	16'h1e0	dvp2_hs_num	dvp2 pixel data cycle number per line
vi_dvp2_axi_ctrl_6	16'h0018	RW	16'h280	dvp3_vs_num	dvp3 pixel data line number per frame
		RW	16'h1e0	dvp3_hs_num	dvp3 pixel data cycle number per line
vi_dvp2_axi_ctrl_7	16'h001c	RW	16'h280	dvp4_vs_num	dvp4 pixel data line number per frame
		RW	16'h1e0	dvp4_hs_num	dvp4 pixel data cycle number per line
vi_dvp2_axi_ctrl_8	16'h0020	RW	16'h280	dvp5_vs_num	dvp5 pixel data line number per frame
		RW	16'h1e0	dvp5_hs_num	dvp5 pixel data cycle number per line
vi_dvp2_axi_ctrl_9	16'h0024	RW	32'h0	dvp0_chn0_baddr	dvp0 id0 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl_10	16'h0028	RW	32'h0	dvp0_chn1_baddr	dvp0 id1 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl_11	16'h002c	RW	32'h0	dvp0_chn2_baddr	dvp0 id2 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl_12	16'h0030	RW	32'h0	dvp1_chn0_baddr	dvp1 id0 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl_13	16'h0034	RW	32'h0	dvp1_chn1_baddr	dvp1 id1 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl_14	16'h0038	RW	32'h0	dvp1_chn2_baddr	dvp1 id2 channel one frame data start base address of DDR

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
14					
vi_dvp2_axi_ctrl 15	16'h00 3c	RW	32'h0	dvp2_chn0_baddr	dvp2 id0 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 16	16'h00 40	RW	32'h0	dvp2_chn1_baddr	dvp2 id1 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 17	16'h00 44	RW	32'h0	dvp2_chn2_baddr	dvp2 id2 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 18	16'h00 48	RW	32'h0	dvp3_chn0_baddr	dvp3 id0 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 19	16'h00 4c	RW	32'h0	dvp3_chn1_baddr	dvp3 id1 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 20	16'h00 50	RW	32'h0	dvp3_chn2_baddr	dvp3 id2 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 21	16'h00 54	RW	32'h0	dvp4_chn0_baddr	dvp4 id0 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 22	16'h00 58	RW	32'h0	dvp4_chn1_baddr	dvp4 id1 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 23	16'h00 5c	RW	32'h0	dvp4_chn2_baddr	dvp4 id2 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 24	16'h00 60	RW	32'h0	dvp5_chn0_baddr	dvp5 id0 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 25	16'h00 64	RW	32'h0	dvp5_chn1_baddr	dvp5 id1 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 26	16'h00 68	RW	32'h0	dvp5_chn2_baddr	dvp5 id2 channel one frame data start base address of DDR
vi_dvp2_axi_ctrl 27	16'h00 6c	RW	32'h0	dvp0_emd_baddr	dvp0 embeded channel data start base address of DDR
vi_dvp2_axi_ctrl 28	16'h00 70	RW	32'h0	dvp1_emd_baddr	dvp1 embeded channel data start base address of DDR
vi_dvp2_axi_ctrl 29	16'h00 74	RW	32'h0	dvp2_emd_baddr	dvp2 embeded channel data start base address of DDR
vi_dvp2_axi_ctrl 30	16'h00 78	RW	32'h0	dvp3_emd_baddr	dvp3 embeded channel data start base address of DDR

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
vi_dvp2_axi_ctrl_31	16'h00 7c	RW	32'h0	dvp4_emd_baddr	dvp4 embeded channel data start base address of DDR
vi_dvp2_axi_ctrl_32	16'h00 80	RW	32'h0	dvp5_emd_baddr	dvp5 embeded channel data start base address of DDR
vi_dvp2_axi_ctrl_33	16'h00 84	RW	16'h0	dvp1_hs_stride	dvp0 one line address stride, 16byte align
		RW	16'h0	dvp0_hs_stride	dvp1 one line address stride, 16byte align
vi_dvp2_axi_ctrl_34	16'h00 88	RW	16'h0	dvp3_hs_stride	dvp3 one line address stride, 16byte align
		RW	16'h0	dvp2_hs_stride	dvp2 one line address stride, 16byte align
vi_dvp2_axi_ctrl_35	16'h00 8c	RW	16'h0	dvp5_hs_stride	dvp5 one line address stride, 16byte align
		RW	16'h0	dvp4_hs_stride	dvp4 one line address stride, 16byte align
vi_dvp2_axi_ctrl_36	16'h00 90			Reserved	
				dvp5_last_id	
				dvp4_last_id	
				dvp3_last_id	
				dvp2_last_id	
				dvp1_last_id	dvp0 hdr mode last id number,or default id number
		RW	2'h0	dvp0_last_id	dvp0 hdr mode first id number,or default id number
		RW	6'h0	dvp_embed_con_en	6 dvp embeded data write to ddr continue enable
		RW	2'h0	dvp5_first_id	dvp5 hdr mode first id number,or default id number
		RW	2'h0	dvp4_first_id	dvp4 hdr mode first id number,or default id number
		RW	2'h0	dvp3_first_id	dvp3 hdr mode first id number,or default id number
		RW	2'h0	dvp2_first_id	dvp2 hdr mode first id number,or default id number
		RW	2'h0	dvp1_first_id	dvp1 hdr mode first id number,or default id number
		RW	2'h0	dvp0_first_id	dvp0 hdr mode first id number,or default id number
vi_dvp2_axi_int0	16'h00 a0			Reserved	
		RW1C	1'h0	dvp2_id2_frame_done	dvp2 id2 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp2_id1_frame_done	dvp2 id1 interrupt status for one frame write ddr done

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW1C	1'h0	dvp2_id0_frame_done	dvp2 id0 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp1_id2_frame_done	dvp1 id2 interrupt status for sone frame write ddr done
		RW1C	1'h0	dvp1_id1_frame_done	dvp1 id1 interrupt status for sone frame write ddr done
		RW1C	1'h0	dvp1_id0_frame_done	dvp1 id0 interrupt status for sone frame write ddr done
		RW1C	1'h0	dvp0_id2_frame_done	dvp0 id2 interrupt status for one frame write ddr done, bit[0]for id0 frame
		RW1C	1'h0	dvp0_id1_frame_done	dvp0 id1 interrupt status for one frame write ddr done, bit[0]for id0 frame
		RW1C	1'h0	dvp0_id0_frame_done	dvp0 id0 interrupt status for one frame write ddr done, bit[0]for id0 frame
		RW1C	1'h0	dvp2_id2_frame_flush	dvp2 id2 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp2_id1_frame_flush	dvp2 id1 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp2_id0_frame_flush	dvp2 id0 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp1_id2_frame_flush	dvp1 id2 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp1_id1_frame_flush	dvp1 id1 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp1_id0_frame_flush	dvp1 id0 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp0_id2_frame_flush	dvp0 id2 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp0_id1_frame_flush	dvp0 id1 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp0_id0_frame_flush	dvp0 id0 interrupt status for software flush next frame ddr base address
vi_dvp2	16'h00			Reserved	

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
axi_int1	a4	RW1C	1'h0	dvp5_id2_frame_done	dvp5 id2 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp5_id1_frame_done	dvp5 id1 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp5_id0_frame_done	dvp5 id0 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp4_id2_frame_done	dvp4 id2 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp4_id1_frame_done	dvp4 id1 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp4_id0_frame_done	dvp4 id0 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp3_id2_frame_done	dvp3 id2 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp3_id1_frame_done	dvp3 id1 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp3_id0_frame_done	dvp3 id0 interrupt status for one frame write ddr done
		RW1C	1'h0	dvp5_id2_frame_flush	dvp5 id2 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp5_id1_frame_flush	dvp5 id1 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp5_id0_frame_flush	dvp5 id0 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp4_id2_frame_flush	dvp4 id2 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp4_id1_frame_flush	dvp4 id1 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp4_id0_frame_flush	dvp4 id0 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp3_id2_frame_flush	dvp3 id2 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp3_id1_frame_flush	dvp3 id1 interrupt status for software flush next frame ddr base address
		RW1C	1'h0	dvp3_id0_frame_flush	dvp3 id0 interrupt status for software flush next frame ddr base address
vi_dvp2	16'h00			Reserved	

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
axi_int2	a8	RW1C	1'b0	axi_idbuffer_afull	
		RW1C	1'h0	dvp5_frame_error	dvp5 incomplete frame detect
		RW1C	1'h0	dvp4_frame_error	dvp4 incomplete frame detect
		RW1C	1'h0	dvp3_frame_error	dvp3 incomplete frame detect
		RW1C	1'h0	dvp2_frame_error	dvp2 incomplete frame detect
		RW1C	1'h0	dvp1_frame_error	dvp1 incomplete frame detect
		RW1C	1'h0	dvp0_frame_error	dvp0 incomplete frame detect
		RW1C	1'h0	axi_resp_error	axi bresp not 2'b00 flag
		RW1C	1'h0	axi_idbuffer_full	axi id buffer full flag
				Reserved	
vi_dvp2 axi_int_ mask0	16'h00 ac	RW	1'h0	dvp2_id2_frame_don e_mask	
		RW	1'h0	dvp2_id1_frame_don e_mask	
		RW	1'h0	dvp2_id0_frame_don e_mask	
		RW	1'h0	dvp1_id2_frame_don e_mask	
		RW	1'h0	dvp1_id1_frame_don e_mask	
		RW	1'h0	dvp1_id0_frame_don e_mask	
		RW	1'h0	dvp0_id2_frame_don e_mask	
		RW	1'h0	dvp0_id1_frame_don e_mask	
		RW	1'h0	dvp0_id0_frame_don e_mask	
		RW	1'h0	dvp2_id2_frame_flush_h_mask	
		RW	1'h0	dvp2_id1_frame_flush_h_mask	
		RW	1'h0	dvp2_id0_frame_flush_h_mask	
		RW	1'h0	dvp1_id2_frame_flush_h_mask	
		RW	1'h0	dvp1_id1_frame_flush_h_mask	
		RW	1'h0	dvp1_id0_frame_flush_h_mask	
vi_dvp2 axi_int_ mask1	16'h00 b0			Reserved	
		RW	1'h0	dvp5_id2_frame_don e_mask	

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW	1'h0	dvp5_id1_frame_don_e_mask	
		RW	1'h0	dvp5_id0_frame_don_e_mask	
		RW	1'h0	dvp4_id2_frame_don_e_mask	
		RW	1'h0	dvp4_id1_frame_don_e_mask	
		RW	1'h0	dvp4_id0_frame_don_e_mask	
		RW	1'h0	dvp3_id2_frame_don_e_mask	
		RW	1'h0	dvp3_id1_frame_don_e_mask	
		RW	1'h0	dvp3_id0_frame_don_e_mask	
		RW	1'h0	dvp5_id2_frame_flush_h_mask	
		RW	1'h0	dvp5_id1_frame_flush_h_mask	
		RW	1'h0	dvp5_id0_frame_flush_h_mask	
		RW	1'h0	dvp4_id2_frame_flush_h_mask	
		RW	1'h0	dvp4_id1_frame_flush_h_mask	
		RW	1'h0	dvp4_id0_frame_flush_h_mask	
		RW	1'h0	dvp3_id2_frame_flush_h_mask	
		RW	1'h0	dvp3_id1_frame_flush_h_mask	
		RW	1'h0	dvp3_id0_frame_flush_h_mask	
vi_dvp2_axi_int_mask2	16'h00 b4	RW		Reserved	
		RW	1'b0	axi_idbuffer_afull_mask	
		RW	1'h0	dvp5_frame_error_mask	
		RW	1'h0	dvp4_frame_error_mask	
		RW	1'h0	dvp3_frame_error_mask	
		RW	1'h0	dvp2_frame_error_mask	
		RW	1'h0	dvp1_frame_error_mask	
		RW	1'h0	dvp0_frame_error_mask	

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW	1'h0	axi_resp_error_mask	
		RW	1'h0	axi_idbuffer_full_ma sk	
vi_dvp2 axi_ctrl 37	16'h00 94	RW	16'h0	dvp1_emd_stride	
		RW	16'h0	dvp0_emd_stride	
vi_dvp2 axi_ctrl 38	16'h00 98	RW	16'h0	dvp3_emd_stride	
		RW	16'h0	dvp2_emd_stride	
vi_dvp2 axi_ctrl 39	16'h00 9c	RW	16'h0	dvp5_emd_stride	
		RW	16'h0	dvp4_emd_stride	
vi_dvp2 axi_ctrl 40	16'h00 e0	RW	16'h0	dvp1_emd_hsnsum	dvp0 embeded data cycle number per line
		RW	16'h0	dvp0_emd_hsnsum	
vi_dvp2 axi_ctrl 41	16'h00 e4	RW	16'h0	dvp3_emd_hsnsum	
		RW	16'h0	dvp2_emd_hsnsum	
vi_dvp2 axi_ctrl 42	16'h00 e8	RW	16'h0	dvp5_emd_hsnsum	
		RW	16'h0	dvp4_emd_hsnsum	
vi_dvp2 axi_ctrl 43	16'h00 ec	RW	23'h0	Reserved	
		RW	9'h100	axi_idbuffer_wrthsh	

#### 8.4.6 Shutter CSR

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
ENABLE	16'h000 0			Reserved	
		RW	6'b0	shutter_en	6 shutters' enable control signal.
STOP	16'h000 4			Reserved	
		W1P	6'b0	stop_pulse	6 shutters' stop control signal.
CFG_EN	16'h000 8			Reserved	
		RO	6'b1111 11	apb_cfg_en	6 shutters' configure enable flag.
				Reserved	
		W1P	6'b0	apb_cfg_vl id	6 shutters' configure info valid.
OUT_CFG	16'h000 c			Reserved	
		RW	6'b0	xtrig_xvs_c fg	6 shutters' XTRIG PAD reuse control signal. 0: output xtrig; 1: output xvs.
				Reserved	
		RW	6'b1111 11	polar	6 shutters' output PAD polar and level setting. 0: active-high; 1:

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW	6'b0	phase_shift	active-low.
					Reserved
					6 shutters' output signal phase shift setting. 0: posedge output; 1: negedge output.
INTR_NEG	16'h0010	RW	6'b0	Reserved	
				xtrig_intr_neg	6 shutters' xtrig interrupt pulse select. 0: posedge; 1: negedge.
		RW	6'b0	Reserved	
				xvs_intr_ne g	6 shutters' xvs interrupt pulse select. 0: posedge; 1: negedge.
TMAX0	16'h0014	RW	32'b0	tmax0	The tmax value set when xtrig output, indicates tmax+1 cycyels. When xvs output, bit 15 to 0 treat as xvs vmax period, indicates vmax+1 xhs lines.
TMAX1	16'h0018	RW	32'b0	tmax1	The tmax value set when xtrig output, indicates tmax+1 cycyels. When xvs output, bit 15 to 0 treat as xvs vmax period, indicates vmax+1 xhs lines.
TMAX2	16'h001c	RW	32'b0	tmax2	The tmax value set when xtrig output, indicates tmax+1 cycyels. When xvs output, bit 15 to 0 treat as xvs vmax period, indicates vmax+1 xhs lines.
TMAX3	16'h0020	RW	32'b0	tmax3	The tmax value set when xtrig output, indicates tmax+1 cycyels. When xvs output, bit 15 to 0 treat as xvs vmax period, indicates vmax+1 xhs lines.
TMAX4	16'h0024	RW	32'b0	tmax4	The tmax value set when xtrig output, indicates tmax+1 cycyels. When xvs output, bit 15 to 0 treat as xvs vmax period, indicates vmax+1 xhs lines.

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
TMAX5	16'h0028	RW	32'b0	tmax5	The tmax value set when xtrig output, indicates tmax+1 ccyels. When xvs output, bit 15 to 0 treat as xvs vmax period, indicates vmax+1 xhs lines.
TDUTY0	16'h002c	RW	32'b0	tduty0	The tduty value set when xtrig output, indicates tduty+1 ccyels. When xvs output, bit 15 to 0 treat as xvs duty, indicates vduty+1 xhs lines;
TDUTY1	16'h0030	RW	32'b0	tduty1	The tduty value set when xtrig output, indicates tduty+1 ccyels. When xvs output, bit 15 to 0 treat as xvs duty, indicates vduty+1 xhs lines;
TDUTY2	16'h0034	RW	32'b0	tduty2	The tduty value set when xtrig output, indicates tduty+1 ccyels. When xvs output, bit 15 to 0 treat as xvs duty, indicates vduty+1 xhs lines;
TDUTY3	16'h0038	RW	32'b0	tduty3	The tduty value set when xtrig output, indicates tduty+1 ccyels. When xvs output, bit 15 to 0 treat as xvs duty, indicates vduty+1 xhs lines;
TDUTY4	16'h003c	RW	32'b0	tduty4	The tduty value set when xtrig output, indicates tduty+1 ccyels. When xvs output, bit 15 to 0 treat as xvs duty, indicates vduty+1 xhs lines;
TDUTY5	16'h0040	RW	32'b0	tduty5	The tduty value set when xtrig output, indicates tduty+1 ccyels. When xvs output, bit 15 to 0 treat as xvs duty, indicates vduty+1 xhs lines;
HSET0	16'h0044	RW	16'b0	hmax0	The hmax value set when xhs output, indicates 1 line has hmax+1 ccyels.
		RW	16'b0	hduty0	The hduty value set when xhs output, indicates hduty+1 ccyels.
HSET1	16'h0048	RW	16'b0	hmax1	The hmax value set when xhs output, indicates 1 line has hmax+1 ccyels.
		RW	16'b0	hduty1	The hduty value set when xhs output, indicates hduty+1 ccyels.

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
HSET2	16'h004c	RW	16'b0	hmax2	The hmax value set when xhs output, indicates 1 line has hmax+1 ccyceles.
		RW	16'b0	hduty2	The hduty value set when xhs output, indicates hduty+1 ccyceles.
HSET3	16'h0050	RW	16'b0	hmax3	The hmax value set when xhs output, indicates 1 line has hmax+1 ccyceles.
		RW	16'b0	hduty3	The hduty value set when xhs output, indicates hduty+1 ccyceles.
HSET4	16'h0054	RW	16'b0	hmax4	The hmax value set when xhs output, indicates 1 line has hmax+1 ccyceles.
		RW	16'b0	hduty4	The hduty value set when xhs output, indicates hduty+1 ccyceles.
HSET5	16'h0058	RW	16'b0	hmax5	The hmax value set when xhs output, indicates 1 line has hmax+1 ccyceles.
		RW	16'b0	hduty5	The hduty value set when xhs output, indicates hduty+1 ccyceles.
TGHDLY0	16'h0060	RW	16'b0	tghdlyf0	XTRIG fall - XHS fall width(pixel cycle), value indicates the real cycles.
		RW	16'b0	tghdlyr0	XTRIG rise - XHS fall width(pixel cycle), value indicates the real cycles.
TGHDLY1	16'h0064	RW	16'b0	tghdlyf1	XTRIG fall - XHS fall width(pixel cycle), value indicates the real cycles.
		RW	16'b0	tghdlyr1	XTRIG rise - XHS fall width(pixel cycle), value indicates the real cycles.
TGHDLY2	16'h0068	RW	16'b0	tghdlyf2	XTRIG fall - XHS fall width(pixel cycle), value indicates the real cycles.
		RW	16'b0	tghdlyr2	XTRIG rise - XHS fall width(pixel cycle), value indicates the real cycles.
TGHDLY3	16'h006c	RW	16'b0	tghdlyf3	XTRIG fall - XHS fall width(pixel cycle), value indicates the real cycles.
		RW	16'b0	tghdlyr3	XTRIG rise - XHS fall width(pixel cycle), value indicates the real cycles.
TGHDLY4	16'h0070	RW	16'b0	tghdlyf4	XTRIG fall - XHS fall width(pixel cycle), value indicates the real cycles.
		RW	16'b0	tghdlyr4	XTRIG rise - XHS fall width(pixel cycle), value indicates the real cycles.
TGHDLY5	16'h0074	RW	16'b0	tghdlyf5	XTRIG fall - XHS fall width(pixel cycle), value indicates the real cycles.

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW	16'b0	tghdlyr5	XTRIG rise - XHS fall width(pixel cycle), value indicates the real cycles.
SHUTTER0_MODE	16'h0078			Reserved	
		RW	10'b0	tnum0	Shutter number set. The EXT Sync mode(shutter_mode[0] = 1) inactive.
				Reserved	
				shutter0_mode	Shutter mode select. [4]: XHS Trig mode, output XHS and XTRIG; [3]: XHS Normal mode, output XHS and XVS; [2]: REG Trig mode, output XTRIG based on register config and enable; [1]: EXT Trig mode, output XTRIG based on external input trig; [0]: EXT Sync mode, output XTRIG after sync the external input.
		RW	5'b0		
		RW	1'b0	io0_neg_trig	External trig pulse select. 0: posedge; 1: negedge.
		RW	1'b0	tfree0	Shutter time free running, unlimited.
SHUTTER1_MODE	16'h007c			Reserved	
		RW	10'b0	tnum1	Shutter number set. The EXT Sync mode(shutter_mode[0] = 1) inactive.
				Reserved	
				shutter1_mode	Shutter mode select. [4]: XHS Trig mode, output XHS and XTRIG; [3]: XHS Normal mode, output XHS and XVS; [2]: REG Trig mode, output XTRIG based on register config and enable; [1]: EXT Trig mode, output XTRIG based on external input trig; [0]: EXT Sync mode, output XTRIG after sync the external input.
		RW	5'b0		
		RW	1'b0	io1_neg_trig	External trig pulse select. 0: posedge; 1: negedge.
		RW	1'b0	tfree1	Shutter time free running, unlimited.
SHUTTER2_MODE	16'h0080			Reserved	
		RW	10'b0	tnum2	Shutter number set. The EXT Sync mode(shutter_mode[0] = 1) inactive.
				Reserved	

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW	5'b0	shutter2_mode	Shutter mode select. [4]: XHS Trig mode, output XHS and XTRIG; [3]: XHS Normal mode, output XHS and XVS; [2]: REG Trig mode, output XTRIG based on register config and enable; [1]: EXT Trig mode, output XTRIG based on external input trig; [0]: EXT Sync mode, output XTRIG after sync the external input.
					External trig pulse select. 0: posedge; 1: negedge.
					Shutter time free running, unlimited.
SHUTTER3_MODE	16'h0084			Reserved	
		RW	10'b0	tnum3	Shutter number set. The EXT Sync mode(shutter_mode[0] = 1) inactive.
				Reserved	
		RW	5'b0	shutter3_mode	Shutter mode select. [4]: XHS Trig mode, output XHS and XTRIG; [3]: XHS Normal mode, output XHS and XVS; [2]: REG Trig mode, output XTRIG based on register config and enable; [1]: EXT Trig mode, output XTRIG based on external input trig; [0]: EXT Sync mode, output XTRIG after sync the external input.
					External trig pulse select. 0: posedge; 1: negedge.
					Shutter time free running, unlimited.
SHUTTER4_MODE	16'h0088			Reserved	
		RW	10'b0	tnum4	Shutter number set. The EXT Sync mode(shutter_mode[0] = 1) inactive.
				Reserved	

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW	5'b0	shutter4_m ode	Shutter mode select. [4]: XHS Trig mode, output XHS and XTRIG; [3]: XHS Normal mode, output XHS and XVS; [2]: REG Trig mode, output XTRIG based on register config and enable; [1]: EXT Trig mode, output XTRIG based on external input trig; [0]: EXT Sync mode, output XTRIG after sync the external input.
					External trig pulse select. 0: posedge; 1: negedge.
					Shutter time free running, unlimited.
SHUTTER5_MODE	16'h008c			Reserved	
		RW	10'b0	tnum5	Shutter number set. The EXT Sync mode(shutter_mode[0] = 1) inactive.
				Reserved	
		RW	5'b0	shutter5_m ode	Shutter mode select. [4]: XHS Trig mode, output XHS and XTRIG; [3]: XHS Normal mode, output XHS and XVS; [2]: REG Trig mode, output XTRIG based on register config and enable; [1]: EXT Trig mode, output XTRIG based on external input trig; [0]: EXT Sync mode, output XTRIG after sync the external input.
					External trig pulse select. 0: posedge; 1: negedge.
					Shutter time free running, unlimited.
IRQ_EN	16'h0090			Reserved	
		RW	3'b0	irq_en5	Interrupt enable [2]: The xvs posedge or negedge interrupt enable signal, [1]: The xtrig posedge or negedge interrupt enable signal, [0]: The task complete interrupt enable signal.
					Reserved

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RW	3'b0	irq_en4	Interrupt enable [2]: The xvs posedge or negedge interrupt enable signal, [1]: The xtrig posedge or negedge interrupt enable signal, [0]: The task complete interrupt enable signal.
					Reserved
		RW	3'b0	irq_en3	Interrupt enable [2]: The xvs posedge or negedge interrupt enable signal, [1]: The xtrig posedge or negedge interrupt enable signal, [0]: The task complete interrupt enable signal.
					Reserved
		RW	3'b0	irq_en2	Interrupt enable [2]: The xvs posedge or negedge interrupt enable signal, [1]: The xtrig posedge or negedge interrupt enable signal, [0]: The task complete interrupt enable signal.
					Reserved
		RW	3'b0	irq_en1	Interrupt enable [2]: The xvs posedge or negedge interrupt enable signal, [1]: The xtrig posedge or negedge interrupt enable signal, [0]: The task complete interrupt enable signal.
					Reserved
		RW	3'b0	irq_en0	Interrupt enable [2]: The xvs posedge or negedge interrupt enable signal, [1]: The xtrig posedge or negedge interrupt enable signal, [0]: The task complete interrupt enable signal.
					Reserved
IRQ_STATE	16'h0094			Reserved	
		RW1C	1'b0	xvs_intr5	The xvs posedge or negedge interrupt.
		RW1C	1'b0	xtrig_intr5	The xtrig posedge or negedge interrupt.
		RW1C	1'b0	task_intr5	The task complete interrupt enable signal.

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
				Reserved	
		RW1C	1'b0	xvs_intr4	The xvs posedge or negedge interrupt.
		RW1C	1'b0	xtrig_intr4	The xtrig posedge or negedge interrupt.
		RW1C	1'b0	task_intr4	The task complete interrupt enable signal.
				Reserved	
		RW1C	1'b0	xvs_intr3	The xvs posedge or negedge interrupt.
		RW1C	1'b0	xtrig_intr3	The xtrig posedge or negedge interrupt.
		RW1C	1'b0	task_intr3	The task complete interrupt enable signal.
				Reserved	
		RW1C	1'b0	xvs_intr2	The xvs posedge or negedge interrupt.
		RW1C	1'b0	xtrig_intr2	The xtrig posedge or negedge interrupt.
		RW1C	1'b0	task_intr2	The task complete interrupt enable signal.
				Reserved	
		RW1C	1'b0	xvs_intr1	The xvs posedge or negedge interrupt.
		RW1C	1'b0	xtrig_intr1	The xtrig posedge or negedge interrupt.
		RW1C	1'b0	task_intr1	The task complete interrupt enable signal.
				Reserved	
DBG_STAT_E	16'h0098			xvs_intr0	The xvs posedge or negedge interrupt.
		RO	3'b0	xtrig_intr0	The xtrig posedge or negedge interrupt.
		RO	3'b0	task_intr0	The task complete interrupt enable signal.
				Reserved	
		RO	3'b0	debug_stat_e5	The debug state
				Reserved	
		RO	3'b0	debug_stat_e4	The debug state
				Reserved	
		RO	3'b0	debug_stat_e3	The debug state
				Reserved	
		RO	3'b0	debug_stat_e2	The debug state

CSR NAME	OFFSET	ACCESS	RESET VALUE	FIELD NAME	SIGNALS
		RO	3'b0	Reserved	
				debug_stat_e1	The debug state
		RO	3'b0	Reserved	
				debug_stat_e0	The debug state

## 8.5 Configure Sequence

### 8.5.1 Combo-PHY MIPI StartUp

Combo-PHY configuration sequence (the difference between CPHY and DPHY is mainly the phy\_mode register):

1. Reset the entire subsystem.
2. Power up the required PHY.
3. Configure the phy interface control signals as shown in the figure below.

Register Name	Value	Bit	Address	
enable_dck	1	[4]	0x510c_c000	combo-phy0
enable_0	1	[5]	0x510c_c000	combo-phy0
enable_1	1	[6]	0x510c_c000	combo-phy0
phy_mode	0	[0]	0x5105_001c	csi2_host0
forcexnmode_0	1	[7]	0x510c_c000	combo-phy0
forcexnmode_1	1	[8]	0x510c_c000	combo-phy0
forcexnmode_dck	1	[9]	0x510c_c000	combo-phy0

4. Configure the relevant internal registers of the phy, see the phy datasheet for details.
5. Configure phy's shutdown\_n = 1

Register Name	Value	Bit	Address	
shutdown_n	1	[0]	0x5105_0040	csi2_host0

6. Polling the phy\_ready register until the signal goes high, indicating that the phy configuration is complete

Register Name	Value	Bit	Address	
phy_ready	/	[0]	0x510c_c004	combo-phy0

### 8.5.2 Combo-PHY LVDS StartUp

1. Configure the phy interface control signals as shown in the figure below

Register Name	Value	Bit	Address	
enable_dck	1	[4]	0x510c_c000	combo-phy0
enable_0	1	[5]	0x510c_c000	combo-phy0
enable_1	1	[6]	0x510c_c000	combo-phy0
phy_mode	0	[0]	0x5105_001c	csi2_host0
forcexnmode_0	1	[7]	0x510c_c000	combo-phy0
forcexnmode_1	1	[8]	0x510c_c000	combo-phy0

forcexnmode_dck	1	[9]	0x510c_c000	combo-phy0
shutdown_n	0	[0]	0x5105_0040	csi2_host0
rst	0	[0]	0x5105_0044	csi2_host0

2. Configure the relevant internal registers of the phy, see the phy datasheet for details.

3. Configure phy's shutdown\_n = 1, configure phy's rst = 1

Register Name	Value	Bit	Address	
shutdown_n	1	[0]	0x5105_0040	csi2_host0
rst	1	[0]	0x5105_0044	csi2_host0

4. Poll the phy\_ready register until the signal goes high, indicating the completion of phy configuration

Register Name	Value	Bit	Address	
phy_ready	/	[0]	0x510c_c004	combo-phy0

5. Configure the phy interface control signals as shown in the figure below

Register Name	Value	Bit	Address	
forcexnmode_0	1	[7]	0x510c_c000	combo-phy0
forcexnmode_1	1	[8]	0x510c_c000	combo-phy0
forcexnmode_dck	1	[9]	0x510c_c000	combo-phy0

6. Configure the relevant internal registers of the phy, please refer to the phy datasheet for details

### 8.5.3 Combo-PHY GPIO StartUp

1. Configure the phy interface control signals as shown in the figure below

Register Name	Value	Bit	Address	
phy_mode	0	[0]	0x5105_001c	csi2_host0

2. Configure the relevant internal registers of the phy, please refer to the phy datasheet for details

### 8.5.4 Combo-PHY Configuration Clock

The register configuration clock of CDPHY is pclk, sourced from the clock divider win2030\_ck\_div\_dynm in the vi\_crg module. The configuration operation of this standard cell needs to occur when the corresponding clock is in the off state. The configuration process is as follows:

1. Turn off the vi\_ahb\_clk clock by setting bit[30] of the register at offset address 0x188 in sys\_crg\_csr to 0.
2. Modify the clock division parameter of win2030\_ck\_div\_dynm by configuring bits[3:0] of the register at offset address 0x68 in vi\_common\_top\_reg.
3. Turn on the vi\_ahb\_clk clock by setting bit[30] of the register at offset address 0x188 in sys\_crg\_csr to 1.

## 9 Video Output

The video output is responsible for the display function, the OSD is responsible for the storage, processing, and output of the display data to the HDMI or MIPI interface, the follow is the function diagram:

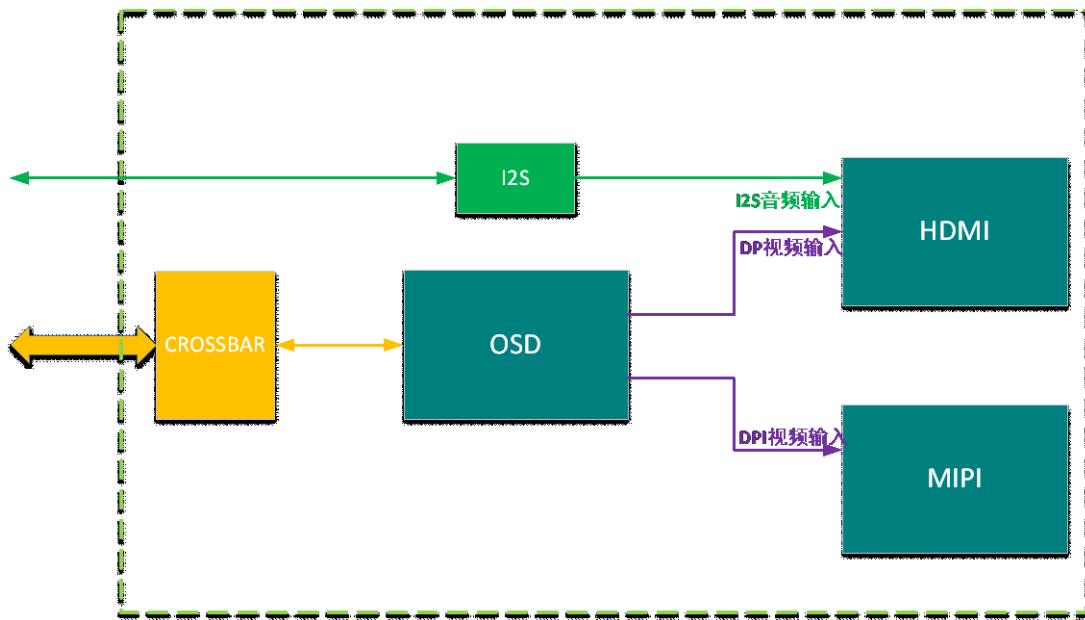


Figure 9-1 Video output

The following table describes the address mappings of each module in the video output system:

Table 9-1 Address mapping of video output

Name	Address range	Memory range size
Mipi_dsi	0x50270000~0x5027ffff	64K
Hdmi_hdcp	0x50290000~0x5029ffff	64K
Hdmi	0x502a0000~0x502bffff	128K
OSD	0x502c0000~0x502fffff	256K

### 9.1 OSD

#### 9.1.1 Function description

OSD is a high-performance area-optimized display processor unit (DPU), that can be used for reading rendered images from the frame buffer to the display. In addition to providing hardware cursor patterns, the Display Controller performs format conversions, dithering, and gamma corrections. This controller supports parallel pixel output and is easily adapted to external serialization logic. The max definition is 4K, the max color depth is 10bit.

#### 9.1.2 Feature

- Video Timing Generation.
  - HSYNC, VSYNC, and Data Enable (DE) signals
  - Programmable timers

- Display Capability.
  - Default display resolution: 1080
  - Maximum display resolution: 4K2K
  - Independent synchronization and blank signals for the display output panel
  - Independent gamma and dither tables for the display output panel
- Output Interface.
  - Parallel pixel output with 30-bit Data, HSync, VSync, and DE
  - Display pixel interface (DPI) with RGB output
  - DisplayPort (DP) with RGB output
  - Various DP and DPI output formats
  - Easy adaptation to external serialization logic
- Input Formats.
  - Various A/XRGB, YUV422, and YUV420 formats
  - Programmable color space conversions of YUV2RGB and RGB2RGB
  - Conversion between BT709 and BT2020
- Hardware Cursor.
- Decompression.
  - Supports lossless decompression
- Color.
  - A separate lookup table for dither
  - A separate lookup table for gamma
  - A separate lookup table for de-gamma
  - Alpha Blending: 8 Porter Duff Blending modes
- Filter and Scaling.
  - Supported on both the video/graphic and overlay layers
  - Vertical and horizontal scaling
  - Horizontal 3-tap or 5-tap and vertical 3-tap filters
  - Programmable filter order
  - 15.16 fixed point scaling factor

### 9.1.3 Function Diagram

#### 9.1.3.1 The main modules of the OSD

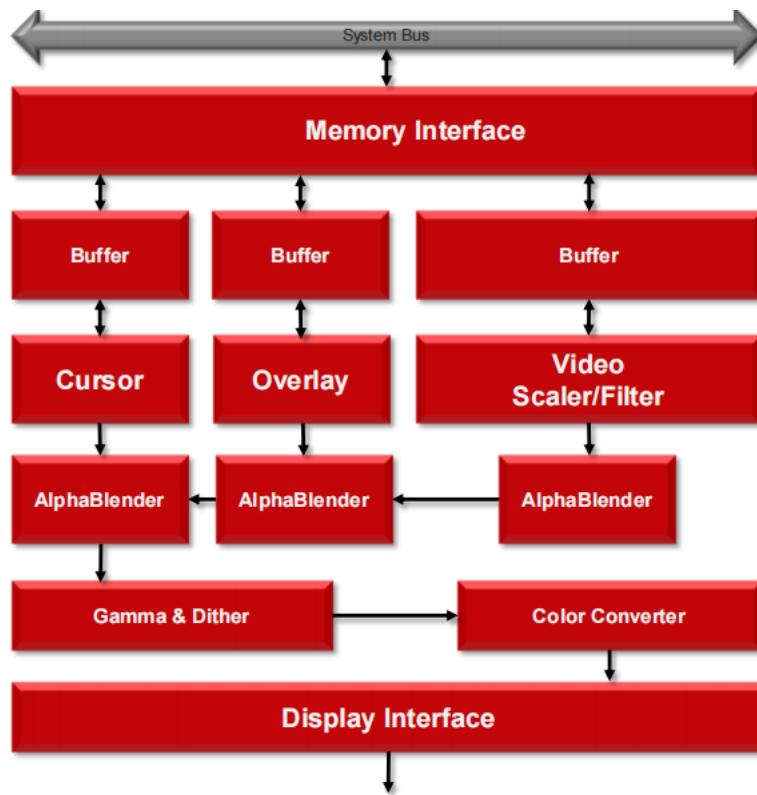


Figure 9-2 OSD function diagram

#### 9.1.3.2 Data input

Swizzle is used to switch the position of components in pixel data. The same color format may be stored in different order in memory. To accommodate this possibility, the Vivante Display Controller will first swizzle an input pixel. Since the input pixel may have been input with four different format orders: ARGB, RGBA, ABGR or BGRA, this initial swizzle is just to convert the format into ARGB. For YUV formats, the U and V pixels may be placed in different positions, so UV-swizzle is used to convert them to a common format.

Note that the Vivante Display Controller assumes the initial input of ARGB data is in ARGB order, which means A is in the upper bits while B is in the lowest bits. If the user input is not in ARGB order, swizzle is needed to reshape the data. For example, if the input format is in BGRA order, the swizzle must be configured to handle the BGRA format.

For YUV formats, especially for UV mixed formats, the Display Controller assumes that for each UV pair, U is in the lower bits while V is in the upper bits. If the user input is not in this order, UV-swizzle reorders the input data.

32bit format	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A8R8G8B8	A	A	A	A	A	A	A	R	R	R	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B	B	B	B	B	B		
X8R8G8B8	X	X	X	X	X	X	X	R	R	R	R	R	R	R	R	G	G	G	G	G	B	B	B	B	B	B	B	B	B	B		
A2B10G10R10	A	A	B	B	B	B	B	B	B	B	B	B	G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R	R	R		
16 bit format	secend pixel												first pixel																			
A1R5G5B5	A	R	R	R	R	R	R	G	G	G	G	G	B	B	B	B	A	R	R	R	R	R	G	G	G	G	B	B	B	B	B	
X1R5G5B5	X	R	R	R	R	R	R	G	G	G	G	G	B	B	B	B	X	R	R	R	R	R	G	G	G	G	B	B	B	B	B	
A4R4G4B4	A	A	A	A	R	R	R	R	G	G	G	G	B	B	B	B	A	A	A	A	R	R	R	R	G	G	G	G	B	B	B	
X4R4G4B4	X	X	X	X	R	R	R	R	G	G	G	G	B	B	B	B	X	X	X	X	R	R	R	R	G	G	G	G	B	B	B	
R5G6B6	R	R	R	R	R	R	R	G	G	G	G	G	B	B	B	B	R	R	R	R	R	R	G	G	G	G	B	B	B	B	B	

Figure 9-3 Expected input organization for RGB data

The following table lists the input formats that the Display Controller supports for the video/graphic and overlay layers. The cursor uses the format of ARGB8888.OSD Video/graphic:

Table 9-2 OSD input data format

Format	Linear Input	Tile Input
ARGB2101010	Yes	Yes
ARBG8888/XRGB8888	Yes	Yes
ARBG1555/XRGB1555	Yes	Yes
RGB565	Yes	Yes
ARGB4444/XRGB4444	Yes	Yes
YUV422-YUY2	Yes	Yes
YUV422-UYVY	Yes	Yes
YUV420-YV12	Yes	No
YUV420-NV12	Yes	Yes
YUV420-P010_10bit	Yes	Yes
YUV422-NV16	Yes	No

### 9.1.3.3 Data output

The display pixel interface (DPI) supports the RGB output formats: DPI\_D16CFG1, DPI\_D16CFG2, DPI\_D16CFG3, DPI\_D18CFG1, DPI\_D18CFG2, DPI\_D24, and DPI\_D30 (R10G10B10). The DisplayPort (DP) interface supports the RGB output formats: RGB101010, RGB888, RGB666, and RGB565. The output format is shown in the follow figure:

Configuration	Bits[2:0]	47	.....	43	42	41	40	39	38	37	.....	31	.....	27	26	25	24	23	22	.....	15	.....	11	10	9	8	7	6	.....	0
RGB101010	3	R	R	R	R	R	R	R	R	R		G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B			
RGB888	2	R	R	R	R	R	R					G	G	G	G	G	G	G	G		B	B	B	B	B	B	B			
RGB666	1	R	R	R	R							G	G	G	G						B	B	B	B	B					
RGB565	0	R	R	R								G	G	G							B	B	B	B						

Figure 9-4 DP port data format

The display pixel interface (DPI) supports the RGB output formats: DPI\_D16CFG1, DPI\_D16CFG2, DPI\_D16CFG3, DPI\_D18CFG1, DPI\_D18CFG2, DPI\_D24, and DPI\_D30 (R10G10B10). The output format is shown in the follow figure:

config	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
30bitRGB	R	R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B	B		
DPI 24bit						R	R	R	R	R	R	R	R	G	G	G	G	G	G	G	B	B	B	B	B	B	B	B	B	
DPI 18bit 1									R	R	R	R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B	B	B	
DPI 18bit 2						R	R	R	R	R	R	R	R		G	G	G	G	G	G		B	B	B	B	B	B	B	B	
DPI 16bit 1										R	R	R	R	R	R	R	G	G	G	G	G	G	B	B	B	B	B	B	B	B
DPI 16bit 2						R	R	R	R	R	R	R	R		G	G	G	G	G	G		B	B	B	B	B	B	B	B	
DPI 16bit 3						R	R	R	R	R	R	R	R		G	G	G	G	G	G		B	B	B	B	B	B	B		

Figure 9-5 DPiport data format

The DPI port is mihi dsi's upstream data port, The DP port is HDMI's upstream data port.

#### 9.1.3.4 Color Keying for Video/Graphic and Overlay

OSD provide for overlay and transparency effects using color keys to blend pixels in images. A chosen color in a source image can be selected and filtered out so that it can be replaced with a different designated color in the destination target image.

The filter mechanism is controlled using the dcregOverlayColorKey0~15 and dcregOverlayKeyHigh0~15 registers. Each pixel color in the overlay or video/graphic layer is compared against the range specified in these registers. If the pixel color is in the range of [ColorKey, ColorKeyHigh], the Display Controller will regard it as a special color and replace it with another color as follows:

- If the source color is on the overlay layer, it is replaced with the corresponding pixel on the video/graphic layer.
- If the source color is on the video/graphic layer, it will be replaced with the configured background color.

#### 9.1.3.5 Dither

In an image where color intensities change slowly, there may be noticeable jumps in intensity levels between pixels. Dithering can be used to diffuse the intensity across neighboring pixels. In dithering mode pixels are scanned in order, and errors in calculating a pixel's intensity are distributed (that is, diffused) to neighboring pixels to keep the overall intensity of the image closer to the input intensity.

Vivante's Display Controller dither implementation requires a lookup table of 4x4 entries of 4 bits. These 64-bit tables are located in the 32-bit registers gcregDisplayDitherTableLow0 and gcregDisplayDitherTableHigh0. The dither lookup table needs to be indexed by the two least significant bits x[1:0] and the two least significant bits y[1:0] of the displays.

Create a lookup table by setting registers dcregDisplayDitherTableLow0 and dcregDisplayDitherTableHigh0.

- The lookup table includes 16 entries, 4 bits for each.
- The lookup table provides a value U[3:0] through the indexes X[1:0] and Y[1:0].

Example: Compare the color value RedColor[3:0] with this U[3:0].

- If RedColor[3:0] > U[3:0] and RedColor[7:4] is not 4'b1111, then the final color value is NewRedColor = RedColor[7:4] + 1'b1.
- If RedColor[3:0] <= U[3:0], then NewRedColor = RedColor[7:4].

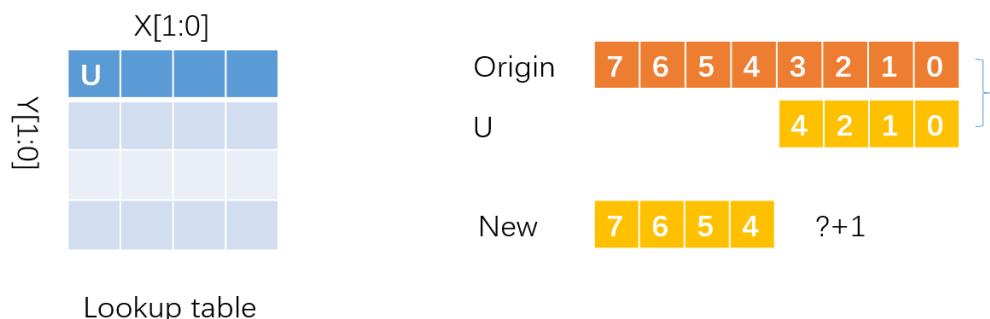


Figure 9-6 Dither algorithm

### 9.1.3.6 Alignment of Stride and Base Address

The following table provides the alignment of stride and base address.

Table 9-3 Alignment of Stride and Base Address

Linear/Tile	Format	Width x Height Alignment (Pixels)	Stride Alignment (Bytes)	Base Address Alignment (Bytes)
Linear	Planar YUV Semi-planar YUV	128x2	128	128
	RGB/Index1/2/4/8 Packed YUV	\	128	128
SuperTileX8x8	16bpp RGB/ YUY2/UYVY	64x64	128	128
SuperTileX8x4/ SuperTileY4x8	32bpp RGB	64x64	256	128
8x8Tile	16bpp RGB/ YUY2/UYVY	8x8	16	128
	NV12-Y planar	16x8	16	64
	P010-Y planar	16x8	32	128
8x4Tile	32bpp RGB	8x8	32	128
	NV12-UV planar	16x8	16	64
	P010-UV planar	16x8	32	128
<b>Decompression</b>				
Linear	NV12-Y planar NV12-UV planar	256x2	256	256
	P010-Y planar P010-UV planar	128x2	256	256
SuperTileX8x4/ SuperTileY4x8	32bpp RGB	64x64	256	128
8x8Tile	YUY2	8x8	16	128
	NV12-Y planar	32x8	32	256
	P010-Y planar	16x8	32	256

Linear/Tile	Format	Width x Height Alignment (Pixels)	Stride Alignment (Bytes)	Base Address Alignment (Bytes)
8x4Tile	NV12-UV planar	32x8	32	256
	P010-UV planar	16x8	32	256

#### 9.1.4 Initialization

The following flow describes the basic steps of setting the display output panel and frame data. Set the timing parameters according to the specifications for the target panel specifications. Refer to the timing diagram for the key registers and register bits. The list below is not comprehensive.

- dcregHDisplay
- dcregHSync
- dcregVDisplay
- dcregVSync

Step 1. Set registers for the cursor, gamma, and dither functions (if needed).

- dcregCursor\*
- dcregGamma\*
- dcregDisplayDither\*

Step 2. Set the frame buffer address and stride registers.

- dcregFrameBufferAddress
- dcregFrameBufferStride

Step 3. Configure panel requirements.

- dcregPanelConfig

Step 4. Configure the data format of the frame buffer.

- dcregFrameBufferConfig

Step 5. Start the signal transfer.

- dcregFrameBufferConfig.RESET=1

Step 6. Update parameters for the next frame.

Step 7. Use the interrupt registers to wait for the signal of which the transfer is complete, or check the interrupt status.

- dcregDisplayIntr
- dcregDisplayIntrEnable

Step 8. Update parameters for each succeeding frame as needed.

#### 9.1.5 Timing

The synchronization pulse of the video signal output by the OSD can be configured with registers as either positive synchronization pulse or negative synchronization pulse. The negative pulse synchronization signal is active at a low level, and the timing diagram is shown below:

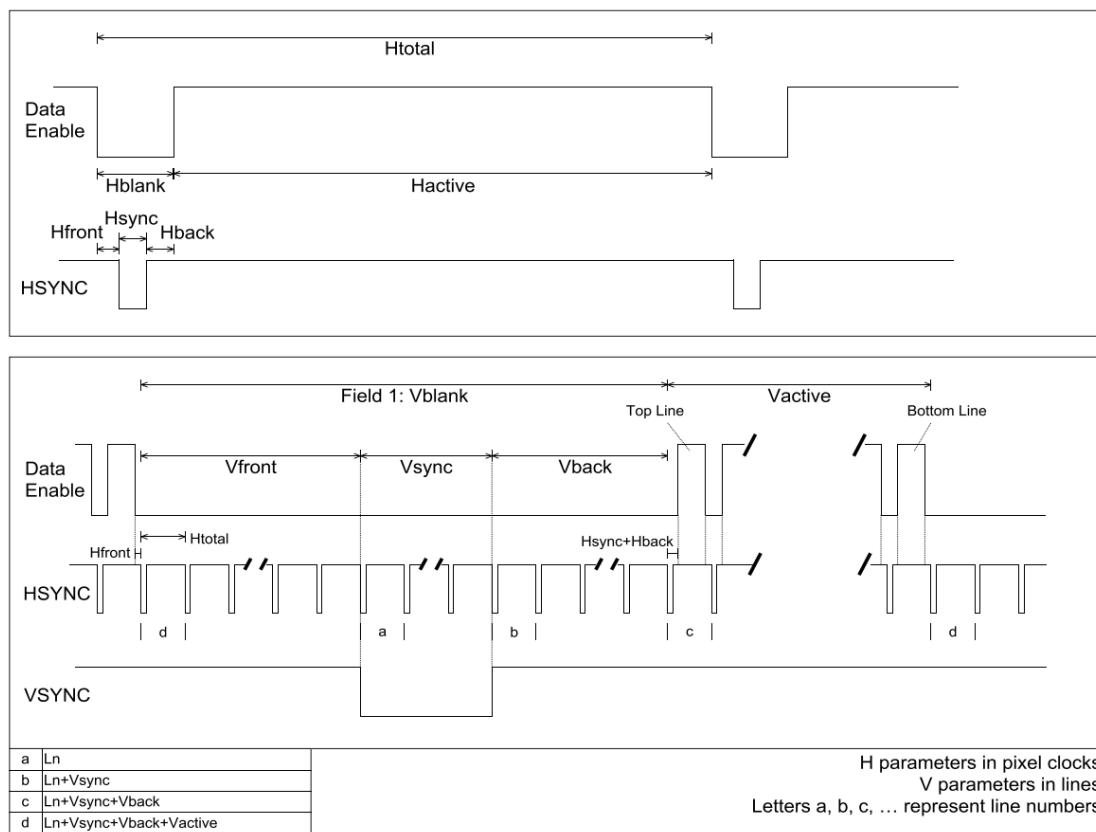


Figure 9-7 Negative pulse timing

The positive pulse synchronizer timing diagram as follow:

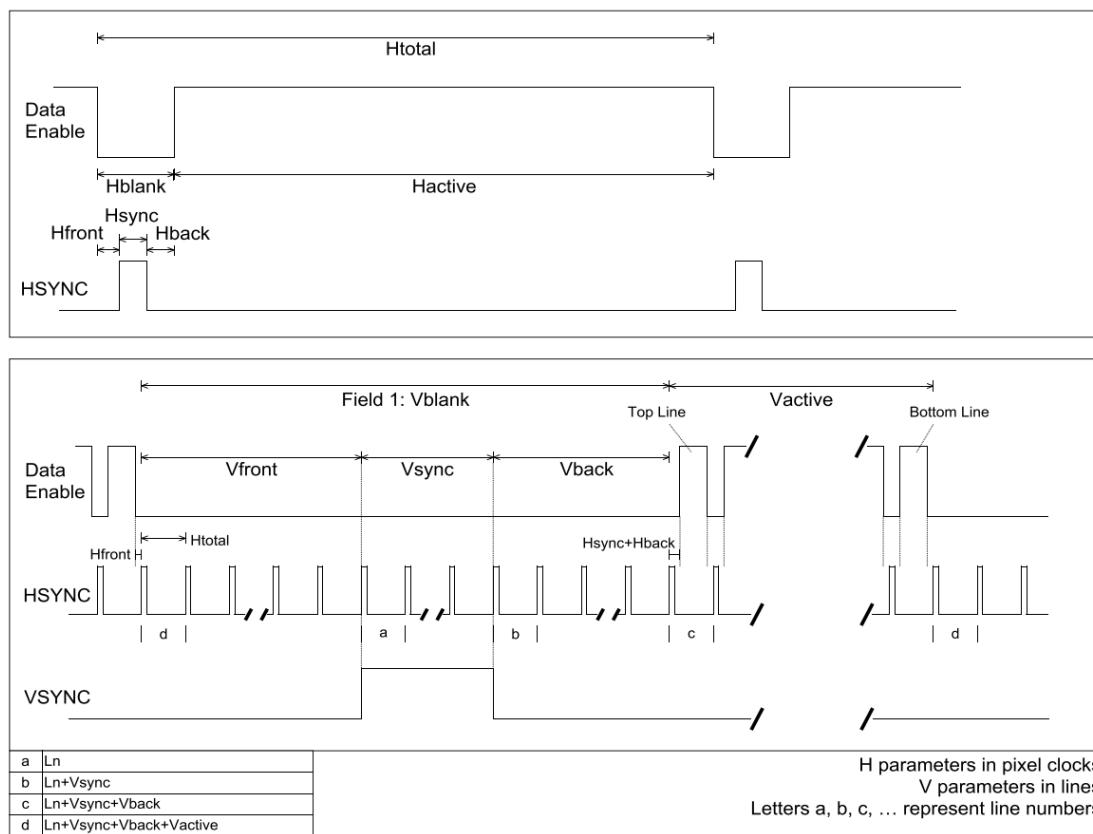


Figure 9-8 Positive pulse synchronizer timing diagram

The width of the pulse, the length of the blank, and the length of the effective area of image is in the follow daigram, the relationship between each area and the register is shown in the figure below:

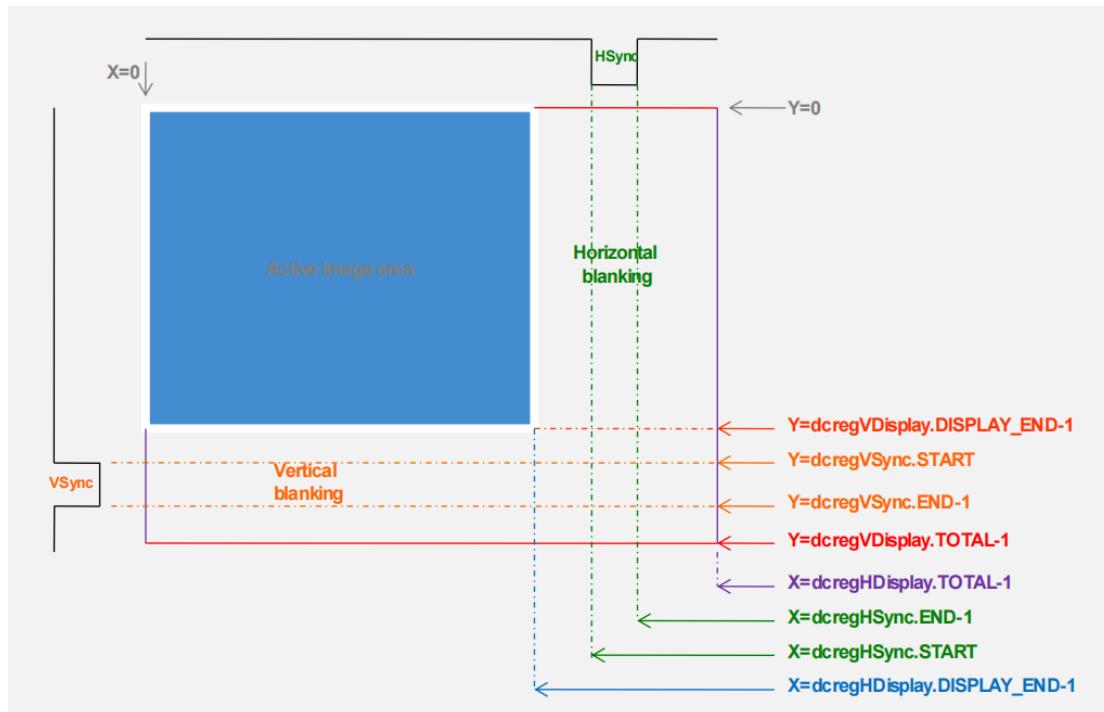


Figure 9-9 Register and frame parameter

## 9.2 MIPI TX

### 9.2.1 Function description

MIPI DSI is used to drive panel with MIPI interface, MIPI has four lanes, Lane operation ranging from 80 Mbps to 2.5 Gbps in forward in high speed mode, Maximum low power data rate supported of 10Mbps, the display data from OSD. The data is packaged into packets specified in the DSI protocol and then output to the DPHY, which serializes the parallel data and outputs it to an external display device. The main functional modules are shown in the figure below:

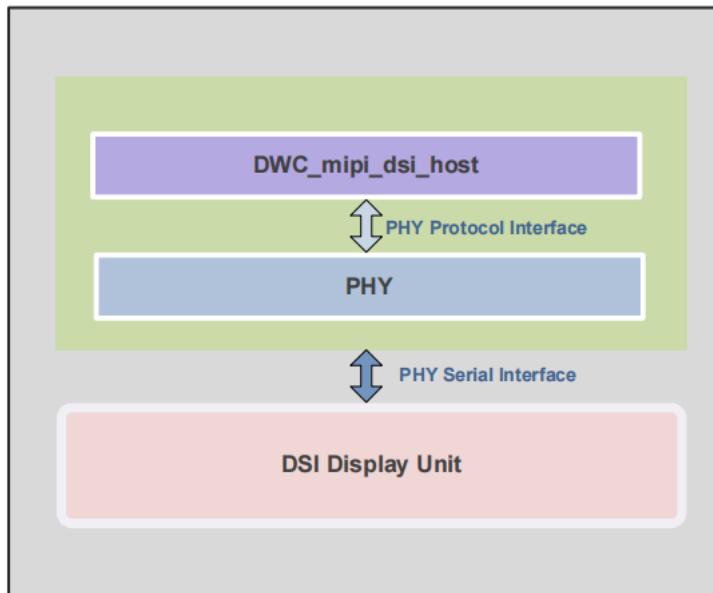


Figure 9-10 MIPI function diagram

### 9.2.2 Feature

Compliant with MIPI Alliance standards.

- Supports up to four lanes for data transfer.
- Supports up to 2.5 Gsps per lane in D-PHY.
- Low power data transfer rate up to 10Mbps.
- Bidirectional communication and escape mode support through data lane 0.
- DPI interface color coding mappings into 30-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
  - 30-bit RGB
  - 36-bit RGB (double clock rate required)
  - 24-bit YCbCr 4:2:2
  - 20-bit YCbCr 4:2:2 loosely packed
  - 16-bit YCbCr 4:2:2
  - 12-bit YCbCr 4:2:0
- Programmable polarity of all DPI interface signals.
- Supports Ultra Low-Power mode with PLL disabled.
- Support for End of Transmission Packet (EoTp).
- Video pattern generator:
  - Vertical and horizontal color bar generation without DPI stimuli

- BER pattern without DPI stimuli
- Auto ULPS control scheme.

### 9.2.3 Function Diagram

The MIPI function diagram is as follow:

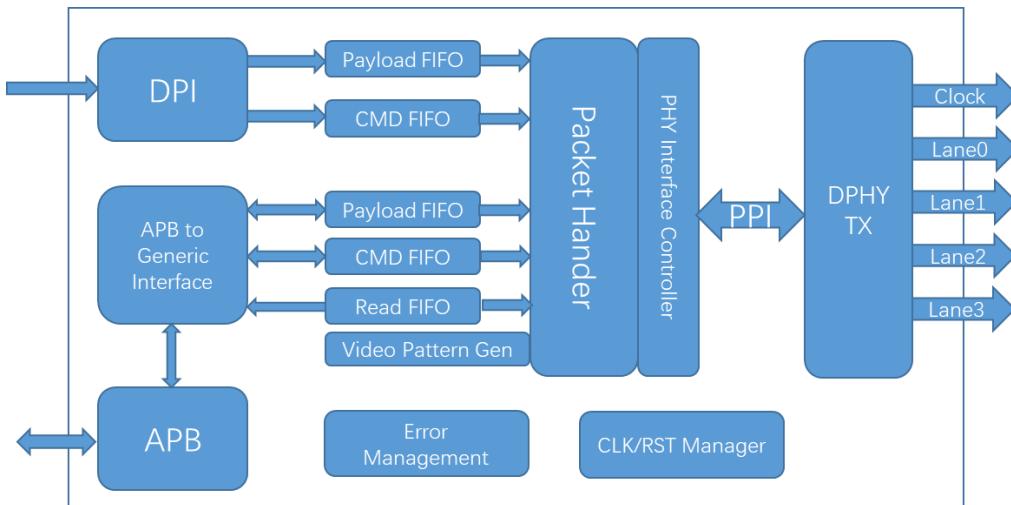


Figure 9-11 MIPI data stream

#### 9.2.3.1 DPI

The DPI interface follows the MIPI DPI-2 specification with pixel data bus width up to 30 bits. It is used to transmit the information in Video mode in which the transfers from the OSD to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by video out register. To transfer additional commands (for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.

It is possible to update the DPI configuration on the fly without impacting the current frame. It is done with the help of shadow registers. This feature is controlled by the VID\_SHADOW\_CTRL register.

The new configuration is only used when the system requests for it. To update the DPI configuration during the transmission of a video frame, the configuration of that frame needs to be stored in the auxiliary registers. This way, the new frame configurations can be set through the APB interface without corrupting the current frame.

By default, this feature is disabled. To enable this feature, set the vid\_shadow\_en bit of the

VID\_SHADOW\_CTRL to 1. When this feature is enabled, the system supplies the configuration stored in the auxiliary registers. The follow diagram shows the necessary steps to update the DPI config:

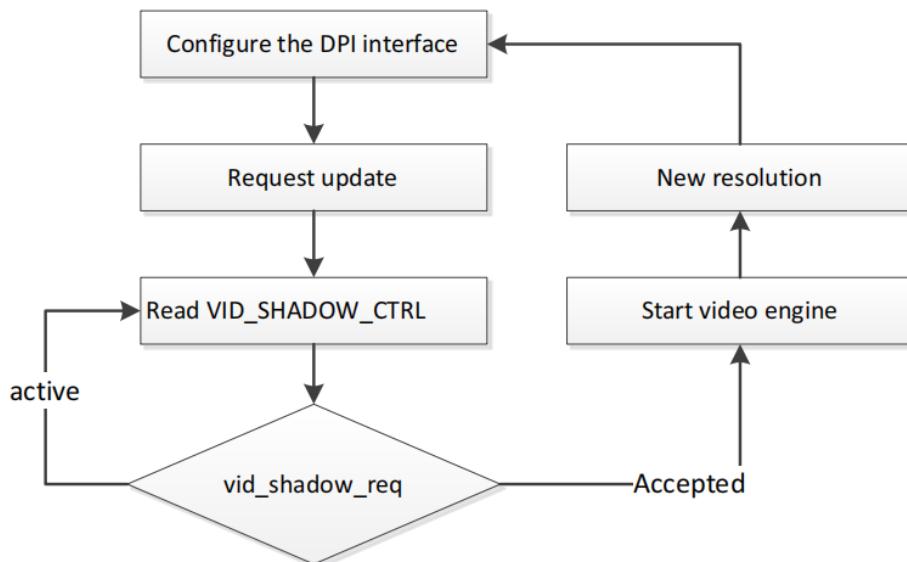


Figure 9-12 Shadow registers configuration

The different video transmission modes are as follows:

- Burst mode
- Non-Burst mode
  - Non-Burst mode with sync pulse
  - Non-Burst mode with sync event DSI

In Burst mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packet with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between the pixel required bandwidth and DSI link bandwidth is very different. This enables the MIPI TX to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.

In NON-Burst mode, the MIPI DSI uses the partitioning properties of the MIPI TX to divide the video line transmission into several DSI packets. This is done to match the pixel required bandwidth with the DSI link bandwidth. With this mode, the MIPI TX does not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.

Selecting the Burst and Non-Burst mode is mainly dependent on the FIFO depth and the device requirements. Choose the video transmission mode that suits the application scenario. The Burst mode is more beneficial because it increases the probability of the link spending more time in the low-power mode, decreasing power consumption. However, the following conditions should be met for availing the maximum benefits from the Burst mode of operation:

- The MIPI TX controller should have sufficient pixel memory to store an entire pixel line to avoid the overflow of the internal FIFOs.
- The display device should support receiving a full pixel line in a single packet burst to avoid the overflow on the reception buffer.
- The DSI output bandwidth should be higher than the DPI system interface input bandwidth in a relation that enables the link to go to low-power once per line.

If the system cannot meet these requirements, it is likely that the pixel data is lost causing the malfunctioning of the display device while using the Burst mode. These errors are related to the

capabilities of the system to store the temporary pixel data.

If all the conditions for using the Burst mode cannot be met, use the Non-Burst mode to avoid the errors caused by the Burst mode. The Non-Burst mode provides a better matching of rates for pixel transmission, enabling:

- Only a certain amount of pixels to be stored in the memory and not requiring a full pixel line (lesser DPI RAM requirements in the MIPI TX)
- Operation with devices that support only a small amount of pixel buffering (less than a full pixel line)

The DSI Non-Burst mode should be configured in such way that the DSI output pixel ratio matches with the DPI input pixel ratio, reducing the memory requirements on both host and/or device side. This is achieved by dividing a pixel line into several chunks of pixels and optionally interleaving them with null packets.

The following equations show how the MIPI TX controller transmission parameters should be programmed in Non-Burst mode to match the DSI link pixel output ratio (left hand side of the "=" sign) and DPI pixel input (right hand side of the "=" sign).

- When the null packets are enabled:
  - $\text{lanebyteclkperiod} * \text{vid\_num\_chunks} (\text{vid\_pkt\_size} * \text{bytes\_per\_pixel} + 12 + \text{vid\_null\_size}) / \text{number\_of\_lanes} = \text{pixels\_per\_line} * \text{dpipclkperiod}$
- When the null packets are disabled:
  - $\text{lanebyteclkperiod} * \text{vid\_num\_chunks} (\text{vid\_pkt\_size} * \text{bytes\_per\_pixel} + 6) / \text{number\_of\_lanes} = \text{pixels\_per\_line} * \text{dpipclkperiod}$

In our system, the dpi pixel FIFO depth is 8192 byte.

### 9.2.3.2 APB interface

The APB Slave interface allows the transmission of generic information in Command mode. MIPI supports the transmission of write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The [GEN\\_PLD\\_DATA](#) register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The [GEN\\_HDR](#) register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the [GEN\\_PLD\\_DATA](#) register.

- Generic Write Short Packet 0 Parameters
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameters
- Generic Read Short Packet 0 Parameters
- Generic Read Short Packet 1 Parameters
- Generic Read Short Packet 2 Parameters
- Maximum Read Packet Configuration
- Generic Long Write Packet
- DCS Write Short Packet 0 Parameters
- DCS Write Short Packet 1 Parameters

- DCS Read Short Packet 0 Parameters
- DCS Write Long Packet.

For more information about of these packages, please refer to the official document of DCS Specification.

### 9.2.3.3 Transmission of Commands

The MIPI supports the transmission of commands, both in high-speed and low-power, while in Video mode. The MIPI uses Blanking or Low-Power (BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of follow diagram:

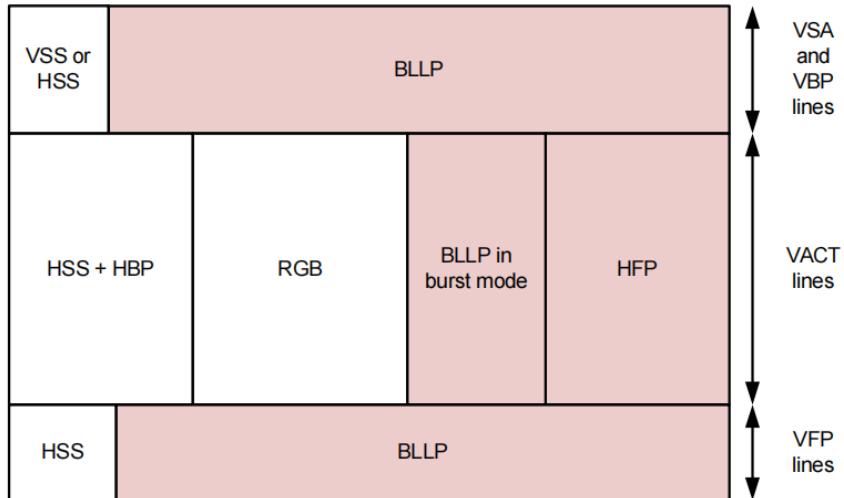


Figure 9-13 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packets/states:

- Vertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Mipi dsi can be configured to send the low-power commands during the high-speed video mode transmission. To enable this feature, set the `lp_cmd_en` bit of the `VID_MODE_CFG` register to 1. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in low-power mode to Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch (VFP) regions.

Bits 8 to 13 of the `VID_MODE_CFG` register indicates if MIPI can go to low-power when in idle. If the `lp_cmd_en` bit is set (1'b1) and non-video packets are in queue, miipi dsi ignores the low-power configuration and transmits low-power commands, even if it is not allowed to enter low-power in a specific region. After the low-power commands transmission, miipi dsi remains in lowpower until a sync event occurs.

For example, consider that the VFP is selected as high-speed region (`lp_vfp_en = 1'b0`) with `lp_cmd_en` set as a command to transmit in low-power in the VPF region. This command is transmitted in low-power, and the line stays in low-power until a new HSS arrives.

### 9.2.3.3.1 Calculating the Time to Transmit Commands in Low-Power Mode in the VSA, VBP, and VFP Regions

The `outvact_lpcmd_time` field of the `DPI_LP_CMD_TIM` register indicates the time available (in bytes) to transmit a command in low-power mode (based on the escape clock) on a line during the VSA, VBP, and the VFP regions.

Calculation of `outvact_lpcmd_time` depends on the Video mode that you use. The follow diagram illustrates the timing intervals for the Video mode in non-Burst with sync pulses and the timing intervals for the Video mode in Burst and non-Burst with sync events.

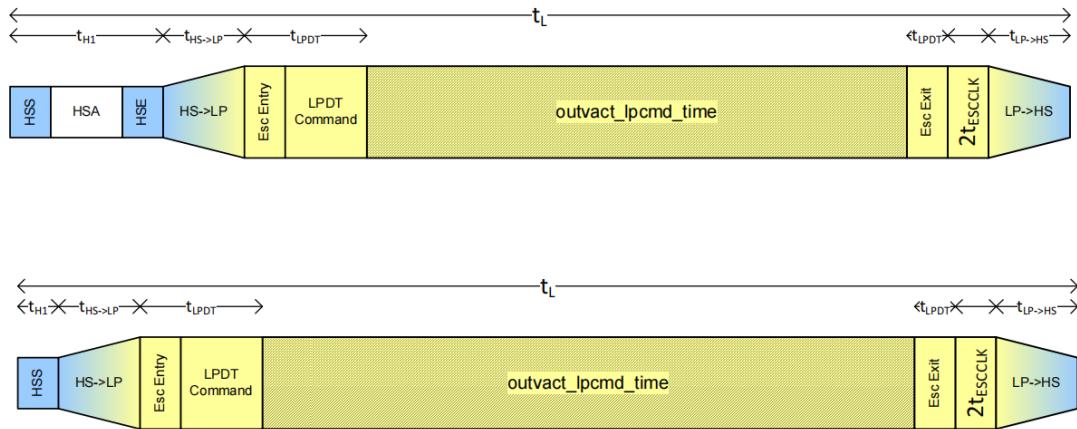


Figure 9-14 `outvact_lpcmd_time` for Non-Burst with Sync event and Sync Pulses

This time is calculated as follows:

$$\text{outvact\_lpcmd\_time} = (t_L - (t_{H1} + t_{HS \rightarrow LP} + t_{LP \rightarrow HS} + t_{LPDT} + 2t_{ESCCCLK})) / (2 \times 8 \times t_{ESCCCLK})$$

Where,

- $t_L$  = Line time
- $t_{H1}$  = Time of the HSA pulse for sync pulses mode or the time to send the HSS packet, including EoTp
- $t_{HS \rightarrow LP}$  = Time to enter the low-power mode
- $t_{LP \rightarrow HS}$  = Time to leave the low-power mode
- $t_{LPDT}$  = PHY timing related with Escape Mode Entry, LPDT Command, and Escape Exit. According to the PHY specification, this value is always 11 bits in low-power (or 22 TX Escape clock cycles).
- $t_{ESCCCLK}$  = Escape clock period as programmed in the `tx_esc_clk_division` field of the `CLKMGR_CFG` register
- $2xt_{ESCCCLK}$  = Delay imposed by the controller implementation

### 9.2.3.3.2 Calculating the Time to Transmit the Commands in Low-Power Mode in the HFP Region

The `invact_lpcmd_time` field of the `DPI_LP_CMD_TIM` register indicates the time available (in bytes) to transmit a command in low-power mode (based on the escape clock) in the Vertical Active (VACT) region. To calculate the value of `invact_lpcmd_time`, consider the video mode that you use. The follow diagram shows the timing intervals for video mode in Non-Burst with sync pulses, timing intervals for video mode in non-Burst with sync events and Burst video mode.

This time is calculated as follows:

$$\text{invact\_lpcmd\_time} = (t_L - (t_{HSA} + t_{HBP} + t_{HACT} + t_{HS \rightarrow LP} + t_{LP \rightarrow HS} + t_{LPDT} + 2t_{ESCCCLK})) / (2 \times 8 \times t_{ESCCCLK})$$

Where

$t_L$  = Line time

$t_{HSA}$  = Time of the HSA pulse (VID\_HSA\_TIME)

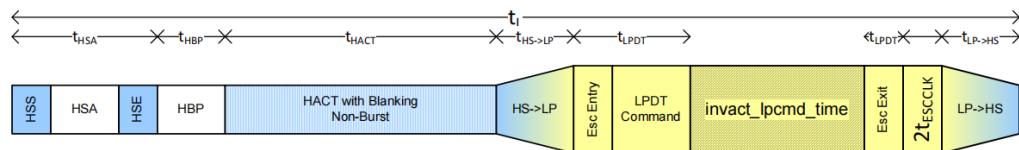
$t_{HBP}$  = Time of Horizontal back porch (VID\_HBP\_TIME)

$t_{HACT}$  = Time of Video active. For Burst mode, the Video active is time compressed and is calculated as follows:

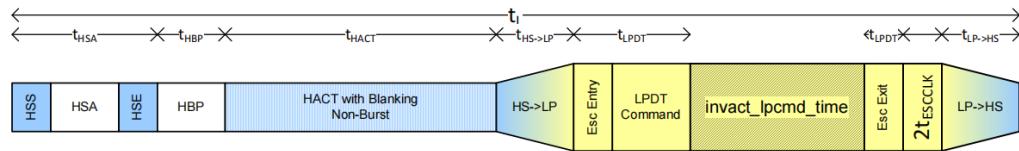
$t_{HACT} = \text{vid\_pkt\_size} * \text{Bytes\_per\_Pixel} / \text{Number\_Lanes} * t_{\text{Lane\_byte\_clk}}$

$t_{\text{ESCCLK}}$  = escape clock period as programmed in tx\_esc\_clk\_division field of the CLKMGR\_CFG register

#### invact\_lpcmd\_time for Non-Burst with Sync Pulses



#### invact\_lpcmd\_time for Non-Burst with Sync Events



#### invact\_lpcmd\_time for Burst Mode

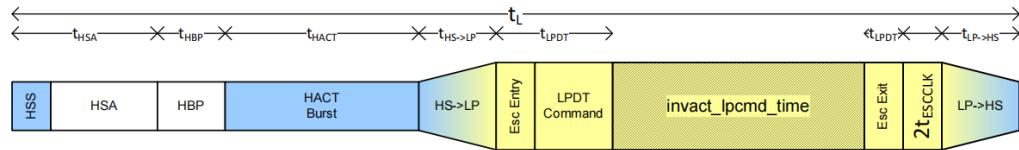


Figure 9-15 invact\_lpcmd\_time

The generation of ESCCLK is shown in the figure below, ESCCLK cannot be greater than 20MHz, and the frequency division coefficient is configured through the register, LANEBYTECLK/tx\_clk\_esc\_division is the actual frequency of ESCCLK.

#### 9.2.3.3.3 Transmission of Commands in High-Speed Mode

If the lp\_cmd\_en bit of the VID\_MODE\_CFG register is 0, the commands are sent in high-speed in Video Mode. In this case, the MIPI TX automatically determines the area where each command can be sent and no programming or calculation is required.

#### 9.2.3.3.4 Read Command Transmission

The max\_rd\_time field of the PHY\_TMR\_RD\_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles. It is calculated as follows:

max\_rd\_time = Time to transmit the read command in low-power mode + Time to enter and leave low power mode + Time to return the read data packet from the peripheral device.

The time to return the read data packet from the peripheral depends on the number of bytes read and the escape clock frequency of the peripheral, not the escape clock of the host. The max\_rd\_time field is

used in both high-speed and low-power mode to determine if there is time to complete a read command in a BLLP period.

In high-speed mode (`lp_cmd_en` = 0), `max_rd_time` is calculated as follows:

$$\text{max\_rd\_time} = (\text{t}_{\text{HS} \rightarrow \text{LP}} + \text{t}_{\text{LP} \rightarrow \text{HS}} + \text{t}_{\text{read}} + 2 \times \text{t}_{\text{BTA}}) / \text{lanebyteclkperiod}$$

In low-power mode (`lp_cmd_en` = 1), `max_rd_time` is calculated as follows:

$$\text{max\_rd\_time} = (\text{t}_{\text{HS} \rightarrow \text{LP}} + \text{t}_{\text{LP} \rightarrow \text{HS}} + \text{t}_{\text{LPDT}} + \text{t}_{\text{IPRD}} + \text{t}_{\text{read}} + 2 \times \text{t}_{\text{BTA}}) / \text{lanebyteclkperiod}$$

Where,

- $\text{t}_{\text{HS} \rightarrow \text{LP}}$  = Time to enter the low-power mode
- $\text{t}_{\text{LP} \rightarrow \text{HS}}$  = Time to leave the low-power mode
- $\text{t}_{\text{LPDT}}$  = PHY timing related to Escape mode entry, LPDT command, and Escape mode exit.
- According to the PHY specification, this value is always 11 bits in low-power (or 22 TX escape clock cycles).
- $\text{t}_{\text{IPRD}}$  = Read command time in low-power mode (64 \* TX esc clock)
- $\text{t}_{\text{read}}$  = Time to return the read data packet from the peripheral
- $\text{t}_{\text{BTA}}$  = time to perform a bus turnaround (PHY dependent)

#### 9.2.3.4 Video pattern generator

The Video Mode Pattern Generator allows the transmission of horizontal/vertical color bar and PHY BER testing pattern without any stimuli.

The frame requirements must be defined in video registers that are listed in follow table:

Table 9-4 Register for pattern generator

Register Name	Description
VID_MODE_CFG	Video mode configuration
VID_PKT_SIZE	Video packet size
VID_NUM_CHUNKS	Number of chunks
VID_NULL_SIZE	Null packet size
VID_HSA_TIME	Horizontal sync active time
VID_HBP_TIME	Horizontal back porch time
VID_HLINE_TIME	Line time
VID_VSA_LINES	Vertical sync active period
VID_VBP_LINES	Vertical back porch period
VID_VFP_LINES	Vertical front porch period
VID_VACTIVE_LINES	Vertical resolution

The color bar pattern comprises eight bars of the colors white, yellow, cyan, green, magenta, red, blue, and black. Each color width is calculated by dividing the line pixel size (vertical pattern) or the number of lines (Horizontal pattern) by eight. In the vertical color bar mode, each single color bar has a width of the number of pixels in a line divided by eight. In case the number of pixels in a line is not divisible by

eight, the last color (black) contains the remaining. In the horizontal color bar mode, each color line has a color width of the number of lines in a frame divided by eight. In case the number of lines in a frame is not divisible by eight, the last color (black) contains the remaining lines.:.

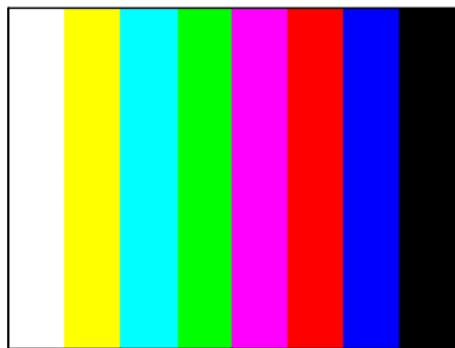


Figure 9-16 Vertical color bar



Figure 9-17 Horizontal Color Bar Mode

### 9.2.3.5 Error Control

The [INT\\_ST0](#) and [INT\\_ST1](#) registers are associated with error condition reporting. These registers can trigger an interrupt pin to inform the system about the occurrence of errors.

The MIPI TX controller has one interrupt pin that is set high when an error occurs in either the [INT\\_ST0](#) or the [INT\\_ST1](#) register.

The triggering of the interrupt pin can be masked by programming the mask registers [INT\\_MSK0](#) and [INT\\_MSK1](#). By default, all errors are masked. When any bit of these registers is set to 1, it enables the interrupt for a specific error. The error bit is always set in the respective INT\_STn register. The [INT\\_ST0](#) and [INT\\_ST1](#) registers are always cleared after a read operation. The interrupt pin is cleared if all registers that caused the interrupt are read.

The interrupt force registers ([INT\\_FORCE0](#) and [INT\\_FORCE1](#)) are used for test purposes, and they allow triggering the interrupt events individually without the need to activate the conditions that trigger the interrupt sources; this is because it is extremely complex to generate the stimuli for that purpose. This feature also facilitates the development and testing of the software associated with the interrupt events. Setting any bit of these registers to 1 triggers the corresponding interrupt.

### 9.2.3.6 PHY's config

The PHY's configuration is mainly the configuration of the PLL, generating lanebyte clock and serialized clock to ensure the serialize conversion of data, the frequency of reference clock Fin is 20MHz, and the output clock frequency of PLL should be half of the lane rate, for example, the lane rate is 2Gbps, and the output frequency of PLL should be 1GHz.

Since the VCO output frequency range is 320MHz~1250MHz, there are some differences in the frequency division coefficient of PLL in different frequency output ranges.

If the ouput of VCO in the range 320MHz~1250MHz, the relation between Fout and Fin as follow:

$$F_{out} = F_{vco} = \frac{M}{N} \times F_{in}$$

If the ouput of VCO in the range 160MHz~320MHz, the relation between Fout and Fin as follow:

$$F_{out} = \frac{F_{vco}}{2} = \frac{M}{2N} \times F_{in}$$

If the ouput of VCO in the range 80MHz ~ 160MHz, the relation between Fout and Fin as follow:

$$F_{out} = \frac{F_{vco}}{4} = \frac{M}{4N} \times F_{in}$$

If the ouput of VCO in the range 80MHz ~160MHz, the relation between Fout and Fin as follow:

$$F_{out} = \frac{F_{vco}}{8} = \frac{M}{8N} \times F_{in}$$

The value of parameter N can be calculated as follow formula, Since the frequency of fin is 20MHz, N can be taken as 10, The value of parameter M can be calculated upper formula.

$$2 \leq \frac{Fin}{N} \leq 8$$

M and N in the formula are not the actual configured register values, and the correspondence between M and N to the register value is shown in the following table:

Table 9-5 The relationship between the register m and coefficient M

Parameter	Description	M	m[9:0]
Minimum	M=m+2	64	10'h3E
Maximum		625	10'h26F

Table 9-6 The relationship between the register n and coefficient N

Parameter	Description	N	n[3:0]
Minimum	N=n+1	1	4'h0
Maximum		16	4'hF

All other PLL register's value VS the frequency as follow table:

Table 9-7 PLL output frequency vs register value

Output frequency [MHz]	vco_cntrl[5:0]	cpbias_cntrl[6:0]	gmp_cntrl[1:0]	int_cntrl[5:0]	prop_cntrl[5:0]
1150 – 1250	000001	0010000	01	000000	001110
1100 – 1152	000001	0010000	01	000000	001101
630 – 1149	000011	0010000	01	000000	001101
420 – 660	000111	0010000	01	000000	001101
320 – 440	001111	0010000	01	000000	001101
210 – 330	010111	0010000	01	000000	001101
160 – 220	011111	0010000	01	000000	001101
105 – 165	100111	0010000	01	000000	001101
80 – 110	101111	0010000	01	000000	001101
52.5 – 82.5	110111	0010000	01	000000	001101
40 – 55	111111	0010000	01	000000	001101

#### 9.2.4 Initialization

The following figure shows the overall initialization process of MIPI:



Figure 9-18 MIPI initialization

- Reset MIPI DSI using the global reset.
- Configure n\_lanes (PHY\_IF\_CFG) to define the number of lanes with which the controller can perform high-speed transmissions.
- Assert a bit corresponding to the error that is supposed to trigger an interrupt in INT\_MSK\_<group>.
- Configure DPI according to the programming sequence described in the panel databook.
- Initialize the PHY by following the programming sequence in the section “DPHY initialization”.
- Assert the PWR\_UP[0] bit to power-up the controller.

### 9.2.4.1 Configuring the Display Pixel Interface

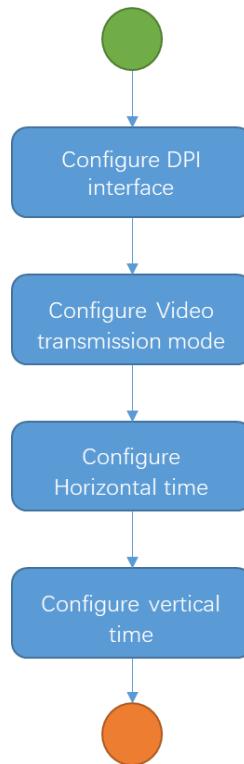


Figure 9-19 DPI configuration

- Configure the DPI interface to define how the DPI interface interacts with the controller.
  - **Configure dpi\_vcid (DPI\_VCID):** This field configures the virtual channel that the packets generated by the DPI interface is indexed.
  - **Configure dpi\_color\_coding (DPI\_COLOR\_CODING):** This field configures the bits per pixel that the interface transmits and also the variant configuration of each bpp.
  - **Configure dataen\_active\_low (DPI\_CFG\_POL):** This bit configures the polarity of the dpidataen signal and sets it to be active low.
  - **Configure vsync\_active\_low (DPI\_CFG\_POL):** This bit configures the polarity of the dpivsync signal and sets it to be active low.
  - **Configure hsync\_active\_low (DPI\_CFG\_POL):** This bit configures the polarity of the dpihsync signal and sets it to be active low.
  - **Configure shutd\_active\_low (DPI\_CFG\_POL):** This bit configures the polarity of the dpishutdn signal and sets it to be active low.
  - **Configure colorm\_active\_low (DPI\_CFG\_POL):** This bit configures the polarity of the dpicolorm signal and sets it to be active low.
- Select the video transmission mode to define how the processor requires the video line to be transported through the DSI link.
  - **Configure the low-power transitions (VID\_MODE\_CFG):** Defines the video periods which are permitted to go to low-power if there is time available to do so.
  - **Configure frame\_bta\_ack\_en (VID\_MODE\_CFG):** Specifies if MIPI TX should request the peripheral acknowledge message at the end of frames.

- Configure **lp\_cmd\_en** (**VID\_MODE\_CFG**): Specifies that commands are to be transmitted in low-power.
- Burst mode:
  - ◆ Configure the register field **vid\_mode\_type** (**VID\_MODE\_CFG**) with value 2'b1x.
  - ◆ Configure **vid\_pkt\_size** (**VID\_PKT\_SIZE**) with the size of the active line period, measured in pixels.
  - ◆ The fields **vid\_num\_chunks** and **vid\_null\_size** are ignored by the MIPI TX.
- Non-Burst mode:
  - ◆ Configure the **vid\_mode\_type** field (**VID\_MODE\_CFG**) with 2'b0x.
  - ◆ Configure the **vid\_mode\_type** field (**VID\_MODE\_CFG**) with 2'b00 to enable the transmission of sync pulses.
  - ◆ Configure the **vid\_mode\_type** field (**VID\_MODE\_CFG**) with 2'b01 to enable the transmission of sync events.
  - ◆ Configure the **vid\_pkt\_size** field (**VID\_MODE\_CFG**) with the number of pixels to be transmitted in a single packet. Selecting this value depends on the available memory of the attached peripheral.
  - ◆ Configure the **vid\_num\_chunks** field (**VID\_NUM\_CHUNKS**) with the number of packets to be transmitted per video line. The value of **vid\_pkt\_size** \* **vid\_num\_chunks** is the number of pixels per line of video, except if **vid\_num\_chunks** is 0, which disables the multi-packets. If you set it to 1, there is still only one packet per line, but it can be part of a chunk, followed by a null packet.
  - ◆ Configure the **vid\_null\_size** field (**VID\_NULL\_SIZE**) with the size of null packets to be inserted as part of the chunks. Setting it to 0, disables null packets.
- Define the DPI horizontal timing configuration as follows:
- Configure the **vid\_hline\_time** field (**VID\_HLINE\_TIME**) with the time taken by a DPI video line measured in cycles of **lane byte clock**. When the periods of DPI clock and lane byte clock are not multiples, the value to program the **vid\_hline\_time** needs to be **rounded up**. A timing mismatch is introduced between the lines due to the rounding of configuration values. If the DSI controller is configured not to go to low-power, then this timing divergence accumulates on every line, introducing a significant amount of mismatch towards the end of the frame. The reason for this is that the MIPI TX cannot re-synchronize on every new line because, it transmits the blanking packets when the horizontal Sync event occurs on the DPI interface. However, the accumulated mismatch should become extinct on the last line of a frame, where, according to the DSI specification, the link should always return to low-power regaining synchronization, when a new frame starts on a vertical sync event. If the accumulated timing mismatch is greater than the time in low-power on the last line, a malfunction occurs. This phenomenon can be avoided by configuring the MIPI TX to go to low-power once per line.
- Configure the **vid\_hsa\_time** field (**VID\_HSA\_TIME**) with the time taken by a DPI Horizontal Sync Active period measured in cycles of **lane byte clock**.
- Configure the **vid\_hbp\_time** field (**VID\_HBP\_TIME**) with the time taken by the DPI Horizontal Back Porch period measured in cycles of **lane byte clock**. Special attention should be given to the calculation of this parameter.
- Define the vertical line configuration:
- Configure the **vsa\_lines** field (**VID\_VSA\_LINES**) with the **number of lines** existing in the DPI Vertical

Sync Active period.

- Configure the vbp\_lines field (VID\_VBP\_LINES]) with the **number of lines** existing in the DPI Vertical Back Porch period.
- Configure the vfp\_lines field (VID\_VFP\_LINES) with the **number of lines** existing in the DPI Vertical Front Porch period.
- Configure the v\_active\_lines field (VID\_VACTIVE\_LINES) with the **number of lines** existing in the DPI Vertical Active Period.

#### 9.2.4.2 Initializing D-PHY

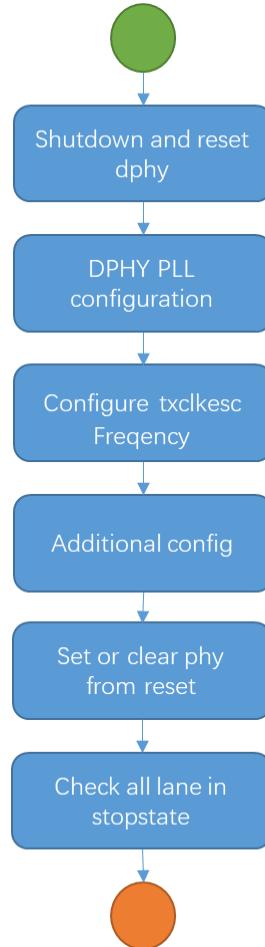


Figure 9-20 Initializing D-PHY

This process is based on the APB register interface access, through the access process, it can generate the test port timing.

- Power-Up and reset the PHY using "PHY\_RSTZ" register.
- Configure the D-PHY PLL clock frequency through the Test interface.
  - Config PHY's register `pll_m_ovr[9:0]` and `pll_m_ovr_en`, the address of `pll_m_ovr` is `0x18`, the address of `pll_m_ovr_en` is `0x19`. `pll_m_ovr` need to be configured in two installments, when bit7=1, it config `pll_m_ovr[9:5]`, when bit7=0, it config `pll_m_ovr[4:0]`.

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	testdin[7] = 1'b1	8'b000001111	Reserved			pll_m_ovr[9:5]				
testdin	testdin[7] = 1'b0	8'b000010000	Reserved			pll_m_ovr[4:0]				
testdout	testdin[7] = 1'b0	8'b0000XXXXXX	Reserved			pll_m[4:0]				
testdout	testdin[7] = 1'b1	8'b0000XXXXXX	Reserved			pll_m[9:5]				

- Config PHY's register pll\_n\_ovr[3:0] and pll\_n\_ovr\_e, the address of pll\_n\_ovr is 0x17, the address of pll\_n\_ovr\_en is 0x19.

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	No	8'b00001011	Reserved			pll_n_ovr				
testdout	No	8'b01101011	pll_lock_de_t_on	pll_gear_shif	pll_reset	pll_pwro_n	pll_n[3:0]			

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	No	8'b000000000	Reserved	pll_m_ovr_en	pll_n_ovr_en	Reserved				
testdout	No	8'b000000000	Reserved	pll_m_ovr_en	pll_n_ovr_en	Reserved				

- Config PHY's register pll\_vco\_cntrl\_ovr[5:0] and pll\_vco\_cntrl\_ovr\_en, the address is 0x12.

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	No	8'b00111111	Reserved	pll_vco_cntrl_o_vr_en	pll_vco_cntrl_ovr					
testdout	No	8'b00111111	Reserved	pll_vco_cntrl_o_vr_en	pll_vco_cntrl_ovr					

- Config PHY's register cpbias\_cntrl[6:0] and pll\_cpbias\_cntrl[6:0], the address is 0x1C.

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	No	8'b000000000	Reserved	pll_cpbias_cntrl						
testdout	No	8'b000000000	Reserved	pll_cpbias_cntrl						

- Config PHY's register pll\_gmp\_cntrl[1:0], the address is 0x13.

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	No	8'b000000000	Reserved	pll_gmp_cntrl	tstplldig					
testdout	No	8'b000000000	pll_testlock	Reserved	pll_gmp_cntrl	tstplldig				

- Config PHY's register pll\_int\_cntrl[5:0], the address is 0x0f.

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	No	8'b00000000	Reserved		pll_int_cntrl					
testdout	No	8'b00000000	Reserved		pll_int_cntrl					

- Config PHY's register `pll_prop_cntrl[5:0]`, the address is 0x0e.

Test Interface	Condition	Default value	Bits [7:0]							
			7	6	5	4	3	2	1	0
testdin	No	8'b00000000	Reserved		pll_prop_cntrl					
testdout	No	8'b00000000	Reserved		pll_prop_cntrl					

- TxClkEsc frequency must be configured between 2 to 20 MHz. This is done by writing into the `tx_esc_clk_division` field of the CLKMGR\_CFG register. The `tx_esc_clk_division` field divides the byte clock, and generates a TX\_ESC clock for the D-PHY. Follow diagram describes how txclkesc is obtained.

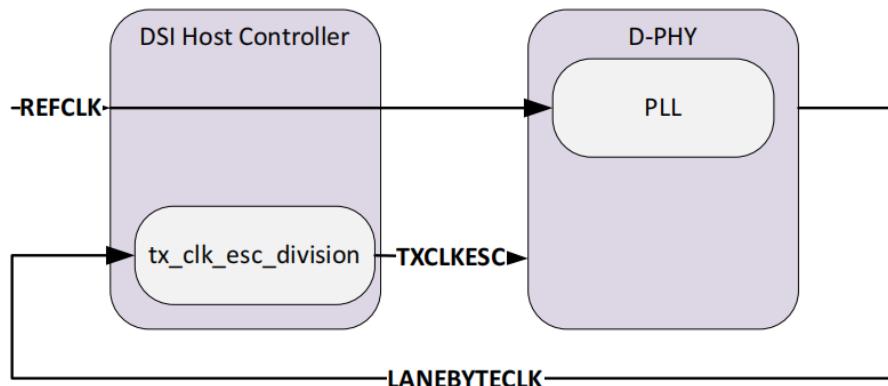


Figure 9-21 txclkesc generation

- Clear `phy_shutdownz` (`PHY_RSTZ[0]`) and `phy_rstz` (`PHY_RSTZ[1]`) to put the PHY in the reset state. Set `phy_shutdownz` (`PHY_RSTZ[0]`) and `phy_rstz` (`PHY_RSTZ[1]`) to remove the PHY from reset state.
- Verify that D-PHY active lanes are in Stop state:
  - `PHY_STATUS[2] = 1'b1`
  - `PHY_STATUS[4] = 1'b1`
  - `PHY_STATUS[7] = 1'b1` – if Lane 2 active
  - `PHY_STATUS[9] = 1'b1` – if Lane 3 active
  - `PHY_STATUS[11] = 1'b1` – if Lane 4 active

#### 9.2.4.3 ULPM (ultra low power mode)

The following are the two methods to enter into ultra low-power mode, one is entering and exiting the ULPM by the software, the other is entering and exiting the ULPM using Auto ULPS Control Scheme.

##### Entering the ULPM Using the Software:

- Set `PHY_ULPS_CTRL[3:0] = 4'h5` to enter ULPM in the data and clock lanes.

- Verify that all the data lanes has entered in ULPM using PHY\_STATUS register.
- The MIPI TX is now in ULPM. Perform next two steps to turn off the PHY PLL.
- Turn off the PHY PLL by setting PHY\_RSTZ[3] = 1'b0.
- Verify that all the D-PHY PLL is unlocked: PHY\_STATUS[0] = 1'b0.

#### Exiting the ULPM Using the Software:

- If the D-PHY PLL is already locked (PHY\_STATUS[0] = 1'b1), go to step 4 else continue.
- Turn on the D-PHY PLL by setting PHY\_RSTZ[3] = 1'b1.
- Verify that D-PHY PLL is turned on: PHY\_STATUS[0] = 1'b1.
- Without deasserting the ULPM request bits, assert the Exit ULPM bits by setting PHY\_ULPS\_CTRL[3:0] = 4'hF.
- Verify that all D-PHY lanes are not in ULPM using PHY\_STATUS register.
- Wait for 1 millisecond.
- De-assert the ULPM requests and the ULPM exit bits by setting PHY\_ULPS\_CTRL [3:0] = 4'h0.

#### Entering and Exiting the ULPM using Auto ULPS Control Scheme:

- Configure the idle time (in lanebyteclk cycles) before MIPI TX enters into ULPM, using AUTO\_ULPS\_ENTRY\_DELAY register:

$$\text{AutoULPSEEntryDelay} = \text{TimeIntended(s)} / \text{Tlanebyteclk(s)}$$

- Configure PHY Wake-Up time (in pclk) using AUTO\_ULPS\_WAKEUP\_TIME register. The default Wake-Up time specified by MIPI PHY specs is 1 millisecond. The AUTO\_ULPS\_WAKEUP\_TIME register is composed by two fields:

t wakeup\_clk\_div [AUTO\_ULPS\_WAKEUP\_TIME[15:0]: This configures the T wakeup counter (measured in pclk cycles). Minimum allowed value is 'd1.

t wakeup\_cnt [AUTO\_ULPS\_WAKEUP\_TIME[31:16] : This configures the T wakeup clock divider (measured in pclk cycles). Minimum allowed value is 'd1.

$$\text{T wakeup(s)} = \text{t wakeup\_clk\_div} * \text{t wakeup\_cnt} * \text{T pclk(s)}$$

- Configure the AutoULPS mode. Auto ULPS feature has two ways to enter and exit ULPM:
  - Turning off the PHY PLL - AUTO\_ULPS\_MODE[16] = 1'b1,Clock and data enters in ULPM.
  - Without Turning off the PHY PLL - AUTO\_ULPS\_MODE[16] = 1'b0,Data lanes enter in ULPM.
- Enable AutoULPS mechanism asserting bit [0] of AUTO\_ULPS\_MODE register.

#### 9.2.5 Interface timing

The DPI port's timing is the same as the OSD's DPI port.

PHY's test port timing as follow:

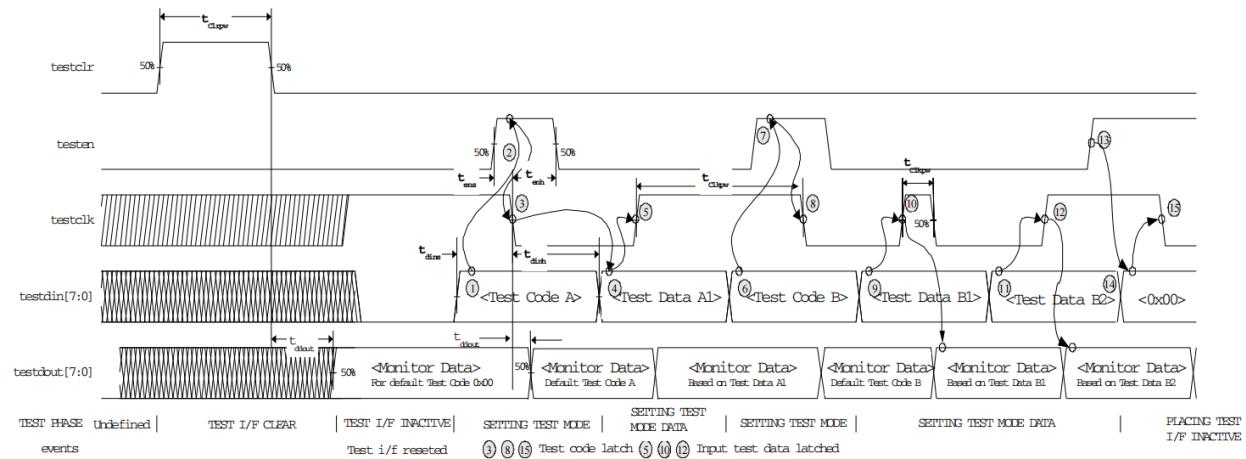


Figure 9-22 Test Port Timing

The follow diagram is test port initializing follow:

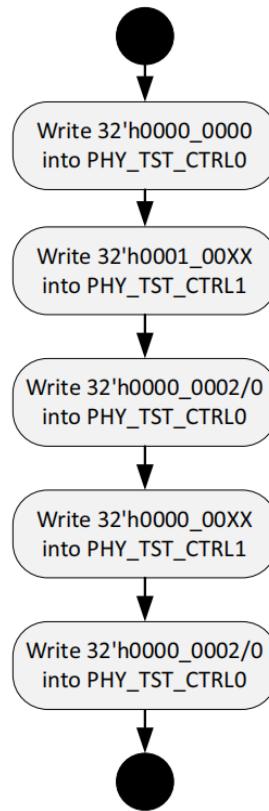


Figure 9-23 The process of PHY's register configuration

- Write 32'h00000000 into PHY\_TST\_CTRL0 to disable the testclr pin enabling the interface to write new values to the D-PHY internal registers.
- Write 32'h000100XX into PHY\_TST\_CTRL1 to enable the testen pin and configure the testdin[7:0] to 8'hXX. This operation initiates the configuration process of the test code number 0xXX.
- Write 32'h00000002 into PHY\_TST\_CTRL0 followed by writing 32'h00000000 into PHY\_TST\_CTRL0 to toggle testclk. The testdin[7:0] is sampled on the falling edge of testclk latching a new test code.

- Write 32'h000000XX into PHY\_TST\_CTRL1 to disable the testen pin and configure the testdin[7:0] to 8'hXX. This operation prepares the interface to load the test code 0xXX.
- Write 32'h00000002 into PHY\_TST\_CTRL0 followed by writing 32'h00000000 into PHY\_TST\_CTRL0 to toggle the testclk and the testdin[7:0] is sampled on the rising edge of testclk latching a new content data to the configured test code.

## 9.2.6 Register

### 9.2.6.1 Register table

Table 9-8 Register table

Register	Offset	Description
VERSION	0x0	Core Version.
PWR_UP	0x4	Power up.
CLKMGR_CFG	0x8	Factor for internal dividers.
DPI_VCID	0xc	DPI Virtual Channel ID.
DPI_COLOR_CODING	0x10	DPI color coding.
DPI_CFG_POL	0x14	DPI signals polarity.
DPI_LP_CMD_TIM	0x18	Low Power commands' timing.
PCKHDL_CFG	0x2c	EoTp, BTA, CRC and ECC Configuration.
GEN_VCID	0x30	Read responses Virtual Channel ID.
MODE_CFG	0x34	Operation mode.
VID_MODE_CFG	0x38	Video mode configuration.
VID_PKT_SIZE	0x3c	Video Packets size.
VID_NUM_CHUNKS	0x40	Number of Chunks.
VID_NULL_SIZE	0x44	Null Packets size.
VID_HSA_TIME	0x48	HSA time.
VID_HBP_TIME	0x4c	HBP time.
VID_HLINE_TIME	0x50	Overall video line time.
VID_VSA_LINES	0x54	VSA period.
VID_VBP_LINES	0x58	VBP period.
VID_VFP_LINES	0x5c	VFP period.
VID_VACTIVE_LINES	0x60	Video vertical resolution.
CMD_MODE_CFG	0x68	Command Mode operation configuration.
GEN_HDR	0x6c	Generic Interface Packet Header.

Register	Offset	Description
GEN_PLD_DATA	0x70	Generic Interface Packets Payload.
CMD_PKT_STATUS	0x74	Generic Interface and DBI FIFO status.
TO_CNT_CFG	0x78	Timeout Trigger Configuration.
HS_RD_TO_CNT	0x7c	Peripheral timeout after HS read operations.
LP_RD_TO_CNT	0x80	Peripheral timeout after LP read operations.
HS_WR_TO_CNT	0x84	Peripheral timeout after HS write operations.
LP_WR_TO_CNT	0x88	Peripheral timeout after LP write operations.
BTA_TO_CNT	0x8c	Peripheral timeout after BTA completion.
SDF_3D	0x90	3D information for VSS packets.
LPCLK_CTRL	0x94	Non-continuous Clock configuration.
PHY_TMR_LPCLK_CFG	0x98	Time configuration for (clock lane) transitions between HS and LP.
PHY_TMR_CFG	0x9c	Time configuration for (data lanes) transitions between HS and LP.
PHY_RSTZ	0xa0	D-PHY's PLL and Resets.
PHY_IF_CFG	0xa4	Active lanes and Stop State minimum time in Stop State.
PHY_ULPS_CTRL	0xa8	Transitions from and to ULPS, using D-PHY.
PHY_TX_TRIGGER	0xac	Pins related to D-PHY triggers.
PHY_STATUS	0xb0	D-PHY Status.
PHY_TST_CTRL0	0xb4	D-PHY control and clear pins.
PHY_TST_CTRL1	0xb8	D-PHY data and enable pins.
INT_ST0	0xbc	Interrupts status 0.
INT_ST1	0xc0	Interrupts Status 1.
INT_MSK0	0xc4	INT_ST0 mask.
INT_MSK1	0xc8	INT_ST1 mask.
PHY_CAL	0xcc	D-PHY skew calibration.
INT_FORCE0	0xd8	Force INT_ST0
INT_FORCE1	0xdc	Force INT_ST1.
DSC_PARAMETER	0xf0	Display Stream Compression.
PHY_TMR_RD_CFG	0xf4	PHY timings.

Register	Offset	Description
VID_SHADOW_CTRL	0x100	DPI Shadow Feature.
DPI_VCID_ACT	0x10c	Actual DPI Virtual Channel ID.
DPI_COLOR_CODING_ACT	0x110	Actual DPI Color Coding
DPI_LP_CMD_TIM_ACT	0x118	Actual DPI Low Power Commands' Timing.
VID_MODE_CFG_ACT	0x138	VID_MODE_CFG.
VID_PKT_SIZE_ACT	0x13c	Actual VID_PKT_SIZE.
VID_NUM_CHUNKS_ACT	0x140	Actual VID_NUM_CHUNKS.
VID_NULL_SIZE_ACT	0x144	Actual VID_NULL_SIZE.
VID_HSA_TIME_ACT	0x148	Actual VID_HSA_TIME.
VID_HBP_TIME_ACT	0x14c	Actual VID_HBP_TIME.
VID_HLINE_TIME_ACT	0x150	Actual VID_HLINE_TIME.
VID_VSA_LINES_ACT	0x154	Actual VID_VSA_LINES.
VID_VBP_LINES_ACT	0x158	VID_VBP_LINES.
VID_VFP_LINES_ACT	0x15c	Actual VID_VFP_LINES.
VID_VACTIVE_LINES_ACT	0x160	Actual VID_VACTIVE_LINES.
VID_PKT_STATUS	0x168	DPI FIFOs status.
SDF_3D_ACT	0x190	SDF_3D.

### 9.2.6.2 MIPI Register description

#### VERSION

**Name:** Core Version.

**Description:** Contains the version of the DSI host controller.

**Size:** 32 bits

**Offset:** 0x0

Bits	Name	Memory Access	Description
31:0	version	R	This field indicates the version of the MIPI DSI. Value After Reset: 0x30313531

#### PWR\_UP

**Name:** Power up.

**Description:** Controls the power up of the controller.

**Size:** 32 bits

**Offset:** 0x4

Bits	Name	Memory Access	Description
31:1	reserved_31_1	R	Reserved and read as zero. Value After Reset: 0x0
0	shutdownz	R/W	This bit configures the controller either to power up or to reset. Values: 0x0 (RESET): Reset the controller 0x1 (POWERUP): Power up the controller Value After Reset: 0x0

### CLKMGR\_CFG

**Name:** Factor for internal dividers.

**Description:** Configures the factor for internal dividers to divide lanebyteclk for timeout purposes.

**Size:** 32 bits

**Offset:** 0x8

Bits	Name	Memory Access	Description
31:16	reserved_31_16	R	Reserved and read as zero. Value After Reset: 0x0
15:8	to_clk_division	R/W	This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of high-speed to low-power and low-power to high-speed transition error. Value After Reset: 0x0
7:0	tx_esc_clk_division	R/W	This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation. Value After Reset: 0x0

### DPI\_VCID

**Name:** DPI Virtual Channel ID.

**Description:** Configures the Virtual Channel ID for DPI traffic.

**Size:** 32 bits

**Offset:** 0xc

Bits	Name	Memory Access	Description
31:2	reserved_31_2	R	Reserved and read as zero. Value After Reset: 0x0
1:0	dpi_vcidx	R/W	This field configures the DPI virtual channel id that is indexed to the Video mode packets. Value After Reset: 0x0

### DPI\_COLOR\_CODING

**Name:** DPI color coding.

**Description:** Configures DPI color coding.

**Size:** 32 bits

**Offset:** 0x10

Bits	Name	Memory Access	Description
31:9	reserved_31_9	R	Reserved and read as zero. Value After Reset: 0x0
8	loosely18_en	R/W	When set to 1, this bit activates loosely packed variant to 18-bit configurations. Value After Reset: 0x0
7:4	reserved_7_4	R	Reserved and read as zero. Value After Reset: 0x0
3:0	dpi_color_coding	R/W	This field configures the DPI color for Video Mode/eDPI Command Mode coding as follows: Values: 0x0 (CC00): 16-bit configuration 1 0x1 (CC01): 16-bit configuration 2 0x2 (CC02): 16-bit configuration 3 0x3 (CC03): 18-bit configuration 1 0x4 (CC04): 18-bit configuration 2 0x5 (CC05): 24-bit 0x6 (CC06): 20-bit YCbCr 4:2:2 loosely packed / Reserved for eDPI Command Mode 0x7 (CC07): 24-bit YCbCr 4:2:2 / Reserved for eDPI Command Mode 0x8 (CC08): 16-bit YCbCr 4:2:2 / Reserved for eDPI Command Mode 0x9 (CC09): 30-bit - DSC_ENC 10bit / Reserved for eDPI Command Mode 0xa (CC10): 36-bit / Reserved for eDPI Command Mode 0xb (CC11): 12-bit YCbCr 4:2:0 / Reserved for eDPI Command Mode 0xc (CC12): DSC24 compressed Data 0xd (CC13): Reserved 0xe (CC14): Reserved 0xf (CC15): Reserved Value After Reset: 0x0

### DPI\_CFG\_POL

**Name:** DPI signals polarity.

**Description:** Configures the polarity of DPI signals.

**Size:** 32 bits

**Offset:** 0x14

Bits	Name	Memory Access	Description
31:5	reserved_31_5	R	Reserved and read as zero. Value After Reset: 0x0
4	colorm_active_low	R/W	When set to 1, this bit configures the color mode pin (dpicolorm) as active low. Value After Reset: 0x0
3	shutd_active_low	R/W	When set to 1, this bit configures the shutdown pin (dpishutdn) as active low. Value After Reset: 0x0
2	hsync_active_low	R/W	When set to 1, this bit configures the horizontal synchronism

Bits	Name	Memory Access	Description
			pin (dipihsync) as active low. Value After Reset: 0x0
1	vsync_active_low	R/W	When set to 1, this bit configures the vertical synchronism pin (dipivsync) as active low. Value After Reset: 0x0
0	dataen_active_low	R/W	When set to 1, this bit configures the data enable pin (dpidataen) as active low. Value After Reset: 0x0

### DPI\_LP\_CMD\_TIM

**Name:** Low Power commands' timing.

**Description:** Configures the timing for low-power commands sent while in video mode.

**Size:** 32 bits

**Offset:** 0x18

Bits	Name	Memory Access	Description
31:24	reserved_31_24	R	Reserved and read as zero. Value After Reset: 0x0
23:16	outvact_lpcmd_time	R/W	This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions. Value After Reset: 0x0
15:8	reserved_15_8	R	Reserved and read as zero. Value After Reset: 0x0
7:0	invact_lpcmd_time	R/W	This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region. Value After Reset: 0x0

### PCKHDL\_CFG

**Name:** EoTp, BTA, CRC and ECC Configuration.

**Description:** Configures how EoTp, BTA, CRC and ECC are to be used, to meet peripherals characteristics

**Size:** 32 bits

Bits	Name	Memory Access	Description
31:6	reserved_31_6	R	Reserved and read as zero. Value After Reset: 0x0
5	eotp_tx_lp_en	R/W	When set to 1, this bit enables the EoTp transmission in low-power. Value After Reset: 0x0
4	crc_rx_en	R/W	When set to 1, this bit enables the CRC reception and error reporting. Value After Reset: 0x0
3	ecc_rx_en	R/W	When set to 1, this bit enables the ECC reception, error correction,

Bits	Name	Memory Access	Description
			and reporting. Value After Reset: 0x0
2	bta_en	R/W	When set to 1, this bit enables the Bus Turn-Around (BTA) request. Value After Reset: 0x0
1	eotp_rx_en	R/W	When set to 1, this bit enables the EoTp reception. Value After Reset: 0x0
0	eotp_tx_en	R/W	When set to 1, this bit enables the EoTp transmission in high-speed. Value After Reset: 0x0

### GEN\_VCID

**Name:** Read responses Virtual Channel ID.

**Description:** Configures the Virtual Channel ID of READ responses to store and return to Generic interface.

**Size:** 32 bits

Offset: 0x30

Bits	Name	Memory Access	Description
31:18	reserved_31_18	R	Reserved and read as zero. Value After Reset: 0x0
17:16	gen_vcid_tx_auto	R/W	This field indicates the Generic interface virtual channel identification where generic packet is automatically generated & transmitted. Value After Reset: 0x0
15:10	reserved_15_10	R	Reserved and read as zero. Value After Reset: 0x0
9:8	gen_vcid_tear_auto	R/W	This field indicates the virtual channel identification for tear effect by hardware Value After Reset: 0x0
7:2	reserved_7_2	R	Reserved and read as zero. Value After Reset: 0x0
1:0	gen_vcid_rx	R/W	This field indicates the Generic interface read-back virtual channel identification. Value After Reset: 0x0

### MODE\_CFG

**Name:** Operation mode.

**Description:** Configures the mode of operation between Video or Command Mode. (Commands can still be sent while in video mode.)

**Size:** 32 bits

Offset: 0x34

Bits	Name	Memory Access	Description
31:1	reserved_31_1	R	Reserved and read as zero. Value After Reset: 0x0

Bits	Name	Memory Access	Description
0	cmd_video_mode	R/W	This bit configures the operation mode: Values: 0x0 (VIDMODE): video mode 0x1 (CMDMODE): command mode Value After Reset: 0x1

**VID\_MODE\_CFG****Name:** Video mode configuration.**Description:** Configures several aspects of Video mode operation, the transmission mode, switching to low-power in the middle of a frame, enabling acknowledge and whether to send commands in low-power.**Size:** 32 bits**Offset:** 0x38

Bits	Name	Memory Access	Description
31:25	reserved_31_25	R	Reserved and read as zero. Value After Reset: 0x0
24	vpg_orientation	R/W	This field indicates the color bar orientation as follows: Values: 0x0 (VPGORENT0): Vertical mode 0x1 (VPGORENT1): Horizontal mode Value After Reset: 0x0
23:21	reserved_23_21	R	Reserved and read as zero. Value After Reset: 0x0
20	vpg_mode	R/W	This field is to select the pattern: Values: 0x0 (COLORBAR): horizontal or vertical 0x1 (BERPATTERN): vertical only Value After Reset: 0x0
19:17	reserved_19_17	R	Reserved and read as zero. Value After Reset: 0x0
16	vpg_en	R/W	When set to 1, this bit enables the video mode pattern generator. Value After Reset: 0x0
15	lp_cmd_en	R/W	When set to 1, this bit enables the command transmission only in low-power mode. Value After Reset: 0x0
14	frame_bta_ack_en	R/W	When set to 1, this bit enables the request for an acknowledge response at the end of a frame. Value After Reset: 0x0
13	lp_hfp_en	R/W	When set to 1, this bit enables the return to low-power inside the HFP period when timing allows. Value After Reset: 0x0
12	lp_hbp_en	R/W	When set to 1, this bit enables the return to low-power inside the HBP period when timing allows. Value After Reset: 0x0
11	lp_vact_en	R/W	When set to 1, this bit enables the return to low-power inside the VACT period when timing allows. Value After Reset: 0x0

Bits	Name	Memory Access	Description
10	lp_vfp_en	R/W	When set to 1, this bit enables the return to low-power inside the VFP period when timing allows. Value After Reset: 0x0
9	lp_vbp_en	R/W	When set to 1, this bit enables the return to low-power inside the VBP period when timing allows. Value After Reset: 0x0
8	lp_vsa_en	R/W	When set to 1, this bit enables the return to low-power inside the VSA period when timing allows. Value After Reset: 0x0
7:2	reserved_7_2	R	Reserved and read as zero. Value After Reset: 0x0
1:0	vid_mode_type	R/W	This field indicates the video mode transmission type as follows: Values: 0x0 (VIDMODE0): Non-burst with sync pulses 0x1 (VIDMODE1): Non-burst with sync events 0x2 (VIDMODE2): Burst mode 0x3 (VIDMODE3): Burst mode Value After Reset: 0x0

### VID\_PKT\_SIZE

**Name:** Video Packets size.

**Description:** Configures the video packet size.

**Size:** 32 bits

**Offset:** 0x3c

Bits	Name	Memory Access	Description
31:14	reserved_31_14	R	Reserved and read as zero. Value After Reset: 0x0
13:0	vid_pkt_size	R/W	This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification. For DSC24, this field configures the number of Bytes. Note that when using slices (i.e chunks) the minimum size packet size must be 3. Value After Reset: 0x0

### VID\_NUM\_CHUNKS

**Name:** Number of Chunks.

**Description:** Configures the number of chunks to use. The data in each chunk has the size provided by VID\_PKT\_SIZE.

**Size:** 32 bits

**Offset:** 0x40

Bits	Name	Memory Access	Description
31:13	reserved_31_13	R	Reserved and read as zero. Value After Reset: 0x0
12:0	vid_num_chunks	R/W	This register configures the number of chunks to be transmitted during a Line period (a chunk is pair made of a video packet and a null packet). If set to 0 or 1, video line is still transmitted in a single packet. If set to 1 that packet is part of a chunk, meaning that a null packet follows it (if vid_null_size>0). Otherwise, multiple chunks are used to transmit each video line. Value After Reset: 0x0

### VID\_NULL\_SIZE

**Name:** Null Packets size.

**Description:** Configures the size of null packets.

**Size:** 32 bits

**Offset:** 0x44

Bits	Name	Memory Access	Description
31:13	reserved_31_13	R	Reserved and read as zero. Value After Reset: 0x0
12:0	vid_null_size	R/W	This register configures the number of bytes inside a null packet. Setting to 0 disables null packets. Value After Reset: 0x0

### VID\_HSA\_TIME

**Name:** HSA time.

**Description:** Configures the video HSA time.

**Size:** 32 bits

**Offset:** 0x48

Bits	Name	Memory Access	Description
31:12	reserved_31_12	R	Reserved and read as zero. Value After Reset: 0x0
11:0	vid_hsa_time	R/W	This field configures the Horizontal Synchronism Active period in lane byte clock cycles. Value After Reset: 0x0

### VID\_HBP\_TIME

**Name:** HBP time.

**Description:** Configures the video HBP time.

**Size:** 32 bits

**Offset:** 0x4c

Bits	Name	Memory Access	Description
31:12	reserved_31_12	R	Reserved and read as zero.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
11:0	vid_hbp_time	R/W	This field configures the Horizontal Back Porch period in lane byte clock cycles. Value After Reset: 0x0

### VID\_HLINE\_TIME

**Name:** Overall video line time.

**Description:** Configures the overall time for each video line.

**Size:** 32 bits

**Offset:** 0x50

Bits	Name	Memory Access	Description
31:15	reserved_31_15	R	Reserved and read as zero. Value After Reset: 0x0
14:0	vid_hline_time	R/W	This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles. Value After Reset: 0x0

### VID\_VSA\_LINES

**Name:** VSA period.

**Description:** Configures the VSA period.

**Size:** 32 bits

**Offset:** 0x54

Bits	Name	Memory Access	Description
31:10	reserved_31_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	vsa_lines	R/W	This field configures the Vertical Synchronism Active period measured in number of horizontal lines. Value After Reset: 0x0

### VID\_VBP\_LINES

**Name:** VBP period.

**Description:** Configures the VBP period.

**Size:** 32 bits

**Offset:** 0x58

Bits	Name	Memory Access	Description
31:10	reserved_31_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	vbp_lines	R/W	This field configures the Vertical Back Porch period measured in number of horizontal lines. Value After Reset: 0x0

**VID\_VFP\_LINES****Name:** VFP period.**Description:** Configures the VFP period.**Size:** 32 bits**Offset:** 0x5c

Bits	Name	Memory Access	Description
31:10	reserved_31_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	vfp_lines	R/W	This field configures the Vertical Front Porch period measured in number of horizontal lines. Value After Reset: 0x0

**VID\_VACTIVE\_LINES****Name:** Video vertical resolution.**Description:** Configures the vertical resolution of video.**Size:** 32 bits**Offset:** 0x60

Bits	Name	Memory Access	Description
31:14	reserved_31_14	R	Reserved and read as zero. Value After Reset: 0x0
13:0	v_active_lines	R/W	This field configures the Vertical Active period measured in number of horizontal lines. Value After Reset: 0x0

**CMD\_MODE\_CFG****Name:** Command Mode operation configuration.**Description:** Configures several aspect of command mode operation, tearing effect, acknowledge for each packet and the speed mode to transmit each Data Type related to commands.**Size:** 32 bits**Offset:** 0x68

Bits	Name	Memory Access	Description
31:25	reserved_31_25	R	Reserved and read as zero. Value After Reset: 0x0
24	max_rd_pkt_size	R/W	This bit configures the maximum read packet size command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
23:20	reserved_23_20	R	Reserved and read as zero. Value After Reset: 0x0
19	dcs_lw_tx	R/W	This bit configures the DCS long write packet command transmission type: Values:

Bits	Name	Memory Access	Description
			0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
18	dcs_sr_0p_tx	R/W	This bit configures the DCS short read packet with zero parameter command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
17	dcs_sw_1p_tx	R/W	This bit configures the DCS short write packet with one parameter command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
16	dcs_sw_0p_tx	R/W	This bit configures the DCS short write packet with zero parameter command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
15	reserved_15	R	Reserved and read as zero. Value After Reset: 0x0
14	gen_lw_tx	R/W	This bit configures the Generic long write packet command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
13	gen_sr_2p_tx	R/W	This bit configures the Generic short read packet with two parameters command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
12	gen_sr_1p_tx	R/W	This bit configures the Generic short read packet with one parameter command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
11	gen_sr_0p_tx	R/W	This bit configures the Generic short read packet with zero parameter command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
10	gen_sw_2p_tx	R/W	This bit configures the Generic short write packet with two parameters command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed

Bits	Name	Memory Access	Description
			0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
9	gen_sw_1p_tx	R/W	This bit configures the Generic short write packet with one parameter command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
8	gen_sw_0p_tx	R/W	This bit configures the Generic short write packet with zero parameter command transmission type: Values: 0x0 (HIGHSPEED): Transition type is high-speed 0x1 (LOWPOWER): Transition type is low-power Value After Reset: 0x0
7:2	reserved_7_2	R	Reserved and read as zero. Value After Reset: 0x0
1	ack_rqst_en	R/W	When set to 1, this bit enables the acknowledge request after each packet transmission. Value After Reset: 0x0
0	tear_fx_en	R/W	When set to 1, this bit enables the tearing effect acknowledge request. Value After Reset: 0x0

## GEN\_HDR

**Name:** Generic Interface Packet Header.

**Description:** Sets the header for new packets sent using the Generic interface.

**Size:** 32 bits

**Offset:** 0x6c

Bits	Name	Memory Access	Description
31:24	reserved_31_24	R	Reserved and read as zero. Value After Reset: 0x0
23:16	gen_wc_msbyte	R/W	This field configures the most significant byte of the header packet's word count for long packets or data 1 for short packets. Value After Reset: 0x0
15:8	gen_wc_lsbyte	R/W	This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets. Value After Reset: 0x0
7:6	gen_vc	R/W	This field configures the Virtual Channel ID of the header packet. Value After Reset: 0x0
5:0	gen_dt	R/W	This field configures the packet Data Type of the header packet. Value After Reset: 0x0

## GEN\_PLD\_DATA

**Name:** Generic Interface Packets Payload.

**Description:** Sets the payload for packets sent using the Generic interface and, when read returns the contents of READ responses from the peripheral.

**Size:** 32 bits**Offset:** 0x70

Bits	Name	Memory Access	Description
31:24	gen_pld_b4	R/W	This field indicates byte 4 of the packet payload. Value After Reset: 0x0
23:16	gen_pld_b3	R/W	This field indicates byte 3 of the packet payload. Value After Reset: 0x0
15:8	gen_pld_b2	R/W	This field indicates byte 2 of the packet payload. Value After Reset: 0x0
7:0	gen_pld_b1	R/W	This field indicates byte 1 of the packet payload. Value After Reset: 0x0

**CMD\_PKT\_STATUS****Name:** Generic Interface and DBI FIFO status.**Description:** Contains information about the status of FIFOs related to DBI and Generic interface.**Size:** 32 bits**Offset:** 0x74

Bits	Name	Memory Access	Description
31:28	reserved_31_28	R	Reserved and read as zero. Value After Reset: 0x0
27	reserved_27	R	Reserved and read as zero Value After Reset: 0x0
26	reserved_26	R	Reserved and read as zero Value After Reset: 0x0
25	reserved_25	R	Reserved and read as zero Value After Reset: 0x0
24	reserved_24	R	Reserved and read as zero Value After Reset: 0x0
23:20	reserved_23_20	R	Reserved and read as zero. Value After Reset: 0x0
19	gen_buff_pld_full	R	This bit indicates the full status of the generic payload internal buffer. Value After Reset: 0x0
18	gen_buff_pld_empty	R	This bit indicates the empty status of the generic payload internal buffer. Value After Reset: 0x1
17	gen_buff_cmd_full	R	This bit indicates the full status of the generic command internal buffer. Value After Reset: 0x0
16	gen_buff_cmd_empty	R	This bit indicates the empty status of the generic command internal buffer. Value After Reset: 0x1
15	reserved_15	R	Reserved and read as zero. Value After Reset: 0x0
14	reserved_14	R	Reserved and read as zero Value After Reset: 0x0

Bits	Name	Memory Access	Description
13	reserved_13	R	Reserved and read as zero Value After Reset: 0x0
12	reserved_12	R	Reserved and read as zero Value After Reset: 0x0
11	reserved_11	R	Reserved and read as zero Value After Reset: 0x0
10	reserved_10	R	Reserved and read as zero Value After Reset: 0x0
9	reserved_9	R	Reserved and read as zero Value After Reset: 0x0
8	reserved_8	R	Reserved and read as zero Value After Reset: 0x0
7	reserved_7	R	Reserved and read as zero. Value After Reset: 0x0
6	gen_rd_cmd_busy	R	This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO for GENERIC interface. Value After Reset: 0x0
5	gen_pld_r_full	R	This bit indicates the full status of the generic read payload FIFO. Value After Reset: 0x0
4	gen_pld_r_empty	R	This bit indicates the empty status of the generic read payload FIFO. Value After Reset: 0x1
3	gen_pld_w_full	R	This bit indicates the full status of the generic write payload FIFO. Value After Reset: 0x0
2	gen_pld_w_empty	R	This bit indicates the empty status of the generic write payload FIFO. Value After Reset: 0x1
1	gen_cmd_full	R	This bit indicates the full status of the generic command FIFO. Value After Reset: 0x0
0	gen_cmd_empty	R	This bit indicates the empty status of the generic command FIFO. Value After Reset: 0x1

### TO\_CNT\_CFG

**Name:** Timeout Trigger Configuration.

**Description:** Configures counters that trigger timeout errors. These are used to warn the system of a failure, through an interrupt, and restart the controller in case of unexpected situations that cause deadlock conditions.

**Size:** 32 bits

Offset: 0x78

Bits	Name	Memory Access	Description
31:16	hstx_to_cnt	R/W	This field configures the timeout counter that triggers a high-speed

Bits	Name	Memory Access	Description
			<p>transmission timeout contention detection (measured in TO_CLK_DIVISION cycles).</p> <p>If using non-burst mode and there is not sufficient time to switch from high-speed to low-power and back in the period which is from one line data finishing to the next line sync start, the DSI link returns low-power state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to satisfy the following formula: <math>hstx\_to\_cnt * lanebyteclkperiod * TO\_CLK\_DIVISION \geq \text{the time of one FRAME data transmission} * (1 + 10\%)</math></p> <p>In burst mode, RGB pixel packets are time-compressed, leaving more time during a scan line. So if in burst mode and there is sufficient time to switch from high-speed to low-power and back in the period of time from one line data finishing to the next line sync start, the DSI link can return low-power mode and back in this time interval to save power. If you choose so, you should configure the TO_CLK_DIVISION and hstx_to_cnt to satisfy the following formula: <math>hstx\_to\_cnt * lanebyteclkperiod * TO\_CLK\_DIVISION \geq \text{the time of one LINE data transmission} * (1 + 10\%)</math></p> <p>Value After Reset: 0x0</p>
15:0	lpxr_to_cnt	R/W	<p>This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles).</p> <p>Value After Reset: 0x0</p>

### HS\_RD\_TO\_CNT

**Name:** Peripheral timeout after HS read operations.

**Description:** Configures the Peripheral Response timeout after high-speed Read operations.

**Size:** 32 bits

**Offset:** 0x7c

Bits	Name	Memory Access	Description
31:16	reserved_31_16	R	<p>Reserved and read as zero.</p> <p>Value After Reset: 0x0</p>
15:0	hs_rd_to_cnt	R/W	<p>This field sets a period for which MIPI TX keeps the link still, after sending a high-speed Read operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts.</p> <p>Value After Reset: 0x0</p>

### LP\_RD\_TO\_CNT

**Name:** Peripheral timeout after LP read operations.

**Description:** Configures the Peripheral Response timeout after low-power Read operations.

**Size:** 32 bits

**Offset:** 0x80

Bits	Name	Memory Access	Description
31:16	reserved_31_16	R	<p>Reserved and read as zero.</p> <p>Value After Reset: 0x0</p>

Bits	Name	Memory Access	Description
15:0	lp_rd_to_cnt	R/W	This field sets a period for which MIPI TX keeps the link still, after sending a low-power Read operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Value After Reset: 0x0

### HS\_WR\_TO\_CNT

**Name:** Peripheral timeout after HS write operations.

**Description:** Configures the Peripheral Response timeout after high-speed Write operations.

**Size:** 32 bits

**Offset:** 0x84

Bits	Name	Memory Access	Description
31:25	reserved_31_25	R	Reserved and read as zero. Value After Reset: 0x0
24	reserved_24	R	Reserved and read as zero Value After Reset: 0x0
23:16	reserved_23_16	R	Reserved and read as zero. Value After Reset: 0x0
15:0	hs_wr_to_cnt	R/W	This field sets a period for which MIPI TX keeps the link still, after sending a high-speed Write operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Value After Reset: 0x0

### LP\_WR\_TO\_CNT

**Name:** Peripheral timeout after LP write operations.

**Description:** Configures the Peripheral Response timeout after low-power Write operations.

**Size:** 32 bits

**Offset:** 0x88

Bits	Name	Memory Access	Description
31:16	reserved_31_16	R	Reserved and read as zero. Value After Reset: 0x0
15:0	lp_wr_to_cnt	R/W	This field sets a period for which MIPI TX keeps the link still, after sending a low-power Write operation. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Value After Reset: 0x0

### BTA\_TO\_CNT

**Name:** Peripheral timeout after BTA completion.

**Description:** Configures the Peripheral Response timeout after Bus Turnaround completion.

**Size:** 32 bits

**Offset:** 0x8c

Bits	Name	Memory Access	Description
31:16	reserved_31_16	R	Reserved and read as zero. Value After Reset: 0x0
15:0	bta_to_cnt	R/W	This field sets a period for which MIPI TX keeps the link still, after completing a Bus Turnaround. This period is measured in cycles of lanebyteclk, starts to count when the D-PHY enters stop state and causes no interrupts. Value After Reset: 0x0

**SDF\_3D****Name:** 3D information for VSS packets.**Description:** Stores 3D control information for VSS packets in video mode.**Size:** 32 bits**Offset:** 0x90

Bits	Name	Memory Access	Description
31:17	reserved_31_17	R	Reserved and read as zero. Value After Reset: 0x0
16	send_3d_cfg	R/W	When set, causes the next VSS packet to include 3D control payload in every VSS packet. Value After Reset: 0x0
15:6	reserved_15_6	R	Reserved and read as zero. Value After Reset: 0x0
5	right_first	R/W	This bit defines the left/right order: Values: 0x0 (LFIRST): left eye is sent first, then right eye 0x1 (RFIRST): right eye data is sent first, then left eye Value After Reset: 0x0
4	second_vsync	R/W	This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: Values: 0x0 (NOSYNC): No sync pulses between left and right data 0x1 (SYNC): Sync pulse HSYNC, VSYNC, blanking between left and right data Value After Reset: 0x0
3:2	format_3d	R/W	This field defines 3D Image Format: Values: 0x0 (LINE): Alternating lines of left and right data 0x1 (FRAME): Alternating frames of left and right data 0x2 (PIXEL): Alternating pixels of left and right data 0x3 (RESERVED): Reserved, not used Value After Reset: 0x0
1:0	mode_3d	R/W	This field defines 3D Mode On/Off and Display Orientation: Values: 0x0 (MODE0): 3D Mode Off , 2D Mode On 0x1 (MODE1): 3D Mode On, Portrait Orientation 0x2 (MODE2): 3D Mode On, Landscape Orientation 0x3 (MODE3): Reserved, not used Value After Reset: 0x0

**LPCCLK\_CTRL****Name:** Non-continuous Clock configuration.**Description:** Configures the possibility for using non continuous clock in the clock lane.**Size:** 32 bits**Offset:** 0x94

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Bits	Name	Memory Access	Description
31:2	reserved_31_2	R	Reserved and read as zero. Value After Reset: 0x0
1	auto_clklane_ctrl	R/W	This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows. Value After Reset: 0x0
0	phy_txrequestclkhs	R/W	This bit controls the D-PHY PPI txrequestclkhs signal. Value After Reset: 0x0

**PHY\_TMR\_LPCCLK\_CFG****Name:** Time configuration for (clock lane) transitions between HS and LP.**Description:** Sets the time that MIPI TX assumes in calculations for the clock lane to switch between high-speed and low-power.**Size:** 32 bits**Offset:** 0x98

Bits	Name	Memory Access	Description
31:26	reserved_31_26	R	Reserved and read as zero. Value After Reset: 0x0
25:16	phy_clkhs2lp_time	R/W	This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles. Value After Reset: 0x0
15:10	reserved_15_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	phy_clklp2hs_time	R/W	This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles. Value After Reset: 0x0

**PHY\_TMR\_CFG****Name:** Time configuration for (data lanes) transitions between HS and LP.**Description:** Sets the time that MIPI TX assumes in calculations for the data lanes to switch between high-speed and low-power.**Size:** 32 bits**Offset:** 0x9c

Bits	Name	Memory Access	Description
31:26	reserved_31_26	R	Reserved and read as zero.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
25:16	phy_hs2lp_time	R/W	This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles. Value After Reset: 0x0
15:10	reserved_15_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	phy_lp2hs_time	R/W	This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles. Value After Reset: 0x0

### PHY\_RSTZ

**Name:** D-PHY's PLL and Resets.

**Description:** Controls resets and the PLL of the D-PHY.

**Size:** 32 bits

**Offset:** 0xa0

Bits	Name	Memory Access	Description
31:4	reserved_31_4	R	Reserved and read as zero. Value After Reset: 0x0
3	phy_forcepll	R/W	When the D-PHY is in ULPS, this bit enables the D-PHY PLL. Value After Reset: 0x0
2	phy_enableclk	R/W	When set to 1, this bit enables the D-PHY Clock Lane Module. Value After Reset: 0x0
1	phy_rstz	R/W	When set to 0, this bit places the digital section of the D-PHY in the reset state. Value After Reset: 0x0
0	phy_shutdownz	R/W	When set to 0, this bit places the complete D-PHY macro in power-down state. Value After Reset: 0x0

### PHY\_IF\_CFG

**Name:** Active lanes and Stop State minimum time in Stop State.

**Description:** Configures the number of active lanes and the minimum time to remain in stop state.

**Size:** 32 bits

**Offset:** 0xa4

Bits	Name	Memory Access	Description
31:16	reserved_31_16	R	Reserved and read as zero. Value After Reset: 0x0
15:8	phy_stop_wait_time	R/W	This field configures the minimum time PHY needs to stay in StopState before requesting an high-speed transmission Value After Reset: 0x0
7:2	reserved_7_2	R	Reserved and read as zero.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
1:0	n_lanes	R/W	<p>This field configures the number of active data lanes:</p> <p>Values:</p> <ul style="list-style-type: none"> <li>0x0 (ONELANES): lane 0</li> <li>0x1 (TWOLANES): lanes 0 and 1</li> <li>0x2 (THREELANES): lanes 0, 1, and 2</li> <li>0x3 (FOURLANES): lanes 0, 1, 2, and 3</li> </ul> <p>Value After Reset: 0x3</p>

### PHY\_ULPS\_CTRL

**Name:** Transitions from and to ULPS, using D-PHY.

**Description:** Configures entering and leaving ULPS in the D-PHY.

**Size:** 32 bits

**Offset:** 0xa8

Bits	Name	Memory Access	Description
31:4	reserved_31_4	R	<p>Reserved and read as zero.</p> <p>Value After Reset: 0x0</p>
3	phy_txexitulpslan	R/W	<p>ULPS mode Exit on all active data lanes.</p> <p>Value After Reset: 0x0</p>
2	phy_txrequlpslan	R/W	<p>ULPS mode Request on all active data lanes.</p> <p>Value After Reset: 0x0</p>
1	phy_txexitulpsclk	R/W	<p>ULPS mode Exit on clock lane.</p> <p>Value After Reset: 0x0</p>
0	phy_txrequlpsclk	R/W	<p>ULPS mode Request on clock lane.</p> <p>Value After Reset: 0x0</p>

### PHY\_TX\_TRIGGER

**Name:** Pins related to D-PHY triggers.

**Description:** Configures the pins that activate triggers in the D-PHY.

**Size:** 32 bits

**Offset:** 0xac

Bits	Name	Memory Access	Description
31:4	reserved_31_4	R	<p>Reserved and read as zero.</p> <p>Value After Reset: 0x0</p>
3:0	phy_tx_triggers	R/W	<p>This field controls the trigger transmissions.</p> <p>Value After Reset: 0x0</p>

### PHY\_STATUS

**Name:** D-PHY Status.

**Description:** Contains information about the status of the D-PHY.

**Size:** 32 bits

**Offset:** 0xb0

Bits	Name	Memory Access	Description
31:13	reserved_31_13	R	Reserved and read as zero. Value After Reset: 0x0
12	phy_ulpsactivenot3lane	R	This bit indicates the status of ulpsactivenot3lane D-PHY signal. Value After Reset: 0x1 Testable: untestable Volatile: true
11	phy_stopstate3lane	R	This bit indicates the status of phy_stopstate3lane D-PHY signal. Value After Reset: 0x0
10	phy_ulpsactivenot2lane	R	This bit indicates the status of ulpsactivenot2lane D-PHY signal. Value After Reset: 0x1 Testable: untestable Volatile: true
9	phy_stopstate2lane	R	This bit indicates the status of phy_stopstate2lane D-PHY signal. Value After Reset: 0x0
8	phy_ulpsactivenot1lane	R	This bit indicates the status of ulpsactivenot1lane D-PHY signal. Value After Reset: 0x1 Testable: untestable Volatile: true
7	phy_stopstate1lane	R	This bit indicates the status of phy_stopstate1lane D-PHY signal. Value After Reset: 0x0
6	phy_rxulpsesc0lane	R	This bit indicates the status of rxulpsesc0lane D-PHY signal. Value After Reset: 0x1
5	phy_ulpsactivenot0lane	R	This bit indicates the status of ulpsactivenot0lane D-PHY signal. Value After Reset: 0x0 Testable: untestable Volatile: true
4	phy_stopstate0lane	R	This bit indicates the status of phy_stopstate0lane D-PHY signal. Value After Reset: 0x0
3	phy_ulpsactivenotclk	R	This bit indicates the status of phyulpsactivenotclk D-PHY signal. Value After Reset: 0x0
2	phy_stopstateclklane	R	This bit indicates the status of phy_stopstateclklane D-PHY signal. Value After Reset: 0x0
1	phy_direction	R	This bit indicates the status of phydirection D-PHY signal. Value After Reset: 0x0
0	phy_lock	R	This bit indicates the status of phylock D-PHY signal. Value After Reset: 0x0

**PHY\_TST\_CTRL0****Name:** D-PHY control and clear pins.**Description:** Controls clock and clear pins of the D-PHY vendor specific interface.**Size:** 32 bits**Offset:** 0xb4

Bits	Name	Memory Access	Description
31:2	reserved_31_2	R	Reserved and read as zero. Value After Reset: 0x0
1	phy_testclk	R/W	This bit is used to clock the TESTDIN bus into the D-PHY. Value After Reset: 0x0
0	phy_testclr	R/W	PHY test interface clear (active high). Value After Reset: 0x1

**PHY\_TST\_CTRL1****Name:** D-PHY data and enable pins.**Description:** Controls data and enable pins of the D-PHY vendor specific interface.**Size:** 32 bits**Offset:** 0xb8

Bits	Name	Memory Access	Description
31:18	reserved_31_18	R	Reserved and read as zero. Value After Reset: 0x0
17	phy_testsel	R/W	PHY BiDIR MUX selector Value After Reset: 0x0
16	phy_testen	R/W	PHY test interface operation selector: Values: 0x1 (WRITEADDR): the address write operation is set on the falling edge of the testclk signal. 0x0 (WRITEDATA): the data write operation is set on the rising edge of the testclk signal. Value After Reset: 0x0
15:8	pht_testdout	R	PHY output 8-bit data bus for read-back and internal probing functionalities. Value After Reset: 0x0
7:0	phy_testdin	R/W	PHY test interface input 8-bit data bus for internal register programming and test functionalities access. Value After Reset: 0x0

**INT\_ST0****Name:** Interrupts status 0.**Description:** Contains the status of interrupt sources from acknowledge reports and the D-PHY.**Size:** 32 bits**Offset:** 0xbc

Bits	Name	Memory Access	Description
31:21	reserved_31_21	R	Reserved and read as zero. Value After Reset: 0x0

Bits	Name	Memory Access	Description
20	dphy_errors_4	RC	This bit indicates LP1 contention error ErrContentionLP1 from Lane 0. Value After Reset: 0x0
19	dphy_errors_3	RC	This bit indicates LP0 contention error ErrContentionLP0 from Lane 0. Value After Reset: 0x0
18	dphy_errors_2	RC	This bit indicates control error ErrControl from Lane 0. Value After Reset: 0x0
17	dphy_errors_1	RC	This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0. Value After Reset: 0x0
16	dphy_errors_0	RC	This bit indicates ErrEsc escape entry error from Lane 0. Value After Reset: 0x0
15	ack_with_err_15	RC	This bit retrieves the DSI protocol violation from the Acknowledge error report. Value After Reset: 0x0
14	ack_with_err_14	RC	This bit retrieves the reserved (specific to device) from the Acknowledge error report. Value After Reset: 0x0
13	ack_with_err_13	RC	This bit retrieves the invalid transmission length from the Acknowledge error report. Value After Reset: 0x0
12	ack_with_err_12	RC	This bit retrieves the DSI VC ID Invalid from the Acknowledge error report. Value After Reset: 0x0
11	ack_with_err_11	RC	This bit retrieves the not recognized DSI data type from the Acknowledge error report. Value After Reset: 0x0
10	ack_with_err_10	RC	This bit retrieves the checksum error (long packet only) from the Acknowledge error report. Value After Reset: 0x0
9	ack_with_err_9	RC	This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report. Value After Reset: 0x0
8	ack_with_err_8	RC	This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report. Value After Reset: 0x0
7	ack_with_err_7	RC	This bit retrieves the Contention Detected error from the Acknowledge error report. Value After Reset: 0x0
6	ack_with_err_6	RC	This bit retrieves the False Control error from the Acknowledge error report. Value After Reset: 0x0
5	ack_with_err_5	RC	This bit retrieves the Peripheral Timeout error from the Acknowledge error report. Value After Reset: 0x0
4	ack_with_err_4	RC	This bit retrieves the low-power Transmit Sync error from the Acknowledge error report.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
3	ack_with_err_3	RC	This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report. Value After Reset: 0x0
2	ack_with_err_2	RC	This bit retrieves the EoT Sync error from the Acknowledge error report. Value After Reset: 0x0
1	ack_with_err_1	RC	This bit retrieves the SoT Sync error from the Acknowledge error report. Value After Reset: 0x0
0	ack_with_err_0	RC	This bit retrieves the SoT error from the Acknowledge error report. Value After Reset: 0x0

**INT\_ST1****Name:** Interrupts Status 1.**Description:** Contains the status of interrupt sources related to timeouts, ECC, CRC, packet size, EoTp, Generic and DBI interfaces.**Size:** 32 bits

Offset: 0xc0

Bits	Name	Memory Access	Description
31:21	reserved_31_21	R	Reserved and read as zero. Value After Reset: 0x0
20	reserved_20	R	Reserved and read as zero Value After Reset: 0x0
19	dpi_buff_pld_under	RC	This bit indicates that an underflow has occurred when reading payload to build DSI packet for video mode Value After Reset: 0x0
18	reserved_18	R	Reserved and read as zero Value After Reset: 0x0
17	reserved_17	R	Reserved and read as zero Value After Reset: 0x0
16	reserved_16	R	Reserved and read as zero Value After Reset: 0x0
15	reserved_15	R	Reserved and read as zero Value After Reset: 0x0
14	reserved_14	R	Reserved and read as zero Value After Reset: 0x0
13	reserved_13	R	Reserved and read as zero Value After Reset: 0x0
12	gen_pld_recev_err	RC	This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted. Value After Reset: 0x0
11	gen_pld_rd_err	RC	This bit indicates that during a DCS read data, the payload

Bits	Name	Memory Access	Description
			FIFO becomes empty and the data sent to the interface is corrupted. Value After Reset: 0x0
10	gen_pld_send_err	RC	This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent. Value After Reset: 0x0
9	gen_pld_wr_err	RC	This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written. Value After Reset: 0x0
8	gen_cmd_wr_err	RC	This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written. Value After Reset: 0x0
7	dpi_pld_wr_err	RC	This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted. Value After Reset: 0x0
6	eopt_err	RC	This bit indicates that the EoTp packet has not been received at the end of the incoming peripheral transmission. Value After Reset: 0x0
5	pkt_size_err	RC	This bit indicates that the packet size error has been detected during the packet reception. Value After Reset: 0x0
4	crc_err	RC	This bit indicates that the CRC error has been detected in the received packet payload. Value After Reset: 0x0
3	ecc_multpl_err	RC	This bit indicates that the ECC multiple error has been detected in a received packet. Value After Reset: 0x0
2	ecc_single_err	RC	This bit indicates that the ECC single error has been detected and corrected in a received packet. Value After Reset: 0x0
1	to_lp_rx	RC	This bit indicates that the low-power reception timeout counter reached the end and contention has been detected. Value After Reset: 0x0
0	to_hs_tx	RC	This bit indicates that the high-speed transmission timeout counter reached the end and contention has been detected. Value After Reset: 0x0

## INT\_MSK0

**Name:** INT\_ST0 mask.

**Description:** Configures masks for the sources of interrupts that affect the INT\_ST0 register. Write 1 to un-mask each error report.

**Size:** 32 bits

**Offset:** 0xc4

Bits	Name	Memory Access	Description
31:21	reserved_31_21	R	Reserved and read as zero.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
20	mask_dphy_errors_4	R/W	Mask for dphy_errors_4 Value After Reset: 0x0
19	mask_dphy_errors_3	R/W	Mask for dphy_errors_3 Value After Reset: 0x0
18	mask_dphy_errors_2	R/W	Mask for dphy_errors_2 Value After Reset: 0x0
17	mask_dphy_errors_1	R/W	Mask for dphy_errors_1 Value After Reset: 0x0
16	mask_dphy_errors_0	R/W	Mask for dphy_errors_0 Value After Reset: 0x0
15	mask_ack_with_err_15	R/W	Mask for ack_with_err_15 Value After Reset: 0x0
14	mask_ack_with_err_14	R/W	Mask for ack_with_err_14 Value After Reset: 0x0
13	mask_ack_with_err_13	R/W	Mask for ack_with_err_13 Value After Reset: 0x0
12	mask_ack_with_err_12	R/W	Mask for ack_with_err_12 Value After Reset: 0x0
11	mask_ack_with_err_11	R/W	Mask for ack_with_err_11 Value After Reset: 0x0
10	mask_ack_with_err_10	R/W	Mask for ack_with_err_10 Value After Reset: 0x0
9	mask_ack_with_err_9	R/W	Mask for ack_with_err_9 Value After Reset: 0x0
8	mask_ack_with_err_8	R/W	Mask for ack_with_err_8 Value After Reset: 0x0
7	mask_ack_with_err_7	R/W	Mask for ack_with_err_7 Value After Reset: 0x0
6	mask_ack_with_err_6	R/W	Mask for ack_with_err_6 Value After Reset: 0x0
5	mask_ack_with_err_5	R/W	Mask for ack_with_err_5 Value After Reset: 0x0
4	mask_ack_with_err_4	R/W	Mask for ack_with_err_4 Value After Reset: 0x0
3	mask_ack_with_err_3	R/W	Mask for ack_with_err_3 Value After Reset: 0x0
2	mask_ack_with_err_2	R/W	Mask for ack_with_err_2 Value After Reset: 0x0
1	mask_ack_with_err_1	R/W	Mask for ack_with_err_1 Value After Reset: 0x0
0	mask_ack_with_err_0	R/W	Mask for ack_with_err_0 Value After Reset: 0x0

**INT\_MSK1**

Name: INT\_ST1 mask.

**Description:** Configures masks for the sources of interrupts that affect the INT\_ST1 register.

**Size:** 32 bits

**Offset:** 0xc8

Bits	Name	Memory Access	Description
31:21	reserved_31_21	R	Reserved and read as zero. Value After Reset: 0x0
20	reserved_20	R	Reserved and read as zero Value After Reset: 0x0
19	mask_dpi_buff_pld_under	R/W	Mask for dpi_buff_pld_under Value After Reset: 0x0
18	reserved_18	R	Reserved and read as zero Value After Reset: 0x0
17	reserved_17	R	Reserved and read as zero Value After Reset: 0x0
16	reserved_16	R	Reserved and read as zero Value After Reset: 0x0
15	reserved_15	R	Reserved and read as zero Value After Reset: 0x0
14	reserved_14	R	Reserved and read as zero Value After Reset: 0x0
13	reserved_13	R	Reserved and read as zero Value After Reset: 0x0
12	mask_gen_pld_recev_err	R/W	Mask for gen_pld_recev_err Value After Reset: 0x0
11	mask_gen_pld_rd_err	R/W	Mask for gen_pld_rd_err Value After Reset: 0x0
10	mask_gen_pld_send_err	R/W	Mask for gen_pld_send_err Value After Reset: 0x0
9	mask_gen_pld_wr_err	R/W	Mask for gen_pld_wr_err Value After Reset: 0x0
8	mask_gen_cmd_wr_err	R/W	Mask for gen_cmd_wr_err Value After Reset: 0x0
7	mask_dpi_pld_wr_err	R/W	Mask for dpi_pld_wr_err Value After Reset: 0x0
6	mask_eopt_err	R/W	Mask for eopt_err Value After Reset: 0x0
5	mask_pkt_size_err	R/W	Mask for pkt_size_err Value After Reset: 0x0
4	mask_crc_err	R/W	Mask for crc_err Value After Reset: 0x0
3	mask_ecc_multpl_err	R/W	Mask for ecc_multpl_err Value After Reset: 0x0
2	mask_ecc_single_err	R/W	Mask for ecc_single_err Value After Reset: 0x0
1	mask_to_lp_rx	R/W	Mask for to_lp_rx Value After Reset: 0x0
0	mask_to_hs_tx	R/W	Mask for to_hs_tx

Bits	Name	Memory Access	Description
			Value After Reset: 0x0

### PHY\_CAL

**Name:** D-PHY skew calibration.

**Description:** Controls the skew calibration of D-PHY.

**Size:** 32 bits

**Offset:** 0xcc

Bits	Name	Memory Access	Description
31:1	reserved_31_1	R	Reserved and read as zero. Value After Reset: 0x0
0	txskewcalhs	R/W	High-speed skew calibration is started when txskewcalhs is set high (assuming that PHY is in Stop state). Value After Reset: 0x0

### INT\_FORCE0

**Name:** Force INT\_ST0

**Description:** Forces interrupt that affect the INT\_ST0 register.

**Size:** 32 bits

**Offset:** 0xd8

Bits	Name	Memory Access	Description
31:21	reserved_31_21	R	Reserved and read as zero. Value After Reset: 0x0
20	force_dphy_errors_4	R/W	Force dphy_errors_4 Value After Reset: 0x0
19	force_dphy_errors_3	R/W	Force dphy_errors_3 Value After Reset: 0x0
18	force_dphy_errors_2	R/W	Force dphy_errors_2 Value After Reset: 0x0
17	force_dphy_errors_1	R/W	Force dphy_errors_1 Value After Reset: 0x0
16	force_dphy_errors_0	R/W	Force dphy_errors_0 Value After Reset: 0x0
15	force_ack_with_err_15	R/W	Force ack_with_err_15 Value After Reset: 0x0
14	force_ack_with_err_14	R/W	Force ack_with_err_14 Value After Reset: 0x0
13	force_ack_with_err_13	R/W	Force ack_with_err_13 Value After Reset: 0x0
12	force_ack_with_err_12	R/W	Force ack_with_err_12 Value After Reset: 0x0
11	force_ack_with_err_11	R/W	Force ack_with_err_11 Value After Reset: 0x0
10	force_ack_with_err_10	R/W	Force ack_with_err_10 Value After Reset: 0x0

Bits	Name	Memory Access	Description
9	force_ack_with_err_9	R/W	Force ack_with_err_9 Value After Reset: 0x0
8	force_ack_with_err_8	R/W	Force ack_with_err_8 Value After Reset: 0x0
7	force_ack_with_err_7	R/W	Force ack_with_err_7 Value After Reset: 0x0
6	force_ack_with_err_6	R/W	Force ack_with_err_6 Value After Reset: 0x0
5	force_ack_with_err_5	R/W	Force ack_with_err_5 Value After Reset: 0x0
4	force_ack_with_err_4	R/W	Force ack_with_err_4 Value After Reset: 0x0
3	force_ack_with_err_3	R/W	Force ack_with_err_3 Value After Reset: 0x0
2	force_ack_with_err_2	R/W	Force ack_with_err_2 Value After Reset: 0x0
1	force_ack_with_err_1	R/W	Force ack_with_err_1 Value After Reset: 0x0
0	force_ack_with_err_0	R/W	Force ack_with_err_0 Value After Reset: 0x0

## INT\_FORCE1

**Name:** Force INT\_ST1.

**Description:** Forces interrupts that affect the INT\_ST1 register.

**Size:** 32 bits

**Offset:** 0xdc

Bits	Name	Memory Access	Description
31:21	reserved_31_21	R	Reserved and read as zero. Value After Reset: 0x0
20	reserved_20	R	Reserved and read as zero Value After Reset: 0x0
19	force_dpi_buff_pld_under	R/W	Force for dpi_buff_pld_under. Value After Reset: 0x0
18	reserved_18	R	Reserved and read as zero Value After Reset: 0x0
17	reserved_17	R	Reserved and read as zero Value After Reset: 0x0
16	reserved_16	R	Reserved and read as zero Value After Reset: 0x0
15	reserved_15	R	Reserved and read as zero Value After Reset: 0x0
14	reserved_14	R	Reserved and read as zero Value After Reset: 0x0
13	reserved_13	R	Reserved and read as zero Value After Reset: 0x0
12	force_gen_pld_recev_err	R/W	Force gen_pld_recev_err

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
11	force_gen_pld_rd_err	R/W	Force gen_pld_rd_err Value After Reset: 0x0
10	force_gen_pld_send_err	R/W	Force gen_pld_send_err Value After Reset: 0x0
9	force_gen_pld_wr_err	R/W	Force gen_pld_wr_err Value After Reset: 0x0
8	force_gen_cmd_wr_err	R/W	Force gen_cmd_wr_err Value After Reset: 0x0
7	force_dpi_pld_wr_err	R/W	Force dpi_pld_wr_err Value After Reset: 0x0
6	force_eopt_err	R/W	Force eopt_err Value After Reset: 0x0
5	force_pkt_size_err	R/W	Force pkt_size_err Value After Reset: 0x0
4	force_crc_err	R/W	Force crc_err Value After Reset: 0x0
3	force_ecc_multpl_err	R/W	Force ecc_multpl_err Value After Reset: 0x0
2	force_ecc_single_err	R/W	Force ecc_single_err Value After Reset: 0x0
1	force_to_lp_rx	R/W	Force to_lp_rx Value After Reset: 0x0
0	force_to_hs_tx	R/W	Force to_hs_tx Value After Reset: 0x0

## DSC\_PARAMETER

**Name:** Display Stream Compression.

**Description:** Configures Display Stream Compression.

**Size:** 32 bits

**Offset:** 0xf0

Bits	Name	Memory Access	Description
31:18	reserved_31_18	R	Reserved and read as zero. Value After Reset: 0x0
17:16	pps_sel	R/W	This field indicates the PPS selector: Values: 0x0 (PPSSEL0): PPS Table 1 0x1 (PPSSEL1): PPS Table 2 0x2 (PPSSEL2): PPS Table 3 0x3 (PPSSEL3): PPS Table 4 Value After Reset: 0x0
15:10	reserved_15_10	R	Reserved and read as zero. Value After Reset: 0x0
9:8	compress_algo	R/W	This field indicates the algorithm identifier: Values: 0x0 (ALGO0): VESA DSC Standard 1.1 0x1 (ALGO1): reserved, not used

Bits	Name	Memory Access	Description
			0x2 (ALGO2): reserved, not used 0x3 (ALGO3): vendor-specific algorithm Value After Reset: 0x0
7:1	reserved_7_1	R	Reserved and read as zero. Value After Reset: 0x0
0	compression_mode	R/W	When set to 1, this bit enables the compression mode. Value After Reset: 0x0

### PHY\_TMR\_RD\_CFG

**Name:** PHY timings.

**Description:** Configures times related to PHY to perform some operations in lane byte clock cycles.

**Size:** 32 bits

**Offset:** 0xf4

Bits	Name	Memory Access	Description
31:15	reserved_31_15	R	Reserved and read as zero. Value After Reset: 0x0
14:0	max_rd_time	R/W	This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress. Value After Reset: 0x0

### VID\_SHADOW\_CTRL

**Name:** DPI Shadow Feature.

**Description:** Controls dpi shadow feature

**Size:** 32 bits

**Offset:** 0x100

Bits	Name	Memory Access	Description
31:17	reserved_31_17	R	Reserved and read as zero. Value After Reset: 0x0
16	vid_shadow_pin_req	R/W	When set to 1, the video request is done by external pin. In this mode vid_shadow_req is ignored. Value After Reset: 0x0
15:9	reserved_15_9	R	Reserved and read as zero. Value After Reset: 0x0
8	vid_shadow_req	R/W	When set to 1, this bit request that the dpi registers from regbank are copied to the auxiliary registers. When the request is completed this bit is auto clear. Value After Reset: 0x0
7:1	reserved_7_1	R	Reserved and read as zero. Value After Reset: 0x0
0	vid_shadow_en	R/W	When set to 1, DPI receives the active configuration from the auxiliary registers. When the feature is set at the same time than vid_shadow_req the auxiliary registers are automatically updated.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0

**DPI\_VCID\_ACT****Name:** Actual DPI Virtual Channel ID.**Description:** Holds the value that controller is using for DPI\_VCID.**Size:** 32 bits**Offset:** 0x10c

Bits	Name	Memory Access	Description
31:2	reserved_31_2	R	Reserved and read as zero. Value After Reset: 0x0
1:0	dpi_vcid	R	This field specifies the DPI virtual channel id that is indexed to the Video mode packets. Value After Reset: 0x0

**DPI\_COLOR\_CODING\_ACT****Name:** Actual DPI Color Coding**Description:** Holds the value that controller is using for DPI\_COLOR\_CODING.**Size:** 32 bits**Offset:** 0x110

Bits	Name	Memory Access	Description
31:9	reserved_31_9	R	Reserved and read as zero. Value After Reset: 0x0
8	loosely18_en	R	When 1, this bit activates loosely packed variant to 18-bit configurations. Value After Reset: 0x0
7:4	reserved_7_4	R	Reserved and read as zero. Value After Reset: 0x0
3:0	dpi_color_coding	R	This field configures the DPI color for Video Mode/eDPI Command Mode coding as follows: Values: 0x0 (CC00): 16-bit configuration 1 0x1 (CC01): 16-bit configuration 2 0x2 (CC02): 16-bit configuration 3 0x3 (CC03): 18-bit configuration 1 0x4 (CC04): 18-bit configuration 2 0x5 (CC05): 24-bit 0x6 (CC06): 20-bit YCbCr 4:2:2 loosely packed / Reserved for eDPI Command Mode 0x7 (CC07): 24-bit YCbCr 4:2:2 / Reserved for eDPI Command Mode 0x8 (CC08): 16-bit YCbCr 4:2:2 / Reserved for eDPI Command Mode 0x9 (CC09): 30-bit - DSC_ENC 10bit / Reserved for eDPI Command Mode 0xa (CC10): 36-bit / Reserved for eDPI Command Mode

Bits	Name	Memory Access	Description
			0xb (CC11): 12-bit YCbCr 4:2:0 / Reserved for eDPI Command Mode 0xc (CC12): DSC24 compressed Data 0xd (CC13): Reserved 0xe (CC14): Reserved 0xf (CC15): Reserved Value After Reset: 0x0

**DPI\_LP\_CMD\_TIM\_ACT****Name:** Actual DPI Low Power Commands' Timing.**Description:** Holds the value that controller is using for DPI\_LP\_CMD\_TIM.**Size:** 32 bits**Offset:** 0x118

Bits	Name	Memory Access	Description
31:24	reserved_31_24	R	Reserved and read as zero. Value After Reset: 0x0
23:16	outvact_lpcmd_time	R	This field is used for the transmission of commands in low-power mode. It specifies the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions. Value After Reset: 0x0
15:8	reserved_15_8	R	Reserved and read as zero. Value After Reset: 0x0
7:0	invact_lpcmd_time	R	This field is used for the transmission of commands in low-power mode. It specifies the size, in bytes, of the largest packet that can fit in a line during the VACT region. Value After Reset: 0x0

**VID\_MODE\_CFG\_ACT****Name:** VID\_MODE\_CFG.**Description:** Holds the value that controller is using for VID\_MODE\_CFG.**Size:** 32 bits**Offset:** 0x138

Bits	Name	Memory Access	Description
31:10	reserved_31_10	R	Reserved and read as zero. Value After Reset: 0x0
9	lp_cmd_en	R	When 1, this bit enables the command transmission only in low-power mode. Value After Reset: 0x0
8	frame_bta_ack_en	R	When 1, this bit enables the request for an acknowledge response at the end of a frame. Value After Reset: 0x0
7	lp_hfp_en	R	When 1, this bit enables the return to low-power inside the HFP period when timing allows.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
6	lp_hbp_en	R	When 1, this bit enables the return to low-power inside the HBP period when timing allows. Value After Reset: 0x0
5	lp_vact_en	R	When 1, this bit enables the return to low-power inside the VACT period when timing allows. Value After Reset: 0x0
4	lp_vfp_en	R	When 1, this bit enables the return to low-power inside the VFP period when timing allows. Value After Reset: 0x0
3	lp_vbp_en	R	When 1, this bit enables the return to low-power inside the VBP period when timing allows. Value After Reset: 0x0
2	lp_vsa_en	R	When 1, this bit enables the return to low-power inside the VSA period when timing allows. Value After Reset: 0x0
1:0	vid_mode_type	R	This field specifies the video mode transmission type as follows: Values: 0x0 (VIDMODE0): Non-burst with sync pulses 0x1 (VIDMODE1): Non-burst with sync events 0x2 (VIDMODE2): Burst mode 0x3 (VIDMODE3): Burst mode Value After Reset: 0x0

### VID\_PKT\_SIZE\_ACT

**Name:** Actual VID\_PKT\_SIZE.

**Description:** Holds the value that controller is using for VID\_PKT\_SIZE.

**Size:** 32 bits

**Offset:** 0x13c

Bits	Name	Memory Access	Description
31:14	reserved_31_14	R	Reserved and read as zero. Value After Reset: 0x0
13:0	vid_pkt_size	R	This field specifies the number of pixels in a single video packet. For 18-bit not loosely packed this number must be a multiple of 4 and YCbCr Data Types, it must be a multiple of 2, as described in DSI specification. Value After Reset: 0x0

### VID\_NUM\_CHUNKS\_ACT

**Name:** Actual VID\_NUM\_CHUNKS.

**Description:** This register holds the value that controller is using for VID\_NUM\_CHUNKS.

**Size:** 32 bits

**Offset:** 0x140

Bits	Name	Memory Access	Description
31:13	reserved_31_13	R	Reserved and read as zero. Value After Reset: 0x0
12:0	vid_num_chunks	R	This register specifies the number of chunks to be transmitted during a Line period (a chunk is pair made of a video packet and a null packet). If set to 0 or 1, video line is still transmitted in a single packet. If set to 1 that packet is part of a chunk, meaning that a null packet follows it (if vid_null_size>0). Otherwise, multiple chunks are used to transmit each video line. Value After Reset: 0x0

#### VID\_NULL\_SIZE\_ACT

**Name:** Actual VID\_NULL\_SIZE.

**Description:** Holds the value that controller is using for VID\_NULL\_SIZE.

**Size:** 32 bits

**Offset:** 0x144

Bits	Name	Memory Access	Description
31:13	reserved_31_13	R	Reserved and read as zero. Value After Reset: 0x0
12:0	vid_null_size	R	This register specifies the number of bytes inside a null packet. Setting to 0 disables null packets. Value After Reset: 0x0

#### VID\_HSA\_TIME\_ACT

**Name:** Actual VID\_HSA\_TIME.

**Description:** Holds the value that controller is using for VID\_HSA\_TIME.

**Size:** 32 bits

**Offset:** 0x148

Bits	Name	Memory Access	Description
31:12	reserved_31_12	R	Reserved and read as zero. Value After Reset: 0x0
11:0	vid_hsa_time	R	This field specifies the Horizontal Synchronism Active period in lane byte clock cycles. Value After Reset: 0x0

#### VID\_HBP\_TIME\_ACT

**Name:** Actual VID\_HBP\_TIME.

**Description:** Holds the value that controller is using for VID\_HBP\_TIME.

**Size:** 32 bits

**Offset:** 0x14c

Bits	Name	Memory Access	Description
31:12	reserved_31_12	R	Reserved and read as zero.

Bits	Name	Memory Access	Description
			Value After Reset: 0x0
11:0	vid_hbp_time	R	This field specifies the Horizontal Back Porch period in lane byte clock cycles. Value After Reset: 0x0

**VID\_HLINE\_TIME\_ACT****Name:** Actual VID\_HLINE\_TIME.**Description:** Holds the value that controller is using for VID\_HLINE\_TIME.**Size:** 32 bits**Offset:** 0x150

Bits	Name	Memory Access	Description
31:15	reserved_31_15	R	Reserved and read as zero. Value After Reset: 0x0
14:0	vid_hline_time	R	This field specifies the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles. Value After Reset: 0x0

**VID\_VSA\_LINES\_ACT****Name:** Actual VID\_VSA\_LINES.**Description:** Holds the value that controller is using for VID\_VSA\_LINES.**Size:** 32 bits**Offset:** 0x154

Bits	Name	Memory Access	Description
31:10	reserved_31_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	vsa_lines	R	This field specifies the Vertical Synchronism Active period measured in number of horizontal lines. Value After Reset: 0x0

**VID\_VBP\_LINES\_ACT****Name:** VID\_VBP\_LINES.**Description:** Holds the value that controller is using for VID\_VBP\_LINES.**Size:** 32 bits**Offset:** 0x158

Bits	Name	Memory Access	Description
31:10	reserved_31_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	vbp_lines	R	This field specifies the Vertical Back Porch period measured in number of horizontal lines. Value After Reset: 0x0

**VID\_VFP\_LINES\_ACT****Name:** Actual VID\_VFP\_LINES.**Description:** Holds the value that controller is using for VID\_VFP\_LINES.**Size:** 32 bits**Offset:** 0x15c

Bits	Name	Memory Access	Description
31:10	reserved_31_10	R	Reserved and read as zero. Value After Reset: 0x0
9:0	vfp_lines	R	This field specifies the Vertical Front Porch period measured in number of horizontal lines. Value After Reset: 0x0

**VID\_VACTIVE\_LINES\_ACT****Name:** Actual VID\_VACTIVE\_LINES.**Description:** Holds the value that controller is using for VID\_VACTIVE\_LINES.**Size:** 32 bits**Offset:** 0x160

Bits	Name	Memory Access	Description
31:14	reserved_31_14	R	Reserved and read as zero. Value After Reset: 0x0
13:0	v_active_lines	R	This field specifies the Vertical Active period measured in number of horizontal lines. Value After Reset: 0x0

**VID\_PKT\_STATUS****Name:** eDPI and DPI FIFOs status.**Description:** Contains information about the status of FIFOs related to DPI and eDPI interfaces.**Size:** 32 bits**Offset:** 0x168

Bits	Name	Memory Access	Description
31:24	reserved_31_24	R	Reserved and read as zero. Value After Reset: 0x0
23	reserved_23	R	Reserved and read as zero Value After Reset: 0x0
22	reserved_22	R	Reserved and read as zero Value After Reset: 0x0
21	reserved_21	R	Reserved and read as zero Value After Reset: 0x0
20	reserved_20	R	Reserved and read as zero Value After Reset: 0x0
19:18	reserved_19_18	R	Reserved and read as zero. Value After Reset: 0x0
17	dpi_buff_pld_full	R	This bit indicates the full status of the payload internal buffer

Bits	Name	Memory Access	Description
			for video Mode. This bit is set to 0 for command Mode. Value After Reset: 0x0
16	dpi_buff_pld_empty	R	This bit indicates the empty status of the payload internal buffer for video Mode. This bit is set to 0 for command Mode. Value After Reset: 0x1
15:8	reserved_15_8	R	Reserved and read as zero. Value After Reset: 0x0
7	reserved_7	R	Reserved and read as zero Value After Reset: 0x0
6	reserved_6	R	Reserved and read as zero Value After Reset: 0x0
5	reserved_5	R	Reserved and read as zero Value After Reset: 0x0
4	reserved_4	R	Reserved and read as zero Value After Reset: 0x0
3	dpi_pld_w_full	R	This bit indicates the full status of write payload FIFO for video Mode. This bit is set to 0 for command Mode. Value After Reset: 0x0
2	dpi_pld_w_empty	R	This bit indicates the empty status of write payload FIFO for video Mode. This bit is set to 0 for command Mode. Value After Reset: 0x1
1	dpi_cmd_w_full	R	This bit indicates the full status of write command FIFO for video Mode. This bit is set to 0 for command Mode. Value After Reset: 0x0
0	dpi_cmd_w_empty	R	This bit indicates the empty status of write command FIFO for video Mode. This bit is set to 0 for command Mode. Value After Reset: 0x1

### SDF\_3D\_ACT

**Name:** SDF\_3D.

**Description:** Holds the value that controller is using for SDF\_3D.

**Size:** 32 bits

**Offset:** 0x190

Bits	Name	Memory Access	Description
31:17	reserved_31_17	R	Reserved and read as zero. Value After Reset: 0x0
16	send_3d_cfg	R	When set, causes the next VSS packet to include 3D control payload in every VSS packet. Value After Reset: 0x0
15:6	reserved_15_6	R	Reserved and read as zero. Value After Reset: 0x0
5	right_first	R	This bit specifies the left/right order: Values: 0x0 (LEFTFIRST): left eye is sent first, then right eye 0x1 (RIGHTFIRST): right eye data is sent first, then left eye Value After Reset: 0x0

Bits	Name	Memory Access	Description
4	second_vsync	R	<p>This field specifies whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based:</p> <p>Values:</p> <ul style="list-style-type: none"> <li>0x0 (NOSYNCPULSE): No sync pulses between left and right data.</li> <li>0x1 (SYNCPULSE): Sync pulse (HSYNC, VSYNC, blanking) between left and right data.</li> </ul> <p>Value After Reset: 0x0</p>
3:2	format_3d	R	<p>This field specifies 3D Image Format:</p> <p>Values:</p> <ul style="list-style-type: none"> <li>0x0 (LINE): Alternating lines of left and right data</li> <li>0x1 (FRAME): Alternating frames of left and right data</li> <li>0x2 (PIXEL): Alternating pixels of left and right data</li> <li>0x3 (RESERVED): Reserved, not used</li> </ul> <p>Value After Reset: 0x0</p>
1:0	mode_3d	R	<p>This field specifies 3D Mode On/Off and Display Orientation:</p> <p>Values:</p> <ul style="list-style-type: none"> <li>0x0 (MODE0): 3D Mode Off, 2D Mode On</li> <li>0x1 (MODE1): 3D Mode On, Portrait Orientation</li> <li>0x2 (MODE2): 3D Mode On, Landscape Orientation</li> <li>0x3 (MODE3): Reserved, not used</li> </ul> <p>Value After Reset: 0x0</p>

### 9.3 HDMI

Please get in touch with ESWIN to request more detailed technical information.  
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