

EE312 Group Project

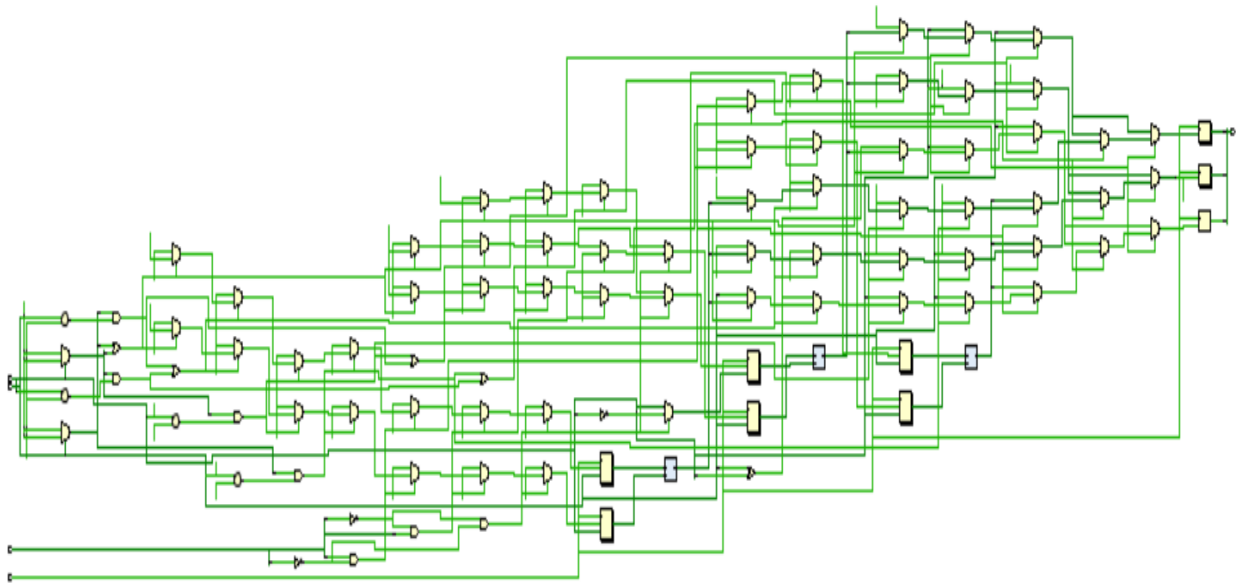
Sidharth Kumar - 190102076

Gandhi Siripuram - 190102077

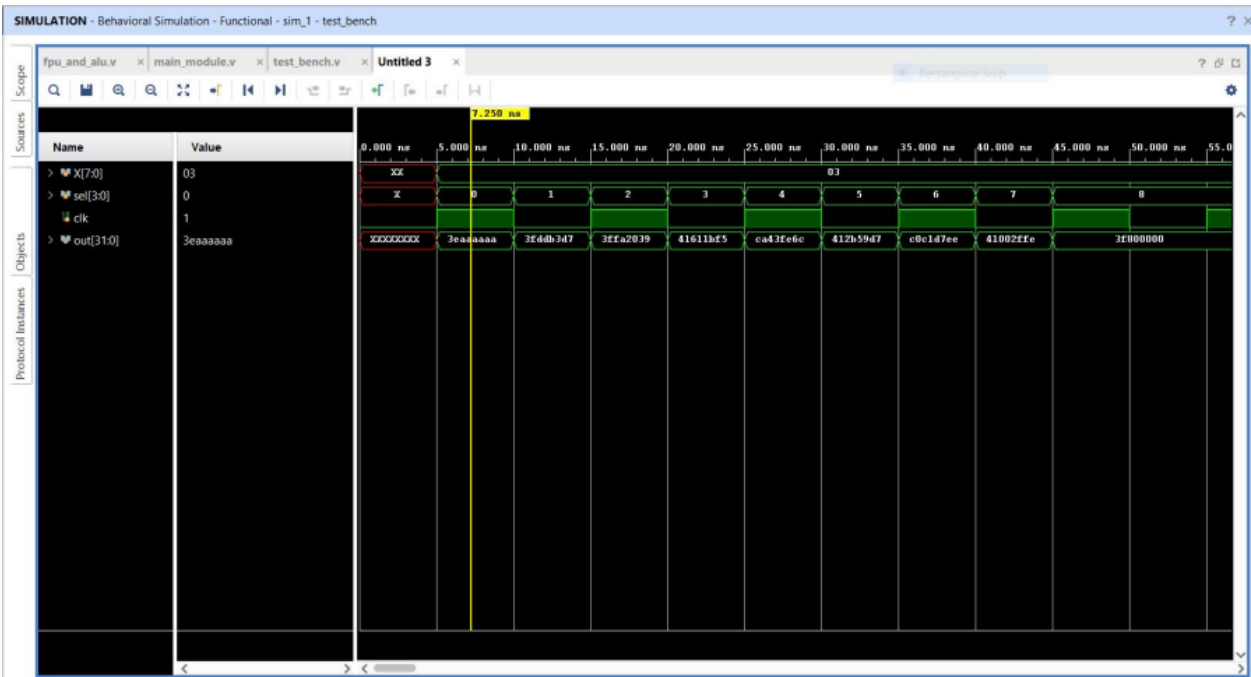
Sumit Choudhary - 190102078

Sumit Kumar Singh - 190102079

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1. Verilog Code For FPU and ALU and Main file have been submitted through ZIP Folder.
 2. Schematic:

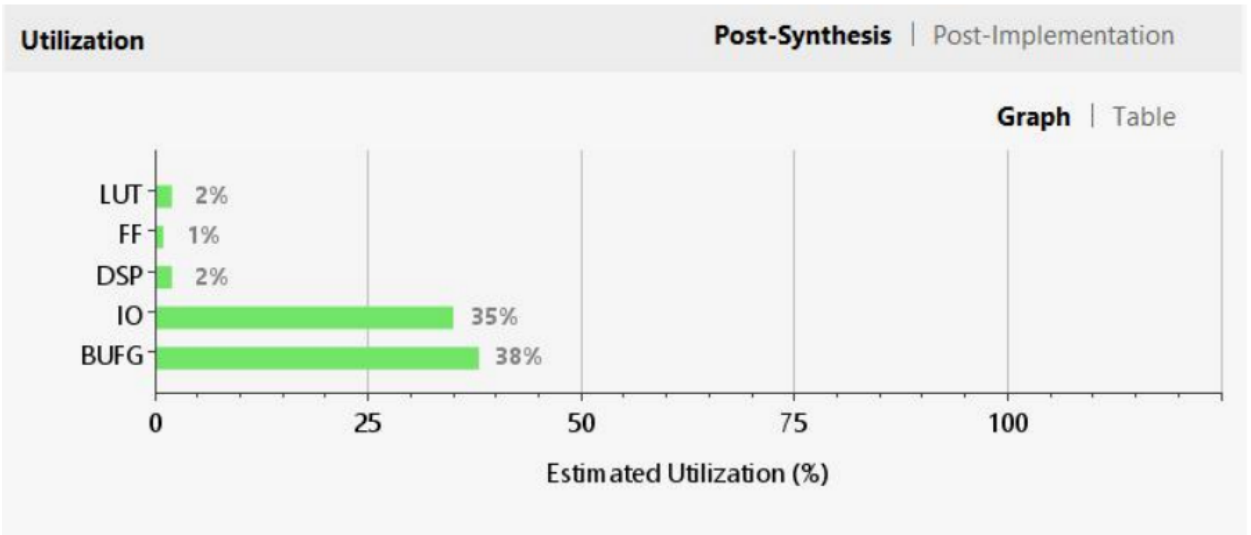


3. Behavioral Simulation Output Form:



4. Synthesis Report:

- Utilisation Summary:



- Power Summary:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: **64.959 W (Junction temp exceeded!)**

Design Power Budget: **Not Specified**

Power Budget Margin: **N/A**

Junction Temperature: **125.0°C**

Thermal Margin: **-155.3°C (-45.6 W)**

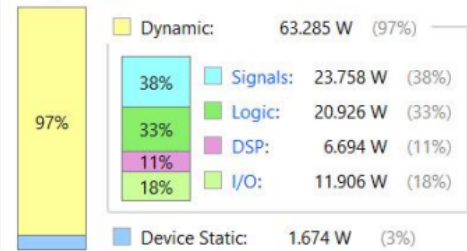
Effective θ_{JA} : **3.3°C/W**

Power supplied to off-chip devices: **0 W**

Confidence level: **Low**

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

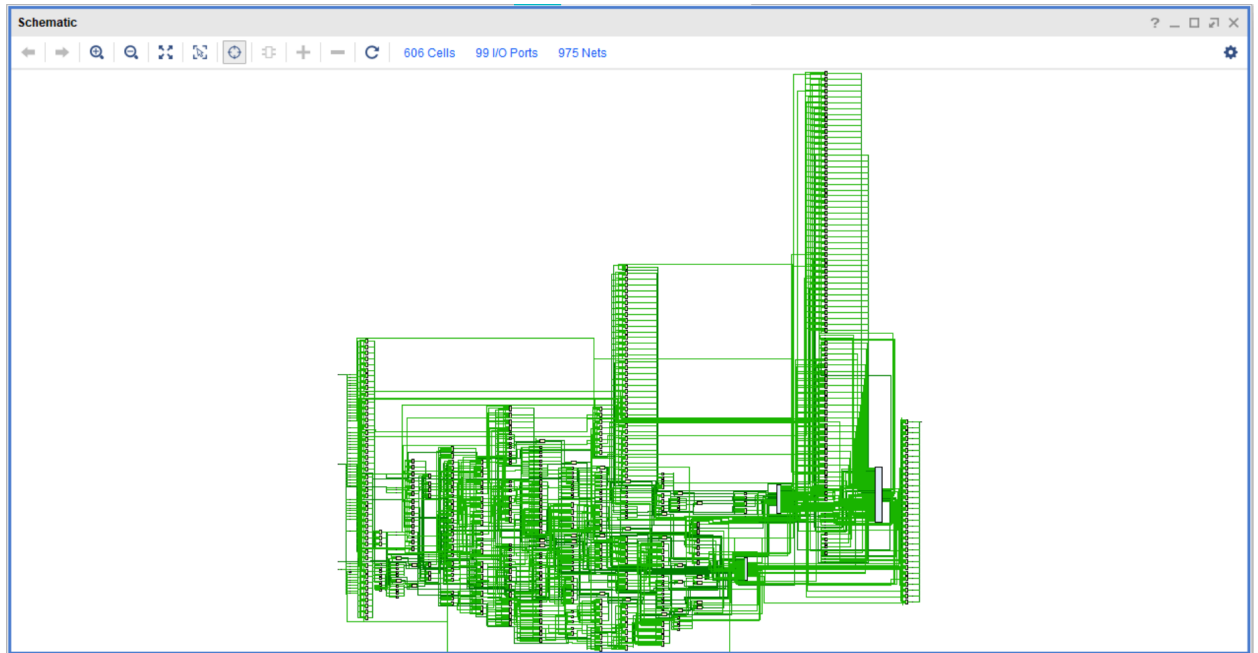
On-Chip Power



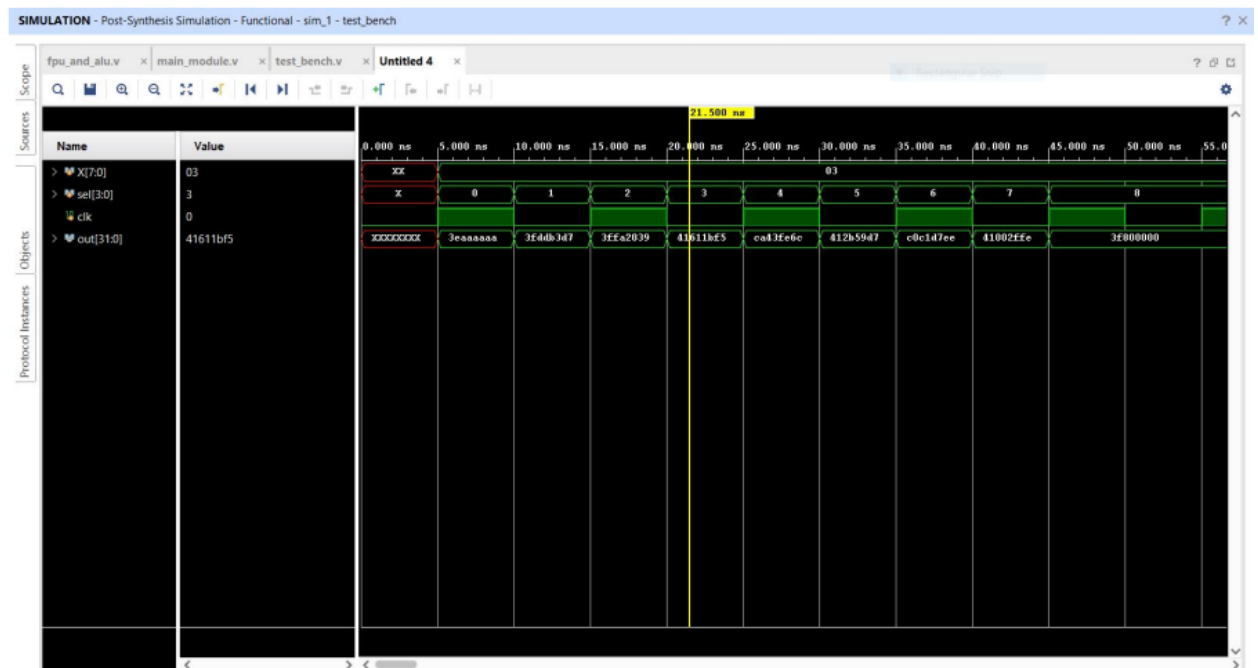
5. Timing Summary

Design Runs	Timing	Power	Utilization
Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 92.454 ns	Worst Hold Slack (WHS): 1.778 ns	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:	NA
Total Number of Endpoints: 1289	Total Number of Endpoints: 1289	Total Number of Endpoints:	
There are no user specified timing constraints.			

6. Schematic Diagram:

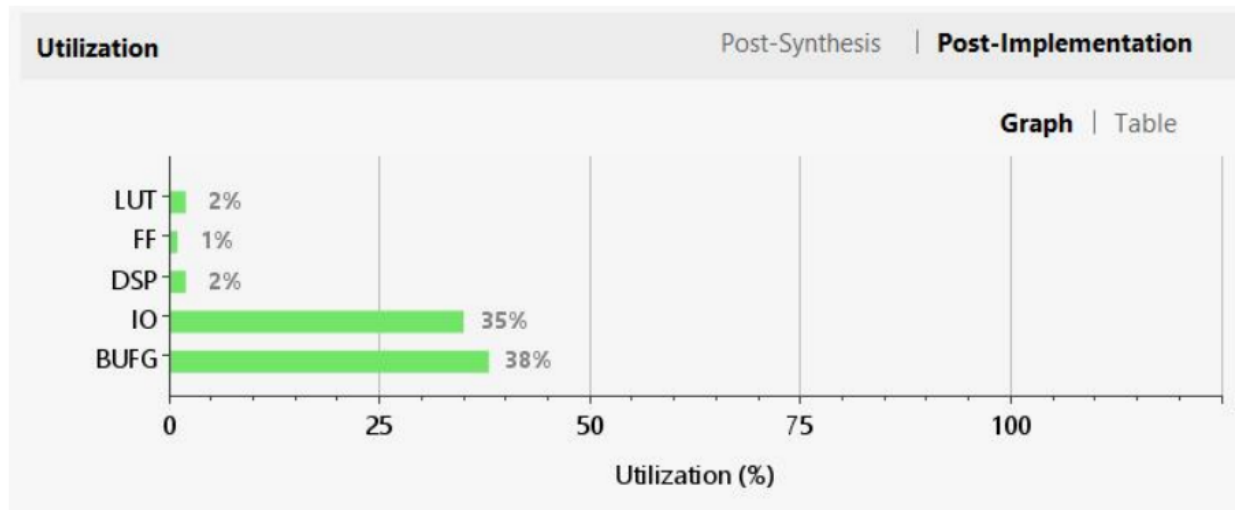


7. Post synthesis functional simulation output waveform



8. Implementation report

- Utilization summary:



- Power summary:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 64.959 W (Junction temp exceeded!)

Design Power Budget: Not Specified

Power Budget Margin: N/A

Junction Temperature: 125.0°C

Thermal Margin: -155.3°C (-45.6 W)

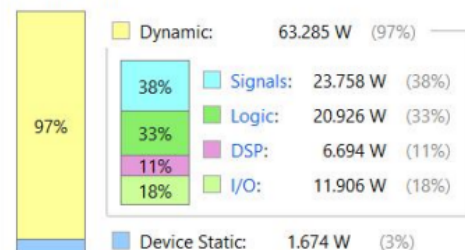
Effective θ_{JA} : 3.3°C/W

Power supplied to off-chip devices: 0 W

Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

On-Chip Power



- Timing report:

Design Timing Summary					
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS): 88.480 ns		Worst Hold Slack (WHS): 2.310 ns		Worst Pulse Width Slack (WPWS): NA	
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns		Total Pulse Width Negative Slack (TPWS): NA	
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0		Number of Failing Endpoints: NA	
Total Number of Endpoints: 16		Total Number of Endpoints: 16		Total Number of Endpoints: NA	
All user specified timing constraints are met.					

9. Post implementation functional simulation output waveform

