COMP ENG 2DX3
Pre-lab #2

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Q1) Starting with a truth table, design a 4-bit combinational digital lock that opens only when the parallel inputs are 1010. State the Boolean expression and draw the schematic for this combinational circuit. When the digital combinational lock is open, the output of the circuit should be a logic 1 to turn on an LED. The LED should remain off until the lock is opened. Flowcharts are useful to describe procedural steps in a simple system, such as this one. While not required for this question, consider how a flowchart would be written for your parallel digital lock.

Ans:

1)

inputs				output
a	b	c	d	x
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 1: Truth Table

boolean expression : $x = ab'cd'$

schematic :

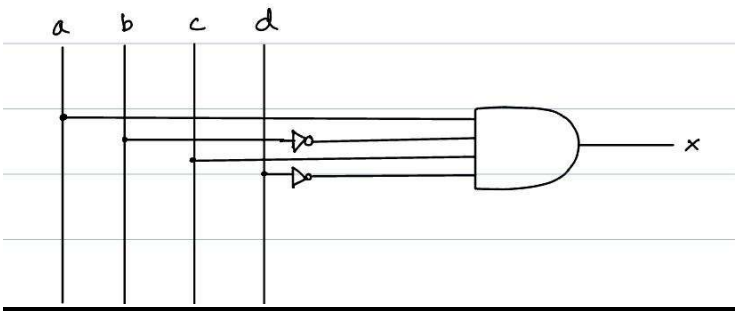

Figure 2: Schematic

Q2) A better way to describe a more complex system is to use a finite state machine (FSM). Using the FSM approach, show the design of a 4-bit digital lock that opens only when the 1-bit serial sequential input is entered as 1,0,1,1. When the digital lock is open, the output of the circuit should be a logic 1 to turn on an LED. When the input serial sequence fails, the design should reset to the initial state. The LED should remain off until the lock is opened. This question is only asking for the FSM - do not design the sequential circuit. Do not worry about microcontroller settings for this question. For simplicity you may assume a Moore implementation.

Ans:

States

- S_0 : locked
- S_1 : Intermediate State 1
- S_2 : Intermediate State 2
- S_3 : Intermediate State 3
- S_4 : Unlocked

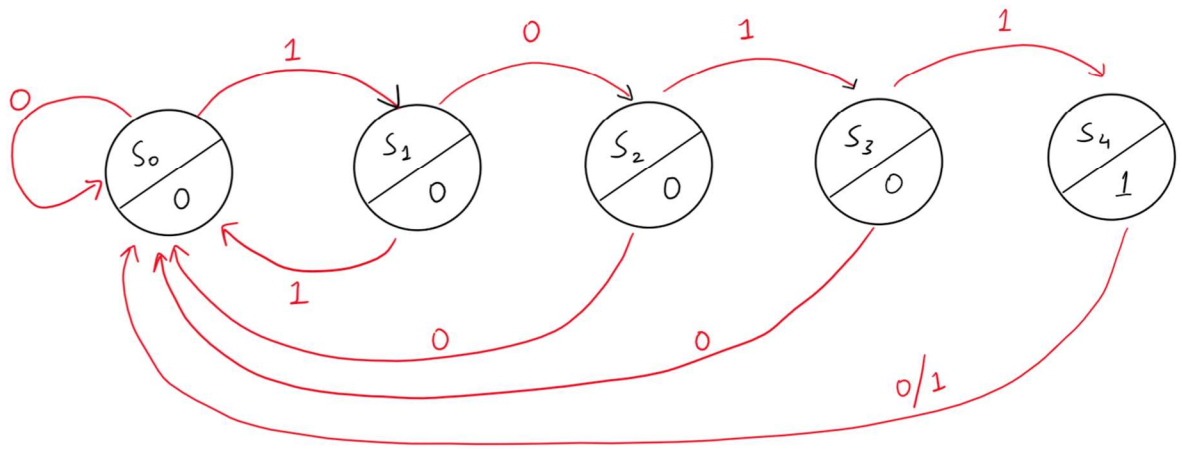

Figure 3: Finite State Machine Diagram