[](http://www.google.com/url?sa=i&rct=j&q=&esrc=s&source=images&cd=&cad=rja&uact=8&docid=33_BMtLTHQXQmM&tbnid=FdA9J51pxhxygM:&ved=0CAUQjRw&url=http://brandguide.tamu.edu/logos-downloads.html&ei=-fHgU_G5HOrl8gG1wIDYBQ&bvm=bv.72197243,d.b2U&psig=AFQjCNFDOGObFbXvp-YmH32j9zZ3RuFN8g&ust=1407337335725924)

**ECEN 684 INTERNSHIP REPORT**

**Last name: Sathyanarayana**

**First name: Ganesh Prabhu**

**UIN: 127004441**

**Date: 10/25/2018**

**Semester & year of internship: Summer 2018**

**Semester & year of expected graduation: Spring 2019**

**Degree program (M.Eng/MS/PhD): M.Eng**

**TAMU Advisor: Dr. Scott Miller**

**ECEN 684 section number, found on Howdy:**

**ECEN 684 - 526**

**TAMU Advisor’s email: smiller@tamu.edu**

About the Company:

Biotronik Inc. is a medical device company that provides solutions for cardiac rhythm management, electrophysiology and vascular intervention. Some of the devices that are developed include pacemakers, implantable defibrillators, remote-monitoring systems for patients, bio-monitors, and neuro-stimulator.

Internship Project: Verification of the digital control unit of a neuro-stimulator chip

Objective:

The objective here was to verify the complete functionality of the digital control unit and its interactions with the analog sensing and actuating unit. This was achieved by implementing test cases at the chip level that cover all functionality specified in the design specification at the inception of the design and also aiming for code coverage and toggle coverage of the design. In order to aid the speed of this process a test generating script was developed.

Background:

Neuro-stimulator provides therapy for chronic pain by delivering low voltage electricity to the peripheral nevres. It helps supress the pain by preventing the signals from reaching the brain. The function of the neuro stimulator can be broadly calssified into the analog section that senses and stimulates the peripheral nerves, and the digital section that controls the stimulating electrodes. The fugure below depicts the digital control block under verification. This block controls the type of therapy that can be provided based on the pulse train that deives the stimulation electrode.

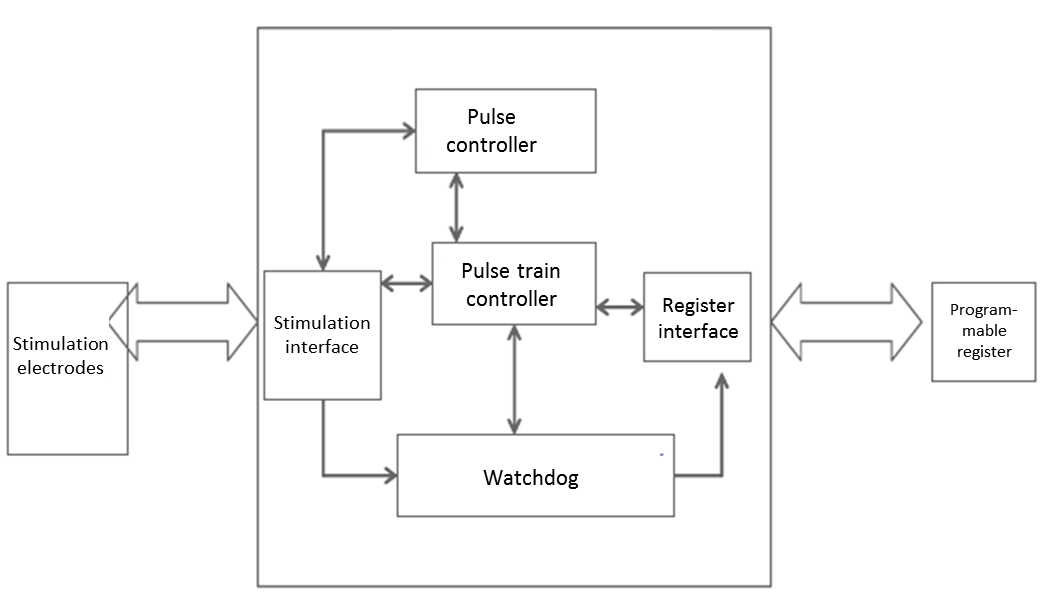


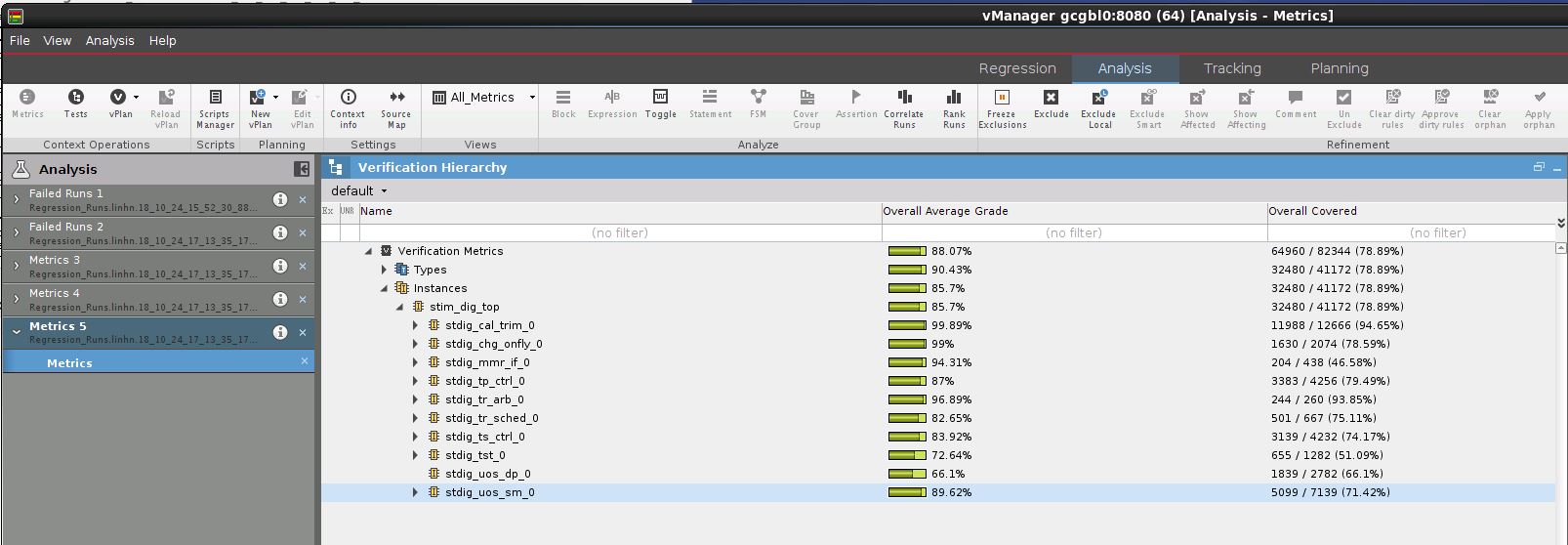
Figure 1: Stimulation control block

Tasks:

The verification process that was tasked follows a three step

The CLI was programmed in C#, it provides users options for different operations that can be performed and based on the operation sends commands and data to the processor and informs the user of a response from the processor. Figure 3 shows the interface.

The FPGA operates on 12MHz clock and this is divided into 1.5MHz and 32KHz and feeds into the IC. Figure 4 shows the FPGA design for the system.

**UART receivers and transmitters handle the UART protocol. They receive inputs from CLI and drive inputs to UART interface of IC and send responses from FPGA and the IC to the CLI. USB to IC controller receive commands from the CLI referring to the different operations that can be performed on the IC, based on which it performs the required procedure. Any data or command to or response from the processor is routed through an 8 byte-deep TX and RX FIFOs. In case of test IEGM interface command the data is stored in 16 byte-wide FIFO where each byte corresponds to each channel of the DMA. In the event that the FIFO is full the controller requests the data to be sent again. The FIFOs act as buffers between the PC and IC which operate at different speeds. The IEGM transmitter reads the data from the FIFO and converts it to the form as shown in the timing diagram in Figure 1.

Project Schedule:

|  |  |
| --- | --- |
| Week 1:   * Setting up workspace. * Reading training documents | Week 2:   * Getting acquainted with the design and verification environment * Reading training documents |
| Week 3:   * Training on Firmware * Understanding and modifying the firmware as required | Week 4:   * Reading simulation test cases * Designing IEGM Transmitter |
| Week 5:   * Designing the IEGM transmitter * Integrating FIFO design | Week 6:   * Designing the USB to IC controller * Running simulations and verification |
| Week 7:   * Designing the USB to IC controller * Running simulations and verification * High level design | Week 8:   * Programming FPGA with the design * CLI programming |
| Week 9:   * Adding features to CLI * Run the SVT and perform certain tests | Week 10:   * Modifications to CLI * Run the SVT and perform certain tests |

Project Evaluation (by Martin Li, Member of Technical Staff):

Ganesh completed this project professionally. The scope of the project involved multiple engineering disciplines including FPGA design/verification in Verilog, firmware development in C/assembly, software application development in C#. All of these tasks were not trivial even for a seasoned developer, but Ganesh was able to pick up these skills, completed all the assignments in a timely fashion, and handled them extremely well.

Most of the mistakes throughout the project he made were all due to the fact that he was not familiar with the full IC functionality, and this was fully understandable. Given his short 3-month of intern time, he was not given enough time to review and understand the full IC specification (which total span thousands of pages), and this was the only area that he required guidance and supervision heavily.

In general, Ganesh is a talented engineer, full of potential, and destined for great success in career.