ECE 319 Project Report

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Section: EM159

AIM:

BCD to Gray Code Converter.

Description:

1) The Most Significant Bit (MSB) of the gray code is always equal to the MSB of the given binary code.

Other bits of the output gray code can be obtained by XORing binary code bit at that index and previous index.

2) The Binary to Gray code converter is a logical circuit that is used to convert the binary code into its equivalent Gray code. By putting the MSB of 1 below the axis and the MSB of 1 above the axis and reflecting the (n-1) bit code about an axis after 2n-1 rows, we can obtain the n-bit gray code.

Circuit implementation:

Truth Table for BCD to Gray converter

Decimal Number	4-bit Binary Code				4-bit Gray Code			
	B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	1
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

K-Map:

k-map for G3

b1b0 / b3b2	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

G3= B3

.

k-map for G2

b1b0 / b3b2	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

G2= b2b3’+b3b2’

G2= b3$\oplus$b2

k-map for G1

b1b0 / b3b2	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

$G1 = b2b1' + b1b2'$

$G1 = b2 \oplus b1$

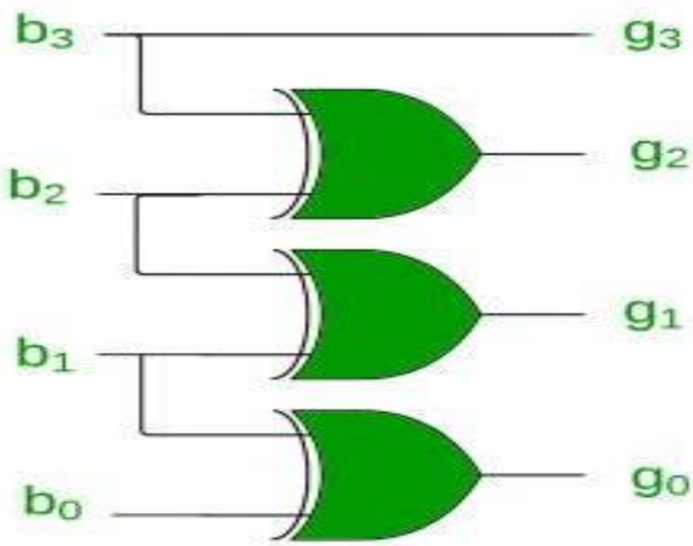
k-map for G0

b1b0 / b3b2	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$G0 = b0b1' + b1b0'$

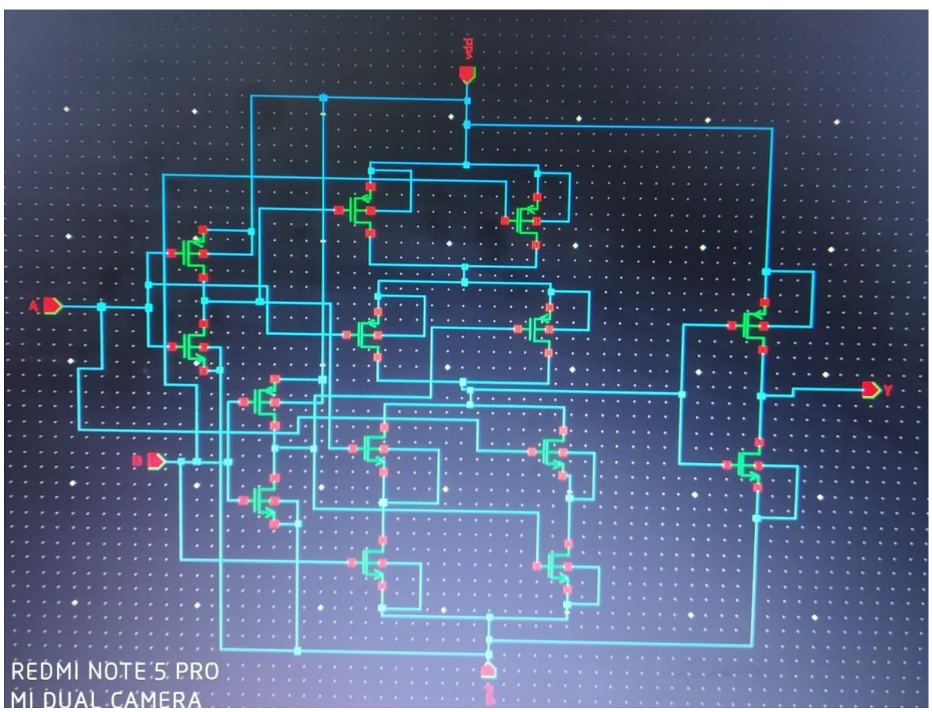
$G0 = b1 \oplus b0$

The corresponding digital circuit is

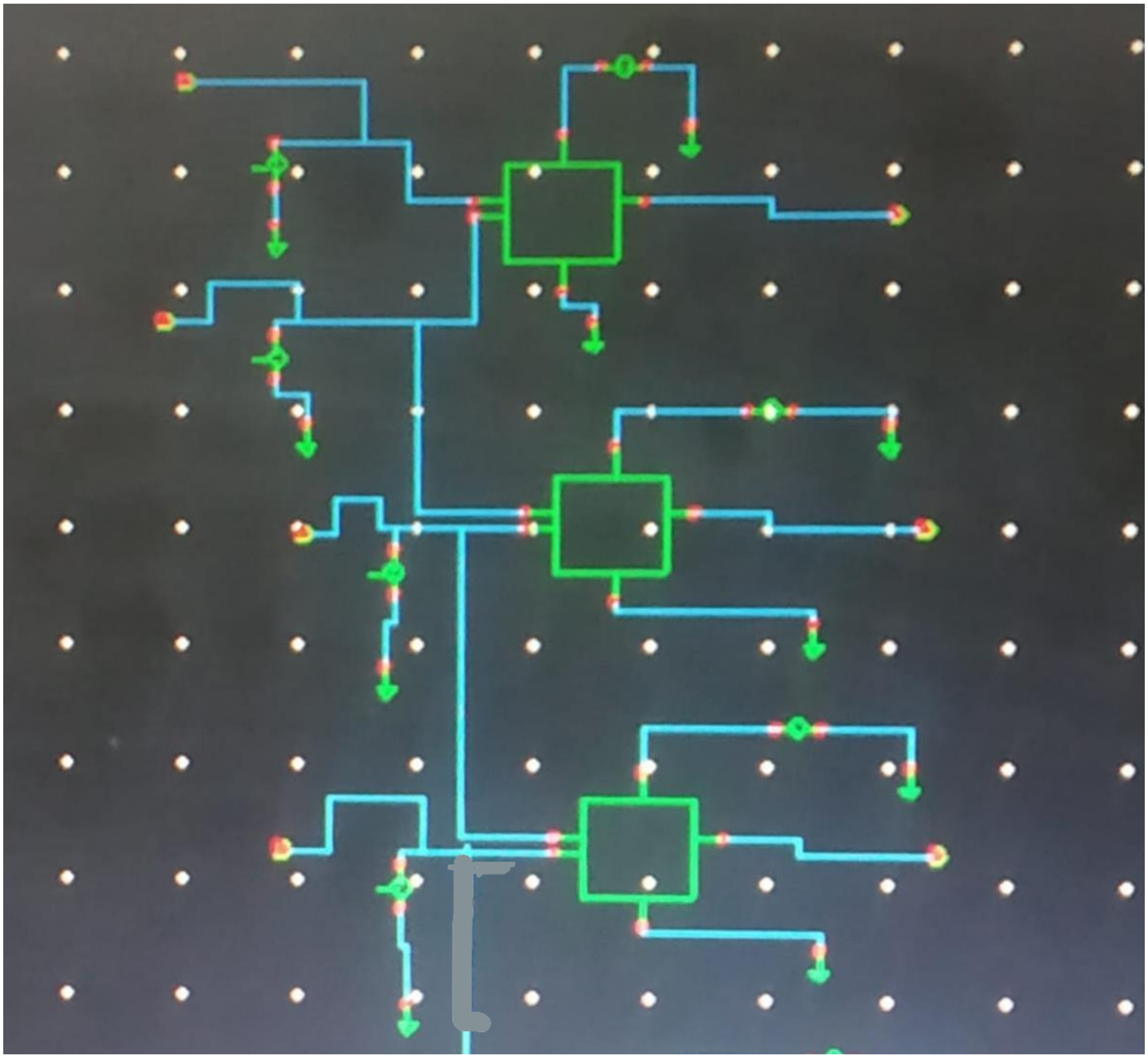


Schematic of EXOR Gate

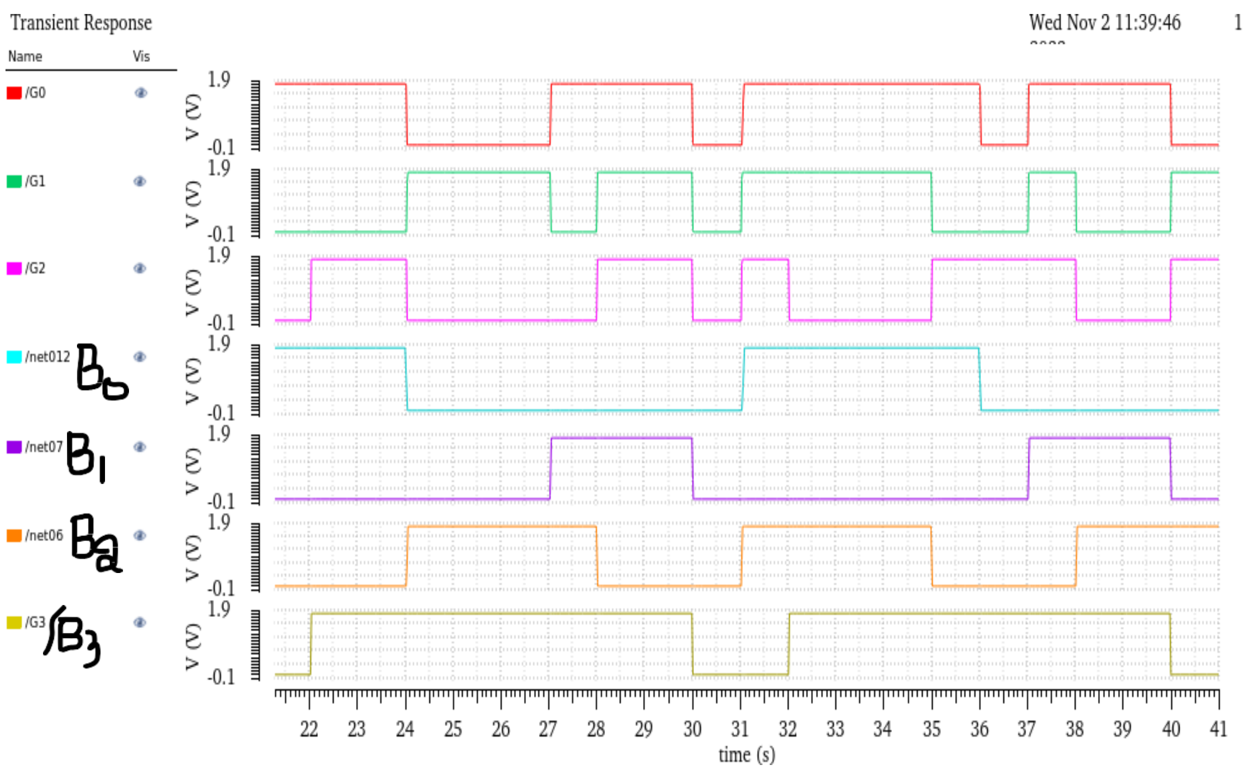
Y= AB’ + BA’



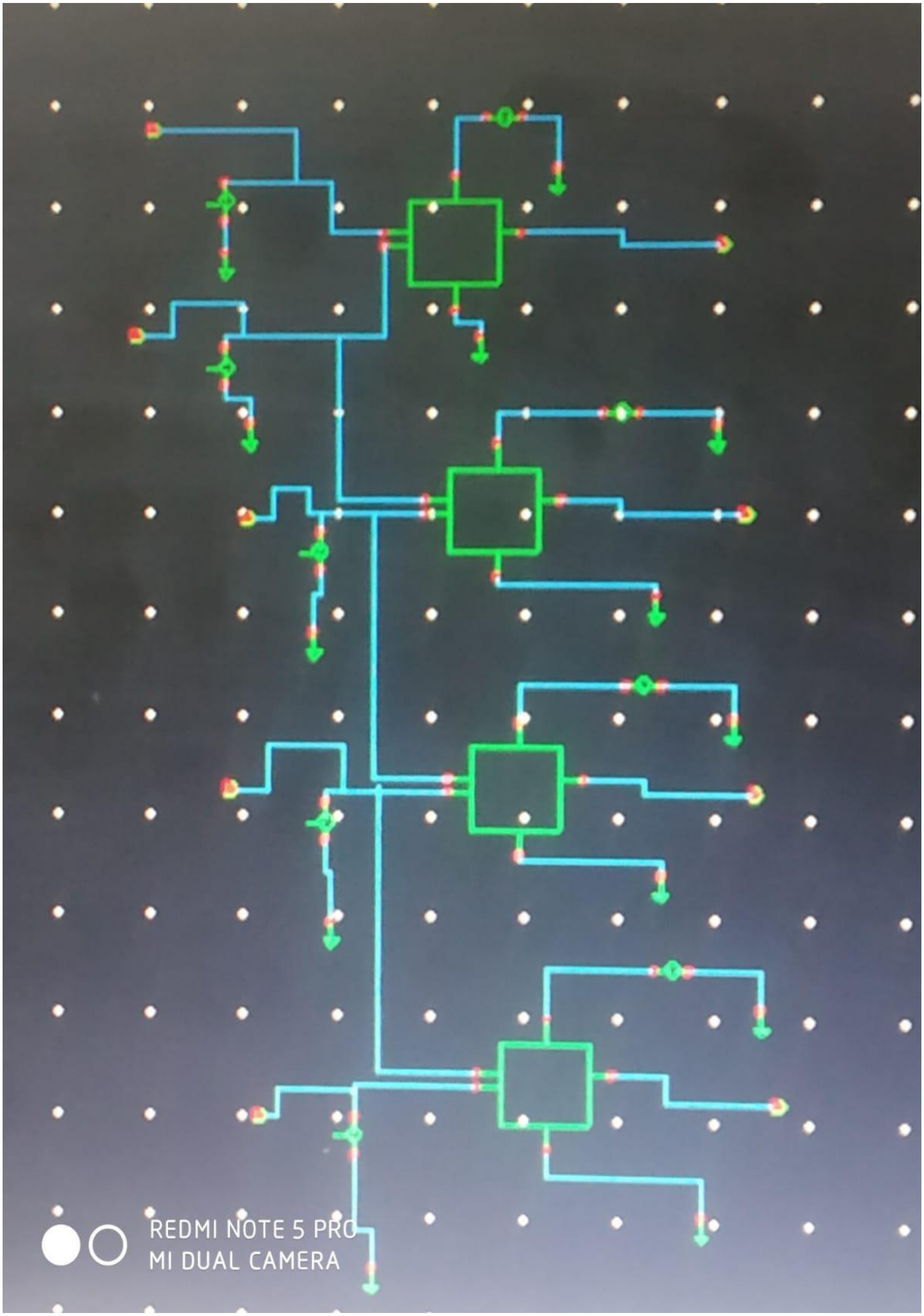
4-bit BCD to Gray Converter Schematic



4- bit binary to gray converter transient wave form



5-bit BCD to Gray Converter Schematic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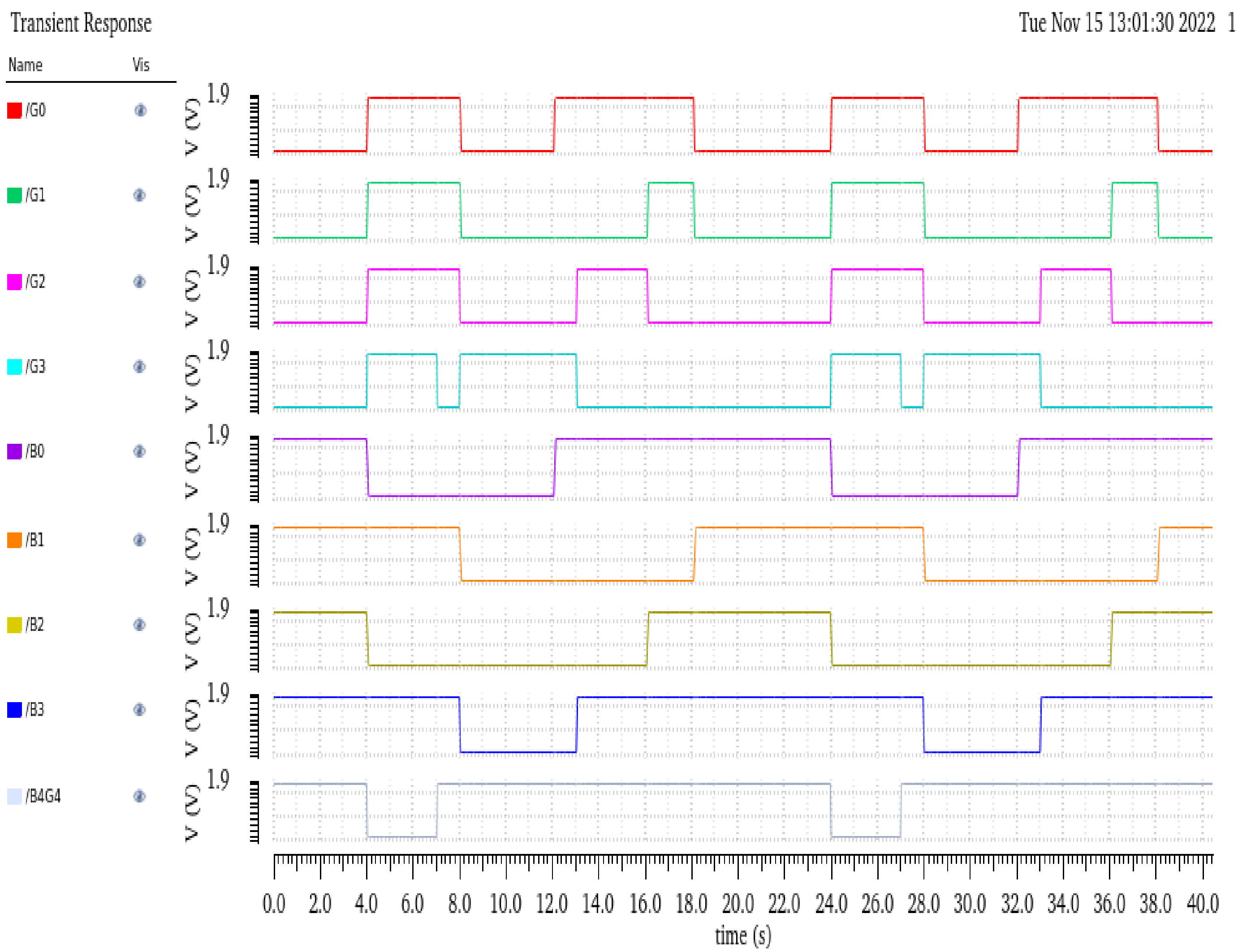
5- bit binary to gray converter transient wave form



Learning Outcome:

1) I have learnt how to design BCD to Gray converter schematic and transient wave form in cadence virtuoso.

2) I have learnt how to design a Static CMOS schematic using pmos and nmos transistors in Cadence Virtuoso.

In AND operation nmos should be series and pmos should be parallel.

In OR operation nmos should be parallel and pmos should be series.

pmos source should connect to vdc and nmos source should connect to ground.

3)Also, I have learnt how much range of value have to give “vpluse” and VDC.