Assignment 5

Class-SE IV
Batch-F4

ROLL NO-21430
DOS-5/12/2020

Title- Digital magnitude Comparator circuit

Objective-:
1. Design and implement 1 bit digital magnitude comparator circuit using logic gates
2. Design and implement 2 bit digital magnitude comparator circuit using logic gates.

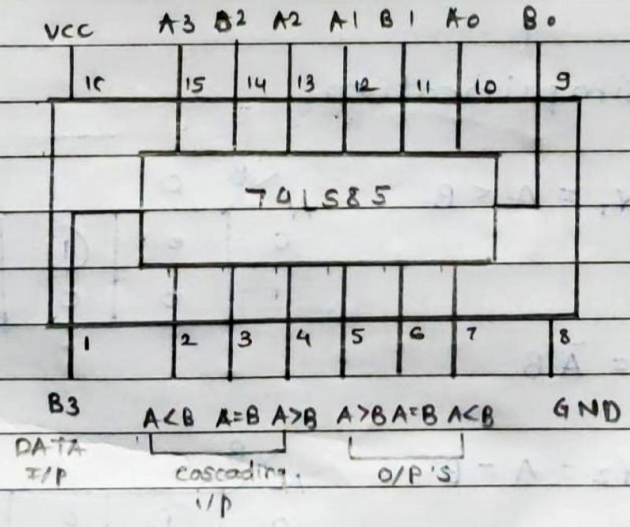
Apparatus-:
Digital Board, GP-4 Patch cords, IC 74LS86, IC 74LS32, IC 74LS08 / IC 74LS04 / IC 74LS85 and required gates if any.

Theory-
Magnitude comparator is a logic circuit, which compares two signals A and B and generates three logical outputs, whether A>B, A=B or A<B. IC 7485 is a high speed 4 bit magnitude comparator which executes two 4 bit words. The A=B input must be held high for proper compare operations. These 4 bit magnitude comparators perform comparison of straight binary to BCD codes. Three fully decoded decisions about two, 4 bit words are made and are externally available at three outputs. These devices are

fully expandable to any number of bits without external gates. Words of greater words of length may be compared by connecting comparators in cascade.

The A > B, A < B and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of next stage handling less-significant bits. The stage handling the least significant bits must have a High level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long word.

* PIN DIAGRAM -:



* Procedure -:

1. Make the connections as per the Logic circuits of 1 bit Digital comparator circuit and verify its truth Table.

2. Make the connections as per logic circuit of 1 bit Digital comparator circuit and verify its Truth Table.

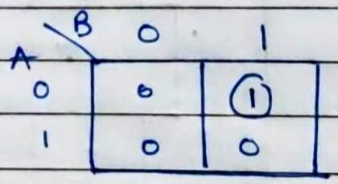
3. Make connections as per the pin Diagram of IC - 74LS85 and verify its function Table.

* Design of 1 bit digital comparator

Input		output		
A	B	$Y_1 = A<B$	$Y_2 = A=B$	$Y_3 = A>B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

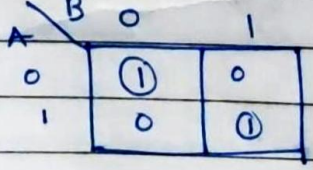
* K-Map simplification

i) for $Y_1 = A < B$



$\therefore Y_1 = \bar{A}B$

ii) for $Y_2 = A = B$



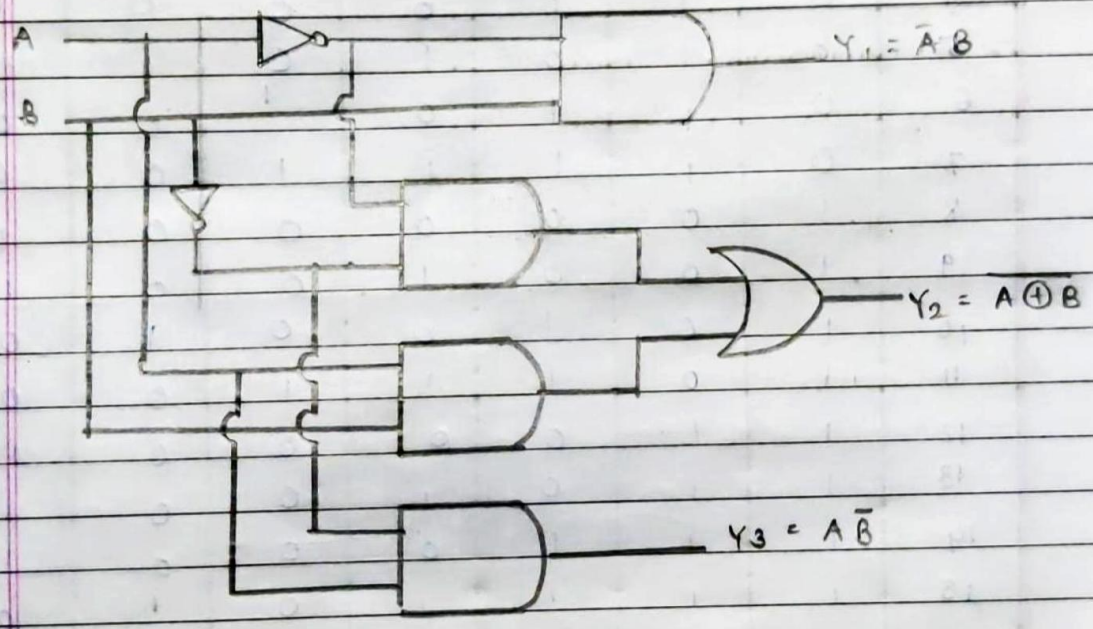
$\therefore Y_2 = \bar{A}\bar{B} + AB$

iii> For $Y_3 = A > B$

A \ B	0	1
0	0	0
1	1	0

$\therefore Y_3 = A\bar{B}$

* Logic Diagram :-



* Design of 2 Bit Comparator :-

* Design Table:-

Dec Eq^{n}.	Input				output		
	A_1	A_0	B_1	B_0	$Y_1 = A<B$	$Y_2 = A=B$	$Y_3 = A>B$
0	0	0	0	0	0	1	0
1	0	0	0	1	1	0	0
2	0	0	1	0	1	0	0
3	0	0	1	1	1	0	0
4	0	1	0	0	0	0	1
5	0	1	0	1	0	1	0
6	0	1	1	0	1	0	0
7	0	1	1	1	1	0	0
8	1	0	0	0	0	0	1
9	1	0	0	1	0	0	1
10	1	0	1	0	0	1	0
11	1	0	1	1	1	0	0
12	1	1	0	0	0	0	1
13	1	1	0	1	0	0	1
14	1	1	1	0	0	0	1
15	1	1	1	1	0	1	0

* K-Map Simplification:-

For $Y_1 = A < B$

A_1A_0 \ B_1B_0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

$\therefore Y_1 = \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_1 B_1 + \bar{A}_0 B_1 B_0$

ii) for $Y_2 = A = B$

A_1A_0 \ B_1B_0	00	01	11	10
00	(1)	0	0	0
01	0	(1)	0	0
11	0	0	(1)	0
10	0	0	0	(1)

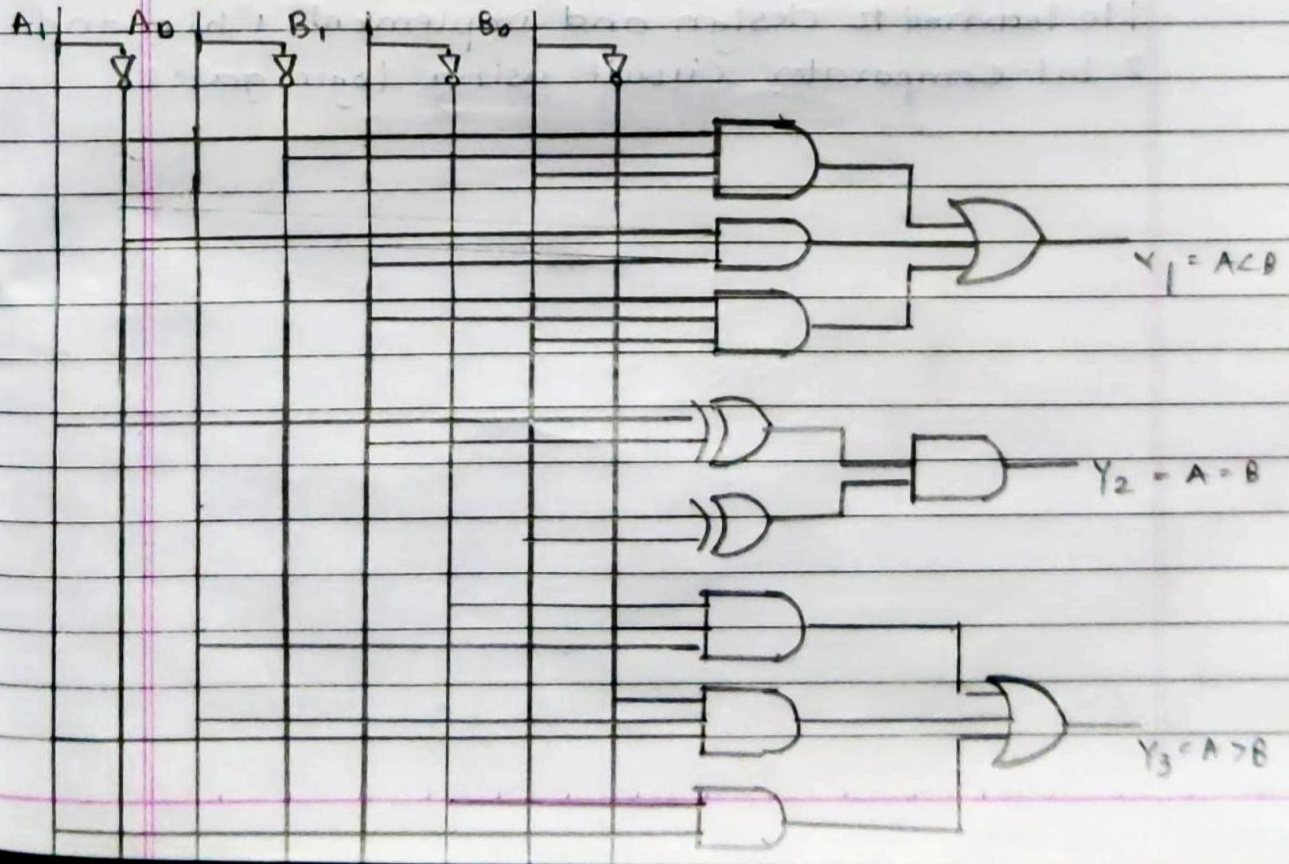
$Y_2 = (A_1 \odot B_1).(A_0 \odot B_0)$

iii) for $Y_3 = A > B$

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$Y_3 = A_0 \overline{B_1} \overline{B_0} + A_1 A_0 \overline{B_0} + A_1 \overline{B_1}$

* Logic Diagram:-



* Logic Gates/MSI devic required for Implementation

		Name of IC	No. of gates required	No. of IC required
1.	1 bit comparator using logic gates	NOT	2	IC 74LS04
		AND	4	74LS08
		XOR	1	74LS86
2.	2 bit comparator using logic gates	NOT	4	74LS04
		AND	7	74LS08
		XOR	2	74LS86
		XNOR	2	74LS32

Conclusion:-
We learned to design and implement 1 bit and 2 bit comparator circuit using logic gates.

DeldSim - Trainer Kit | Sanam Teri Kasam-Sanam Te | CircuitVerse - Digital Circuit Simu

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Main

- Gates
- Decoders & Plexers
- Sequential Elements
- Memory Elements
- Test Bench
- Misc

PROPERTIES

PROJECT PROPERTIES

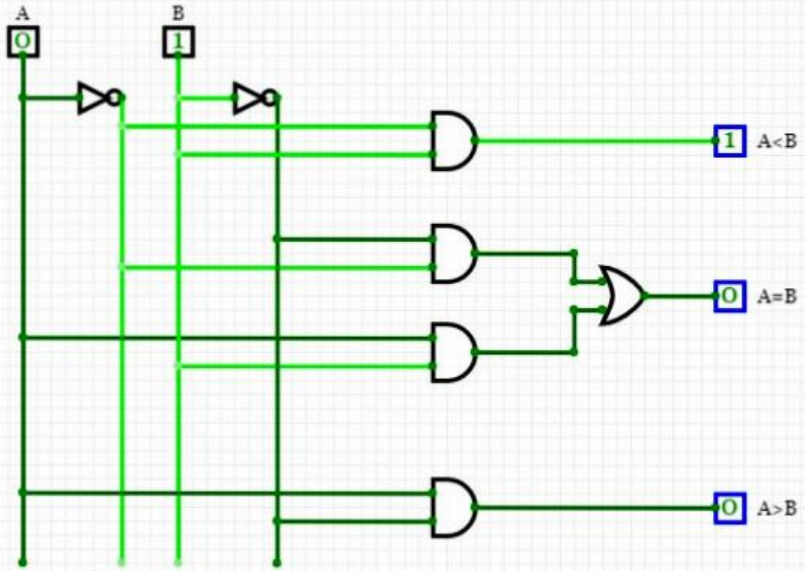
Project : 1 Bit Comparator

Circuit : Main

Clock Time : 500 ms

Clock Enabled :

Lite Mode :



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- Gates
- Decoders & Plexers
- Sequential Elements
- Memory Elements
- Test Bench
- Misc

PROPERTIES

PROJECT PROPERTIES

Project : 2 Bit Comparator

Circuit : Main

Clock Time : 500 ms

Clock Enabled :

Lite Mode :

Delete Circuit

Edit Layout

Main