Assignment 4

class-SE IV. ROLL NO-21430
Batch-F4 DOS - 5/12/2020.

Title :- Multiplexer / Demultiplexer.

Objective :-
1. Verification of function table of IC-74LS153
2. Design and implement 8:1 Mux using IC-74LS153 and verify its truth table.
3. Realization of the following Boolean expression using IC-74153 and verify its truth Table.
$F(A,B,C,D) = \Sigma m(0,2,4,7,9,10,12,13,15)$
4. Verification of function table of IC-74LS138.
5. Realization of following Boolean expression using IC-74138 and verify its truth table
$F(A,B,C) = \Sigma m(2,3,4,5,8,9,14,15)$

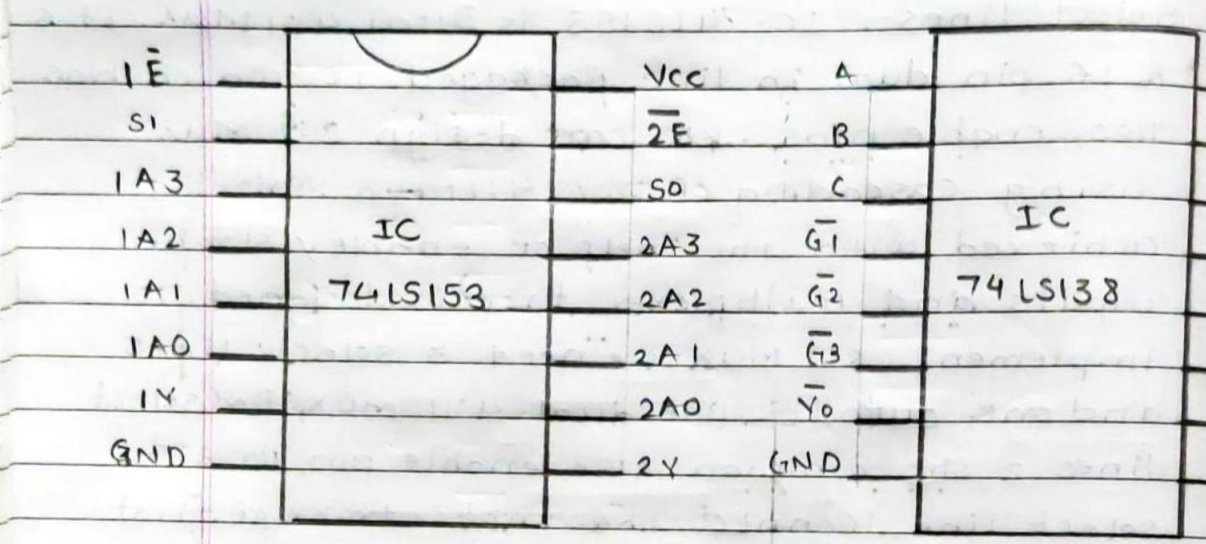
Apparatus :-
Digital board, GP-4 patch-cords, IC-74LS32, IC-74LS08 / IC-74LS04 / IC-74LS153 / IC-74LS138 and required logic gates if any

Theory :-
Multiplexer is a combinational logic device, which has many input and one output this output can be selected according to

select lines. IC-74LS153 is Dual 4:1 MUX. It is a 16 pin dual in line packaged IC which has two enable pins. We can design 8:1 Mux using cascading of Two 4:1 MUX. This is achieved with the help of enable / strobe inputs and multiplexer tree is designed. To implement 8:1 MUX we need 3 select lines and one output. Use dual 4:1 MUX for select lines 2 are common, use enable pin for 3rd select line. Connect the first strobe of first 4:1 MUX and the second strobe of second 4:1 MUX through one Inverter. This is 3rd select line only one 4:1 MUX will be become active at one time. Correct outputs of 2-MUX to OR gate so that we get one output

De-Multiplixer / Decoder is a combinational logic device, which has one input and many output one output can be selected according to select lines. IC-74LS183 is 3 to 8 line decoder/ Demultiplixer. It is a 16 pin dual packaged IC which has three enable pins. IC-74LS138 produces complementary output i.e. O/P of 74LS138 is active low. We can design any Combinational circuits using IC-74LS138. DEMUX performs reverse operation that of Multiplexer.

* PIN Digram:-



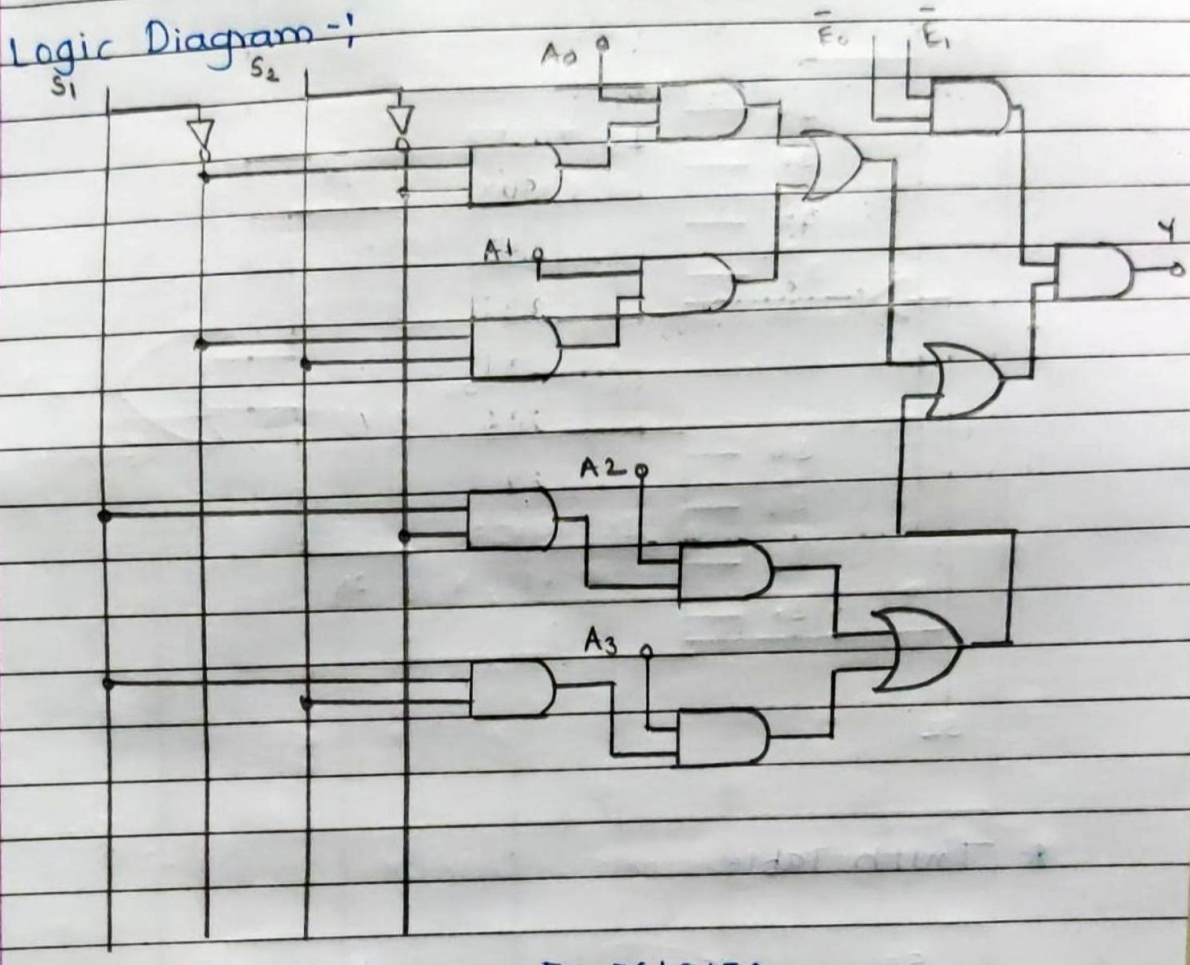
* Procedure -1

1. Make connections as per the pin Diagram of IC-74LS153 and verify its Truth Table.
2. Make the connections as per the logic circuit of 8:1 MUX and verify its Truth Table.
3. Make the connections as per logic circuit of the given function and verify its Truth Table.
4. Make the connections as per the pin diagram of IC-74LS138 and verify its Truth Table.
5. Make the connections as per the logic circuit of given function and verify its truth Table.

* function Table- IC 74LS153

Chip Enable		Select Input		Output	
1E	2E	S1(MSB)	S0(LSB)	MUX-1	MUX-2
0	0	0	0	1A0	2A0
0	0	0	1	1A1	2A1
0	0	1	0	1A2	2A2
0	0	1	1	1A3	2A3

* Logic Diagram :-

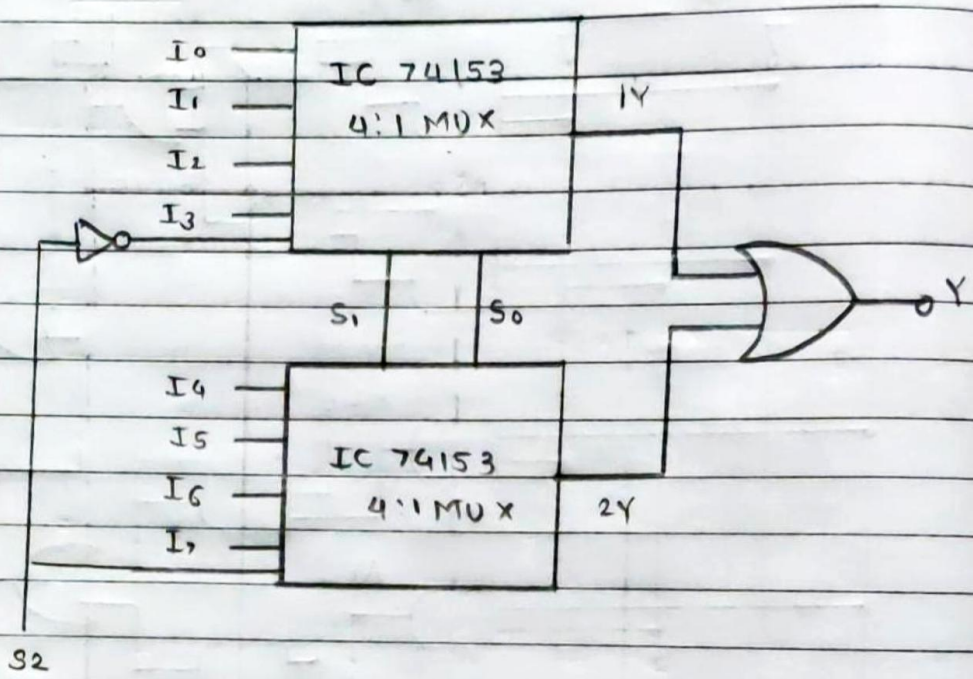


Design of 8 : 1 MUX using IC-74LS153

* Design Table

S_2 (msb)	S1	S_0 (LSB)	OUTPUT (Y)
0	0	0	1A0
0	0	1	1A1
0	1	0	1A2
0	1	1	1A3
1	0	0	2A0
1	0	1	2A1
1	1	0	2A2
1	1	1	2A3

* Logic Diagram :-



* Truth Table

S2	S1	S0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

Design of Realization of Boolean expression using IC74153

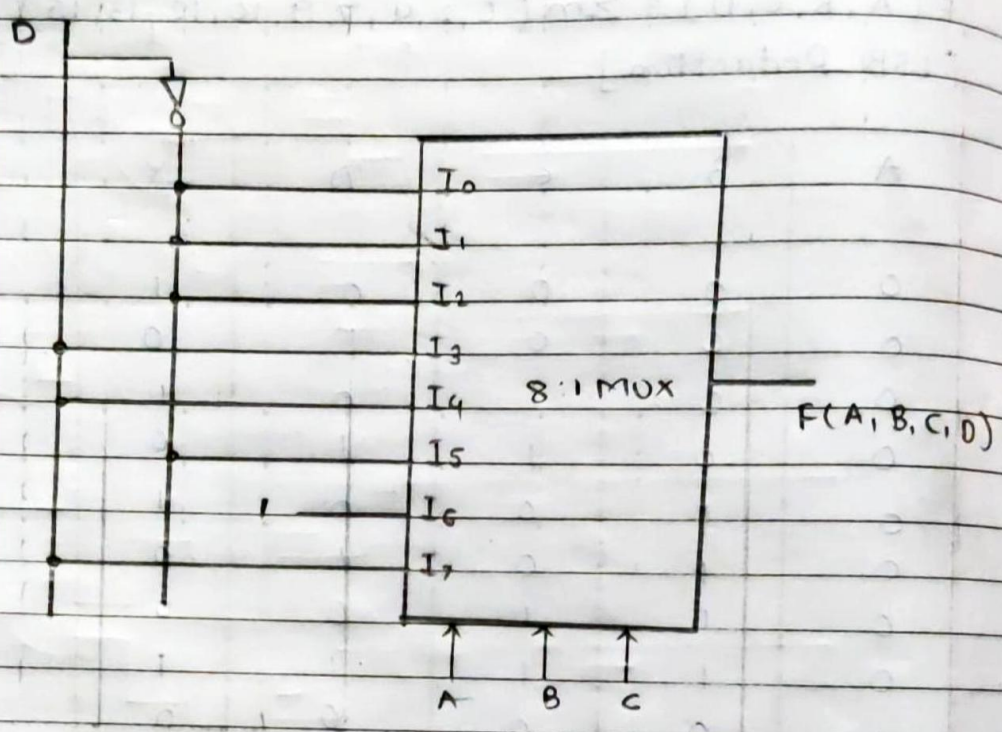
$F(A,B,C,D) = \Sigma m(0,2,4,7,9,10,12,13,15)$

[LSB Reduction]

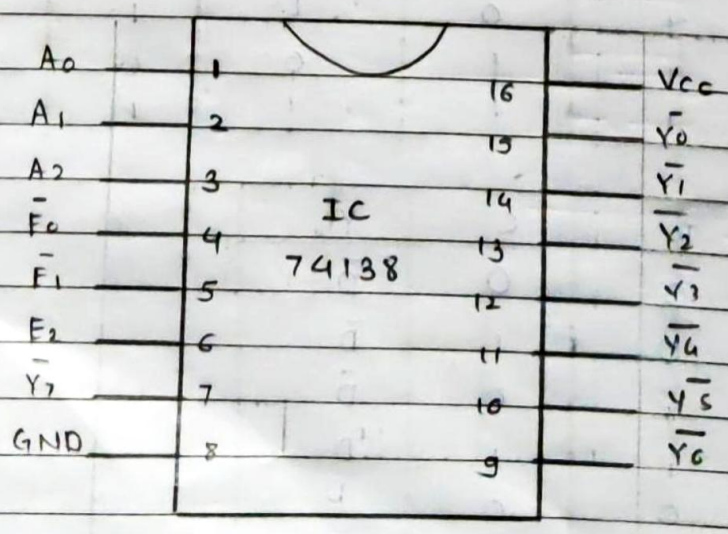
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

A	B	C	Y
0	0	0	$\bar{D}$
0	0	1	$\bar{D}$
0	1	0	$\bar{D}$
0	1	1	D
1	0	0	D
1	0	1	$\bar{D}$
1	1	0	1
1	1	1	D

* Logic Diagram

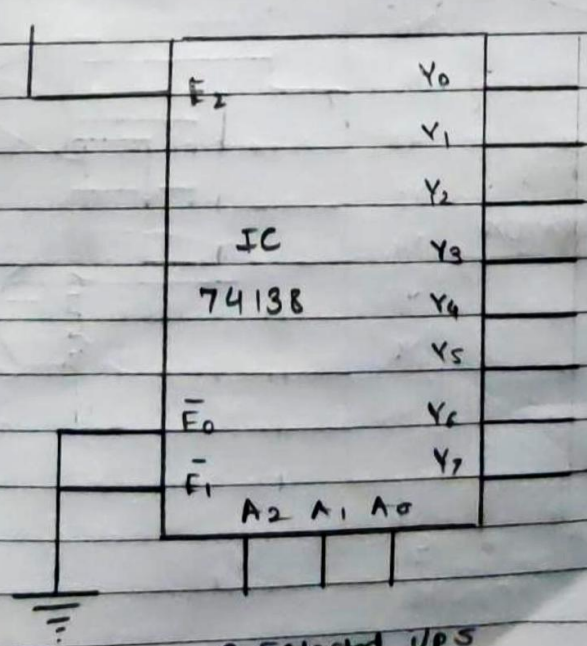


* Design of Decoder / DeMUX :-



$\bar{E}_0$	$\bar{E}_1$	$\bar{E}_2$	A_2	A_1	A_0	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$
1	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	0	x	x	x	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Logic Diagram:

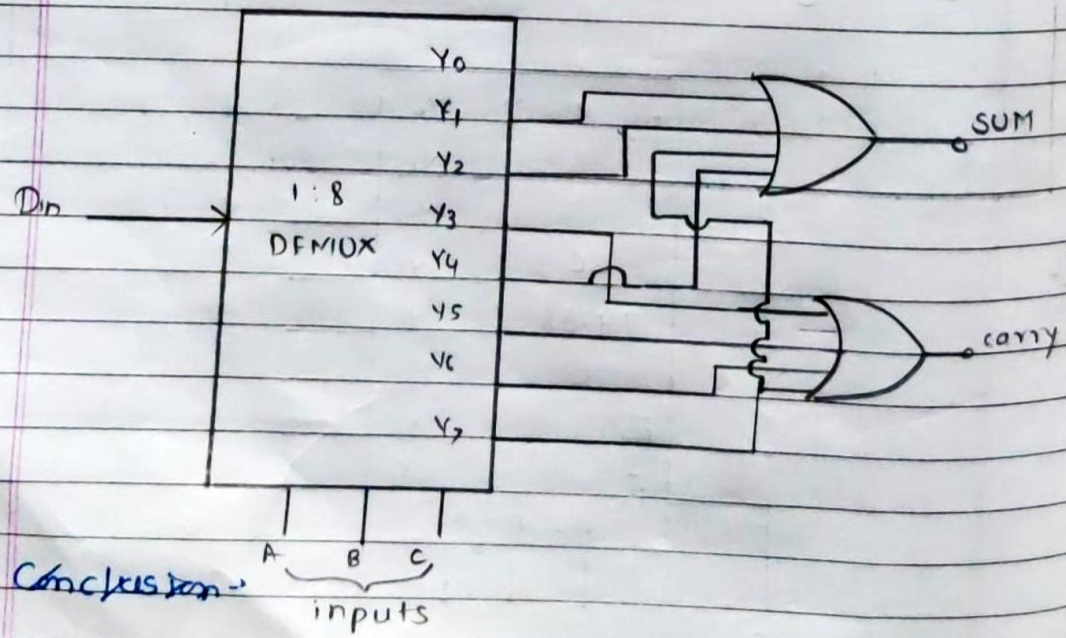


* Full Adder Using IC 74138 -:

Truth Table -:

Input			output	
A	B	Cm	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

* Logic Diagram -:



* Conclusion -

* Logic Gates/MSI Device required for implementation

NO.	Title	Name of IC	NO. of gate required	IC required
1.	Design of 8:1 MUX	IC 7404	1	1
		IC 7432	1	1
		IC 74153	2	1
2.	Realization of expⁿ using LSB reduction method	IC 7404	2	1
		IC 7432	1	1
		IC 74153	2	1
3.	Realization of expⁿ using MSB reduction method	IC 7404	2	1
		IC 7432	1	1
		IC 74153	2	1
4.	Realization of expⁿ using Decoder Ic	IC 7400	3	1
		IC 7432	1	1
		IC 74138	1	1

Conclusion-

We have learnt to design and implement multiplexer and demultiplexer with ICs and also verified the implementation using different examples

Output

Gates

Decoders & Plexers

Sequential Elements

Memory Elements

Test Bench

Misc

PROPERTIES

INPUT

BitWidth: 2

Delay: 0

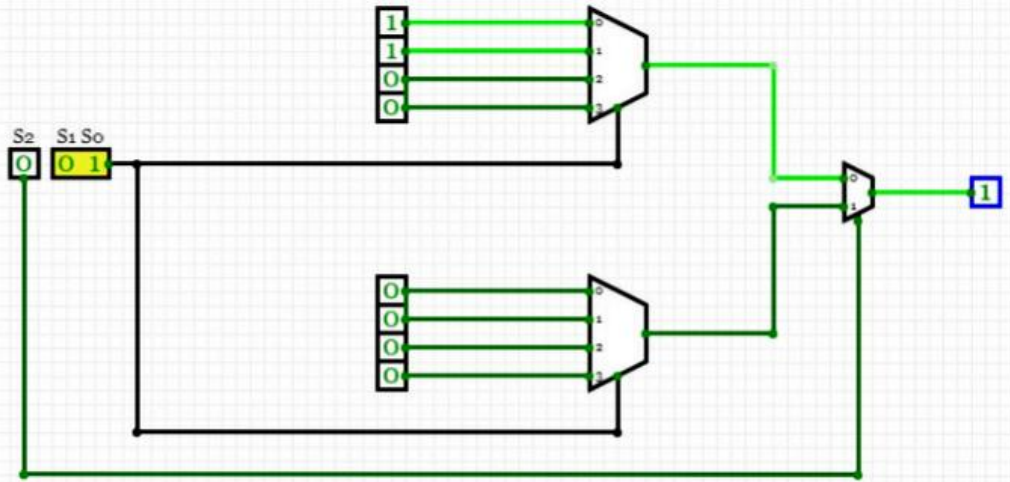
Label: S1 S0

Label Direction: UP

Orientation: RIGHT

Help

Main



CIRCUIT ELEMENTS

- Input
- Output
- Gates
- Decoders & Plexers
- Sequential Elements
- Memory Elements
- Test Bench
- Misc

PROPERTIES

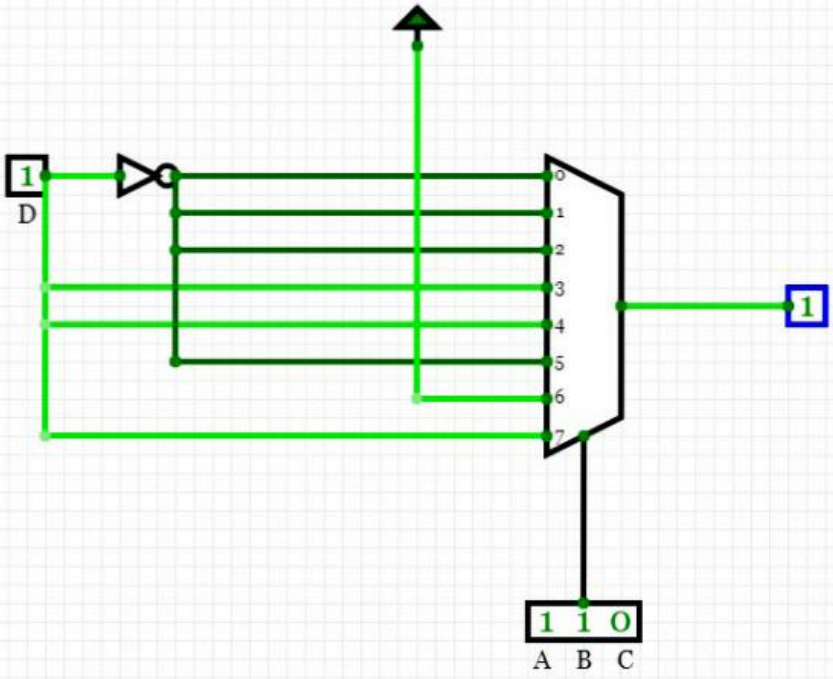
PROJECT PROPERTIES

Project : Implement boolean expr

Circuit : Main

Clock Time : 500 ms

Main



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Implement boolean expression using single 4:1 Mux

Ganesh Kandepalli

Main

- Decoders & Plexers
- Sequential Elements
- Memory Elements
- Test Bench
- Misc

PROPERTIES

PROJECT PROPERTIES

Project : ion using single 4:1 Mux

Circuit : Main

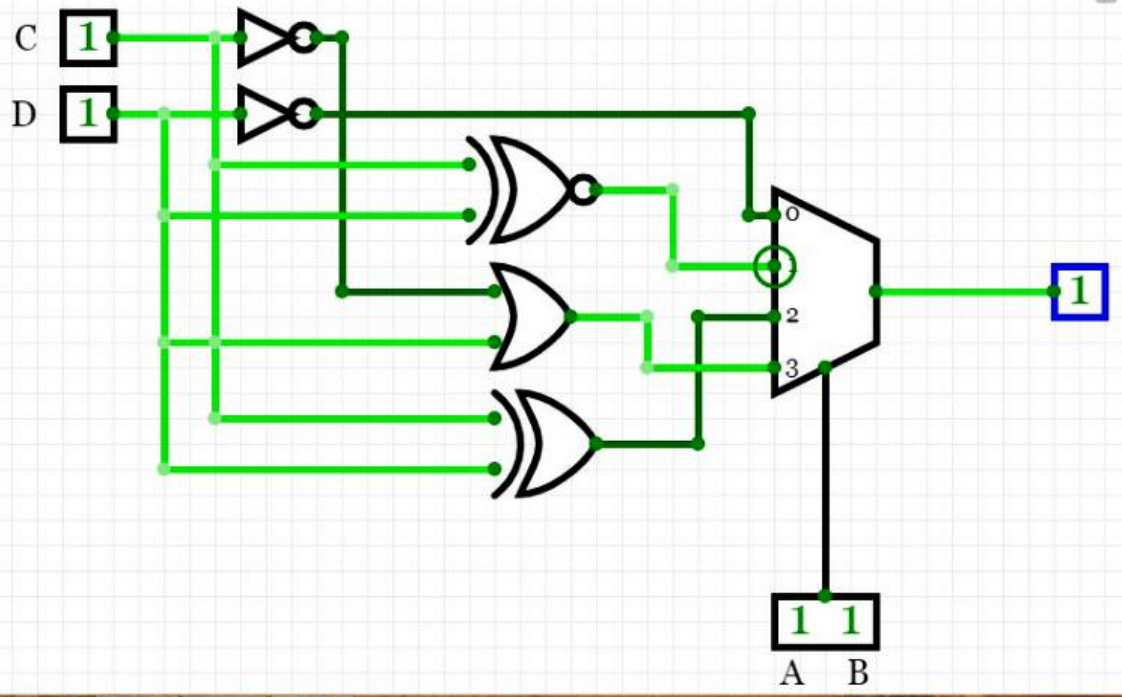
Clock Time : 500 ms

Clock Enabled :

Lite Mode :

Delete Circuit

Edit Layout



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CIRCUIT ELEMENTS

- Input
- Output
- Gates

- Decoders & Plexers
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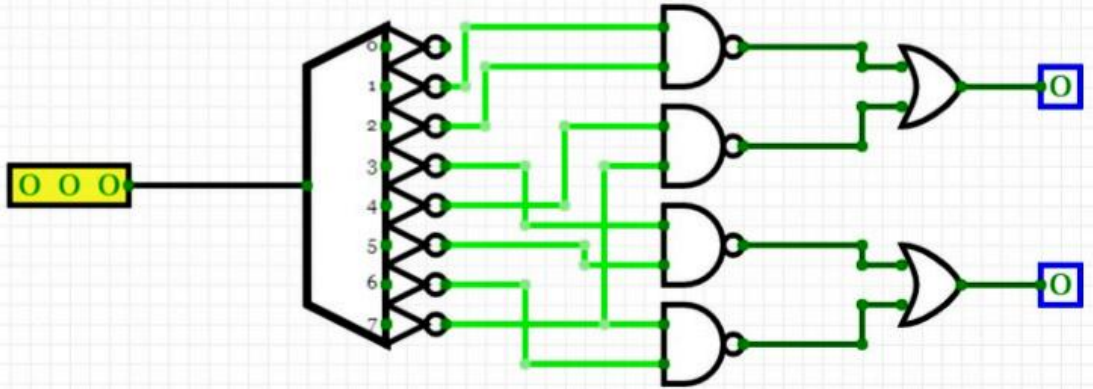
- Test Bench

Main



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