classmate
Date
Page

Assignment 12

class - SE IV
Batch - F4

ROLL NO - 21430
DOS - 14/01/2021

Title - Design and implement sequence detector using MS JK Flip Flop.

objective :- Design and implement the following Sequence detector circuit using IC - 74LS76 and verify its truth table

Apparatus :- Digital board, GP-4 patch cords, IC-74LS76, IC - 74LS04, IC - 74LS08 and required logic gates if any.

Theory :-
Sequence Detector is a sequential logic circuits which can take a string of bits as input and gives an output of 1 whenever the sequence occurs. Sequence Detector is of 2 types, overlapping & non-overlapping In an overlapping sequence detector the last bit of one sequence becomes the first bit of next sequence. However in non-overlapping sequence detector the last bit of one sequence does not become the first bit of next sequence detectors can be made using a mealy or moore machine

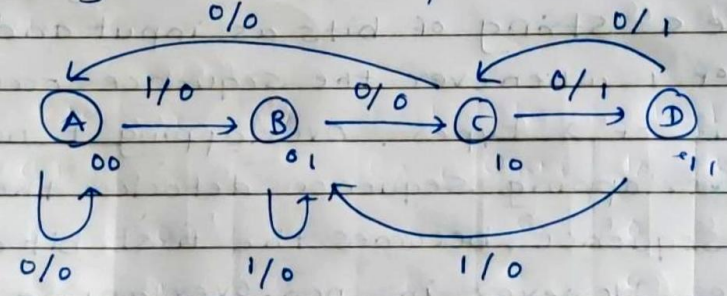
Procedure :-
1. Make the connections as per the logic circuit of Sequence developer using IC-74LS76 & verify the

truth table

* PIN DIAGRAM :-

Sequence Detector for sequence 1010 (mealy machine)

State Diagram - 1010 (Mealy Machine)



* State Table :-

Present State	Next State O/P	
	x=0	x=1
A	A, 0	B, 0
B	B, 0	B, 0
C	A, 0	D, 0
D	C, 1	B, 0

* Truth Table as per logic diagram-:

Present state		x	y	Next state		Flip Flop Outputs			
Q_A	Q_B			Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	x	0	x
0	0	1	0	0	1	0	x	1	x
0	1	0	0	1	0	1	x	x	1
0	1	1	0	0	1	0	x	x	0
1	0	0	0	0	0	x	1	0	x
1	0	1	0	1	1	x	0	1	x
1	1	0	1	1	0	x	0	x	1
1	1	1	0	0	1	x	1	x	0

* K-Map & Simplification -:

Q_A \ $Q_B x$	00	01	11	10
0	0	0	0	1
1	x	x	x	x

$J_A = Q_B \bar{x}$

Q_A \ $Q_B x$	00	01	11	10
0	x	x	x	x
1	1	0	1	0

$K_A = \bar{Q}_B \bar{x} + Q_B x$

Q_A \ $Q_B x$	00	01	11	10
0	0	1	x	x
1	0	1	x	x

$J_B = x$

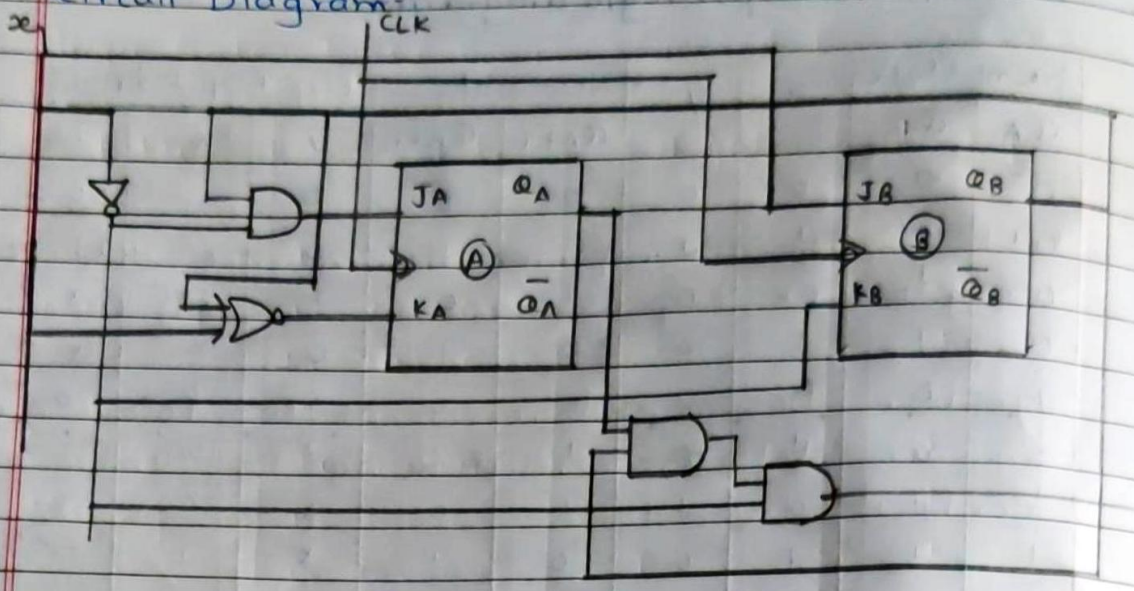
Q_A \ $Q_B x$	00	01	11	10
0	0	0	0	0
1	0	0	0	1

$Y = Q_A Q_B \bar{x}$

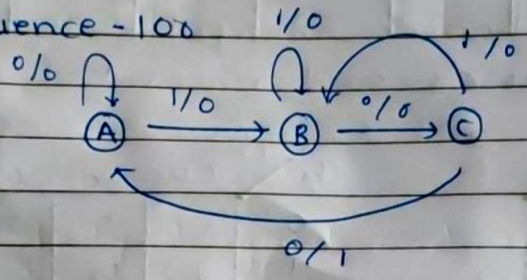
Q_A \ $Q_B x$	00	01	11	10
0	x	x	0	1
1	x	x	0	1

$K_B = \bar{x}$

* Circuit Diagram:-



* Sequence - 100



* Truth Table:-

Present state		x	y	Next State		FlipFlop I/P's			
Q_A	Q_B			Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	0	0	1	0	X	1	X
0	1	0	0	1	0	1	X	X	1
0	1	1	0	0	1	0	X	X	0
1	0	0	1	0	0	X	1	0	X
1	0	1	0	0	1	X	1	1	X
1	1	0	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X

* K-Map Simplification:-

Q_A \ $Q_B x$	00	01	11	10
0	0	0	0	1
1	x	x	x	x

$J_A = Q_B \bar{x}$

Q_B \ $Q_B x$	00	01	11	10
0	x	x	x	x
1	1	1	x	x

$K_A = 1$

Q_A \ $Q_B x$	00	01	11	10
0	0	1	x	x
1	0	1	x	x

$J_B = x$

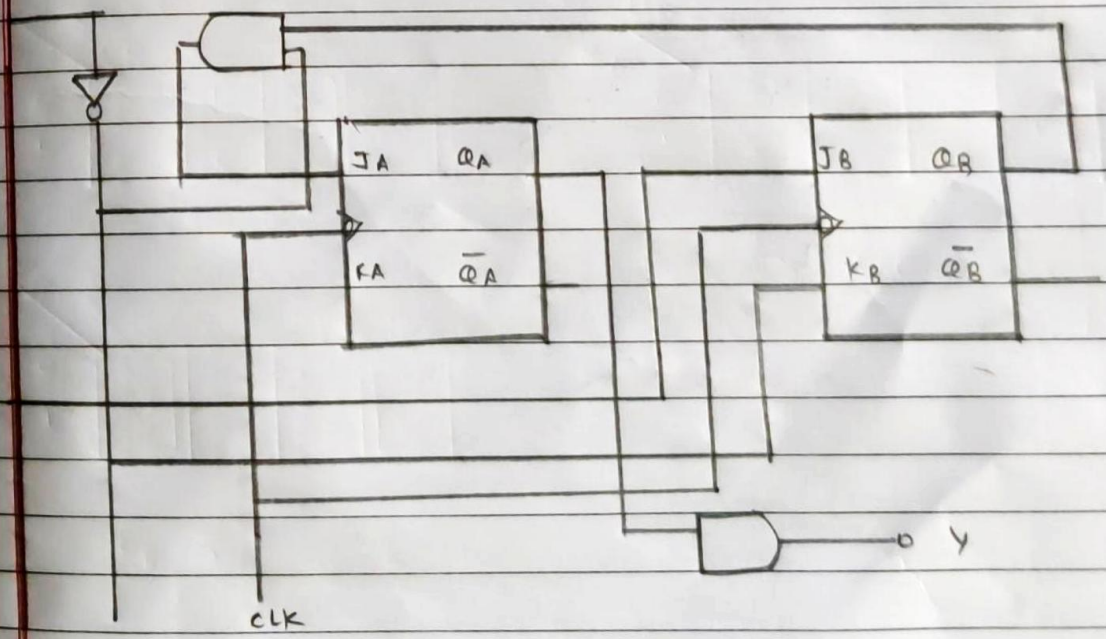
Q_A \ $Q_B x$	00	01	11	10
0	x	x	0	1
1	x	x	x	x

$K_B = \bar{x}$

Q_A \ $Q_B x$	00	01	11	10
0	0	0	0	0
1	1	0	x	x

$y = Q_A \cdot \bar{x}$

* Circuit Diagram:-

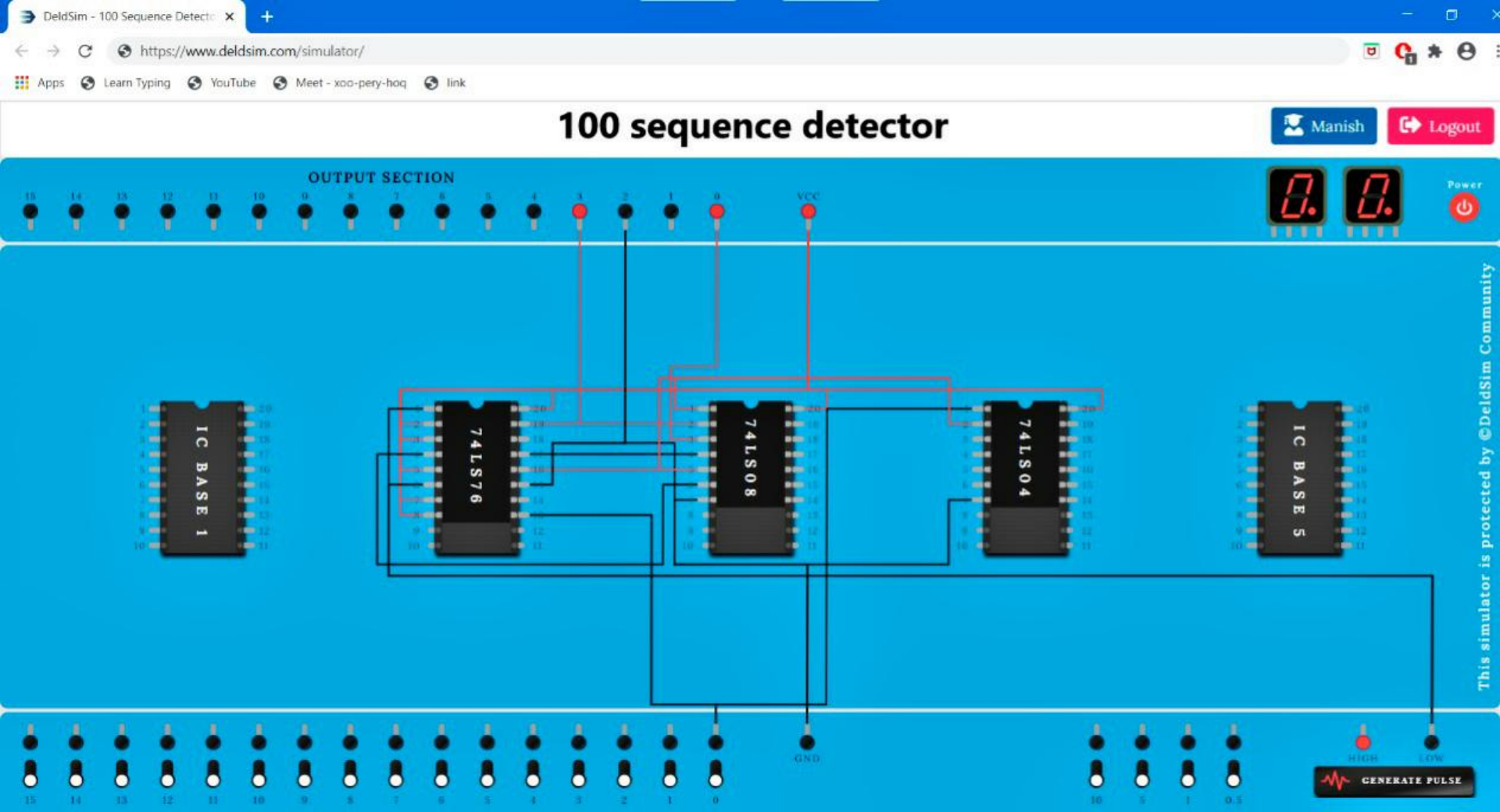


* logic Gates MSI/ Device required for implementation

Title	Name of Ic	No. of gates	Ic req.
1010 seq.	IC 74LS76	-	1
	IC 74LS08	5	2
	IC 74LS04	1	1
100 seq.	IC 74LS76	-	1
	IC 74LS08	2	1
	IC 74LS04	1	1

Conclusion :-

Succesfully designed and implemented seq. detector using IC 74LS76 on an online digital CKt.


DeldSim - 100 Sequence Detecto
https://www.deldsim.com/simulator/
Apps
Learn Typing
YouTube
Meet - xoo-pery-hoq
link
100 sequence detector
Manish
Logout
OUTPUT SECTION
VCC
Power
IC BASE 1
74LS76
74LS08
74LS04
IC BASE 5
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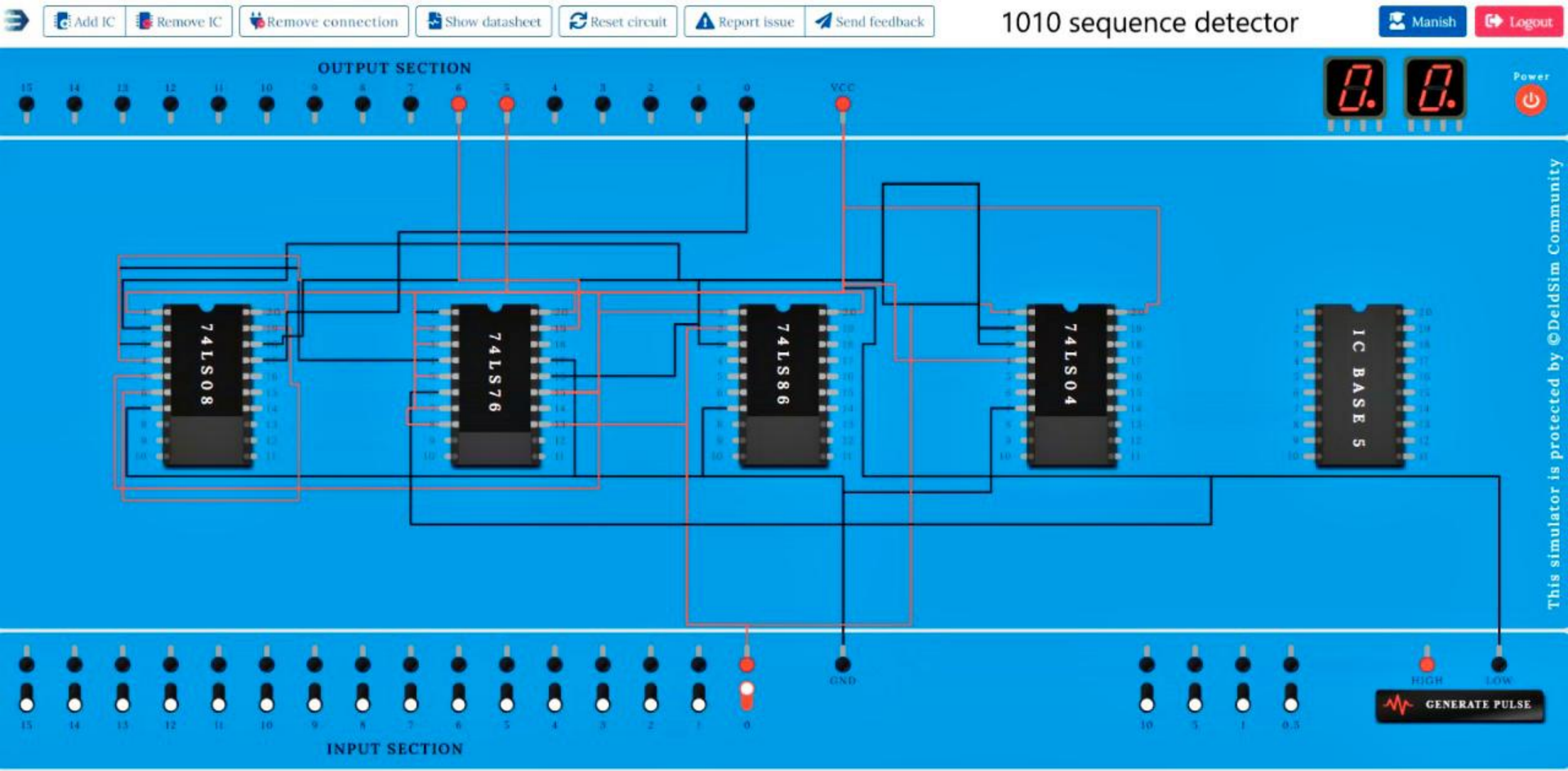
GND
HIGH
LOW
GENERATE PULSE


Add IC
Remove IC
Remove connection
Show datasheet
Reset circuit
Report issue
Send feedback
1010 sequence detector
Manish
Logout
OUTPUT SECTION
VCC
Power
74LS08
74LS76
74LS86
74LS04
IC BASE 5
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GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION