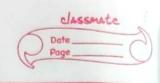


Assignment 14

Title - Design of ASM Chart using MUX controller method Objective - 1 Design and implement waveform generator (t using ASM based multiplexex controller method Apparatus - Digital board, GP-4 patch cords, IC-741574, IC-741532, IC-741508 and required logic gates if any Theory -: Algorithm State machine (ASM) charts-1. Used to design complex sequential cits 2. Concepts is similar to software flow-chart 3. Also known as "Hardware flow chart". 4. Asm chart is one step forward towards the implementing hardware ckt ie using Asmichart we can directly design the hardware cit. Basic concept of ASM charts: 1. State box. & Design box. . Conditional output box. 1. state box i rectangular shape 2. Each state box represents one state of segickt

3. It is having one entry pt and one exit pt



iv. Name of the state is placed to the left of state box

V. The unconditional outputs corresponding to that

State can be placed inside state box.

vi. Make state machine outputs can also be placed inside state box

pt

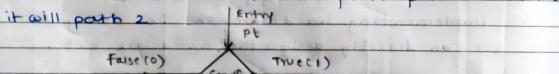
Unanditional

State name

O/P. S

exit

- 2. Decision Box -:
 - 1. Diamond shape
 - in Having one entry pt and two exit pts.
 - iii. Inputs or boolean expr. can be placed inside the
 - decision box which are checked to be whether the or
 - iv. IF condition is true then it will prefer path 1. Otherwise



Path 1

3. Conditional output box -:

path 2

- 1. Oval Shape
 - 2. Having one entry pt and one exit pt. similar to state
 3. Input path to be conditional outputs can be
 placed inside the statements.



IV. The conditional ofp can be placed inside the statement v. Ingeneral, mealy state machine ofps are represented inside conditional output box.

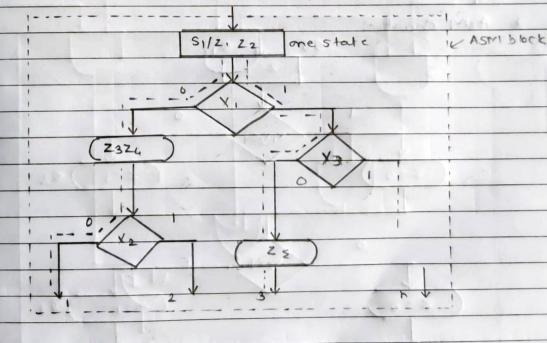
> conditional 0/p'5 exit pt

* ASM block -:

1. It is a structure consisting of one state box and all the decision and conditional boxes connected to its exit path

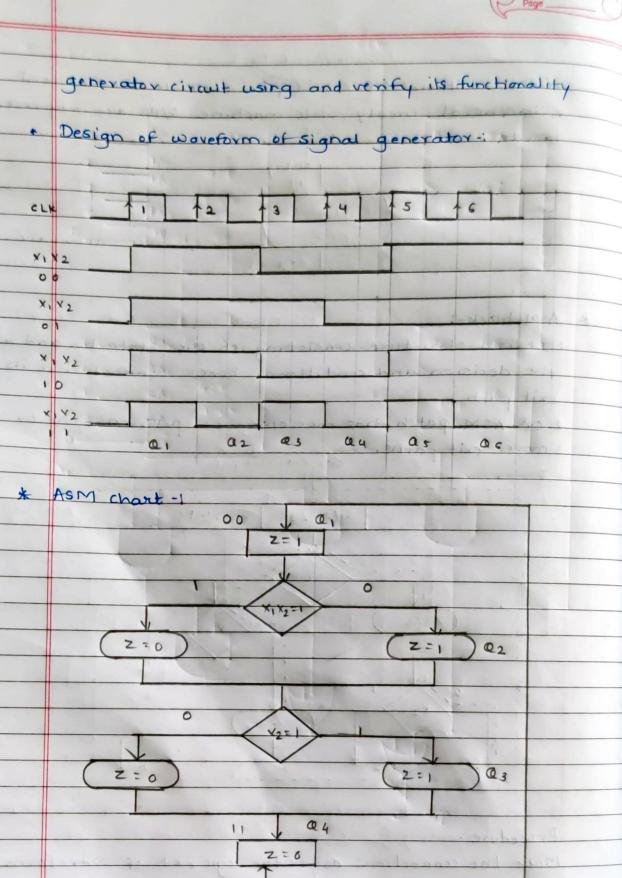
2. on ASM patch has one entrance path and one ox more exit paths

one entrance path



Procedure.

Make the connections asper the logic okt of waveform

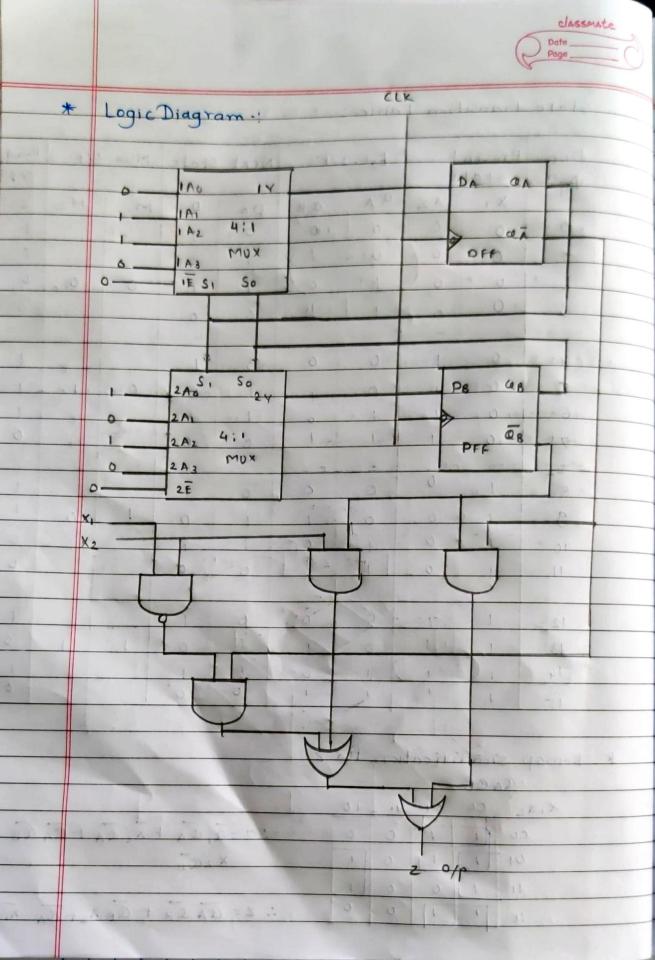


State transition Table:

Dec Fgn	Present		Est. I/P's		Next State		Mux o/p		Pind or a	
	×ι	X 2	Q.A.	QB	DA	DB	M.	11/2	Z	
0	0	6	0	0	0	1			1	
	0	0	0	1	1	0			1	
2	0	0		0	1		0	ō	0	
3	0	0	-	1	0	0			6	
4	0	1	0	0	G	1			1	
5	0	1	0			6	0	1	1	
6	0	1	1			1			1	
7	0	1	1	1	0	0			0	
8	1	0	0	0	6	1			1	
9	1	0	0		1	0	1	0	1	
10	1	0	1	6		-		1	0	
11	1	0		1	0	0			0	
12	1	1	0	0	b	1			ı	
13	1	1	0	1	1	0		1	0	
14	1	1	1	0	1				1	
15	1	1	1	1	0	0			0	

* K-map simplification for z

QA QB						
	2122	00	01	1	10	
	60	1	1	0	0	: Z = 2, QA + X2 QA + QA QB +
	01	-	1	0	1	X 2 0 0
	l ₁	1	0	0	1	
	10	1	1	0	0	: Z= QA QB + QB X2+ QA XIX2
1						21 04





Logic Gates (MSI device required for implementation)
1. IC 74153 (4:1MUX) -2
2.TC-7476 (DUAL DFF) -1
3. tc - 7408 (AND Gate) - 1 (4 AND gates reg)
4 TC-7/32 (OR gate) - 1 (2 OR gates reg)
5. Ic - 7404 (NOT gate) - 1 (1 NOT gates req)

Conclusion:

Hence, algorithm state machine by multiplexer

controller method was understood, designed and

implemented successfully.

