

## Assignment 7

Class-SE IV

Batch-F9

Roll NO-21430

DOS - 9/12/2020

Title- flipflop

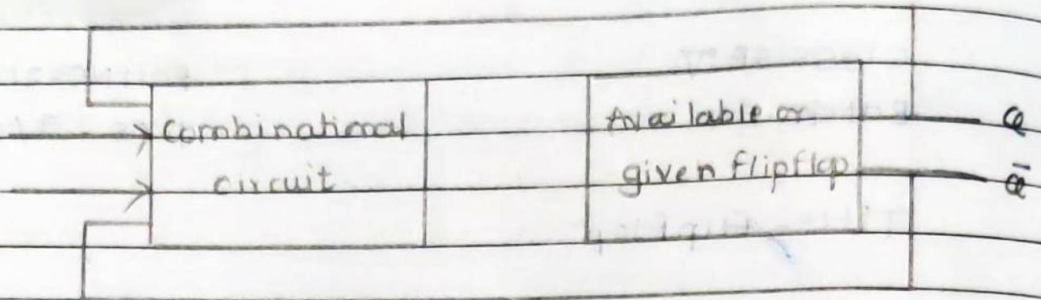
Objective - Conversion of flipflop

Apparatus- Digital trainer kit, IC 7476, IC 7474, IC 7408, IC 7432, IC 7404, Patch cords, +5 v power supply

Theory:-

1. A flipflop is an electronic device which is having two stable states and a feedback path which is used to store 1 bit of information by using the clock signal as input. Latches are also used to do the same task except that they do not use clock signal.
2. There are four types of flipflop SR, D, JK and T flipflop.
3. Generally, JK flip-flops and D flip-flops are the most widely used flipflops. And so their availability in the form of integrated circuits.
4. Common conversions are  $SR \rightarrow JK$ ,  $SR \rightarrow D$ ,  $SR \rightarrow T$ ,  $JK \rightarrow SR$ ,  $JK \rightarrow D$ ,  $JK \rightarrow T$ ,  $D \rightarrow SR$ ,  $D \rightarrow JK$ ,  $D \rightarrow T$ .

General model used to convert one type of flipflop to other:-



### Derived Flipflop

#### \* SR to JK flip flop Conversion-1

Here we are required to convert the SR to JK ff. so first we design a combinational circuit with J and K as its inputs and we connect output to the input of our available flipflop i.e. on SR flip flop so its output is same as that of JK flip flop

#### \* Conversion Table-

FF Inputs		Present state	Next state	Outputs	
J	K	$Q_n$	$Q_{n+1}$	S	R
0	0	0	0	0	X
0	1	0	0	0	X
1	0	0	1	1	0
1	1	0	1	1	0
0	1	1	0	0	1
1	1	1	0	0	1
0	0	1	1	X	0
1	0	1	1	X	0



# \* K-Map Simplification :-

i. For S -

J \ K $\bar{a}_n$	00	01	11	10
0	0	x	0	0
1	1	x	0	1

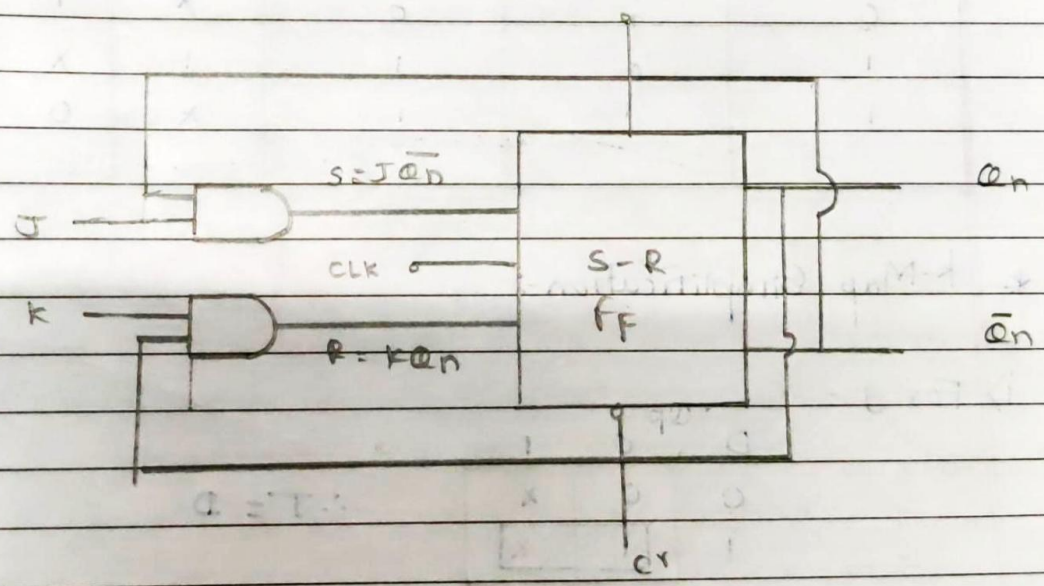
$\therefore S = J\bar{a}_n$

$\Rightarrow$  For R -

J \ K $\bar{a}_n$	00	01	11	10
0	x	0	1	x
1	0	0	1	0

$\therefore R = K\bar{a}_n$

## \* Logic Diagram - 1



### 8. JK flipFlop to D FlipFlop Conversion:-

The design of the Combinational circuit should be in such a way that D is the input and J & K are its output. The outputs of the combinational circuit J and K are connected as inputs to the flipFlop.  $Q_p$  is the present state output of flipFlop and  $\bar{Q}_p$  is its complementary and  $Q_{p+1}$  is the next state.

#### \* Conversion Table:-

Inputs	Present	Next ( $Q_{p+1}$ )	Outputs	
D	( $Q_p$ ) state	state	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

#### \* K-Map Simplification:-

i) For J -

D \ $Q_p$	0	1
0	0	X
1	1	X

$\therefore J = D$

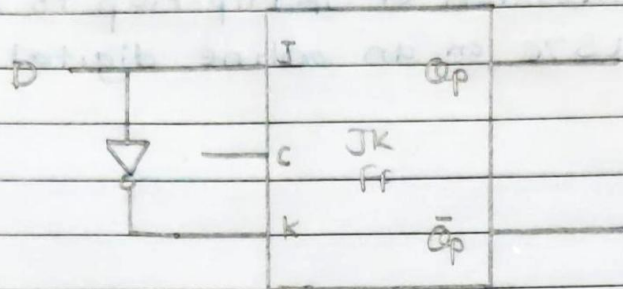
ii) For K -

D \ $Q_p$	0	1
0	X	1
1	X	0

$K = \bar{D}$



### \* Logic Diagram:-



### \* PIN DIAGRAM -)

<u>Clock 1</u>	IC	1K
<u>Preset 1</u>	74LS76	1Q
<u>Clear 1</u>	DUAL MS JK FF	1Q
1J		GND
VCC		2K
<u>CLOCK 2</u>		2Q
<u>PRESET 2</u>		2Q
<u>CLEAR 2</u>		2J

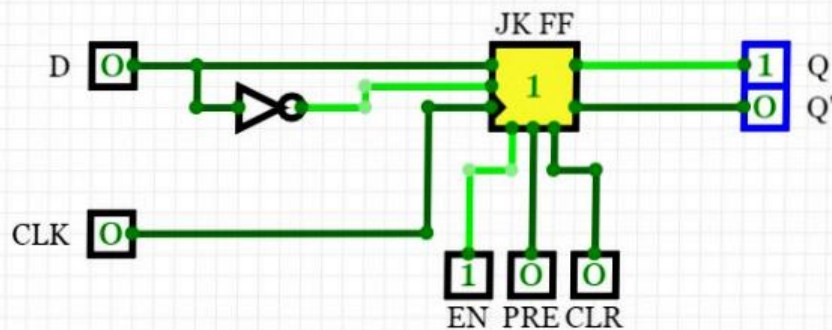
### \* Logic Gates/MSI Devices required for Implementation:

NO.	Time	Name of IC	Numbers of FF's required	IC's required
1.	Flip-flop conversion	IC 74LS76	1	1
		IC 74LS04	-	1

\* Conclusion:-

We successfully designed and implemented circuit for conversion of JK flip-flop to D flip flop using IC-74LS76 on an online digital trainer kit.

Main



### PROPERTIES

#### JKFLIPFLOP

Delay: 100

Label: JK FF

Label Direction: UP

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SR TO JK FF

Ganesh Kandepalli

Decoders & Plexers

Sequential Elements

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PROPERTIES

INPUT

BitWidth: 1

Delay: 0

Label: CLR

Label Direction: DOWN

Main

SR FF

Q

Q'

EN

PRE

CLR

J

K

1

0

1

0

1

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