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Assignment 8

Class-SE IT
Batch-F4
ROLL NO-21430
DOS-2/12/2020

Title :- Design of 2 bit and 3 bit Ripple counter using MS JK Flip-Flop.

Objective :-
1. Design and implement 2 bit Asynchronous (Ripple) Up counter circuit using IC-74LS 76. Draw timing diagram.
2. 2 bit Ripple down counter & timing diagram (IC 7476)
3. 3 bit Ripple up counter and timing diagram (IC 7476)
4. 3 bit Ripple down counter and timing diagram (IC 7476)

Apparatus :-
Digital-Board, GP-4 patch-cords, IC-74LS76, IC 74LS32, IC 74LS04, IC 74LS08 and required Logic gates if any.

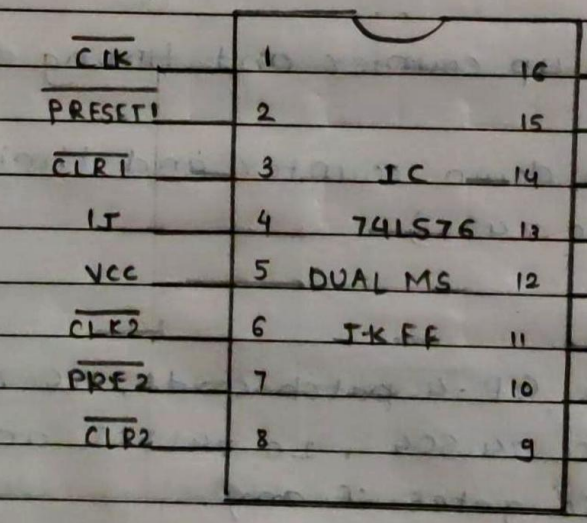
Theory :-
Counter is a sequential logic device which can be use to count the number of pulses given to the circuit counter can be classified into two category one is synchronous and other is Asynchronous (Ripple). In case of Ashynchrous

Counter output of first flipflop goes to the clock of the next and so-on and input of all flip-flop is connected to Vcc from IC-74LS76.

All set and reset pin is connected to Vcc.

Asynchronous counter is easy to begin as compared to synchronous counter. Synchronous counter is faster than Asynchronous counter. IC 74LS76 is Dual MS JK flip-flop which means in one IC There are two MS-JK flip-flop are contained.

* PIN DIAGRAM-:

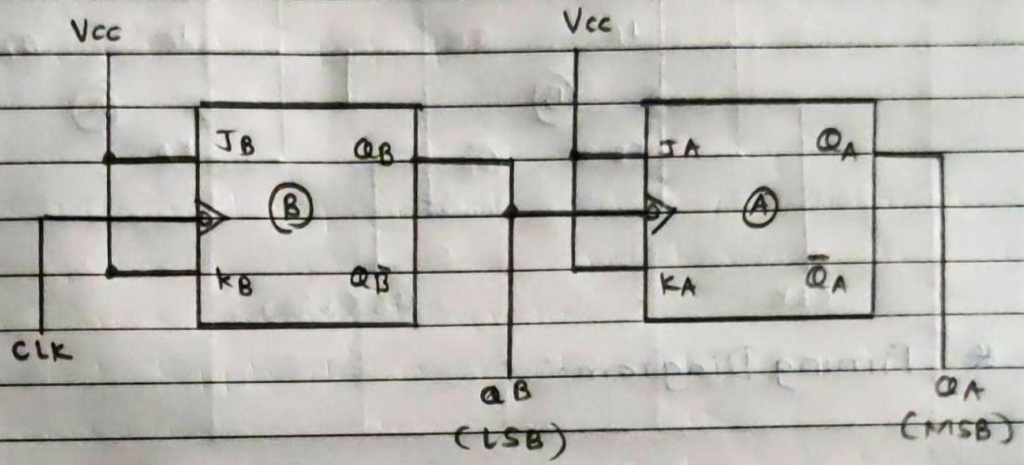


* Procedure-:

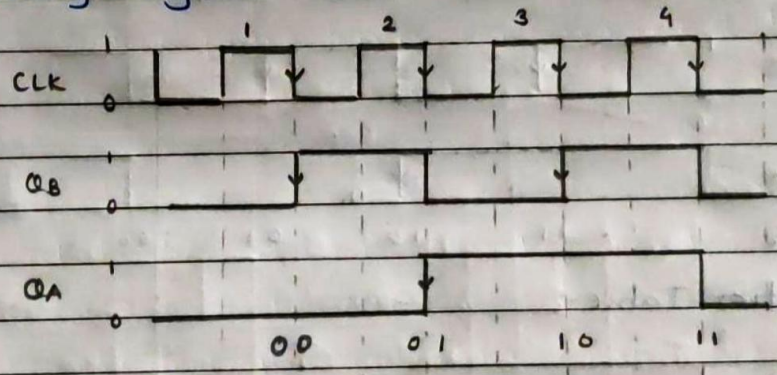
1. Make the connections as per logic diagram of 2 bit ripple up and down counter circuit using IC-74LS76 and verify its truth table.
2. Make the connections as per logic circuit of 3-bit

Ripple up and down counter circuit using IC 74LS76 and verify its truth table.

* Design of 2 bit Ripple up counter:-



* Timing Diagram:-

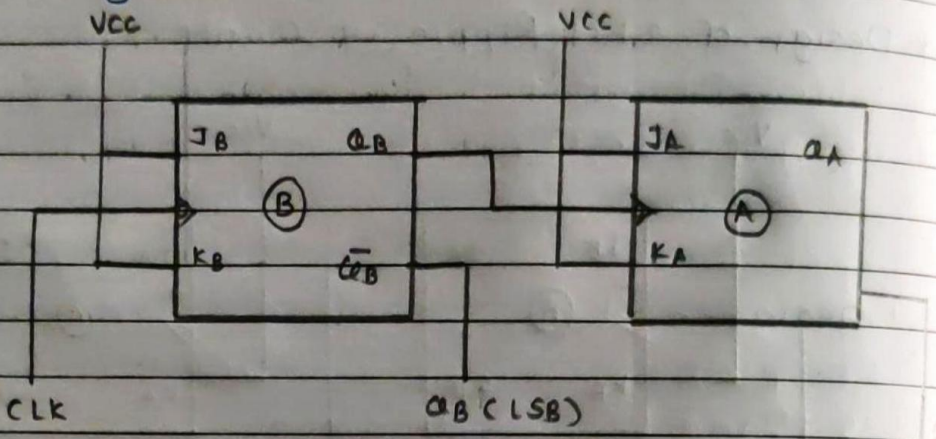


* observation Table:-

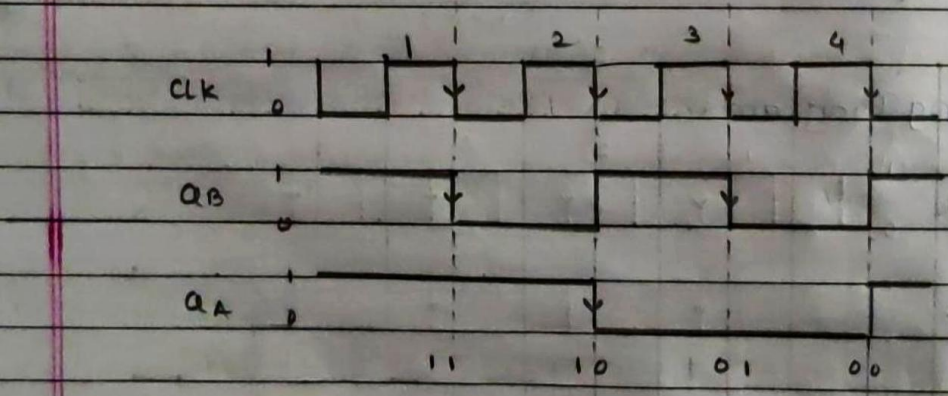
Clock Pulse	QA	QB
1	0	0
2	0	1
3	1	0
4	1	1

* Design of 2 bit Down Counter (Ripple) →

* Logic Diagram :-



* Timing Diagram :-

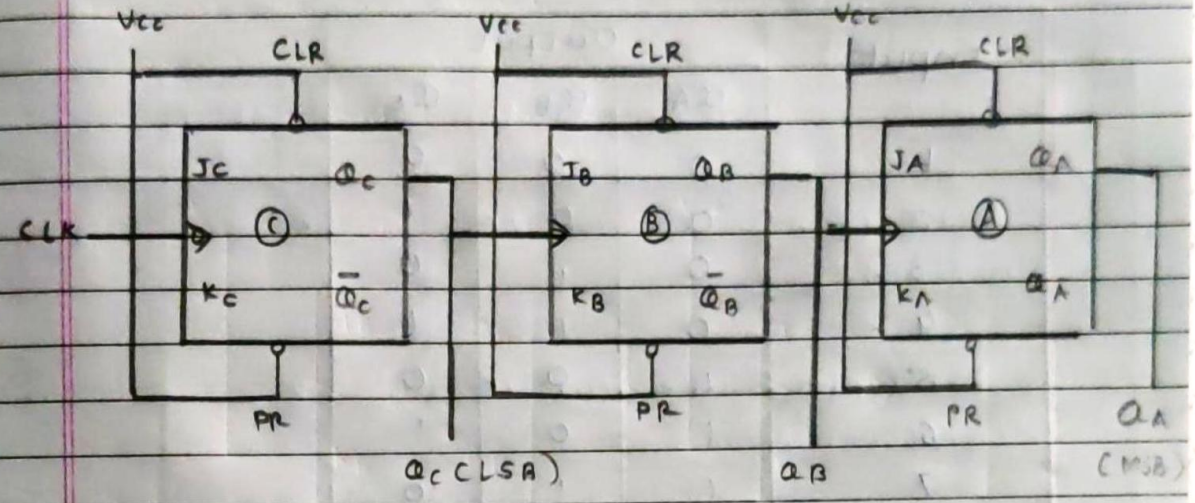


* Observation Table :-

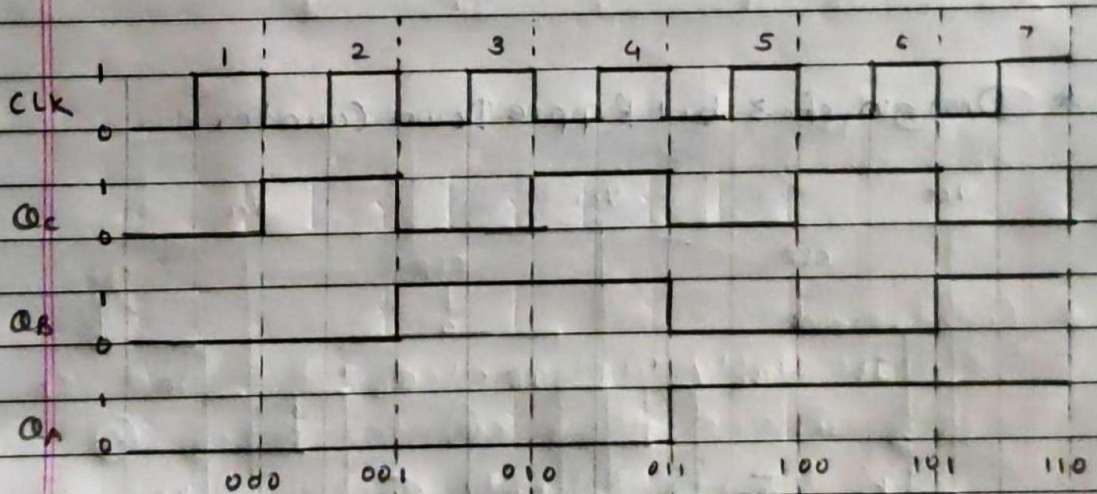
Clock Pulse	output	
	Q_A	Q_B
1	1	1
2	1	0
3	0	1
4	0	0

* Design of 3 bit Ripple Up-Counter :

* Logic Diagram :



* Timing Diagram :



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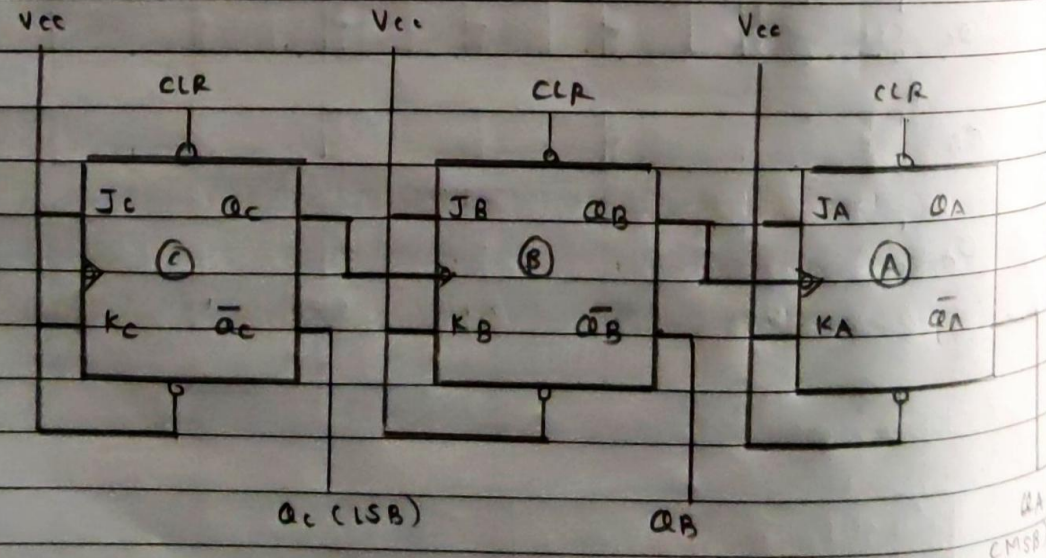
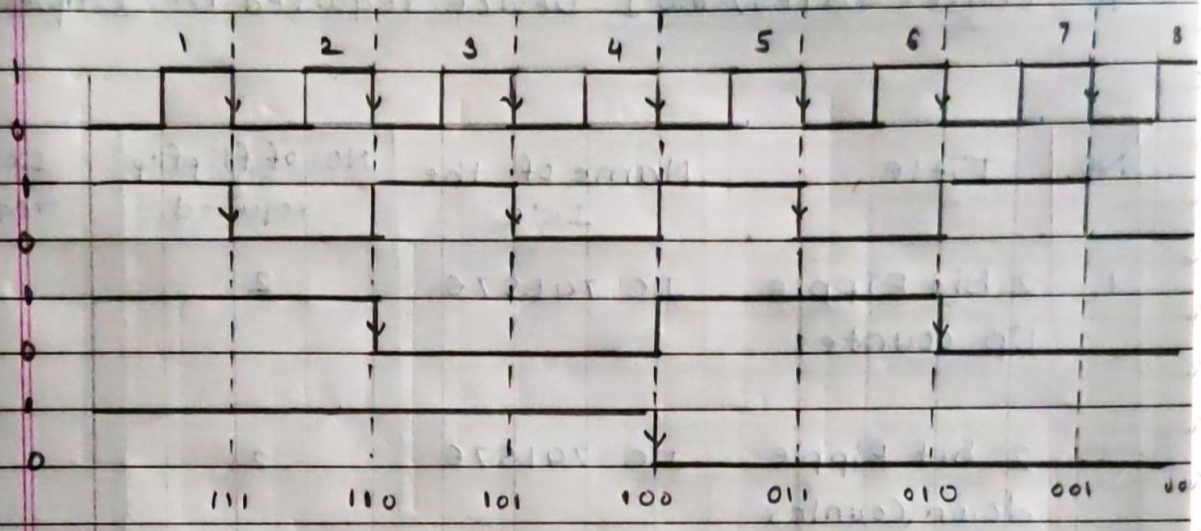
* Observation Table :-

Input	Output		
	Q_A	Q_B	Q_C
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

* Design of 3 bit Ripple Down Counter :-



* Timing Diagram:-



* Observation Table:-

Clock Pulse	Output		
	Q_A	Q_B	Q_C
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

* Logic Gates/MSI Device required for Implementation

No.	Title	Name of the Ic's	No. of flipflop required	Ic's required
1.	2 bit Ripple Up counter	IC 74LS76	2	1
2.	2 bit Ripple down counter	IC 74LS76	2	1
3.	3 bit Ripple Up counter	IC 74LS76	3	2
4.	3 bit Ripple down counter	IC 74LS76	3	2

* Conclusion:

We successfully implemented 2 bit and 3 bit ripple up and down counter on an online digital trainer kit with appropriate output.

3bit up ripple counter

Manish
Logout

OUTPUT SECTION

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 VCC

Power

IC BASE 1
74LS76
74LS76
IC BASE 4
IC BASE 5

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

GND

10 5 1 0.5

HIGH LOW

GENERATE PULSE

DeldSim - Trainer Kit

deldsim.com/simulator/

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3bit ripple down counter

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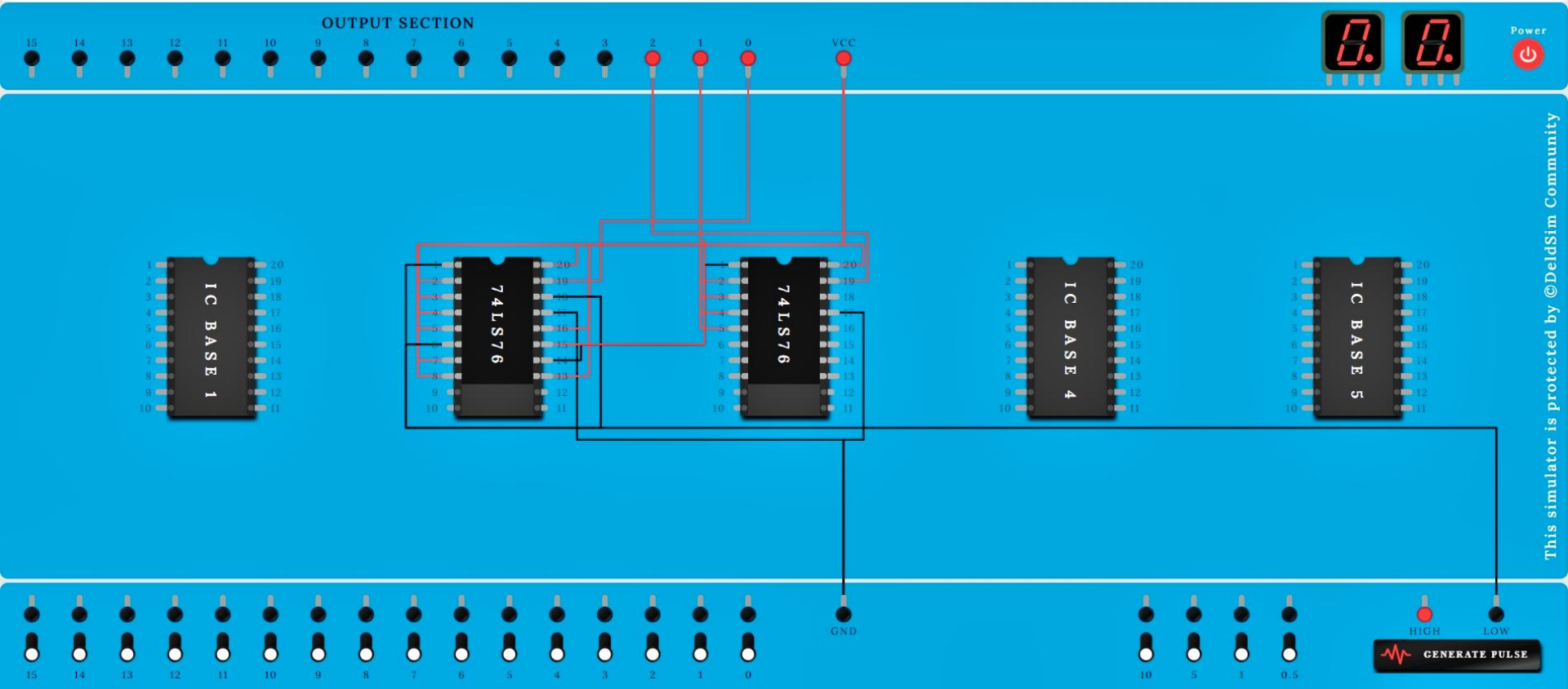

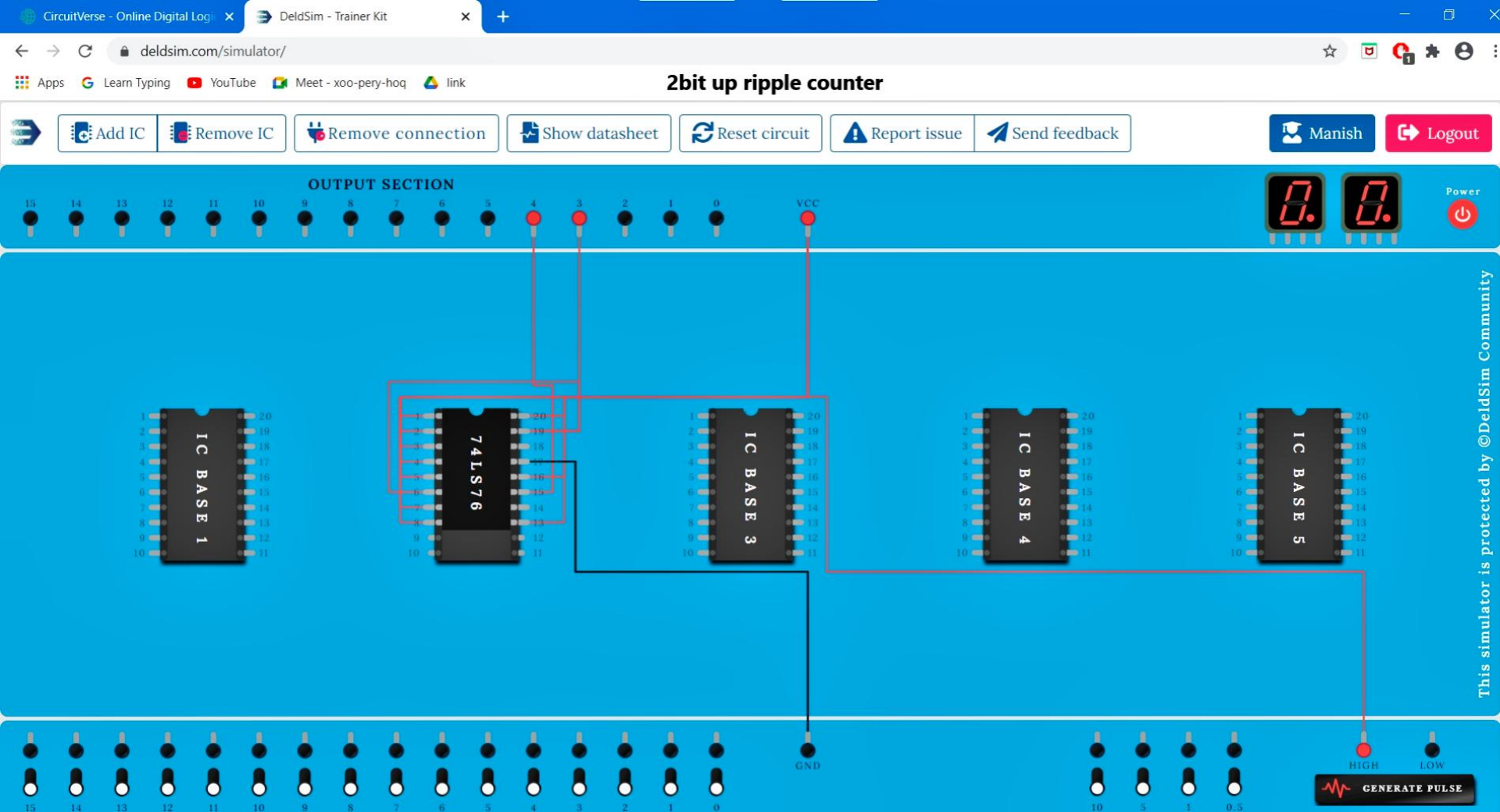
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link
2bit up ripple counter
Add IC
Remove IC
Remove connection
Show datasheet
Reset circuit
Report issue
Send feedback
Manish
Logout
OUTPUT SECTION
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
VCC
Power
IC BASE 1
74LS76
IC BASE 3
IC BASE 4
IC BASE 5
GND
HIGH
LOW
GENERATE PULSE
10 5 1 0.5
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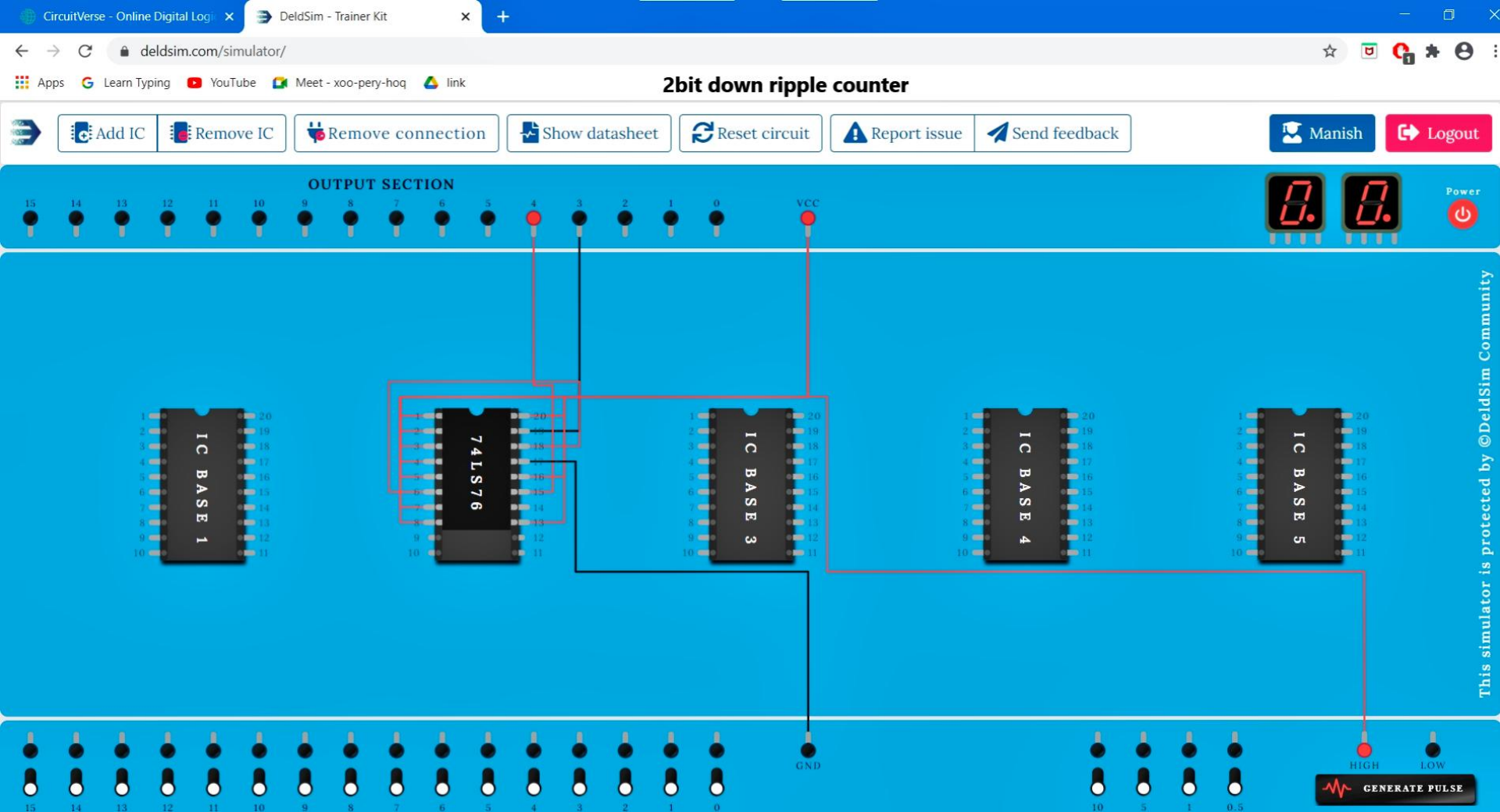
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link
2bit down ripple counter
Add IC
Remove IC
Remove connection
Show datasheet
Reset circuit
Report issue
Send feedback
Manish
Logout
OUTPUT SECTION
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
VCC
Power
IC BASE 1
74LS76
IC BASE 3
IC BASE 4
IC BASE 5
GND
HIGH
LOW
GENERATE PULSE
10 5 1 0.5
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