Assignment 9

Class- SE IV Roll NO - 21430
Batch - F4 DOS - 14/01/2021

Title - Design of 3 bit Synchronous Conter (Up/down)

Objective -:
1. Design and implement 3 bit Synchronous up Counter using IC 74LS76.
2. Design and implement 3 bit Synchronous Down counter using IC74LS76.

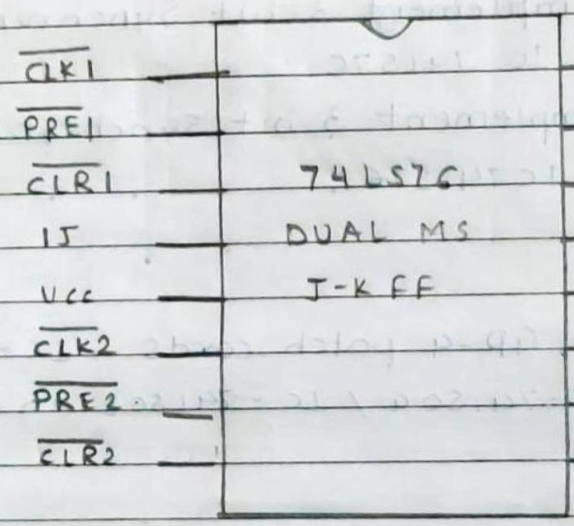
Apparatus -:
Digital board, GP-4 patch cords, IC - 74LS76, IC - 74LS32, IC - 74LS04 / IC - 74LS08 and required logic gates.

Theory -:
1. The ripple counters have the advantages of simplicity (only flip-flops are required) but their speed is low because of ripple action.
2. The maximum time is required when the output changes from 111 ...1 to 000...0 and this limit the frequency of operations of ripple counters.
3. The speed of operation improves significantly if the flipflops are clocked simultaneously.
4. The resulting circuit is known as synchronous counter.
5. Common Clock input is connected to all flipflops, hence each FF is triggered at the same time such

Counters are known as Synchronous Counters

1. Synchronous Up counter
2. Synchronous DOWN counter.
3. Synchronous Up-DOWN counder.

* PIN DIAGRAM-:



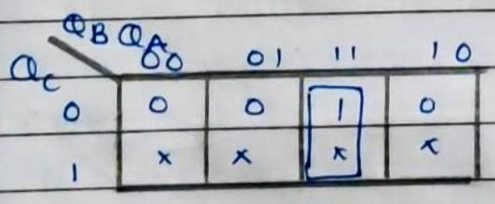
* Procedure-:
1. Make connections as per logic circuit of 3-bit Synchronous up counter using IC-74LS76 and verify its truth table.
2. Make connections as per logic circuit of 3 bit Synchronous DOWN counter using IC-74LS76 and verify its truth table.

* Synchronous 3 bit up Counter-
for 3 bit counter, we need 3 flip-flops

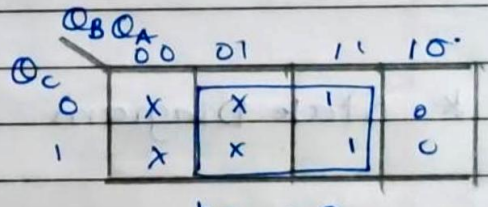
Truth Table-:

Present State			Next State			Flip-Flop Inputs					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	1	1	x	x	1
1	1	0	1	1	1	x	x	x	0	1	x
1	1	1	0	0	0	x	x	x	1	x	1

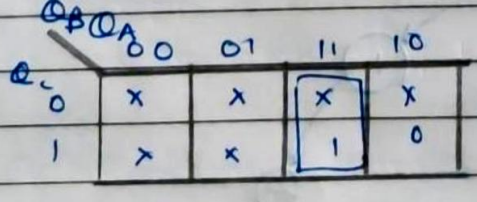
* K-map Simplification :-



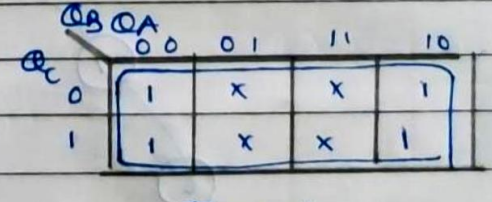
$J_C = Q_B . Q_A$



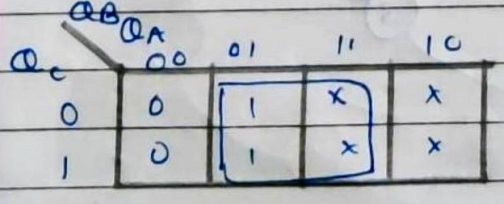
$K_B = Q_A$



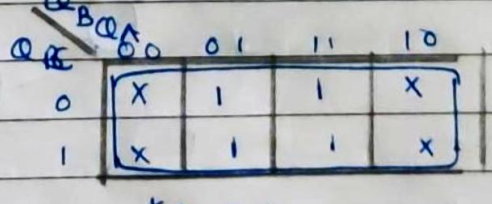
$K_C = Q_B . Q_A$



$J_A = 1$

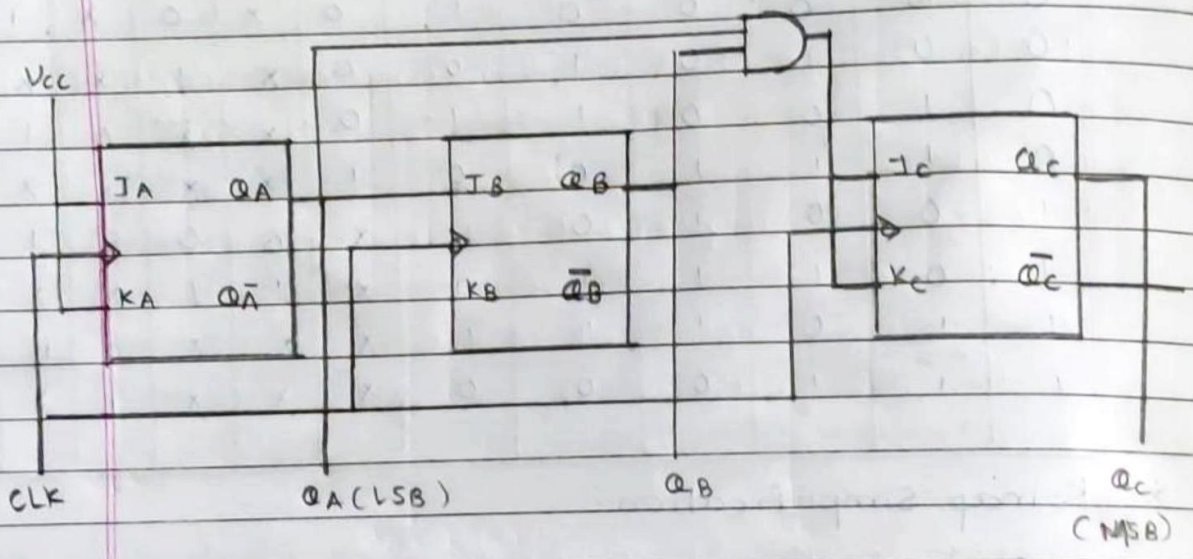


$J_B = Q_A$

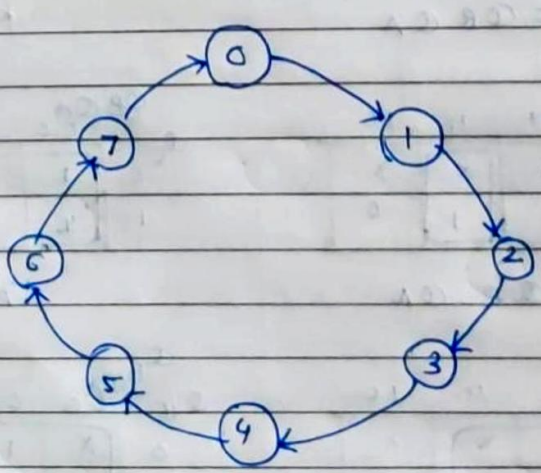


$K_A = 1$

* Logic Diagram :-



* State Diagram.



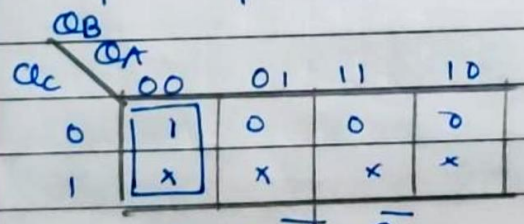
* Synchronous 3 bit DOWN Counter :-

For 2-bit counter, we need 3 flip flops.

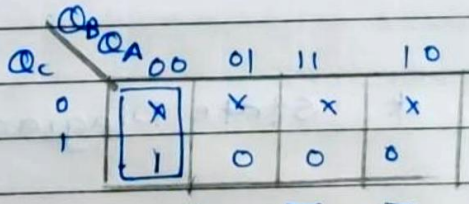
Truth Table:-

Present State			Next State			flip flop Inputs					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	1	1	1	1	x	1	x	1	x
1	1	1	1	1	0	x	0	x	0	x	1
1	1	0	1	0	1	x	0	x	1	0	x
1	0	1	1	0	0	x	0	0	x	x	1
1	0	0	0	1	1	x	1	1	x	1	x
0	1	1	0	1	0	0	x	x	0	x	1
0	1	0	0	0	1	0	x	x	1	1	x
0	0	1	0	0	0	0	x	0	x	x	1

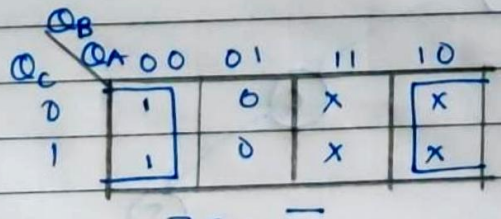
* K-Map Simplification:-



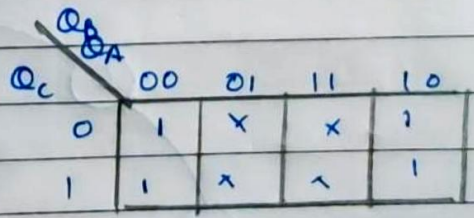
$J_C = \overline{Q_B} \cdot \overline{Q_A}$



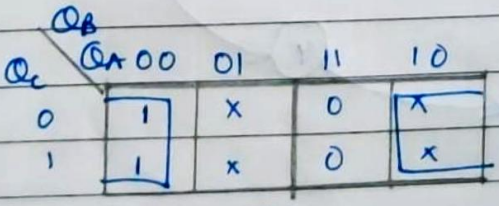
$K_C = \overline{Q_B} \cdot \overline{Q_A}$



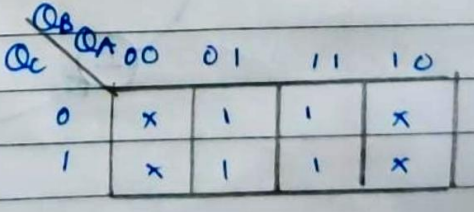
$J_B = \overline{Q_A}$



$J_A = 1$

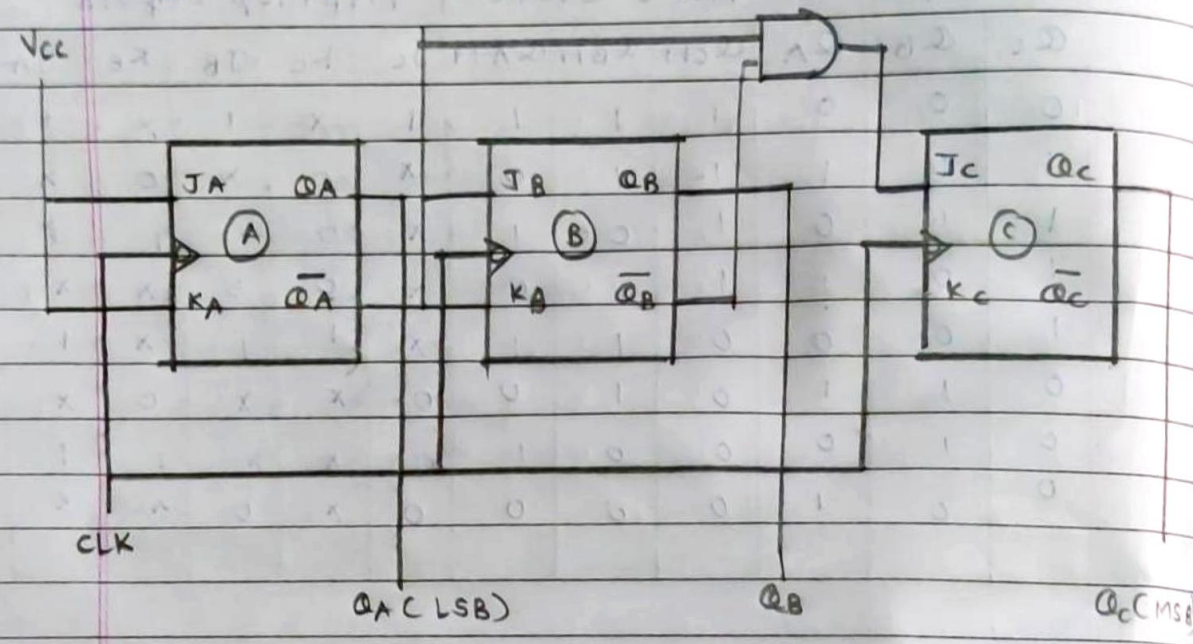


$K_B = \overline{Q_A}$

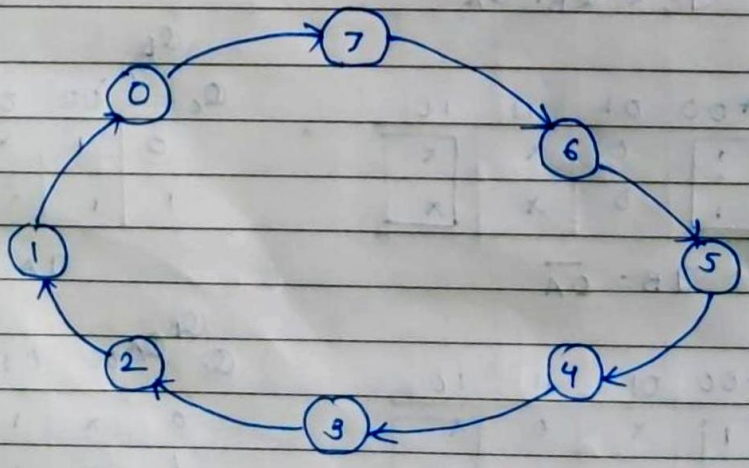


$K_A = 1$

* Logic Diagram :-



* State Diagram



* Logic Gates required for implementation :-

NO.	Title.	Name of Ic	NO. of FlipFlop Gates required	Ic required
1.	3 bit up synchronous counter	Ic 7476 IC 7400	3FF 1 AND Gate	2 Ic 7476 1 Ic 7408
2.	3 bit DOWN synchronous counter	Ic 7476 IC 7408	3 FF 1 AND Gate	2 Ic 7476 1 Ic 7408

* Conclusion.

Succesfully implemented 3 bit synchronous up and DOWN counter using IC-7476 on an online digital trainer kit with appropriate circuit & output.

3bit synchronous down counter

Manish Logout

OUTPUT SECTION

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 VCC

Power

IC BASE 1

74LS76

74LS76

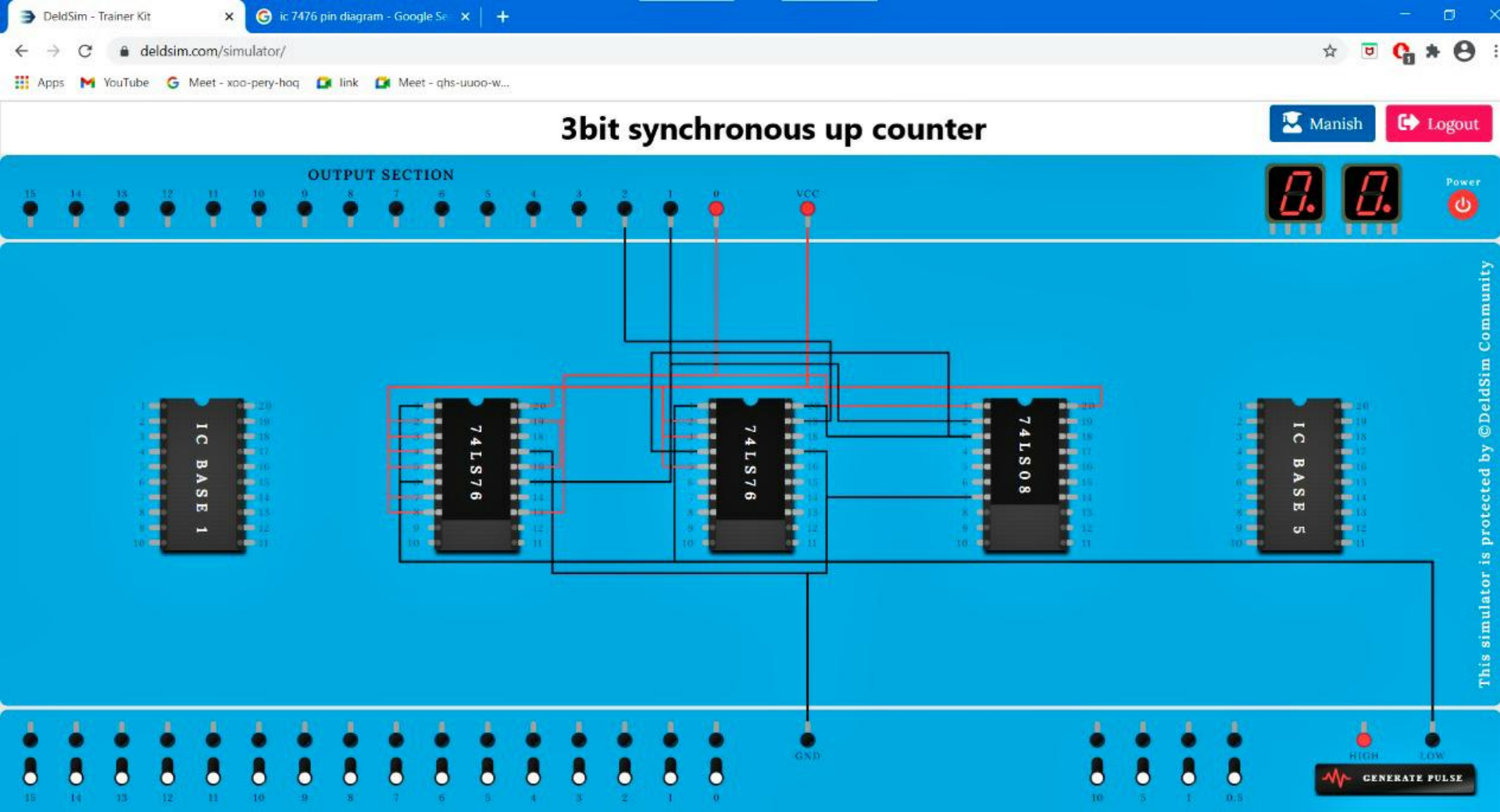
74LS08

IC BASE 5

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 GND

10 5 1 0.5 HIGH LOW

GENERATE PULSE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ic 7476 pin diagram - Google Se
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Apps
YouTube
Meet - xoo-pery-hoq
link
Meet - qhs-uuoo-w...
3bit synchronous up counter
Manish
Logout
OUTPUT SECTION
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
VCC
Power
IC BASE 1
74LS76
74LS76
74LS08
IC BASE 5
GND
HIGH
LOW
GENERATE PULSE
10 5 1 0.5
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