Assignment 3

Class - SE IV
Batch - F4

ROLL NO - 21430
D.O.S - 5/12/2020

Title - Design and realization of BCD Adder using 4 bit binary Adder (IC 7483)

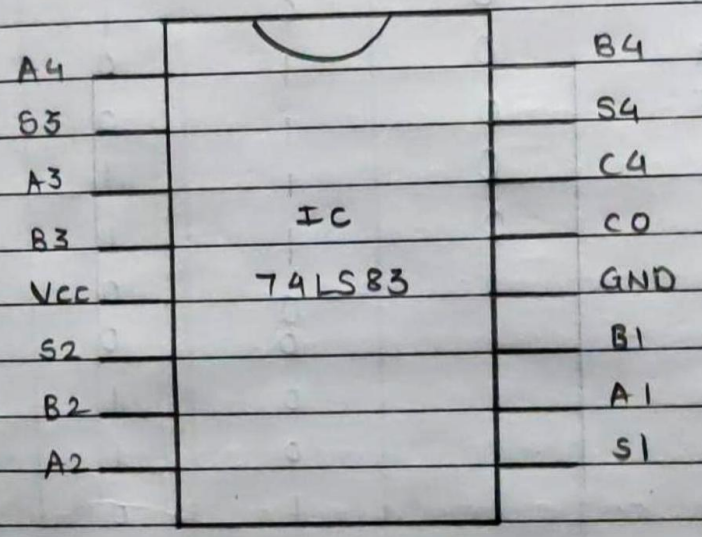
Objective:
1. Design and implement BCD Adder circuit using IC - 74LS83
2. Design and Implement 9's complement circuit using IC - 74LS83

Apparatus -
Digital - Board, GP - 4 patch - cords, IC - 74LS83, IC - 74LS04 / IC - 74LS08 and required logic gates if any.

Theory -:
IC 74LS83 is a 4 bit binary parallel adder. By using 74LS83 we can implement BCD adder. BCD means binary coded decimal. BCD numbers are valid from 0 to 9. for BCD adder when addition is below 9, carry is 0 result is valid BCD. When addition is more than 9 and carry is 0 as well as when addition is more than 15 and carry is 1 result of binary Adder IC is Invalid BCD. We can convert invalid BCD to Valid BCD by adding six. Max addition

result is 18 if carry is 0 and 19 if carry input is 1. Thus for binary results greater than 9 six should be added to the result as correction factor using combination circuit.

PIN Diagram:-



Procedure

1. Make the connections as per the Logic circuit of 1 digit BCD adder using IC 74LS83 and verify its Truth Table
2. Make the connections as per the Logic circuit of 9's complement circuits using IC 74LS83 and verify the Truth Table

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Truth Table

Dec. Eqn	S4	S3	S2	S1	Tens place
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

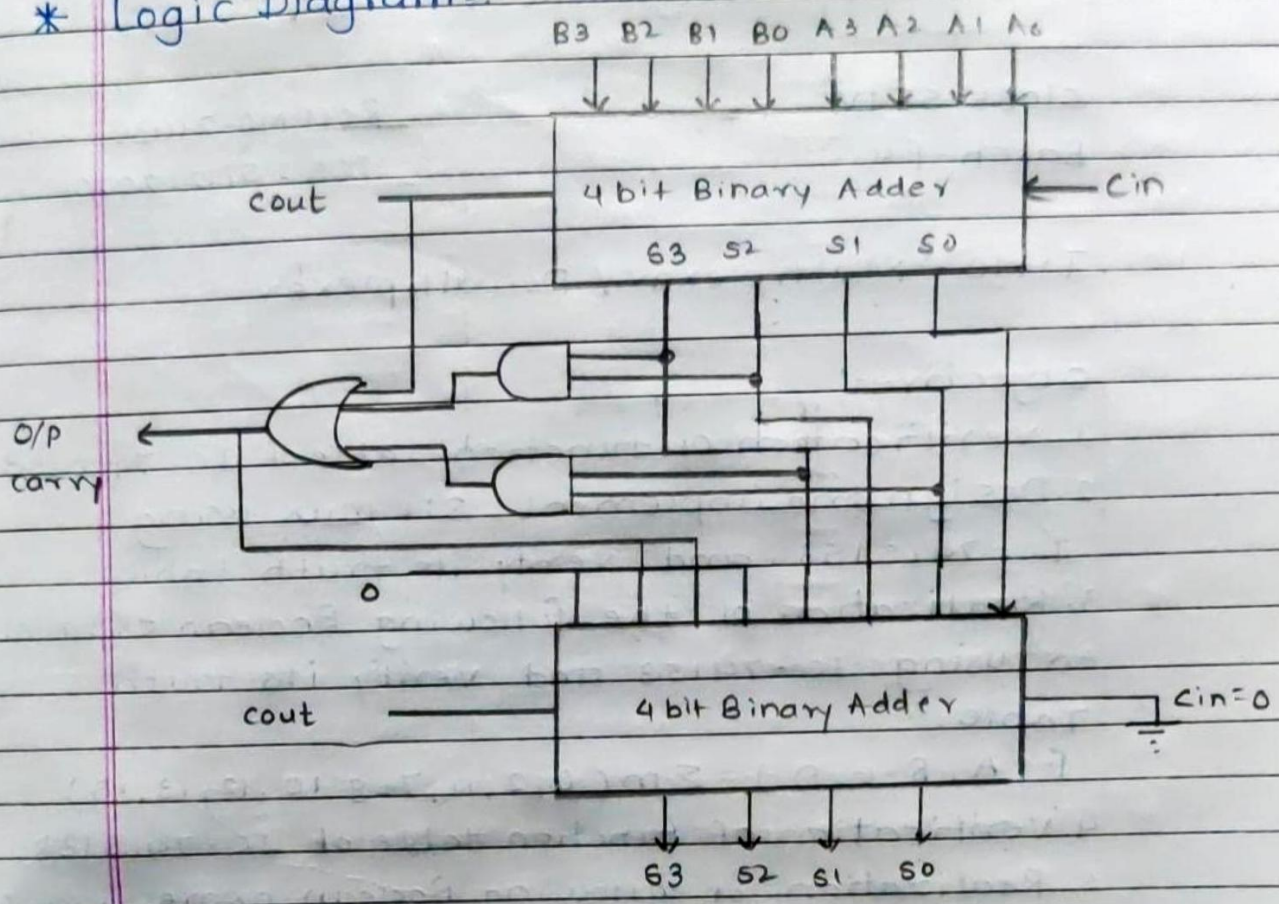
* K-map simplification

S_4S_3 \ S_2S_1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

$\therefore Y = S_4S_3 + S_4S_2$

$\therefore Y = S_4(S_2 + S_2)$

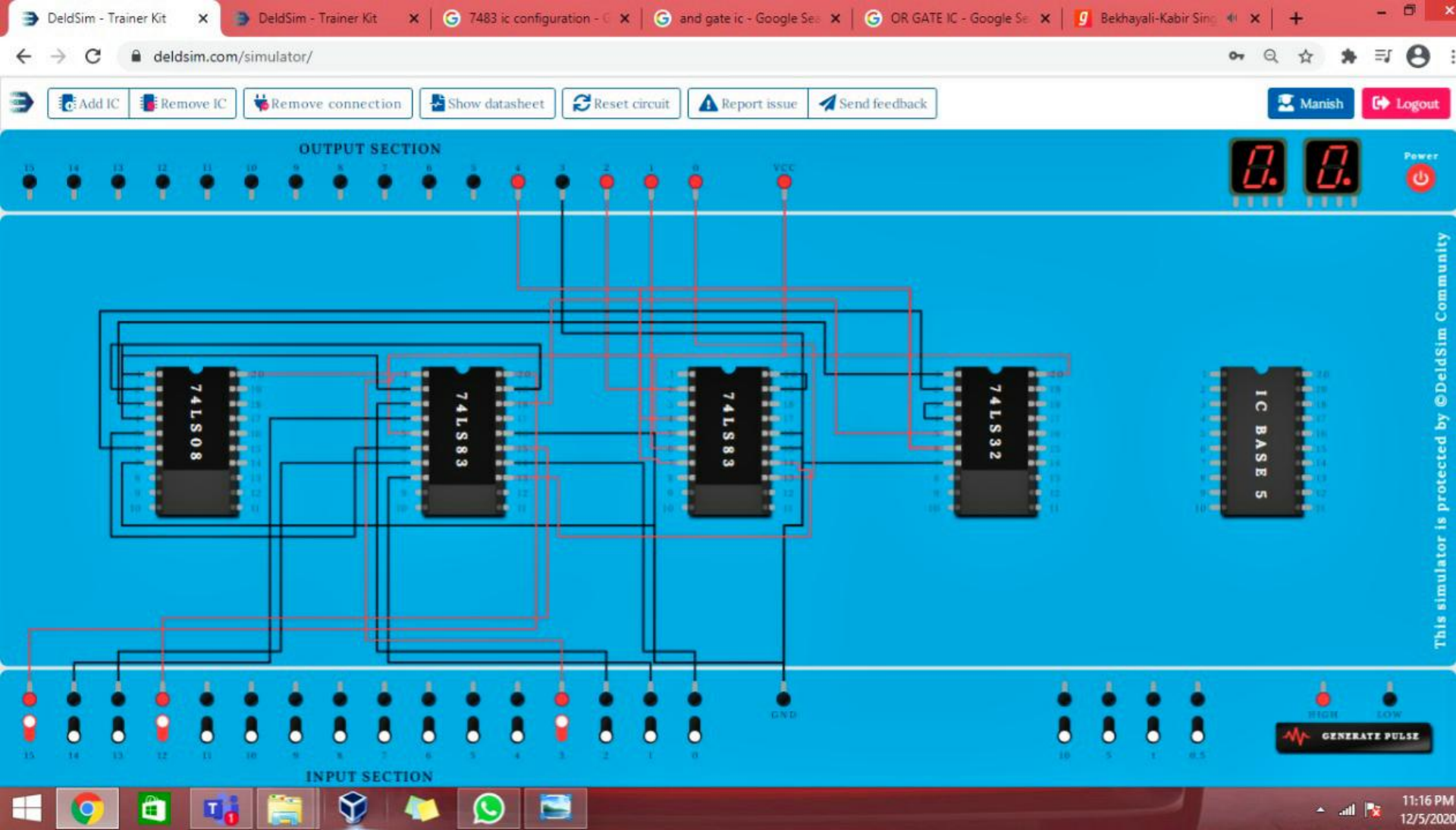
* Logic Diagram :-



* Logic Gates/MSI Devices required for Implementation :-

NO.	Title	Name of IC	No. of gates required	IC required
1.	BCD Adder Circuit	IC 7483	2	2
		IC 7408	1	1
		IC 7432	3	1

Conclusion :-
We learnt to implement BCD Adder circuit using IC74LS83 Successfully.


DeldSim - Trainer Kit
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7483 ic configuration -
and gate ic - Google Sea
OR GATE IC - Google Se
Bekhayali-Kabir Sing
deldsim.com/simulator/
Add IC
Remove IC
Remove connection
Show datasheet
Reset circuit
Report issue
Send feedback
Manish
Logout
OUTPUT SECTION
Power
74LS08
74LS83
74LS83
74LS32
IC BASE 5
This simulator is protected by ©DeldSim Community
GND
HIGH
LOW
GENERATE PULSE
INPUT SECTION
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