Assignment 13

Class - SE IV
Batch - F4

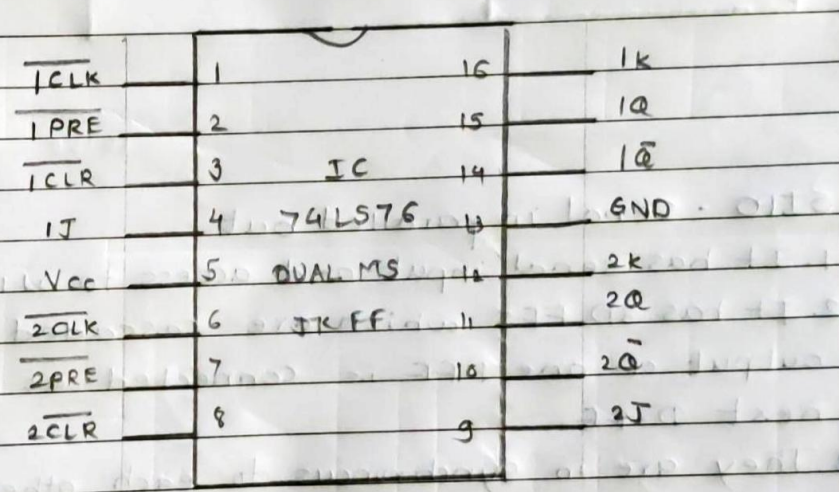
Roll NO - 21436
DOS - 14/01/2021

Title - Study of Shift register (SISO, SIPO, PISO, PIPO)

Objective : To study Shift register SISO, SIPO, PISO, PIPO.

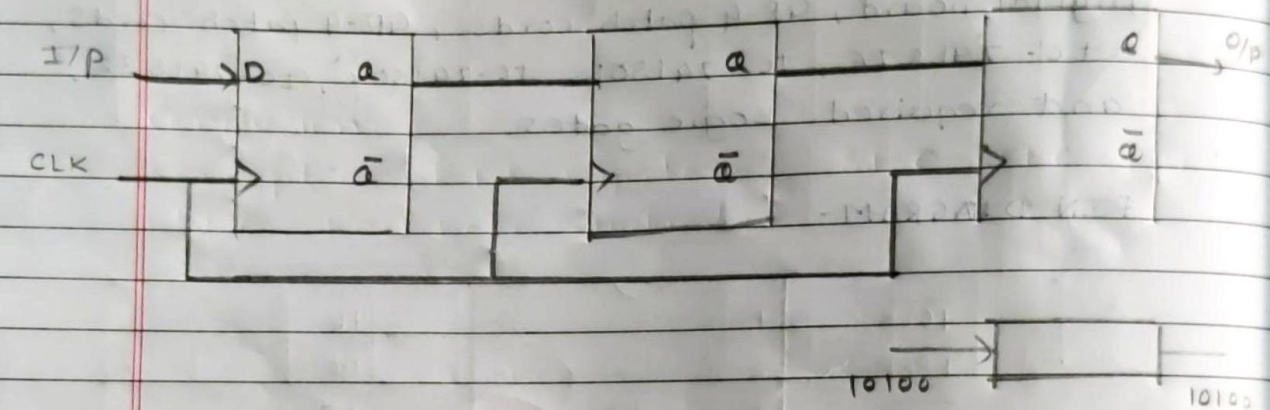
Apparatus :
Digital board, GP-4 patch cords, GP-4 patch cords, IC-74LS76, IC-74LS08, IC-74LS04, IC-74LS32, and required Logic gates.

PIN DIAGRAM -

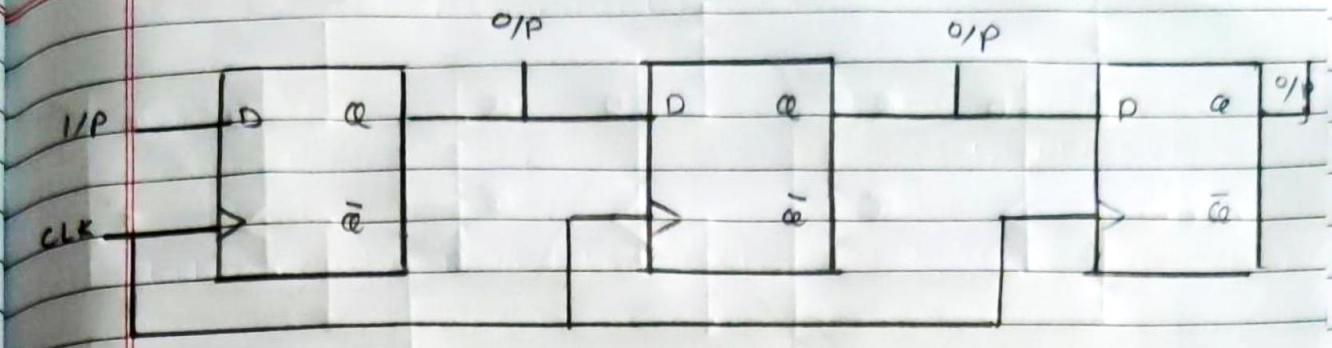


Theory :
i) SISO - Serial in serial out
1. It has a single input and single output.
2. It's block diagram has 3 D Flip-flops connected as input of next D-FF.

iii. They are in synchronous with each other
iv. In this shift register we can send the bits serially from i/p of left most D-flip-flop Hence, this i/p is called serial input. for every positive edge triggering of clock signal the data shifts from one stage to next so we can receive bits serially from output of right most D flip-flop hence, called as serial output.

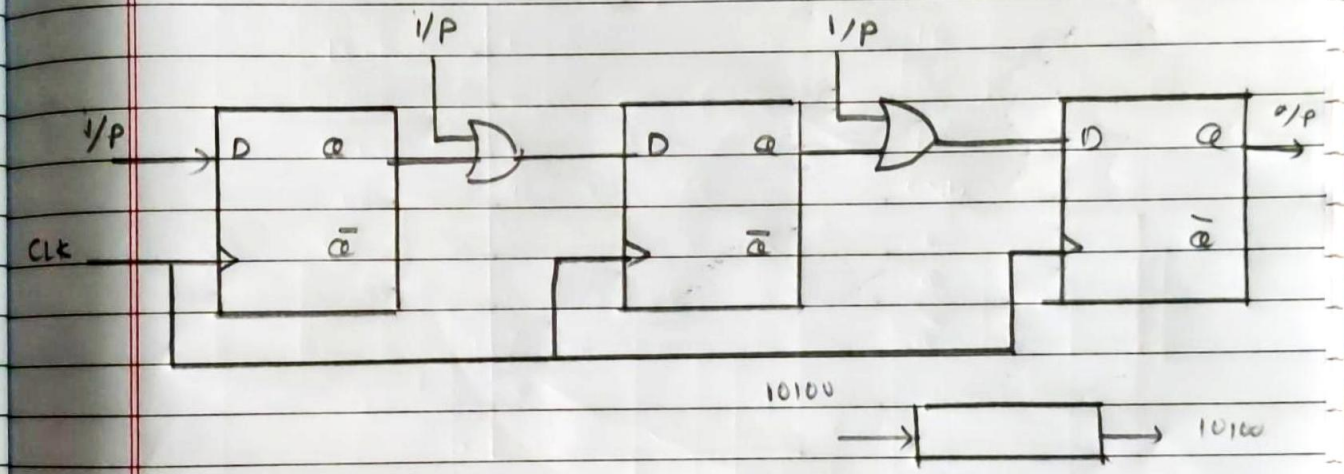


* SIPO - Serial in paralled out
1. It has serial input and access to all output
2. It has 3D FFs which are cascaded that mean output of one DFF is connected as input of next D-FF.
3. They are in synchronous to each other.
4. In this we can send the bits serially from i/p of left most FF. Hence i/p is called serial i/p.
5. In this we can access the o/ps of each DFF in parallel so we will get parallel o/p s.



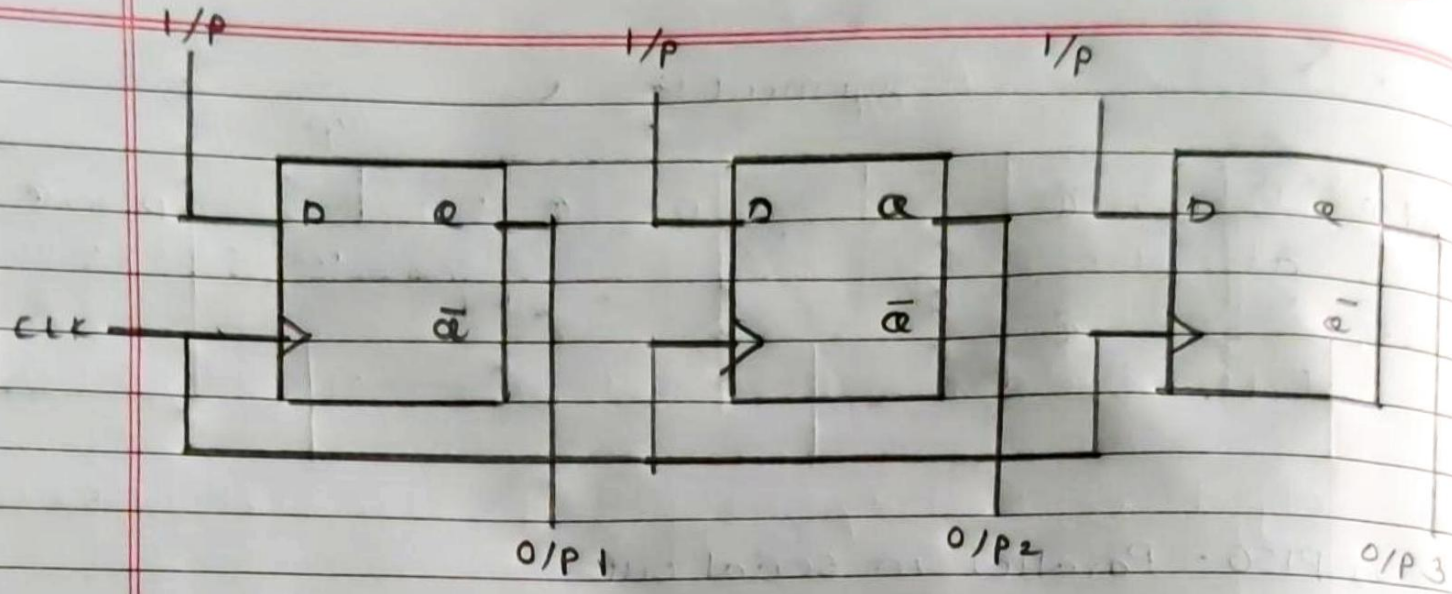
3) PISO - Parallel in serial out.

1. It has 3 D FF's cascaded.
2. We can apply parallel input to each D flipflop by making present & enable to 1.
3. for every positive edge triggering of clock signal the data shifts from one stage to next. So we will get serial output from right most D flip-flop



4. PIPO - Parallel in parallel out.

1. All i/p s are loaded simultaneously and are available at the o/p simultaneously.
2. It has simplest configuration and represents a memory device



Conclusion :-

Concept of shift registers : SISO, SIPO, PIPO, PISO, has been studied.