Assignment 6

Class- SE IV
Batch - F4

Roll NO-21430
DOS - 5/12/2020

Title- Parity generator and checker

Objective-:
Design and implement parity generator and checker using EX-OR

Apparatus : Digital trainer kit, IC-7486 (EX-OR) IC-7480 patch cord, +5 power supply etc.

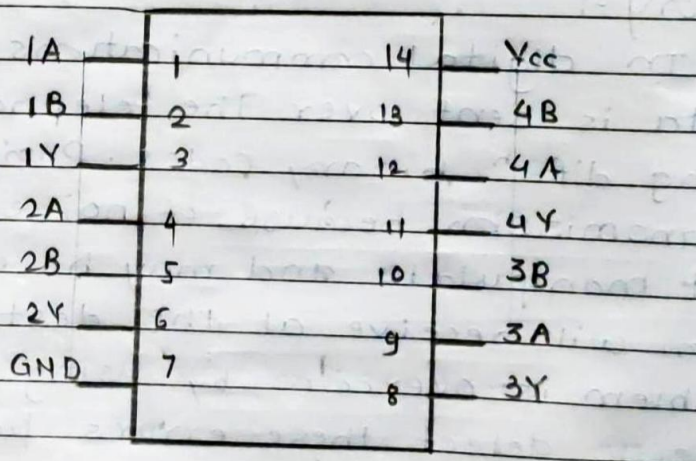
Theory-1
Ans: In digital communications, the digital data is sent over the telephone lines using diff^n binary codes. During the transmission because of noise signal may get manipulate and may be wrong information will receive at the destination. This problem is overcome by using error detecting code. To detect these errors parity bit is usually transmitted along with the data bits.
Parity generator - It is combinational logic circuit that generates the parity bit in the transmitter.

Parity checker :- It is a circuit that checks the parity in the receiver.
Parity generator and checker device are commonaly used in digital system to detect the single bit error.

Even parity - Added parity will make total no of 1's even.

odd parity - Added parity will make total no of 1's odd.

* PIN DIAGRAM :-



* Procedure :-
1. Design logic circuit of even-odd parity generator and checker using truth table
2. Implement the circuit by making connections as per logic diagram

* Truth Table :-

i. Even parity ~~checker~~ generator :-

A	B	C	Parity
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

ii. odd parity generator

A	B	C	Parity
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Even parity checker

A	B	C	P	output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-Map for Even parity checker

AB \ CP	00	01	11	10
00	0	(1)	0	(1)
01	(1)	0	(1)	0
11	0	(1)	0	(1)
10	(1)	0	(1)	0

$Y = \bar{A}\bar{B}(\bar{C}P + C\bar{P}) + \bar{A}B(\bar{C}\bar{P} + CP) + AB(\bar{C}P + C\bar{P}) + A\bar{B}(\bar{C}\bar{P} + CP)$

$= ((C \oplus P)(A \odot B) + (C \odot P)(A \oplus B)$

$Y = A \oplus B \oplus C \oplus P$

Odd parity checker

A	B	C	P	output
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

* K-Map for odd ~~Eve~~ parity checker

AB \ CP	00	01	11	10
00	(1)	0	(1)	0
01	0	(1)	0	(1)
11	(1)	0	(1)	0
10	0	(1)	0	(1)

$Y = \bar{A}B(c \oplus P) + A\bar{B}(c \oplus P) + AB(c \odot P) + \bar{A}\bar{B}(c \oplus P)$

$= (c \oplus P)(A \oplus B) + c \odot P(A \odot B)$

$= A \odot B \odot c \odot P$

* K-Map for Even parity generator

A \ BC	00	01	11	10
0	0	(1)	0	(1)
1	(1)	0	(1)	0

$\therefore Y = A \oplus B \oplus C$

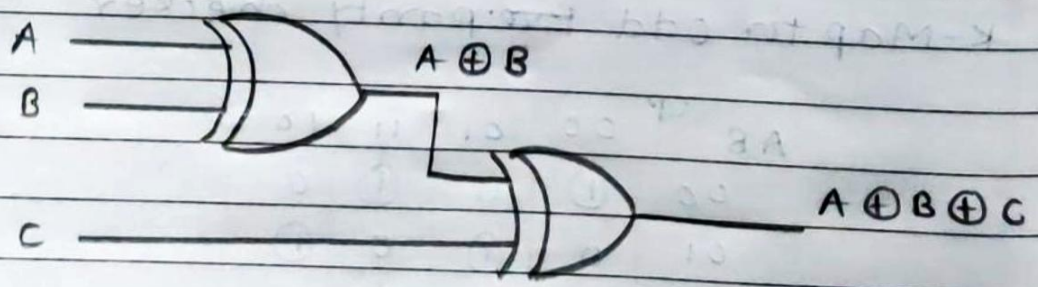
* K-Map for odd parity generater

A \ BC	00	01	11	10
0	(1)	0	(1)	0
1	0	(1)	0	(1)

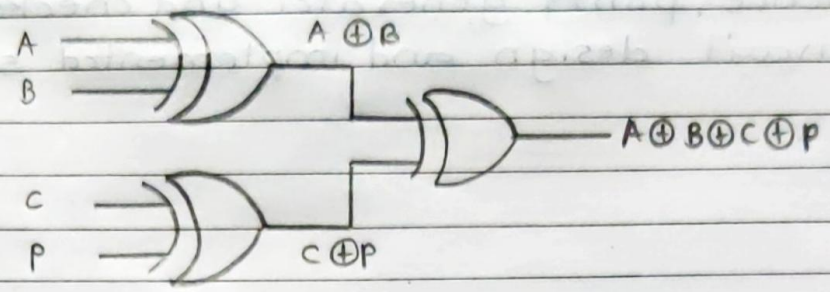
$\therefore Y = A \odot B \odot C$

* Logic Diagram

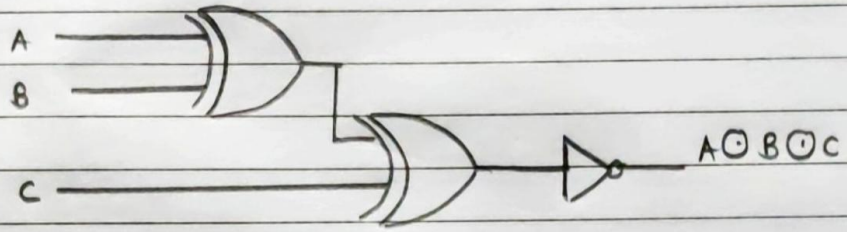
i. Even parity generater :-



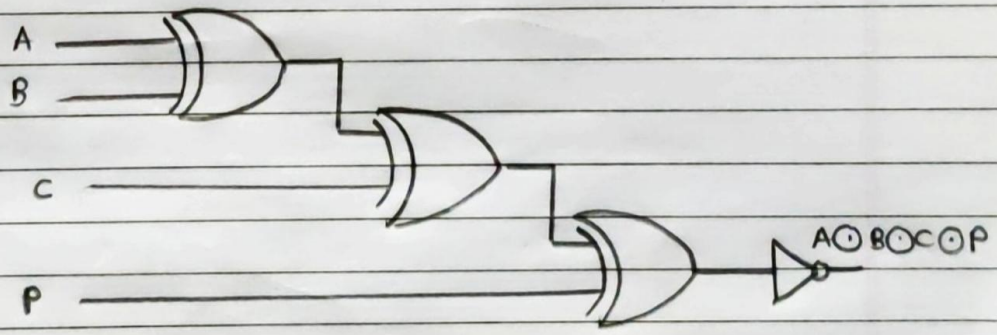
2. Even parity checker -



3. Odd parity generator :



4. Odd parity checker :



* Logic gates required for implementation :
1. Even parity checker - 3 EX-OR gate
2. Even parity generator - 2 EX-OR gate
3. Odd parity generator - 2 EX-OR, 1 NOT gate
4. Odd parity checker - 3 EX-OR, 1 NOT gate

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Conclusion -:

Hence, parity generator and checker circuit design and implemented succesfully.

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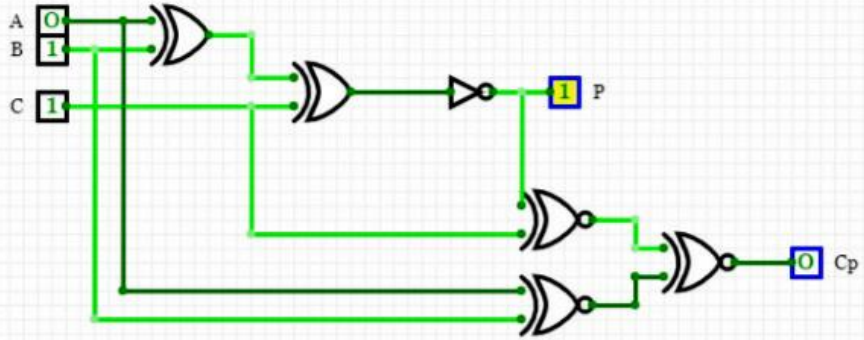
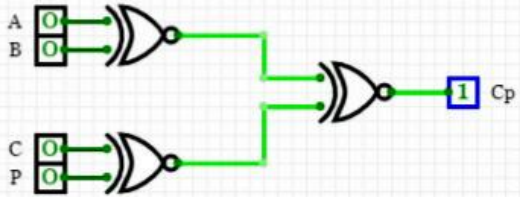
Main





- Decoders & Plexers
- Sequential Elements
- Memory Elements
- Test Bench
- Misc

PROPERTIES

OUTPUT

BitWidth: 1

Delay: 0

Label: P

Label Direction: RIGHT

Orientation: LEFT

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Main

- Gates
- Decoders & Plexers
- Sequential Elements
- Memory Elements
- Test Bench
- Misc

PROPERTIES

OUTPUT

BitWidth: 1

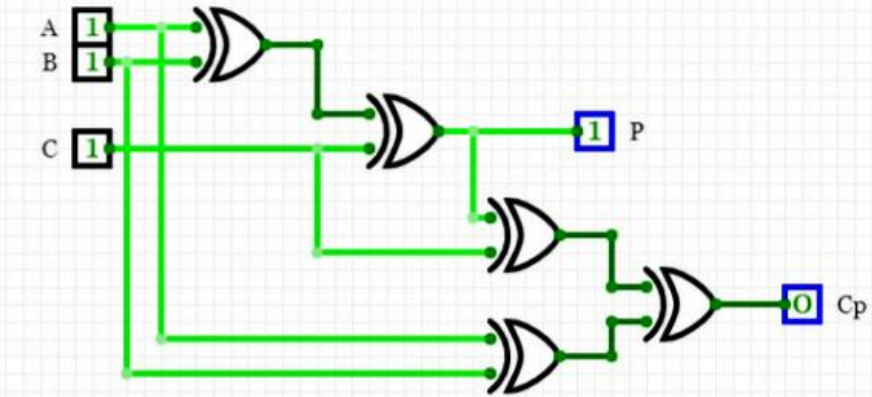
Delay: 0

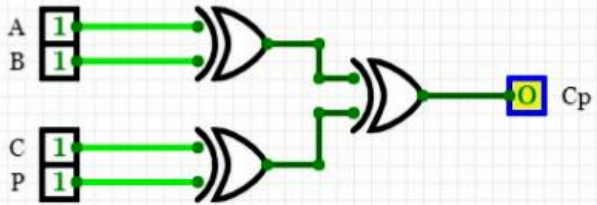
Label: Cp

Label Direction: RIGHT

Orientation: LEFT

Help





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