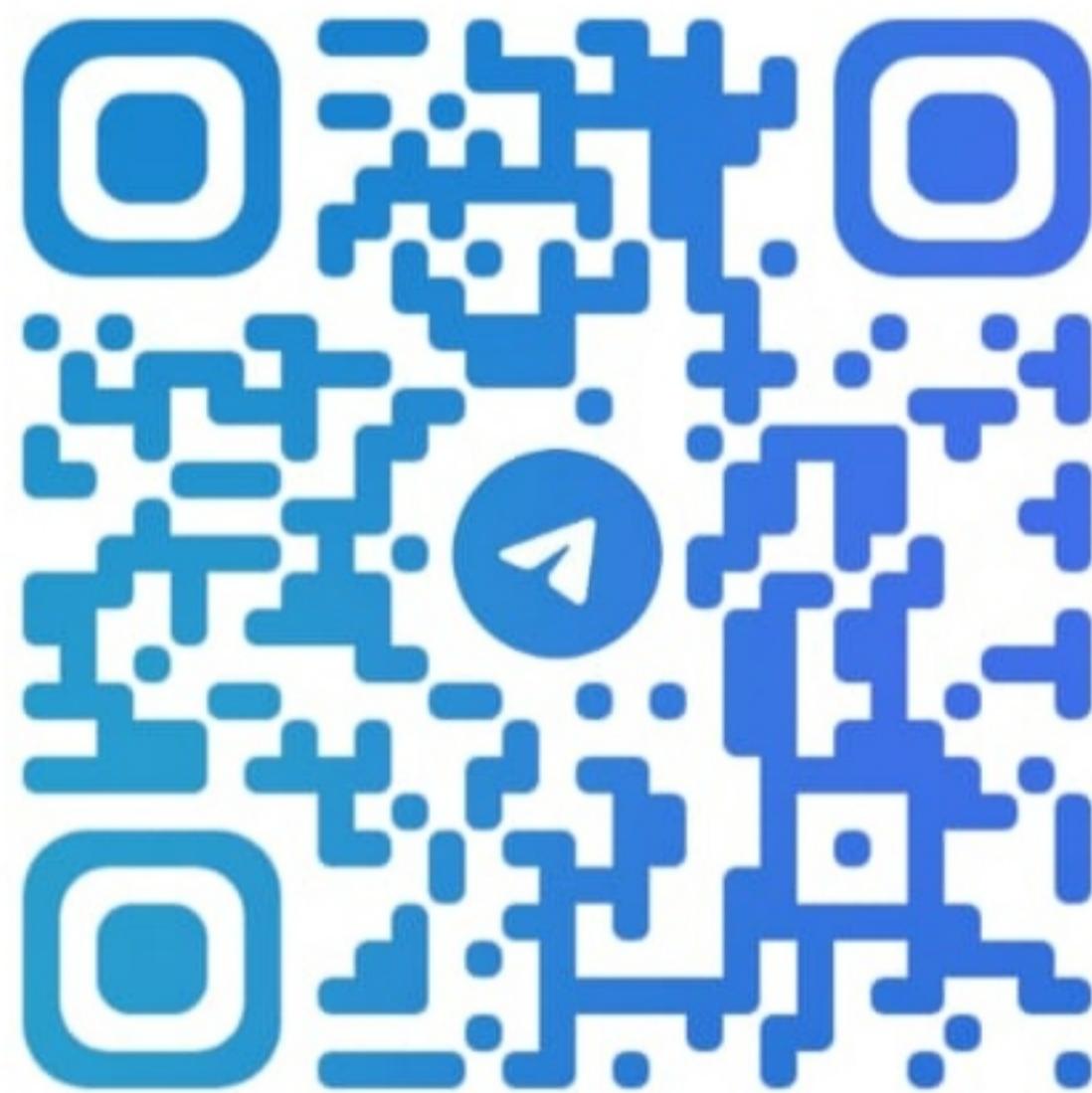


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UNIT 2

Transistor and OPAMP

Syllabus

Unit II

Transistor and OPAMP

[7L]

- **Bipolar Junction Transistor : Construction, type, Operation, V-I Characteristics, region of operation, BJT as switch and CE amplifier**
- **Metal Oxide Semiconductor Field Effect Transistors (MOSFET): Construction, Types, Operation, V-I characteristics, Regions of operation, MOSFET as switch & amplifier.**
- **Operational amplifier:** Functional block diagram of operational amplifier, ideal operational amplifier, Op-amp as Inverting and Non inverting amplifier

Singad College of Engineering, Pune – 41.

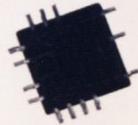
Department of Electronics & Telecommunication Engineering

Introduction

- The semiconductor device like a diode cannot amplify a signal, therefore its application area is limited.
- The next development of semiconductor device after diode is a BJT (bipolar junction transistor).
- It is a three terminal device. The terminals are – collector, emitter, and base. Out of which the base is a control terminal.
- A signal of small amplitude applied to the base is available in the “magnified” form at the collector of the transistor.
- Thus the large power signal is obtained from a small power signal.

Pictorial History of Transistors

1967



1957



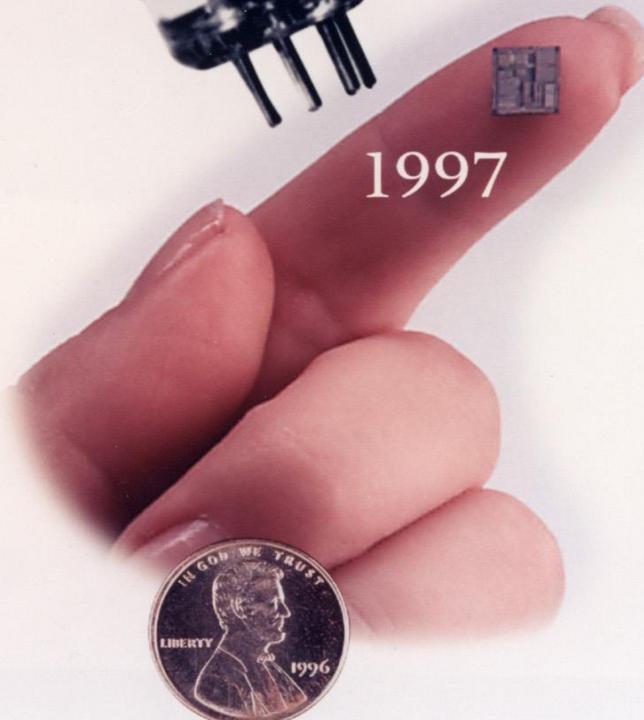
1941



1948



1997



1955



Why is it called transistor ?

- The term transistor was derived from the words **TRANSFER & RESISTOR.**
- Transfers input signal current from a low resistance path to a high resistance path.

Why it is called as a “Bipolar” transistor ?

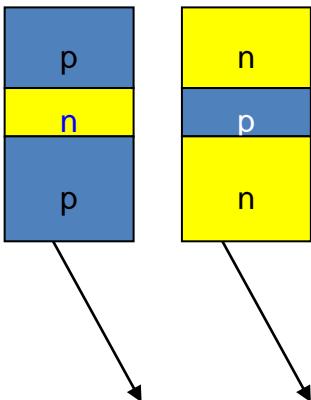
- The conduction in a bipolar junction transistor takes place due to both, ELECTRONS and HOLES
- A transistor is a Current operated device.
- The input impedance of a transistor is HIGH
- The example of a unipolar device is the field effect transistor (FET)

Types of transistor

- The bipolar transistors are of two types :
- P-N-P Transistor
- N-P-N Transistor
- All three regions are provided with terminals which labeled as
E (emitter),
B (Base), and
C (collector)

Emitter :

- It is a region situated in one side of transistor, which supplies charge carriers (i.e. electrons and holes) to the other two regions
- The emitter is heavily doped region



Base :

- It is a middle region that forms two P-N junctions in the transistor.
 - the base of transistor is thin as compared to Emitter.
- And it is lightly doped region

collector :

- It is situated in the other side of transistor (i.e. Opposite to the emitter), which collect charge carriers (electrons or holes)
- The collector of a transistor is always larger than the emitter and base of transistor.
- The doping level of the collector is intermediate between the heavy Doping of emitter and light doping of the base

- Doping Level

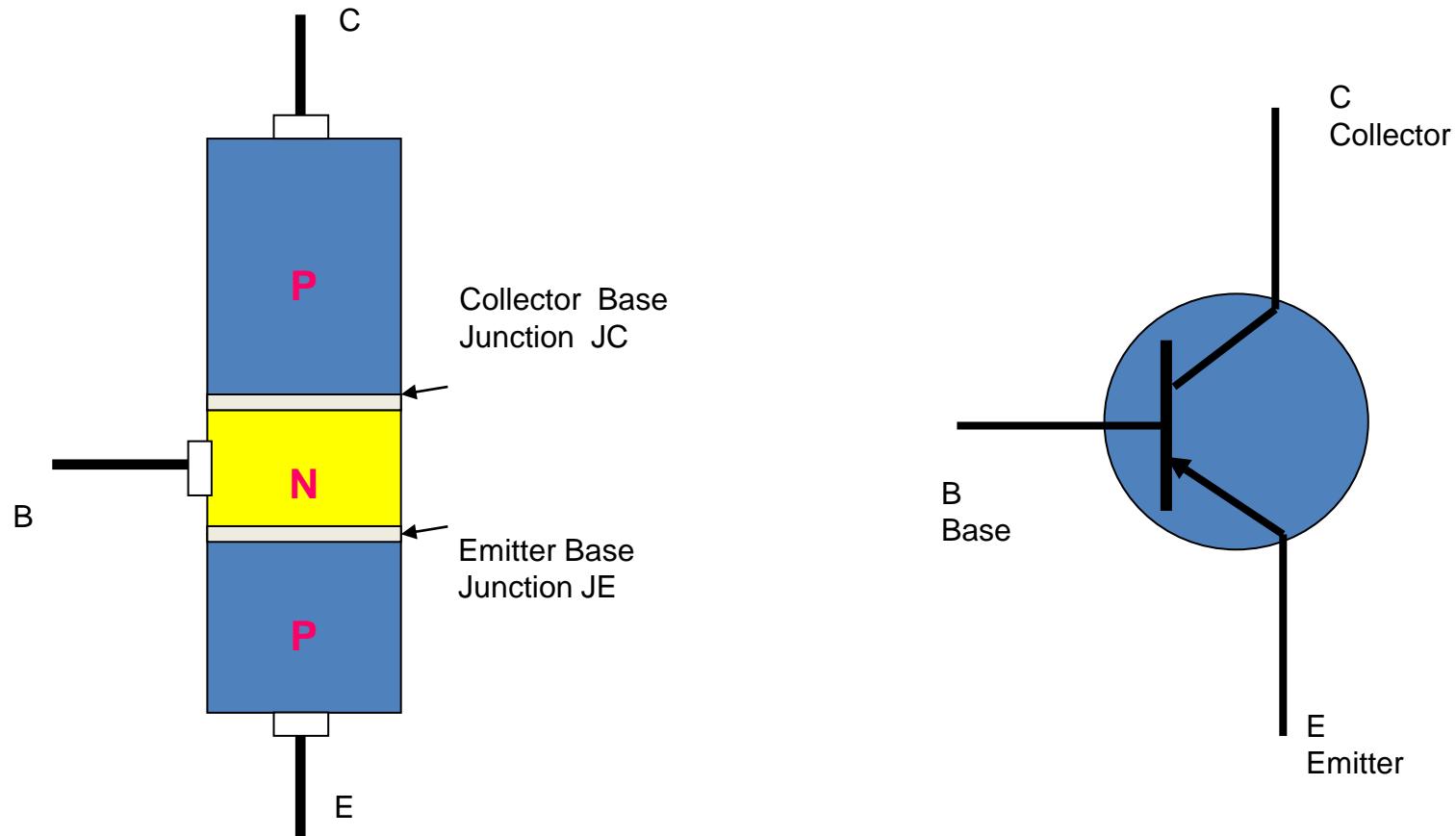
Emitter > Collector > Base

- Area or Size

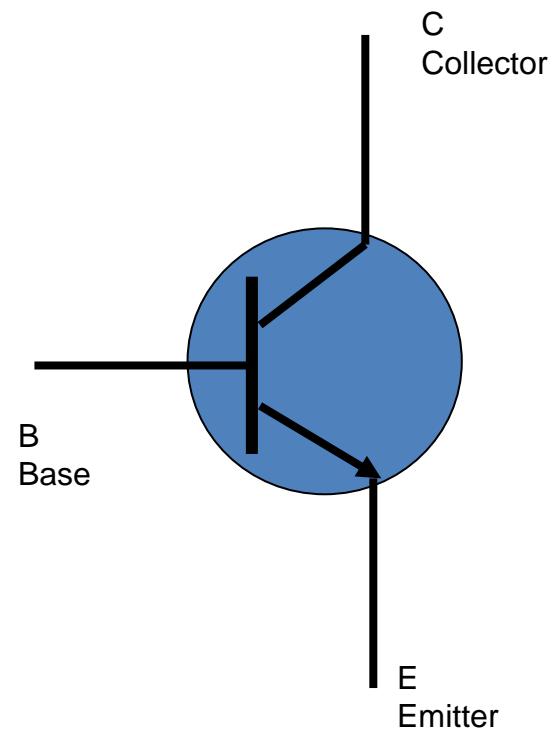
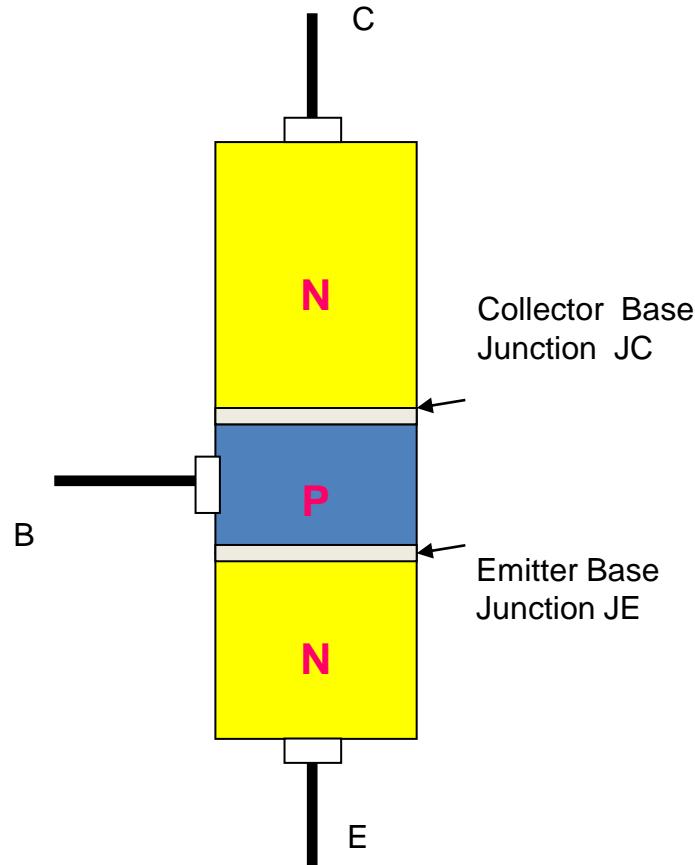
Collector > Emitter > Base

Base is Thin & Lightly Doped

P-N-P transistor



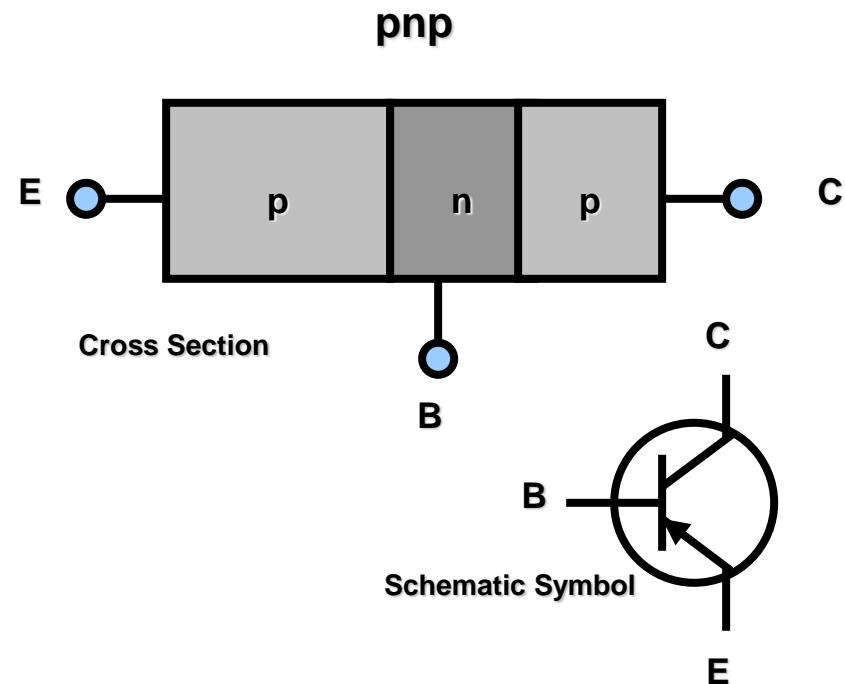
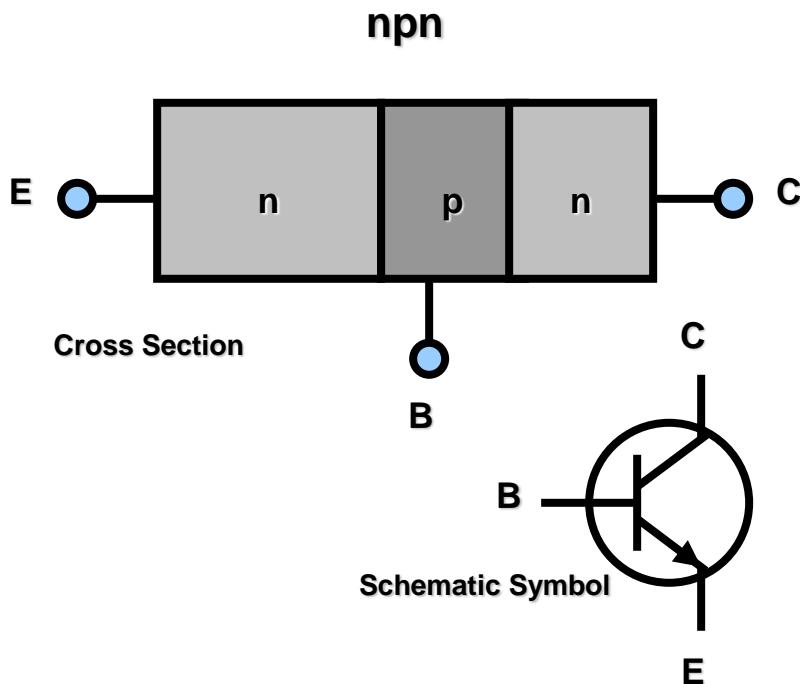
N-P-N transistor



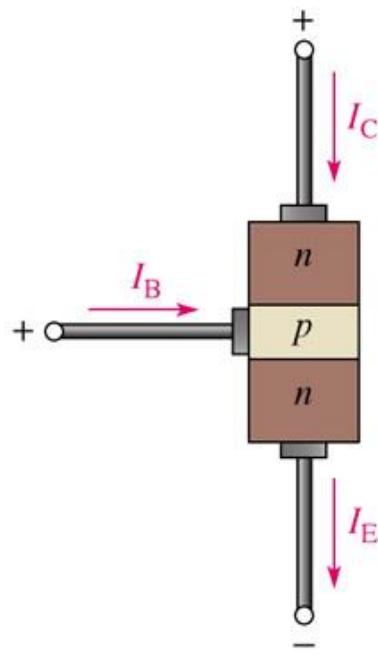
The BJT – Bipolar Junction Transistor

Note: Normally Emitter layer is heavily doped, Base layer is lightly doped and Collector layer has Moderate doping.

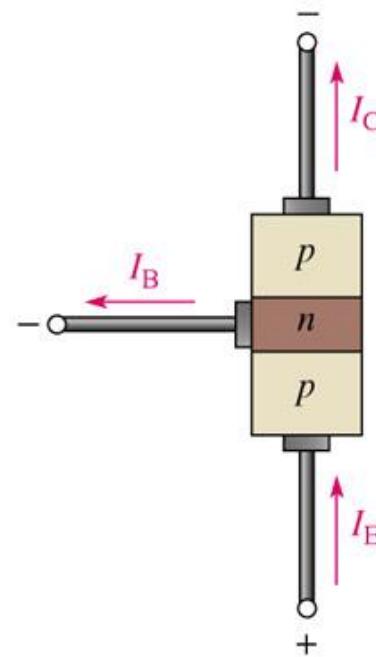
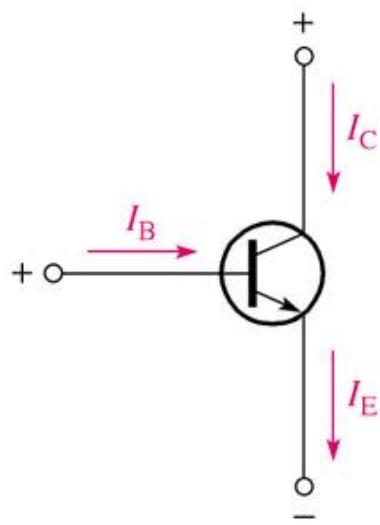
The Two Types of BJT Transistors:



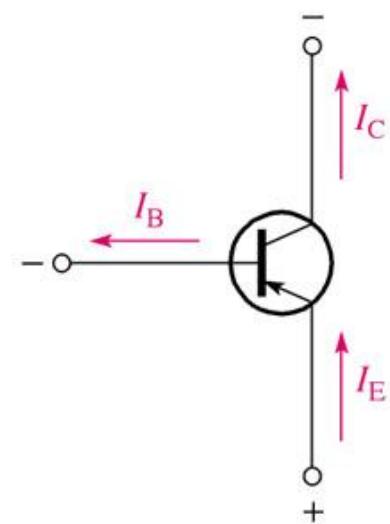
Transistor currents



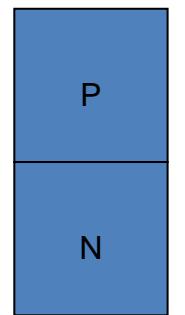
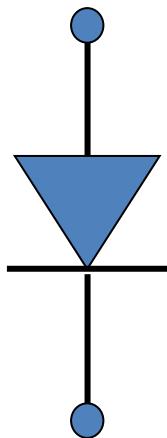
(a) *npn*



(b) *pnp*

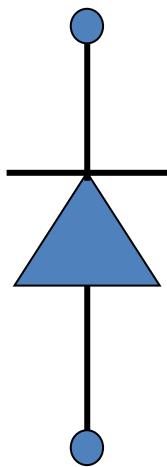


Number of P-N junctions and equivalent circuit



E

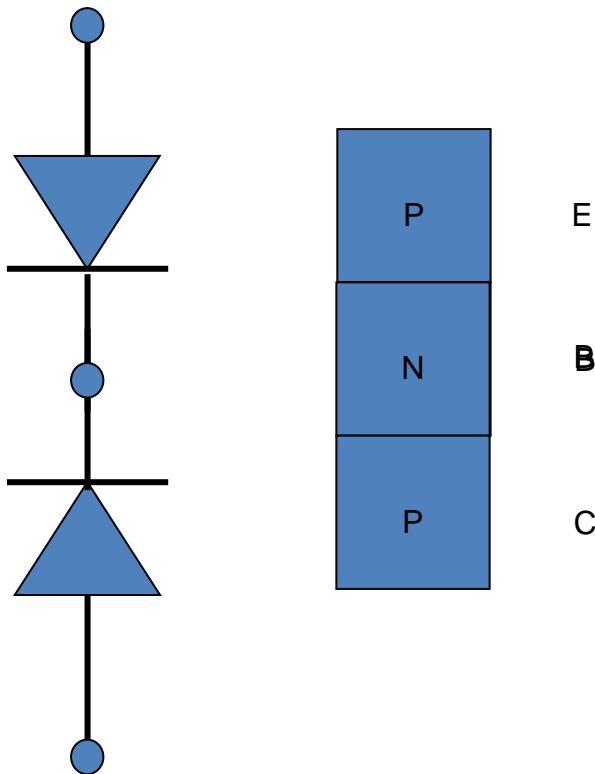
B



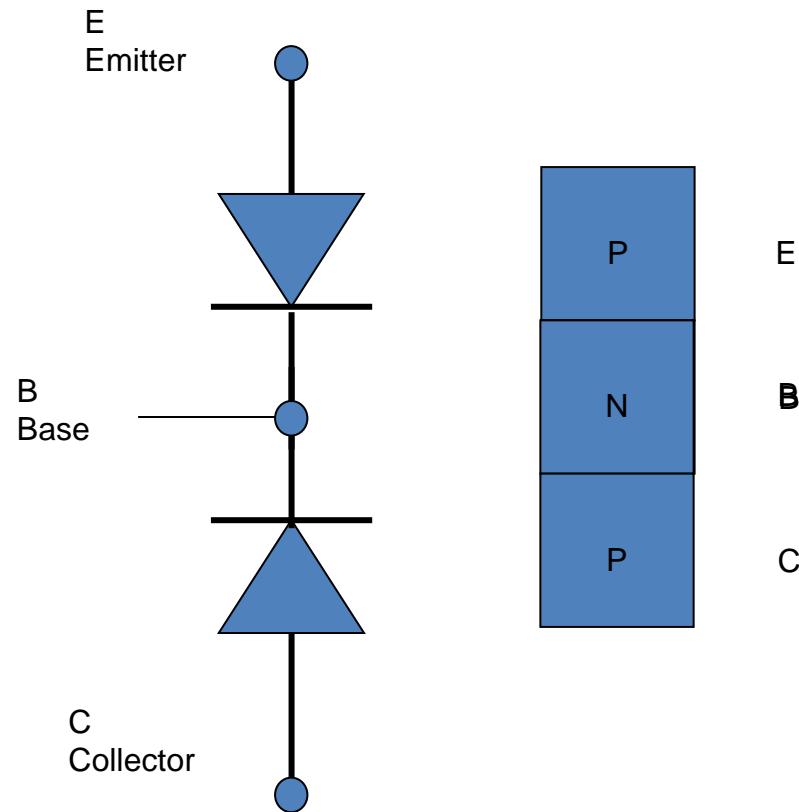
B

C

Number of P-N junctions and equivalent circuit

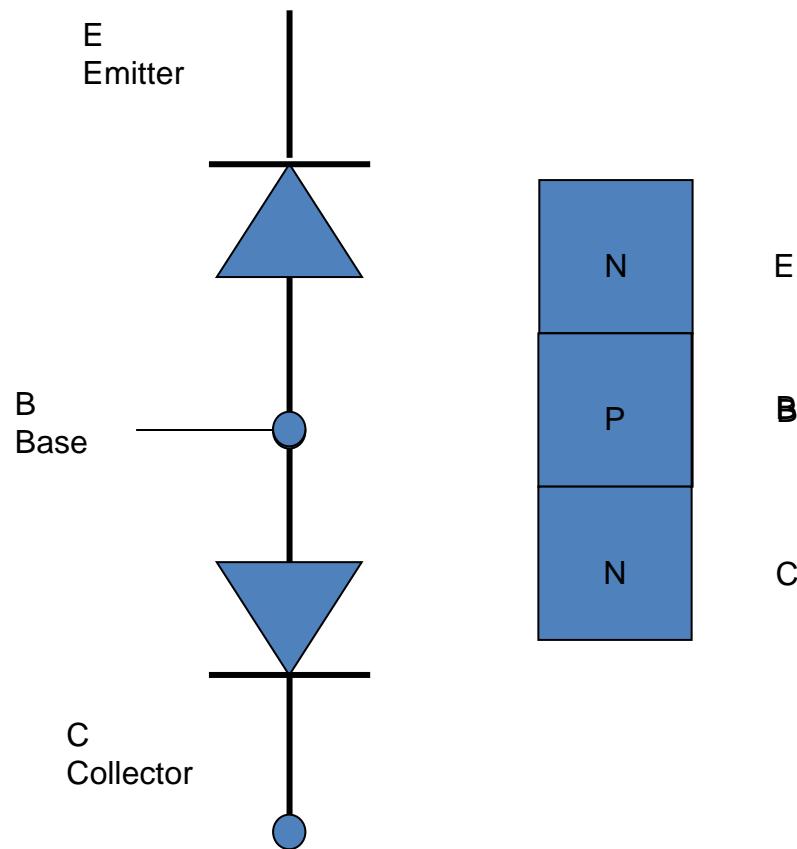


Number of P-N junctions and equivalent circuit



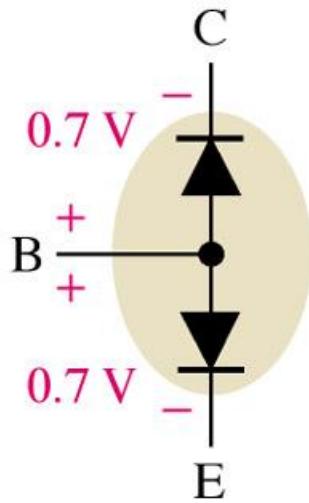
Equivalent for P-N-P Transistor

Number of P-N junctions and equivalent circuit

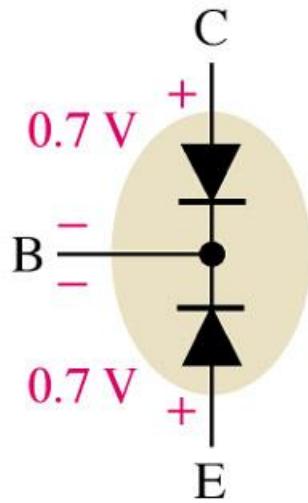


Equivalent for N-P-N Transistor

Number of P-N junctions and equivalent circuit

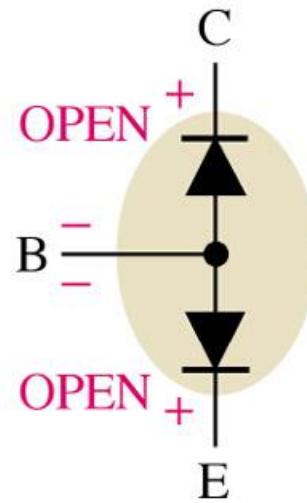


npn

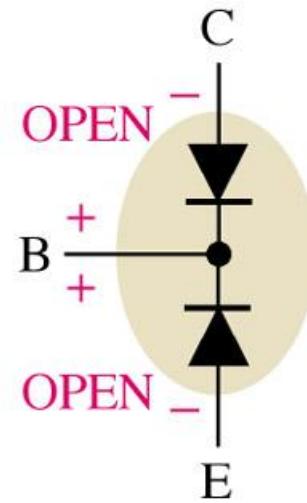


pnp

- (a) Both junctions should read $0.7 \text{ V} \pm 0.2 \text{ V}$ when forward-biased.



npn

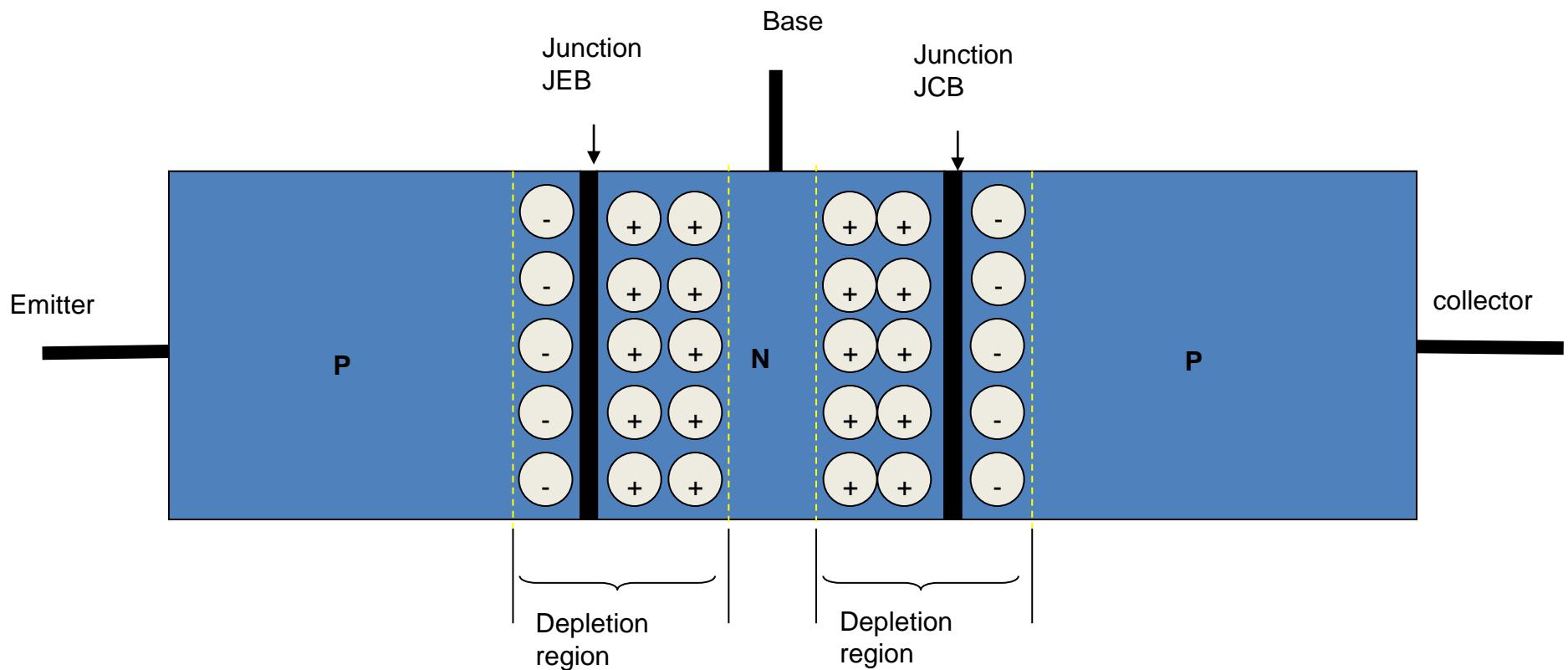


pnp

- (b) Both junctions should ideally read OPEN when reverse-biased.

An unbiased Transistor

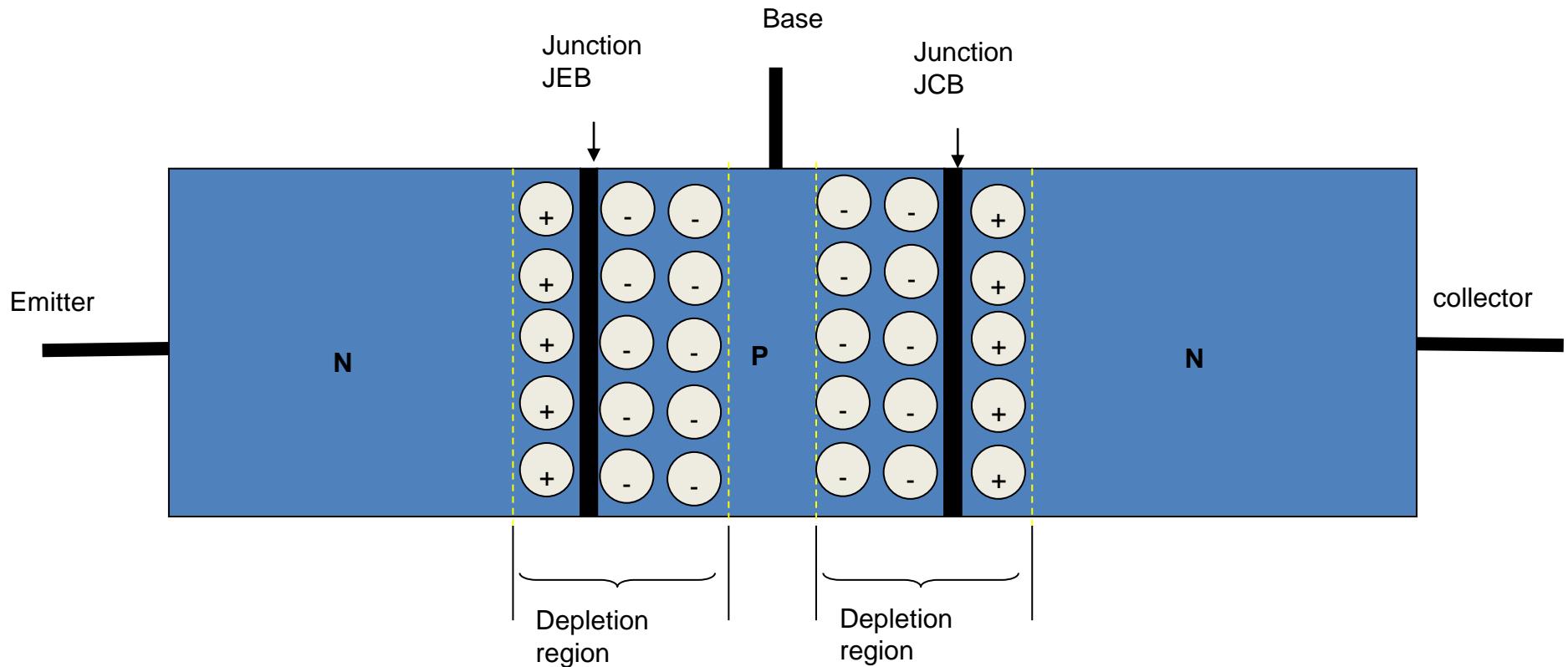
- For an unbiased transistor no external power supplies are connected to it



Depletion Regions in an unbiased P-N-P transistor

An unbiased Transistor

- For an unbiased transistor no external power supplies are connected to it



Depletion Regions in an unbiased N-P-N transistor

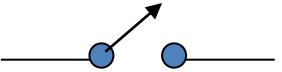
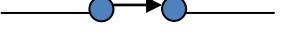
Penetration of depletion region

- The width of depletion region is not same on the two sides of the junction.
- The depletion region is always penetrates more in the lightly doped region i.e. the base region.
- Therefore the penetration of depletion region is less in the heavily doped collector and emitter regions, and more into the base region.

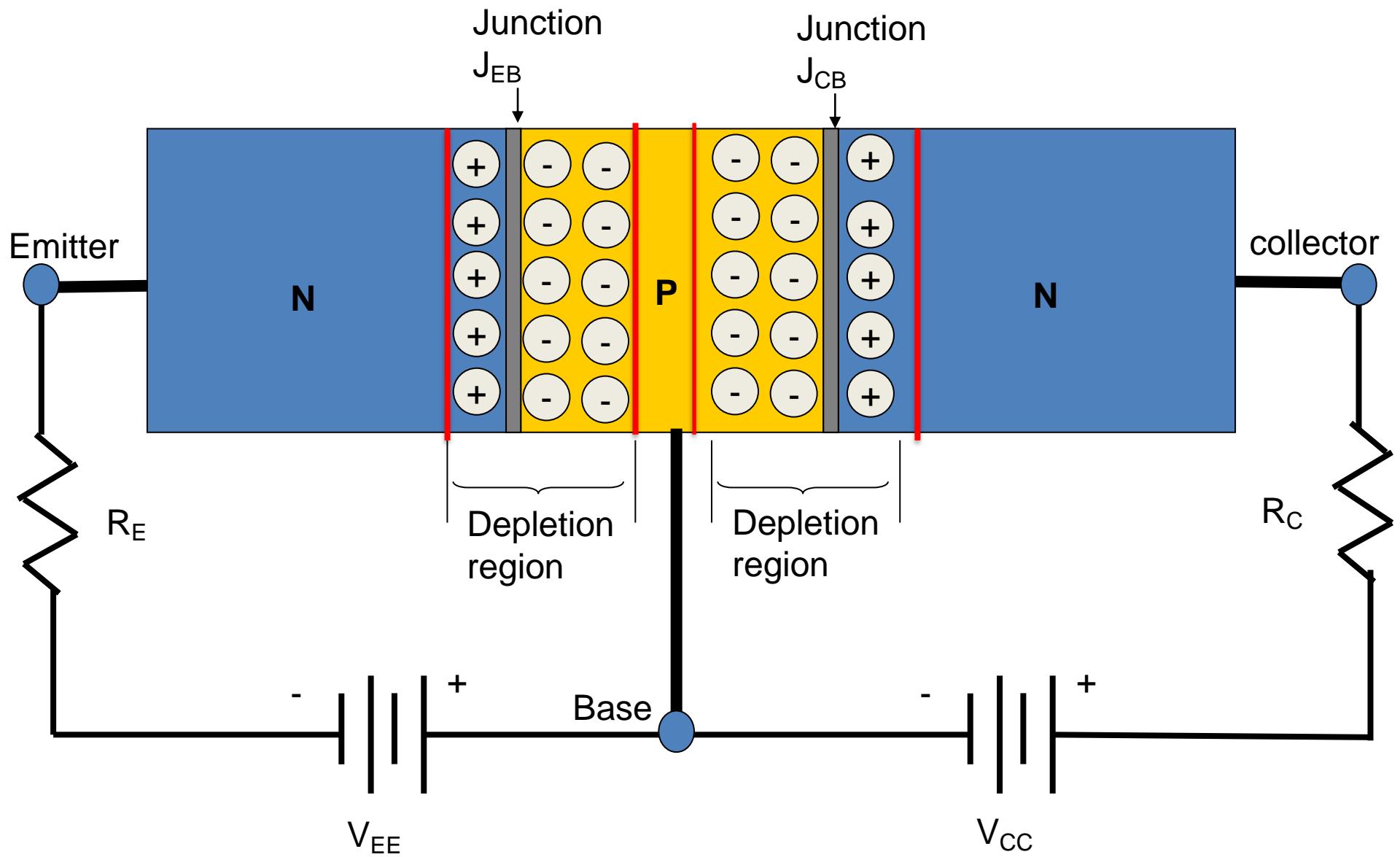
Transistor biasing in the active region

- Biasing is the process of applying external voltages to the transistor. The two junctions in a BJT must be biased properly in order to operate it as an amplifier.
- A BJT is capable of operating in three different regions, depending on the biasing.
- The regions of operations are:
 - Cutoff region (transistor is off)
 - Saturation region (transistor is fully on)
 - Active region (in between saturation and cutoff)

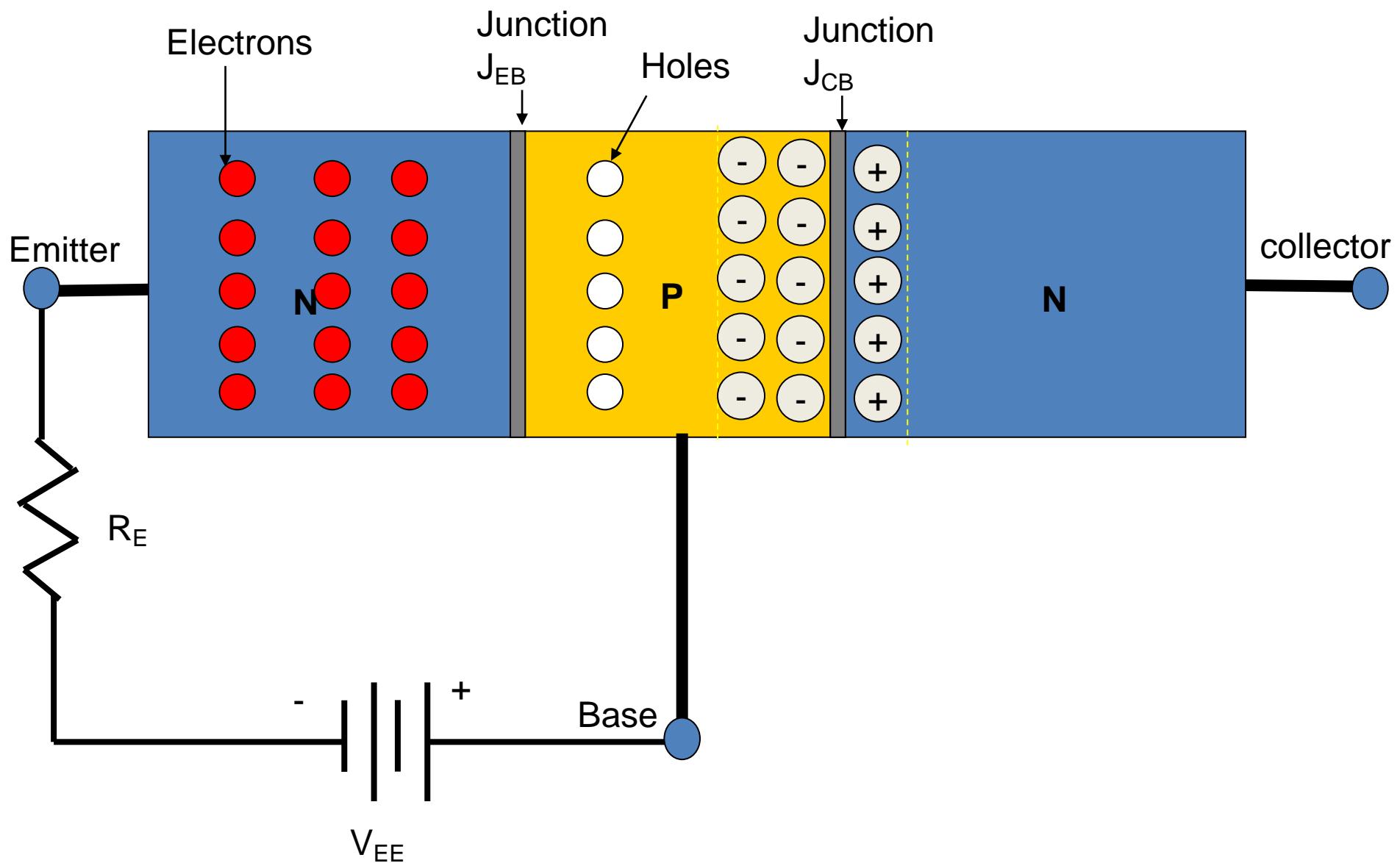
Transistor biasing in the active region

Sr. No.	Region of operation	Base emitter junction	Collector base junction	application
1	Cutoff region	Reverse biased	Reverse biased	transistor is OFF 
2	Saturation region	Forward biased	Forward biased	transistor is ON 
3	Active region	Forward biased	Reverse biased	Amplifier

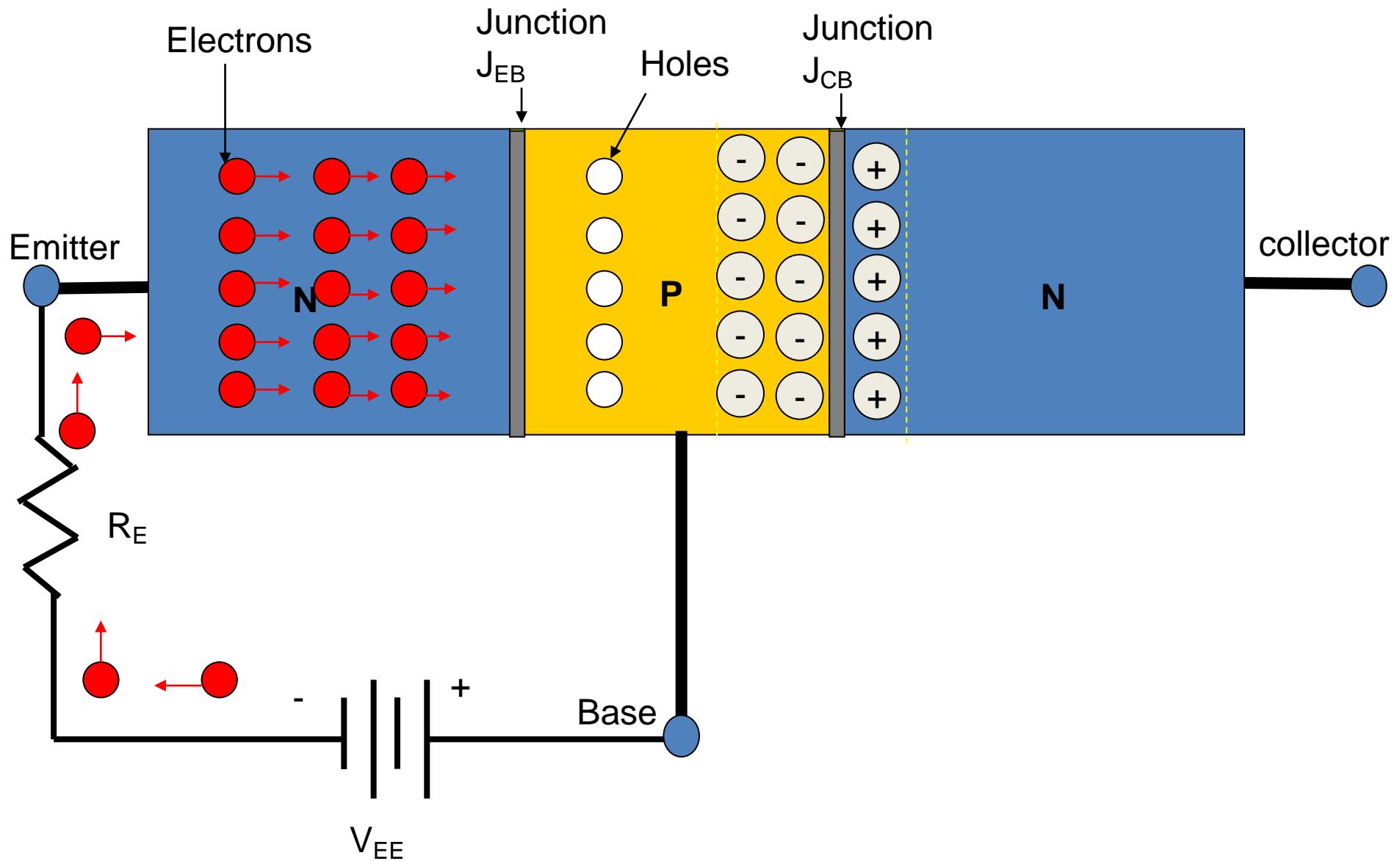
Transistor operation in the active region N-P-N



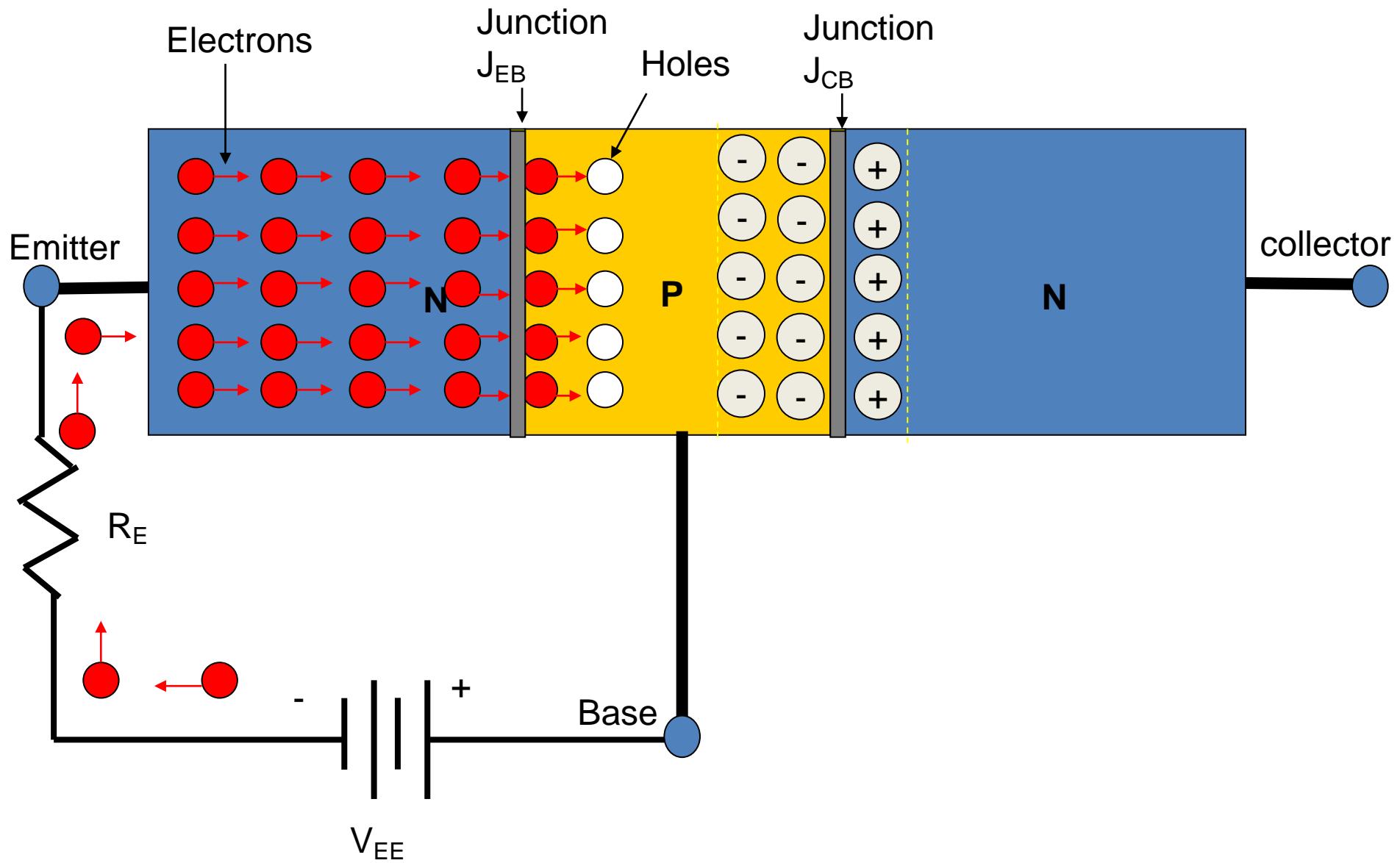
Transistor operation in the active region N-P-N



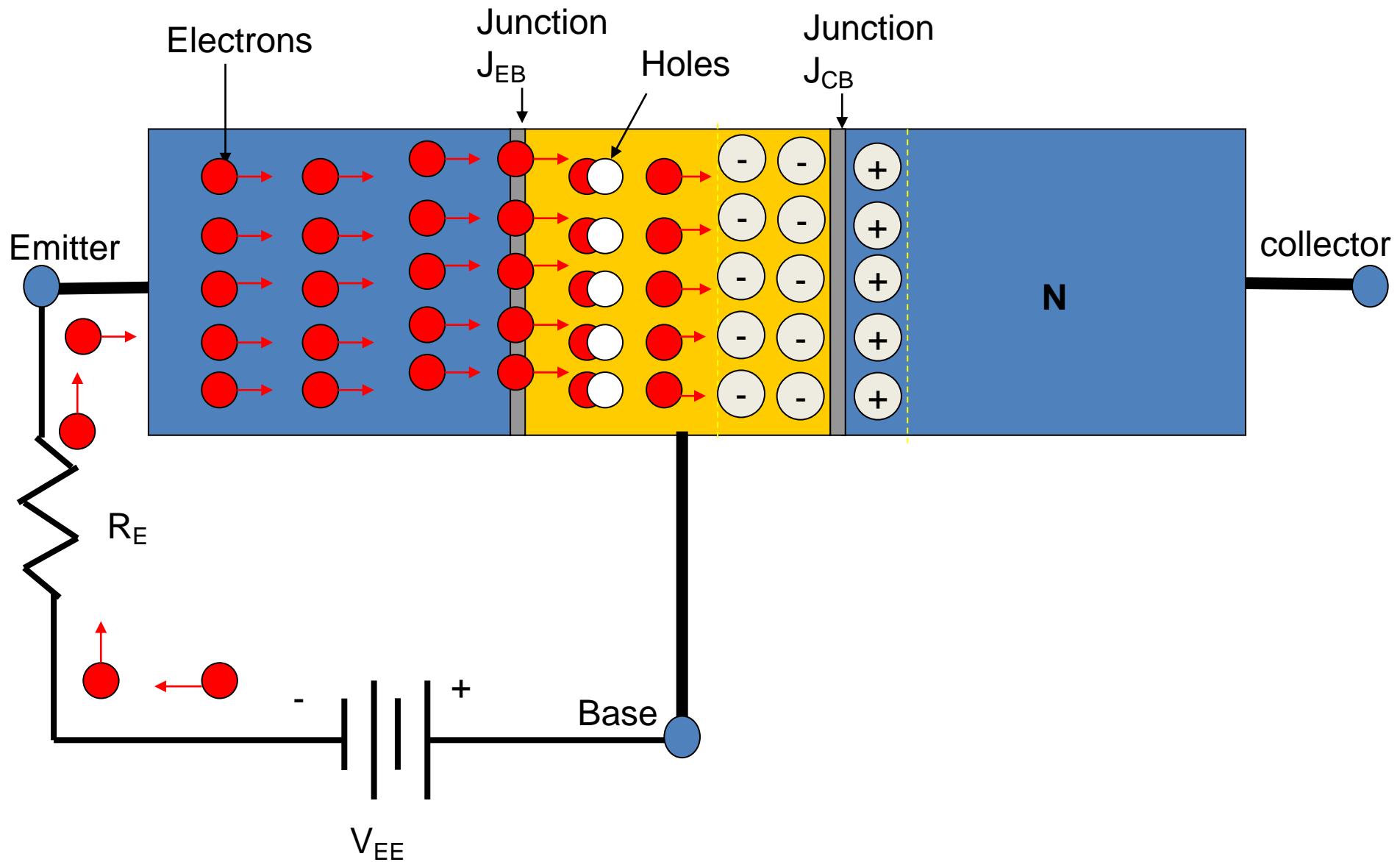
Transistor operation in the active region N-P-N



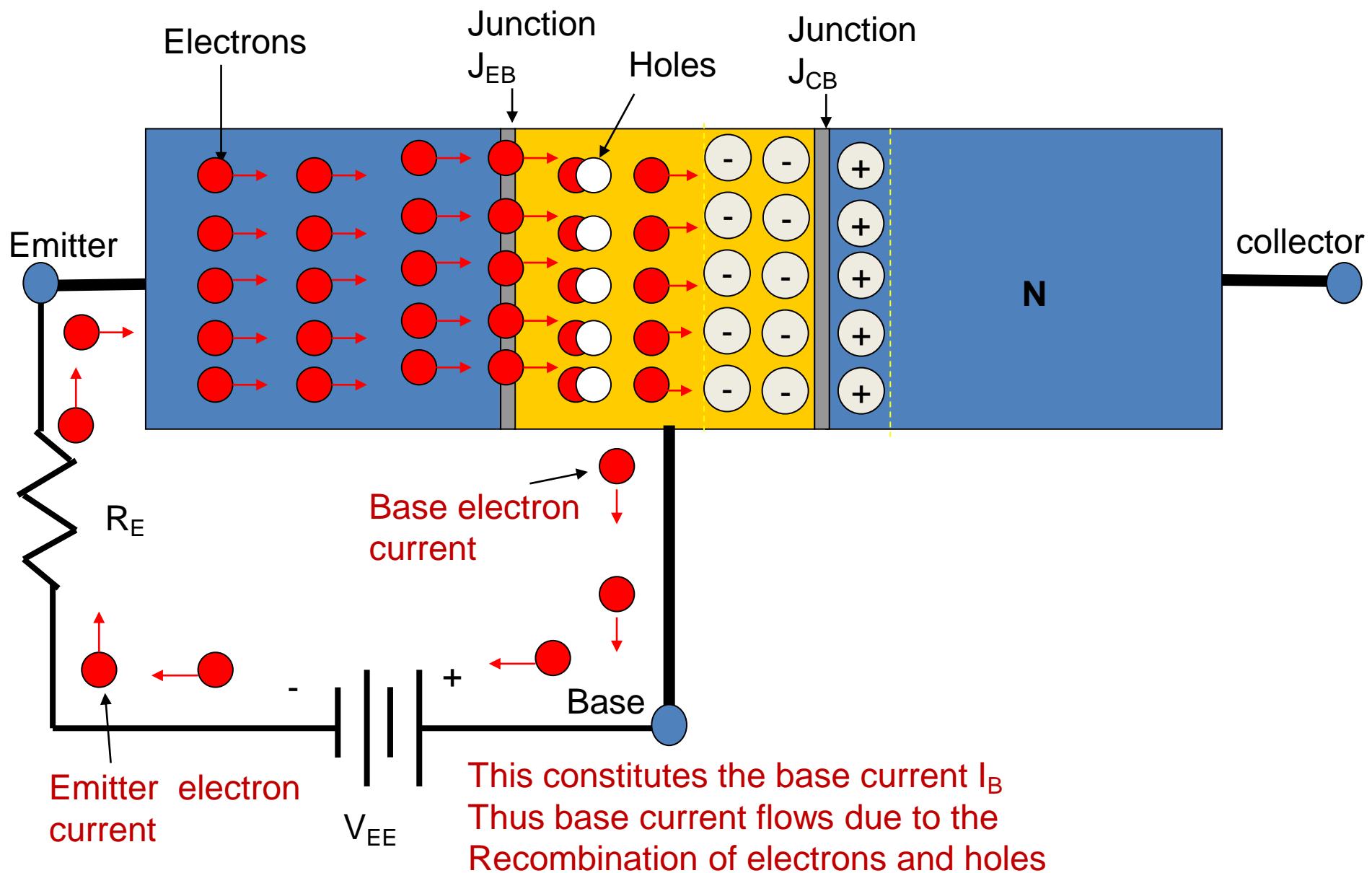
Transistor operation in the active region N-P-N



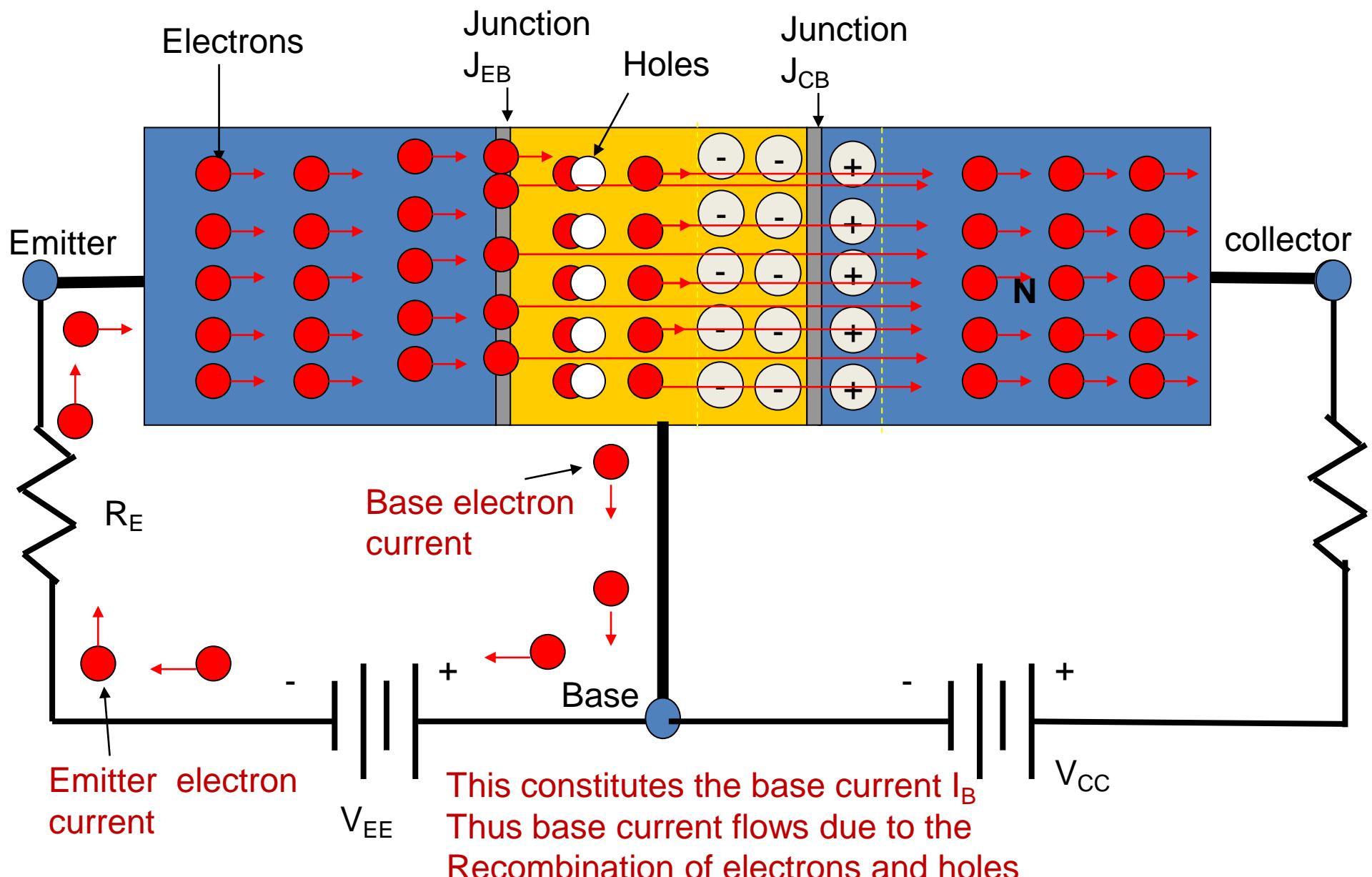
Transistor operation in the active region N-P-N



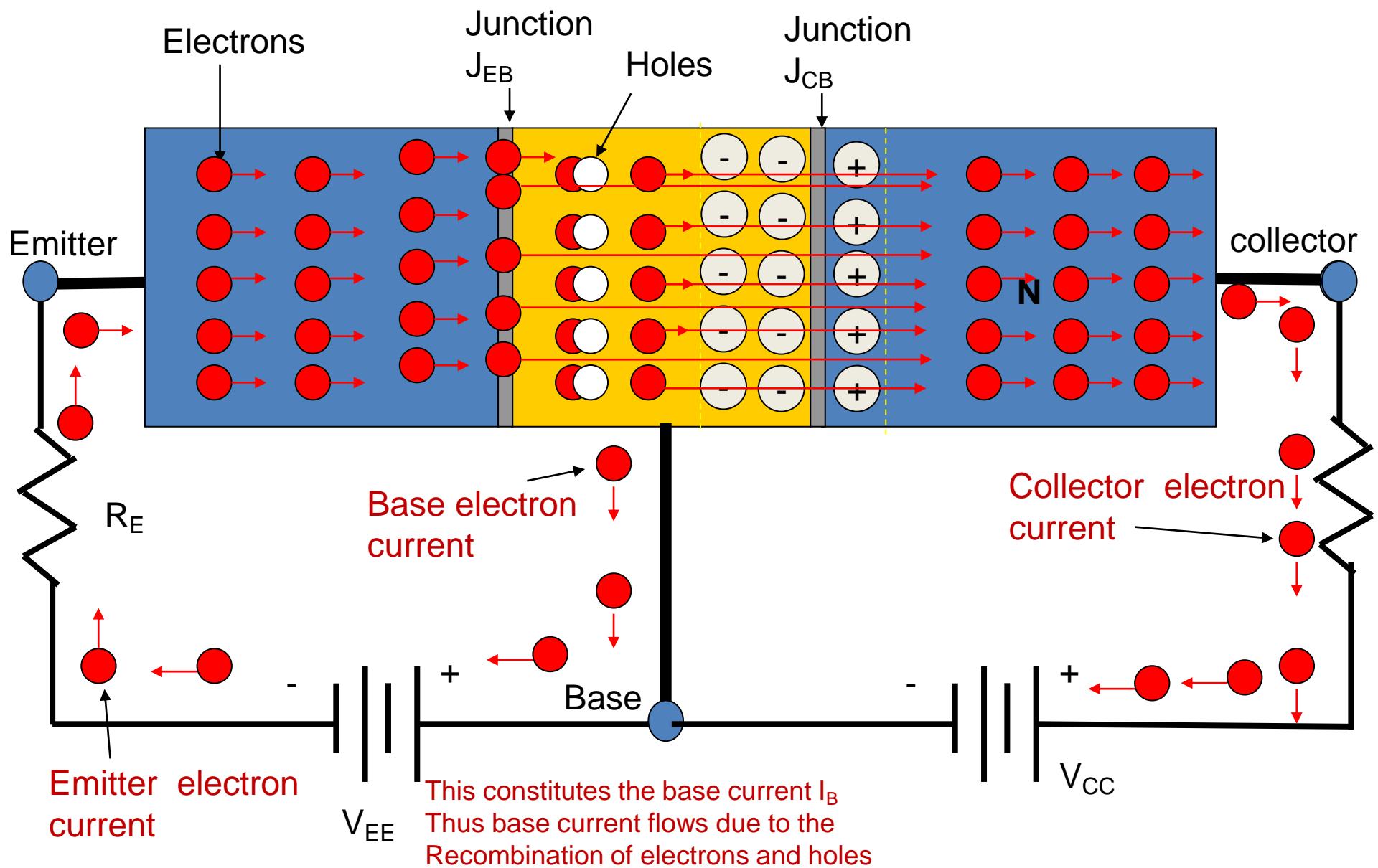
Transistor operation in the active region N-P-N



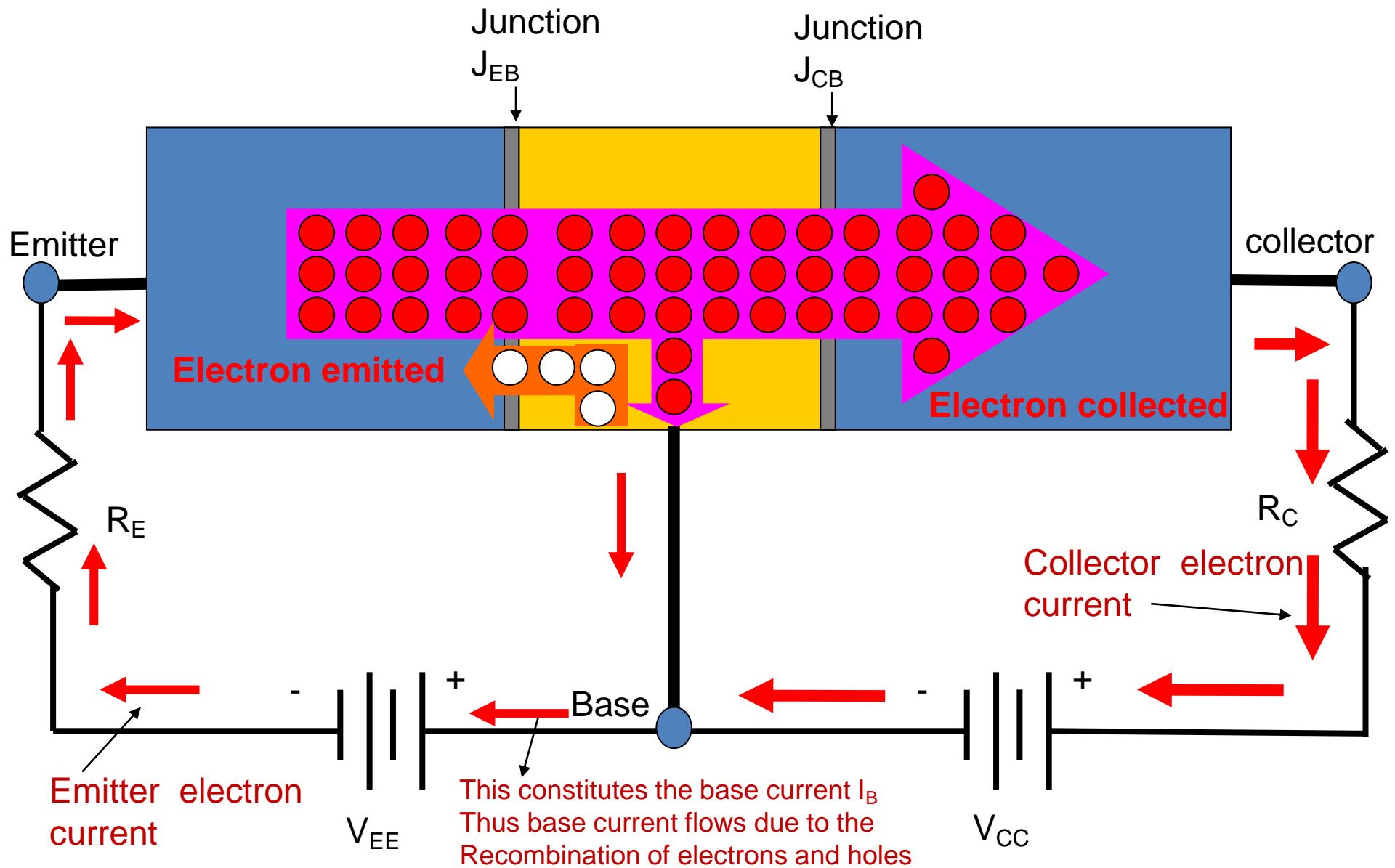
Transistor operation in the active region N-P-N



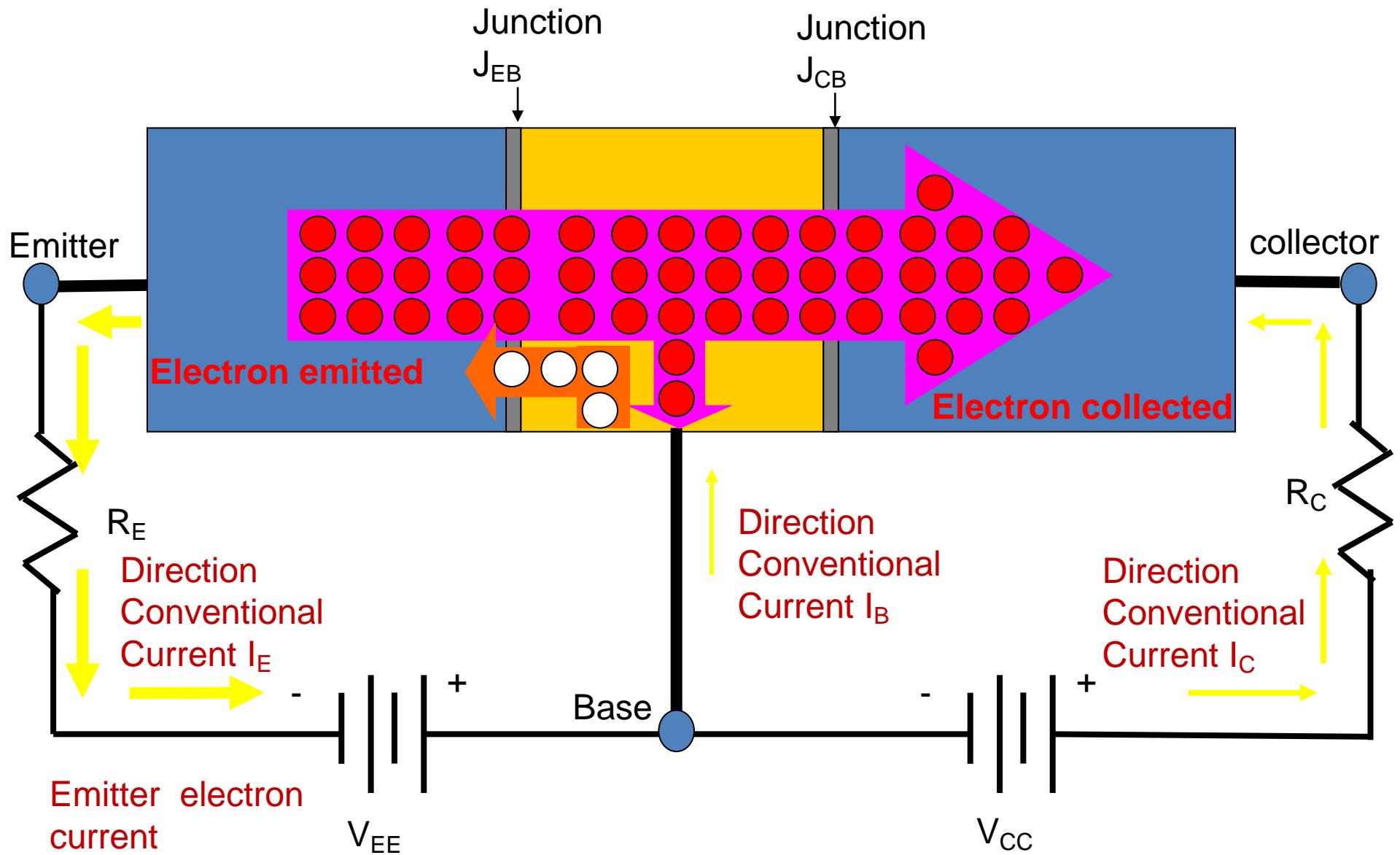
Transistor operation in the active region N-P-N



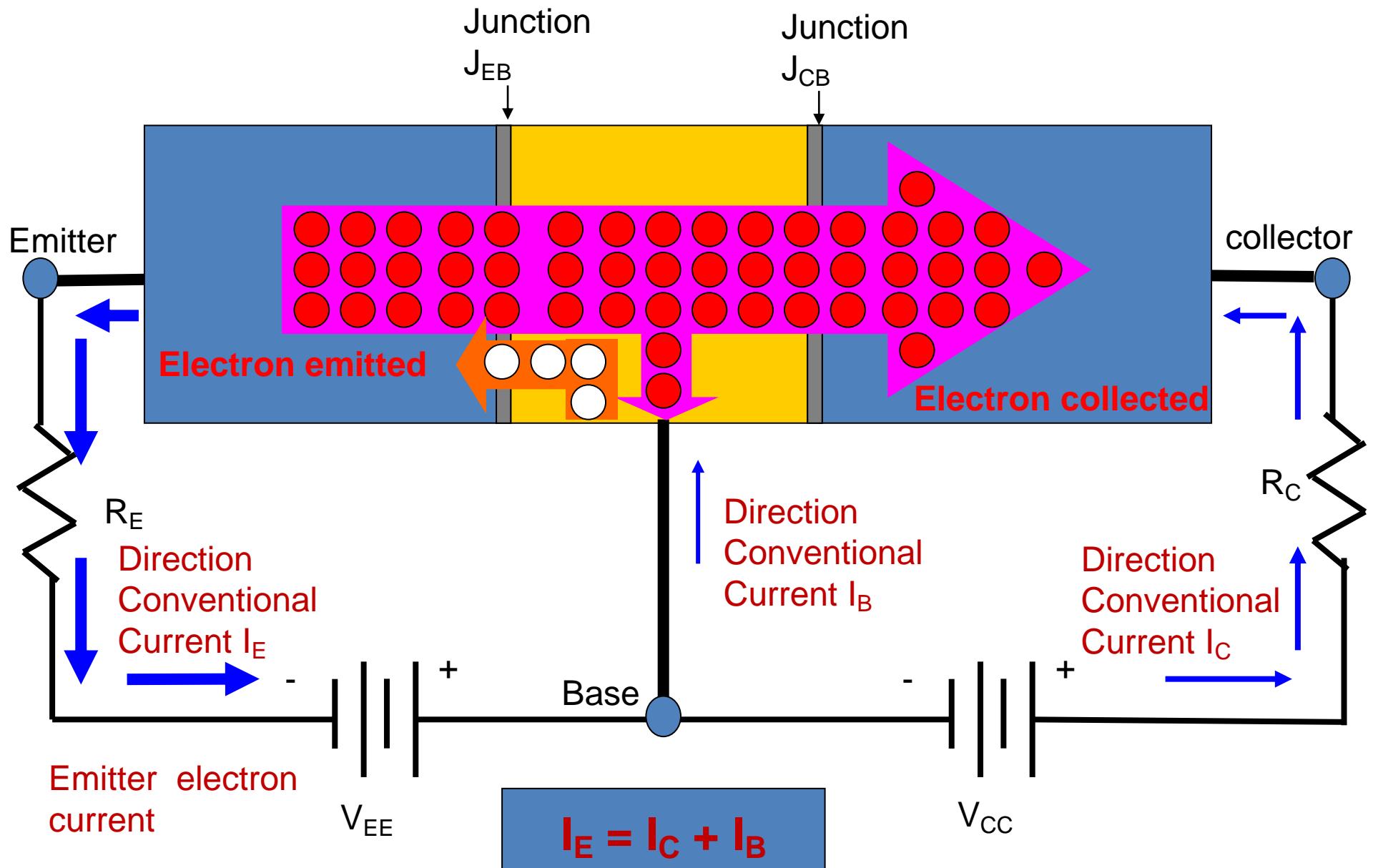
Transistor operation in the active region N-P-N



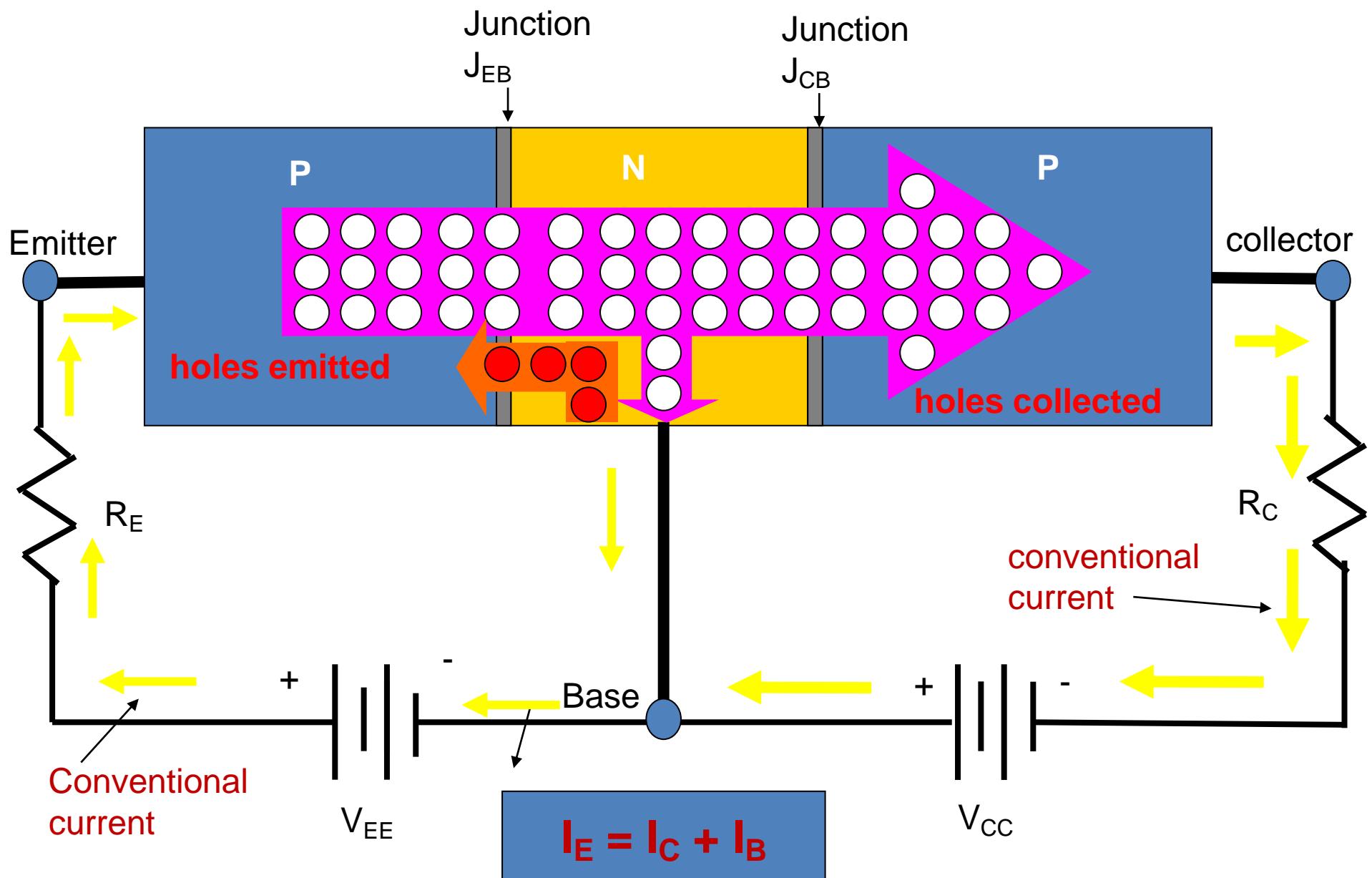
Transistor operation in the active region N-P-N



Transistor operation in the active region N-P-N



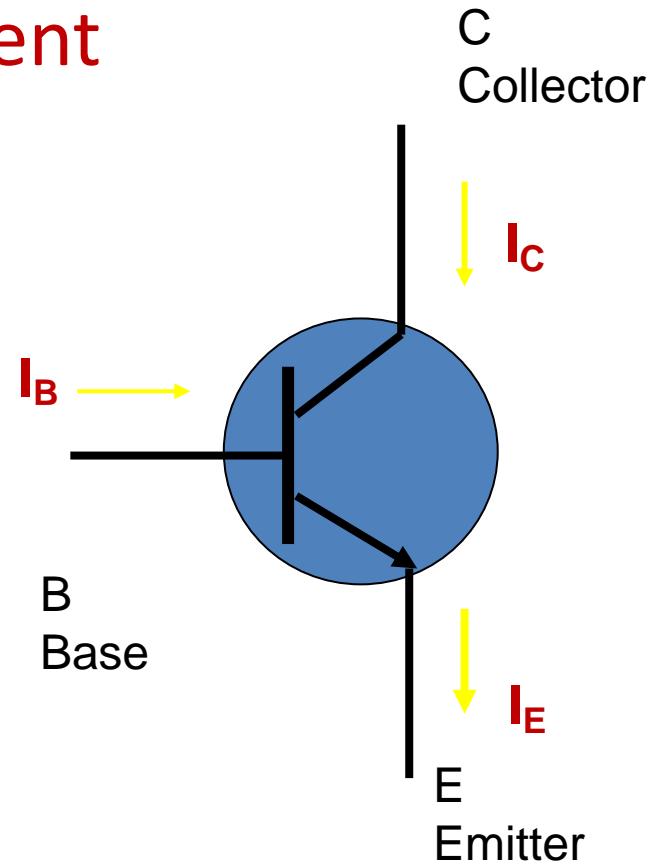
Transistor operation in the active region P-N-P



Transistor current

- Therefore we can write that

$$I_E = I_C + I_B$$



- Emitter current is always equal to the sum of collector current and base current.
- As I_B is very small as compared to I_E we can assume the collector current to be nearly equal to the emitter current

$$I_E \approx I_C$$

Transistor configuration

- Depending on which terminal is made common to input and output port there are three possible configurations of the transistor. They are as follows:
- Common base configuration
- Common emitter configuration
- Common collector configuration

Transistor configuration

Terminal	Emitter	Base	Collector
Priority	---	Input	Output

- Common base configuration I/P: Emitter, O/P: Collector

E	B	C
Input	Common	Output

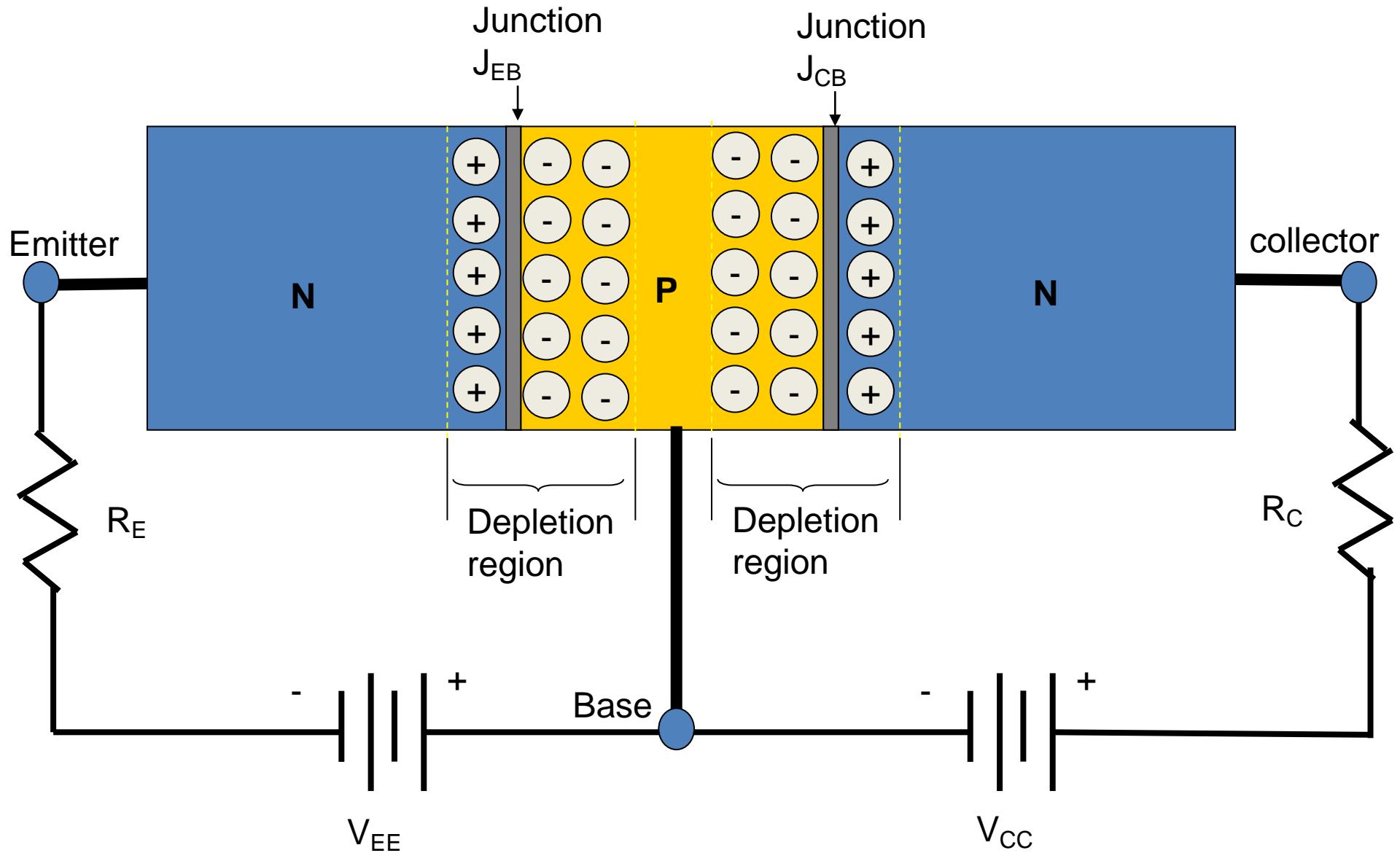
- Common Emitter configuration I/P: base, O/P: Collector

E	B	C
Common	Input	Output

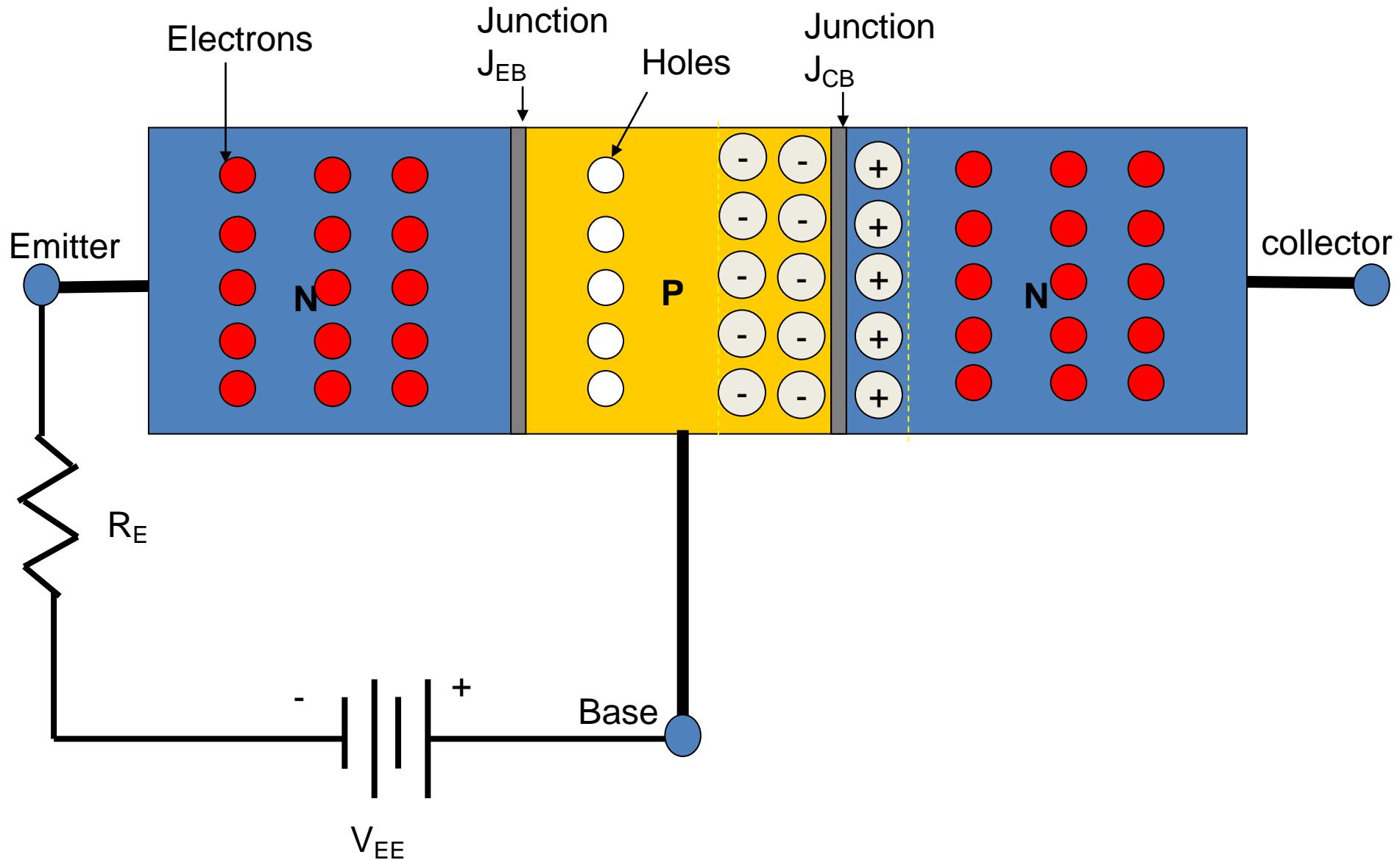
- Common collector configuration I/P: base, O/P: Emitter

E	B	C
Output	Input	Common

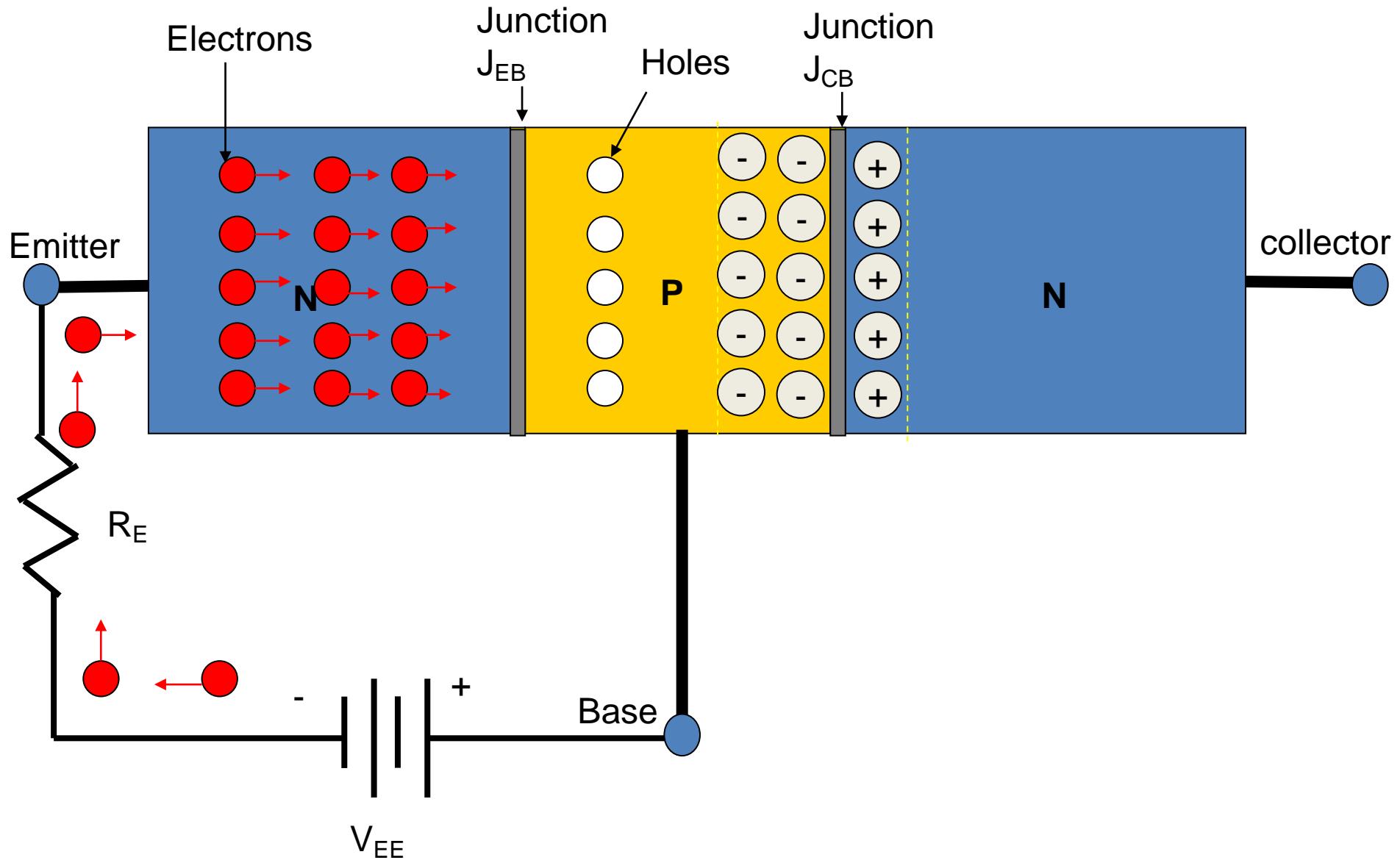
Transistor operation in the active region N-P-N common base configuration



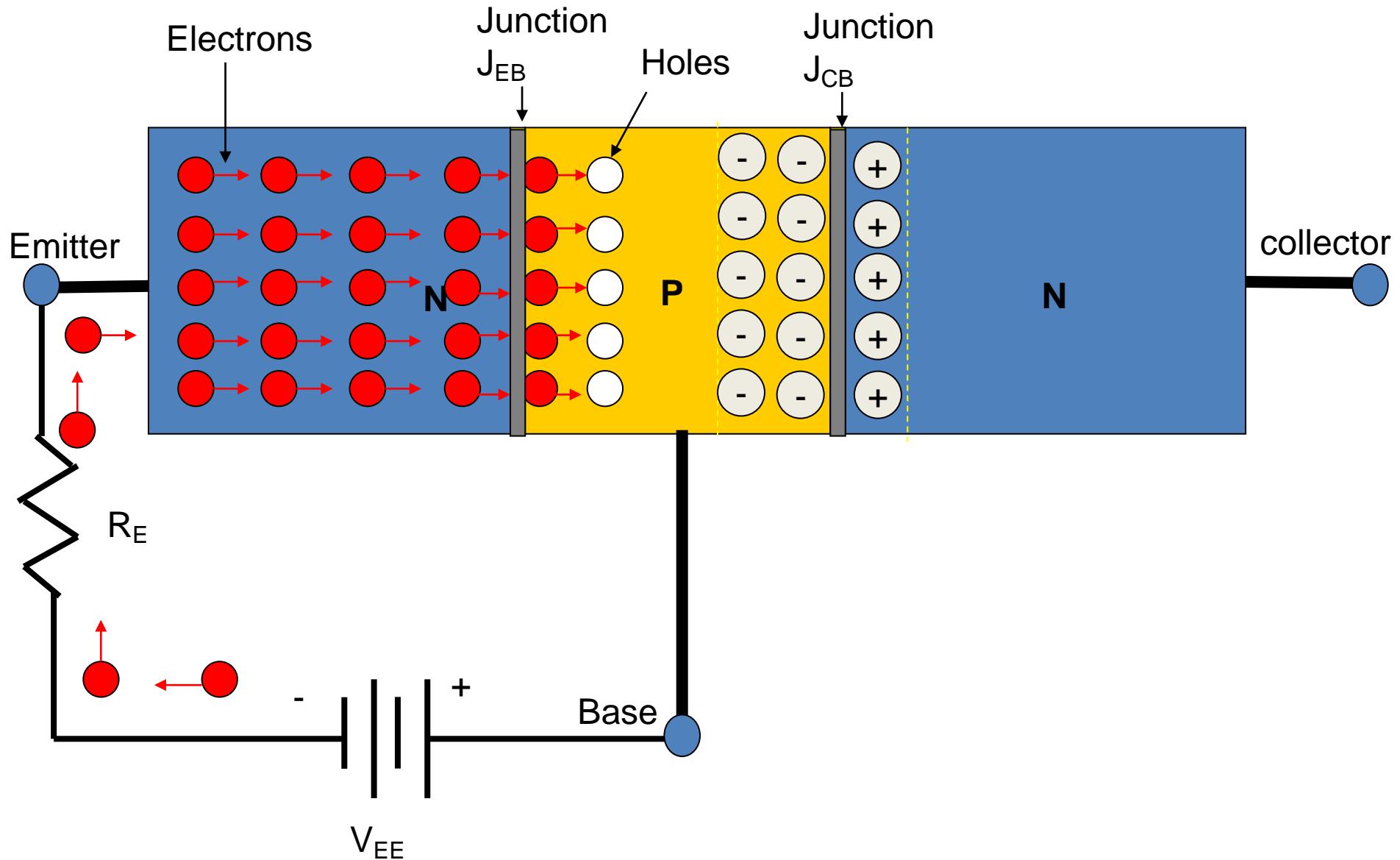
Transistor operation in the active region N-P-N common base configuration



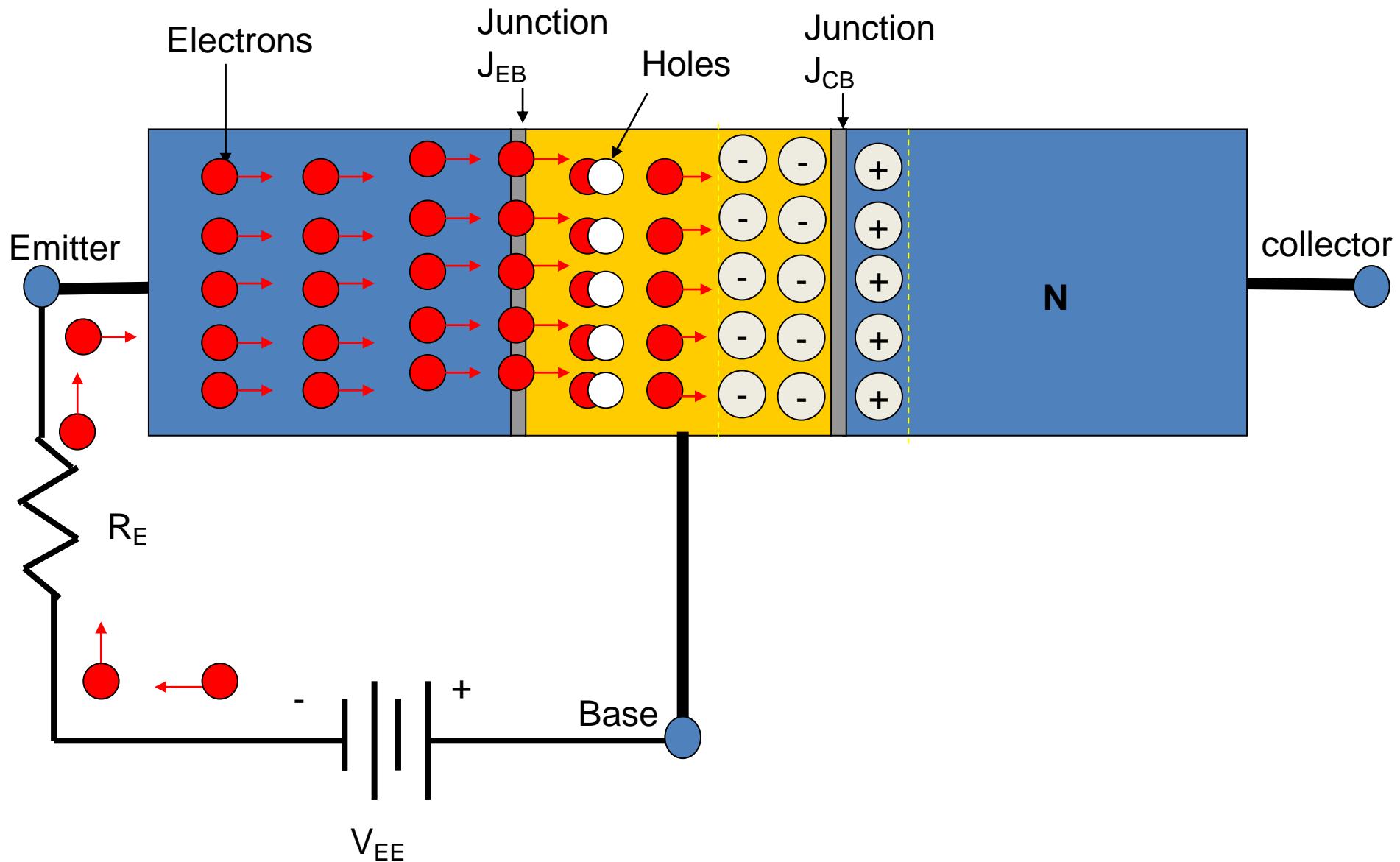
Transistor operation in the active region N-P-N common base configuration



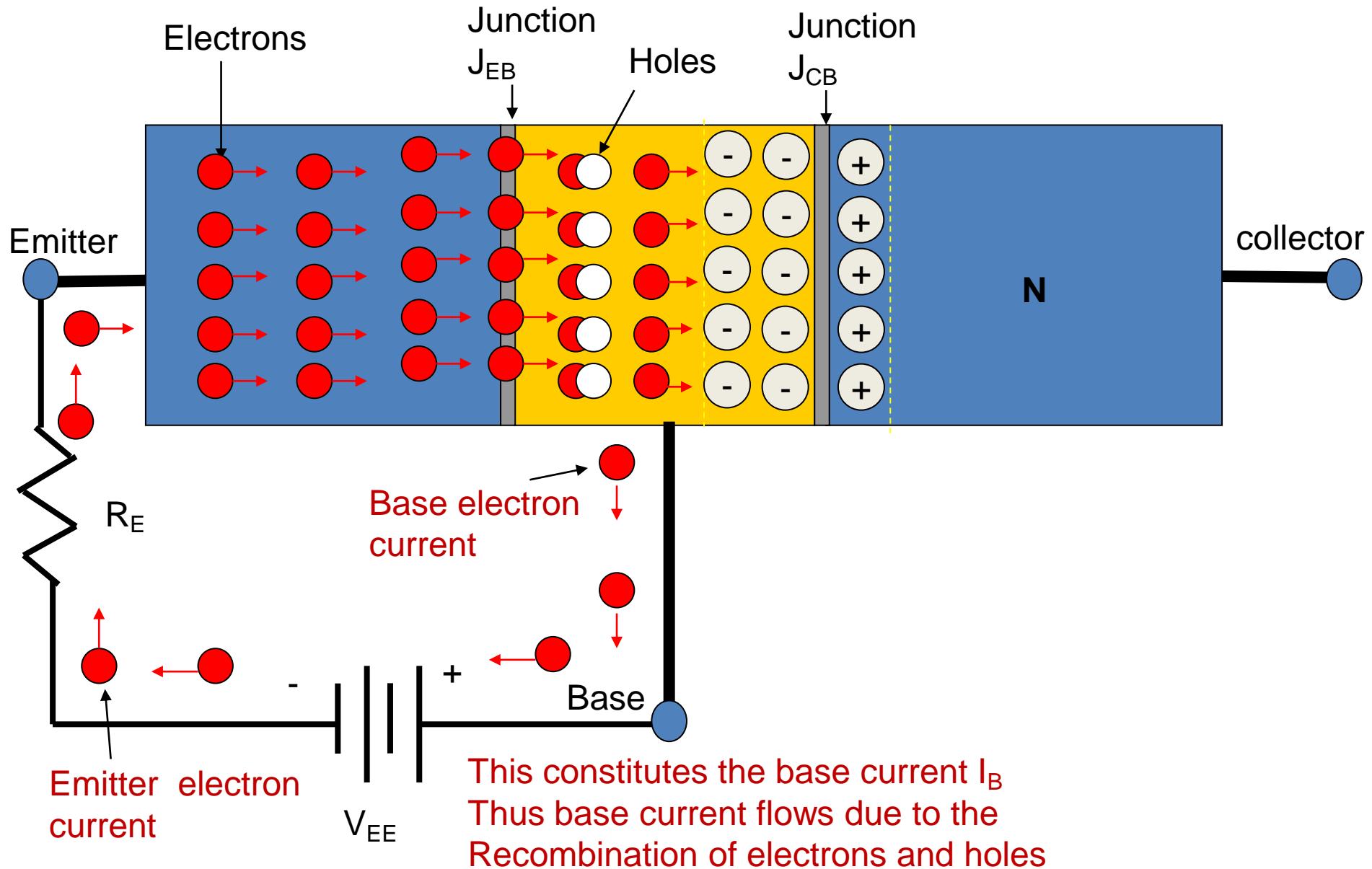
Transistor operation in the active region N-P-N common base configuration



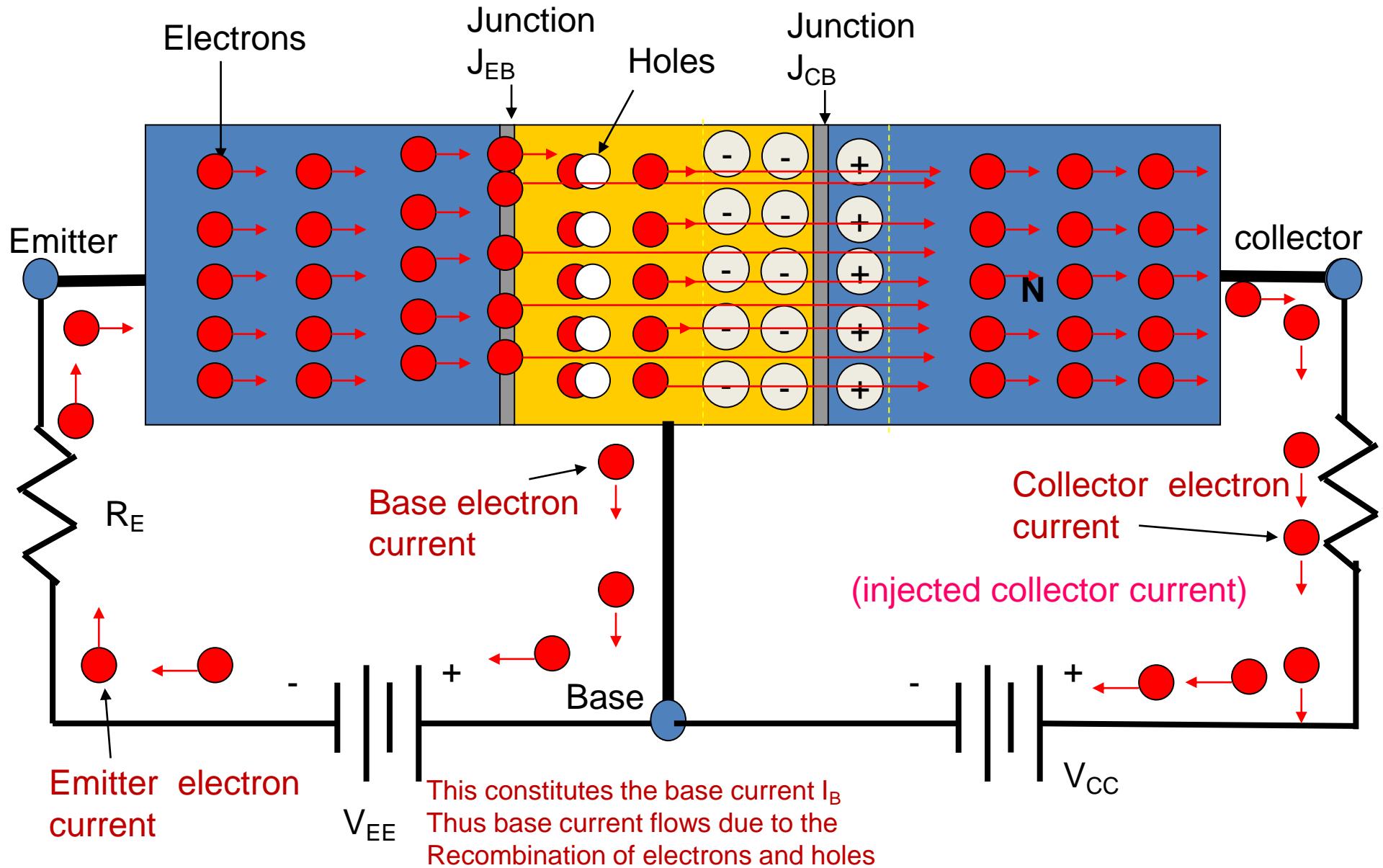
Transistor operation in the active region N-P-N common base configuration



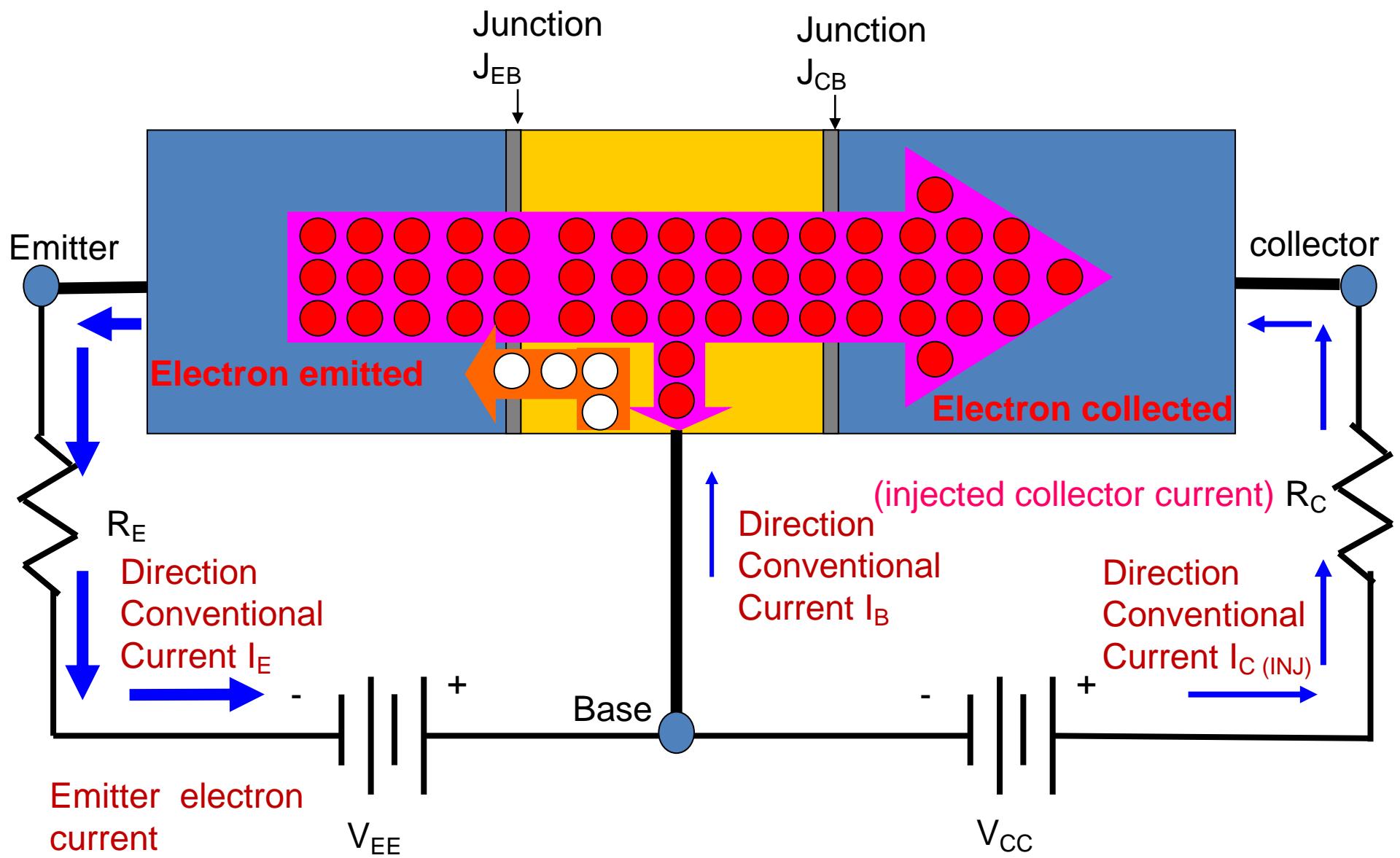
Transistor operation in the active region N-P-N common base configuration



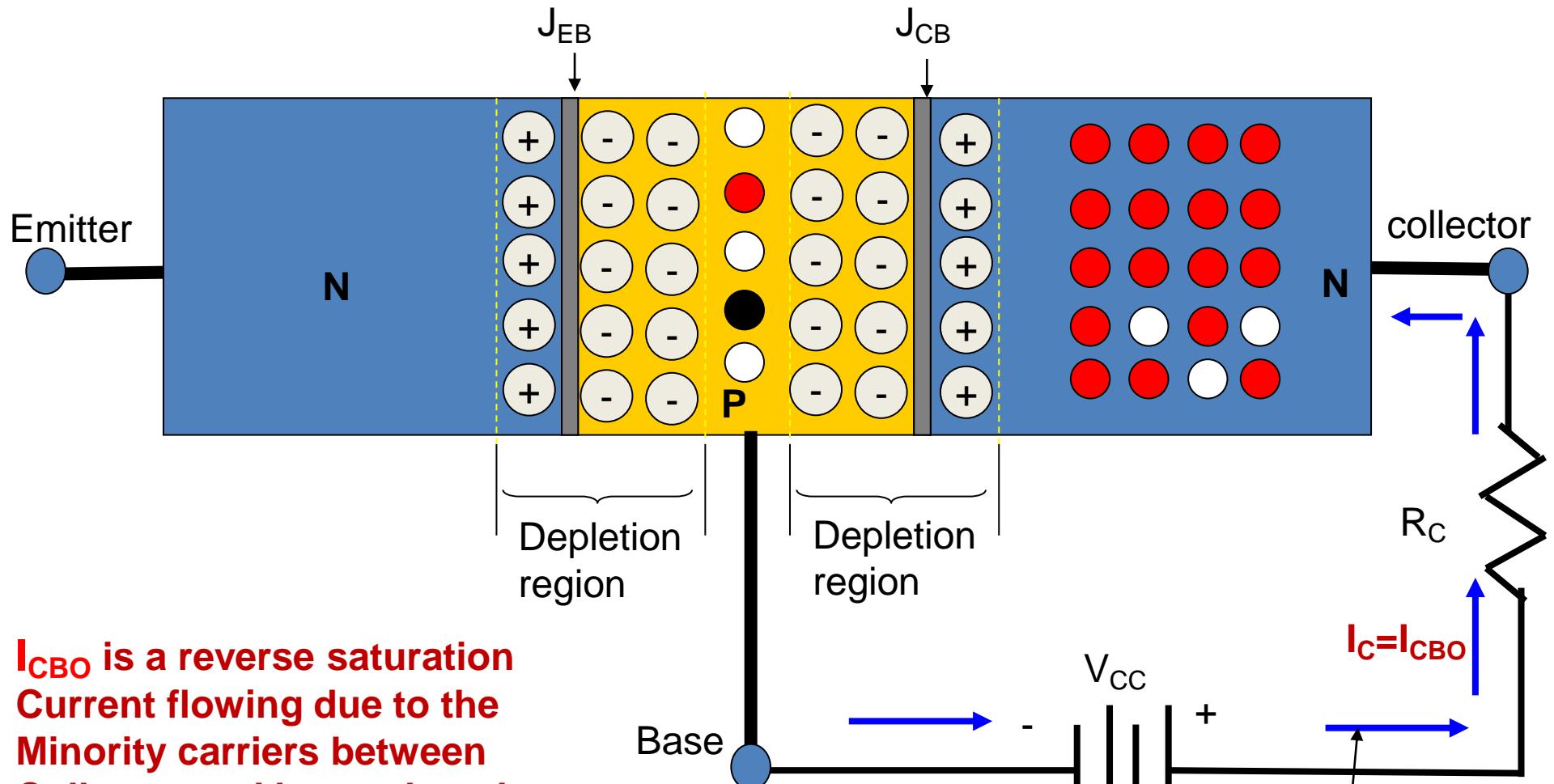
Transistor operation in the active region N-P-N common base configuration



Transistor operation in the active region N-P-N common base configuration



Transistor operation in the active region N-P-N common base configuration



I_{CBO} is a reverse saturation Current flowing due to the Minority carriers between Collector and base when the Emitter is open. I_{CBO} flows due to the reverse Biased collector base junction. I_{CBO} is neglected as compared to $I_{C(INJ)}$

I_{CBO} Is a collector to base leakage current With open emitter

Current relations in CB configuration

- As I_{CBO} is negligible as compared to $I_{C(INJ)}$
- $I_C = I_{C(INJ)}$ ----- (Practically)
- $I_C = I_{CBO}$ ----- (with emitter open)
- Since I_{CBO} , flows due to thermally generated carriers, it increases with increase in temperature. It doubles its value for every 10°C rise in temperature

Current relations in CB configuration

- The collector current I_C of the common base configuration is given by :
- $$I_C = I_{C(INJ)} + I_{CBO}$$
- $I_{C(INJ)}$: it is called as the injected collector current and it is due to the number of electrons crossing the collector base junction.
- I_{CBO} : this is the reverse saturation current flowing due the minority carriers between collector and base when the emitter is open.
- I_{CBO} flows due to the reverse biased collector base junction.

Current relations in CB configuration

- Current amplification factor (α_{dc})
- the current amplification factor is the ratio of collector current due to the injection of total emitter current

$$\alpha_{dc} = I_{C(INJ)} / I_E$$

- The value of α_{dc} for CB configuration will always be less than 1. this is because $I_{C(INJ)} < I_E$
- Typically The value of α_{dc} ranges between 0.95 to 0.995 depending on the thickness of the base region.
- Larger is the thickness of the base is, smaller is the value of α_{dc}

Current relations in CB configuration

- Current amplification factor (α_{dc})
 - the current amplification factor is the ratio of collector current due to the injection of total emitter current

$$a_{dc} = I_{C(INJ)} / I_E$$

$$I_{C(INJ)} = \alpha_{dc} I_E$$

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

But I_{CBO} is negligibly small

$$I_C = \alpha_{dc} I_E$$

Therefore the current amplification factor

$$\alpha_{dc} = I_C / I_F$$

Current relations in CB configuration

- Expression for I_B

We know that

$$I_E = I_C + I_B$$

since $I_C = \alpha_{dc} I_E + I_{CBO}$

$$I_E = (\alpha_{dc} I_E + I_{CBO}) + I_B$$

therefore $I_B = I_E - \alpha_{dc} I_E - I_{CBO}$

$$I_B = (1 - \alpha_{dc}) I_E - I_{CBO}$$

Neglecting I_{CBO} we get

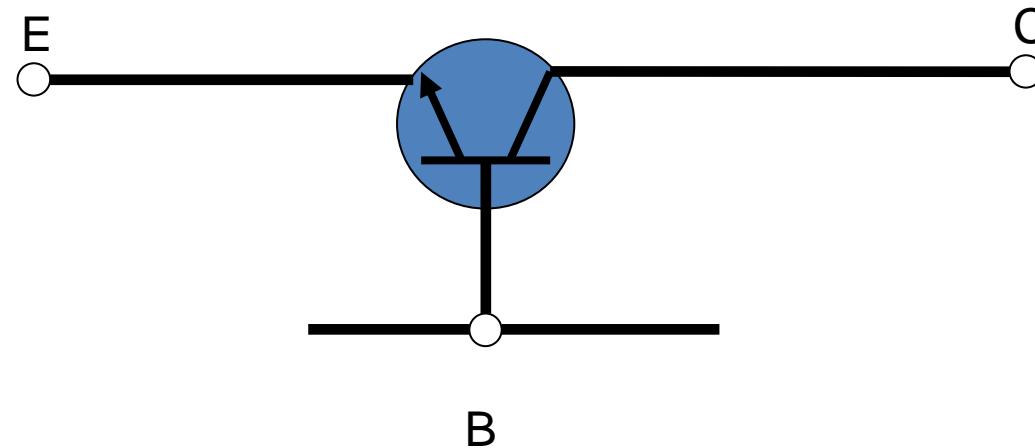
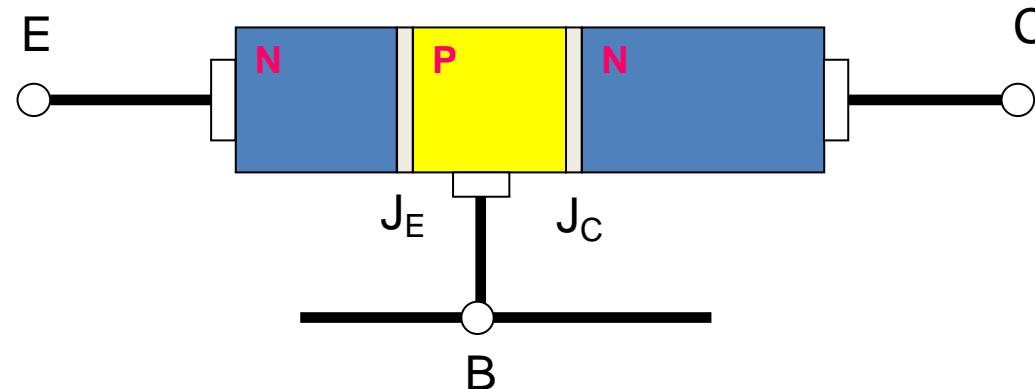
$$I_B = (1 - \alpha_{dc}) I_E$$

Characteristics of a transistor in CB configuration

- **The characteristics of a transistor help us to understand its behavior.**
- **The transistor characteristics are of three types :**
- **Input characteristics**
- **Output characteristics**
- **Transfer characteristics**

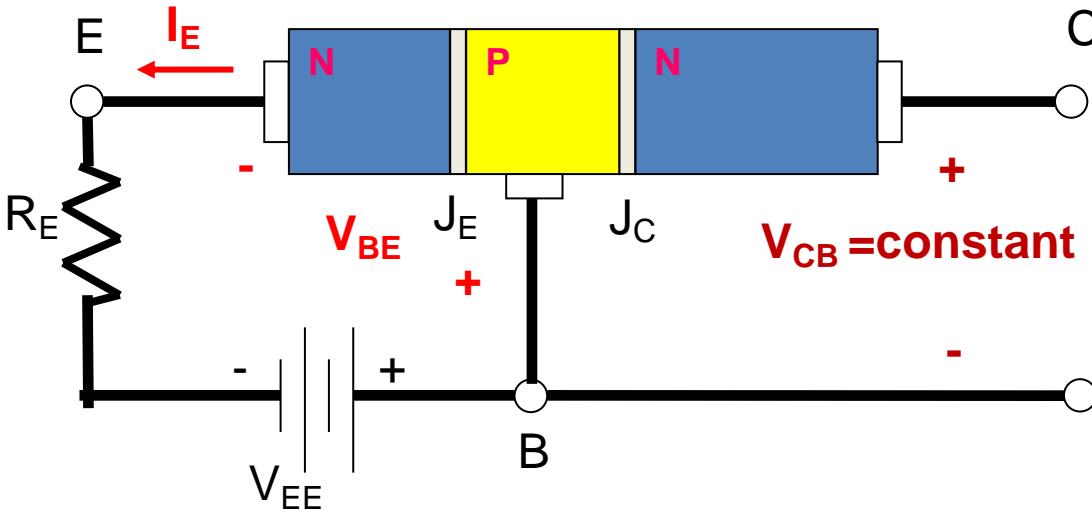
Characteristics of a transistor in CB configuration

Input characteristics

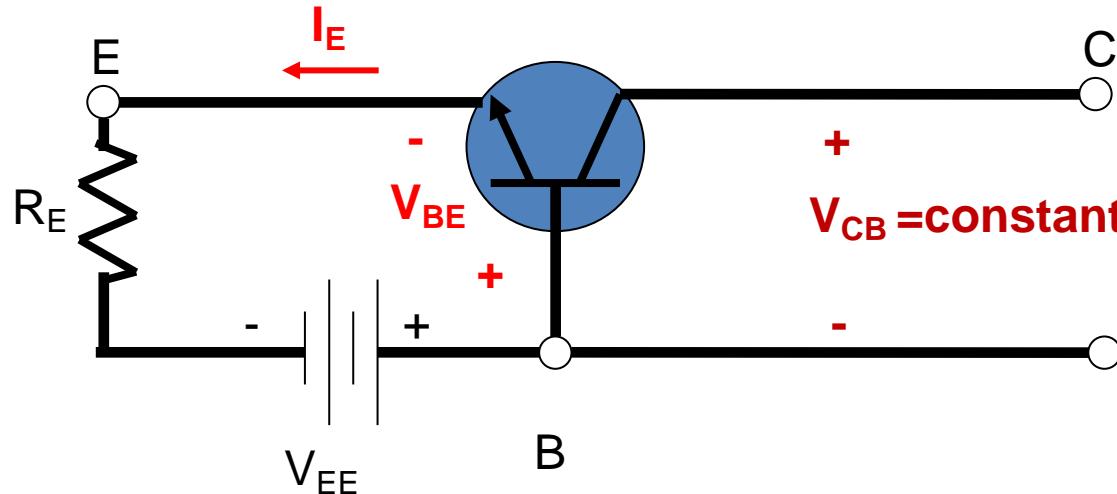


Characteristics of a transistor in CB configuration

Input characteristics

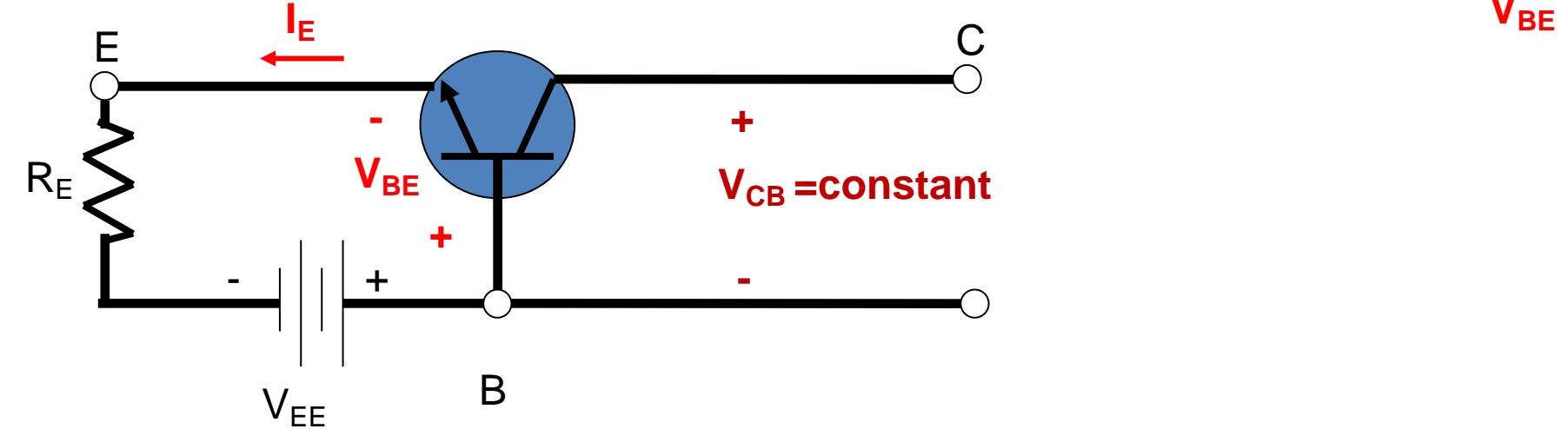
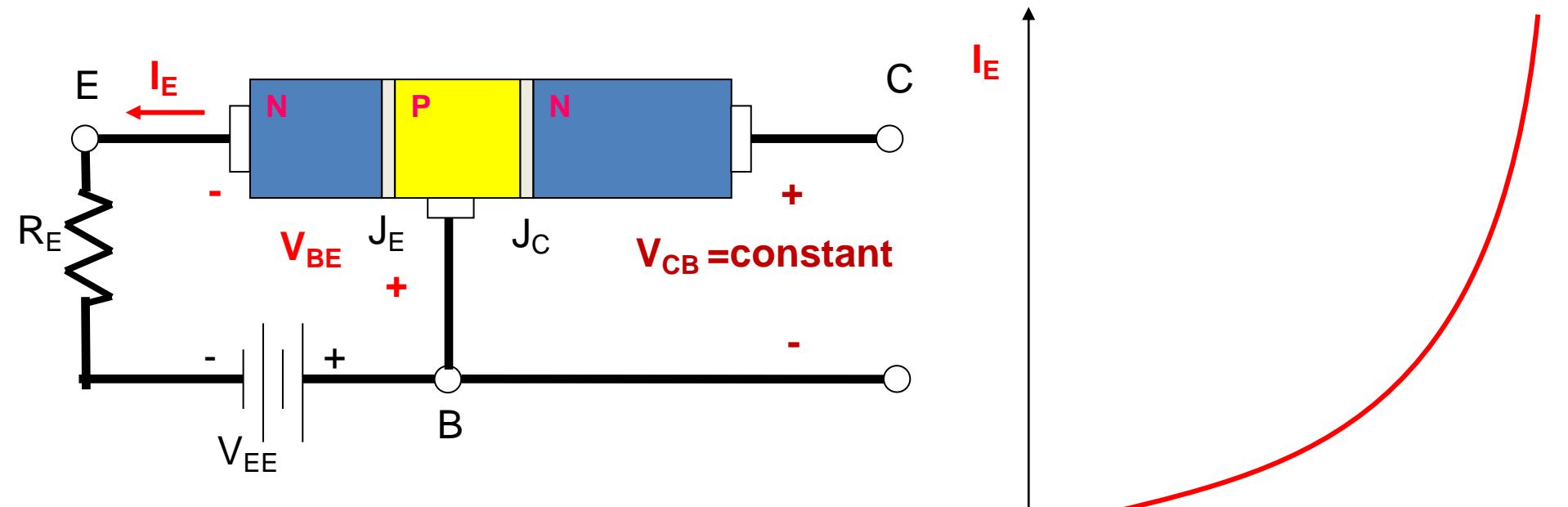


- Input characteristics is always A graph of input current versus Input voltage.
- For the CB configuration, input Current is I_E and input voltage Is the emitter to base voltage V_{BE}
- Input characteristics is plotted at a constant output voltage V_{CB}



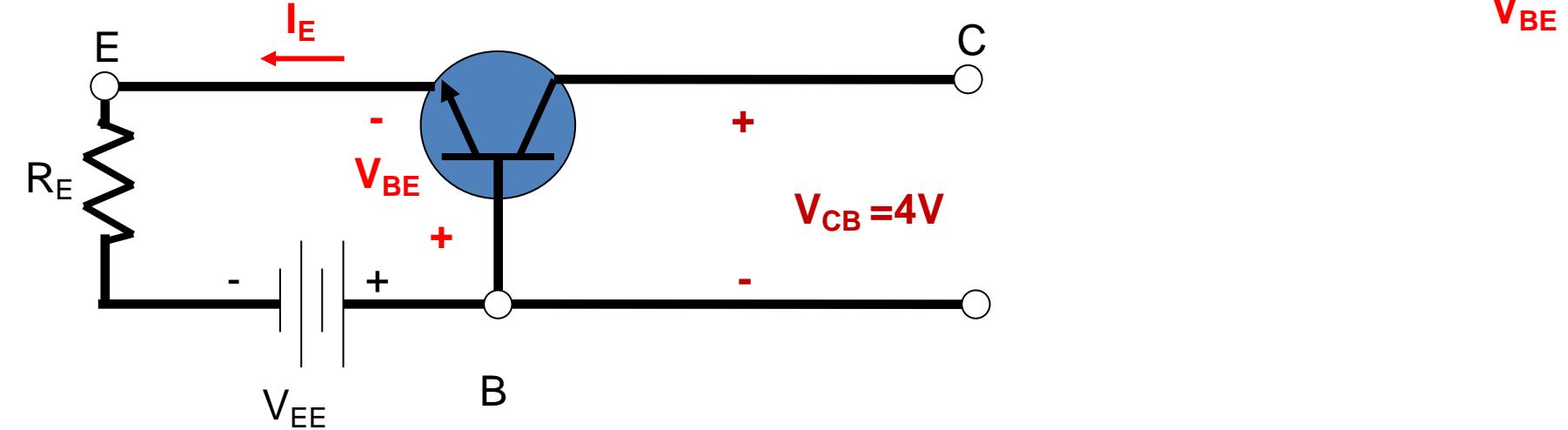
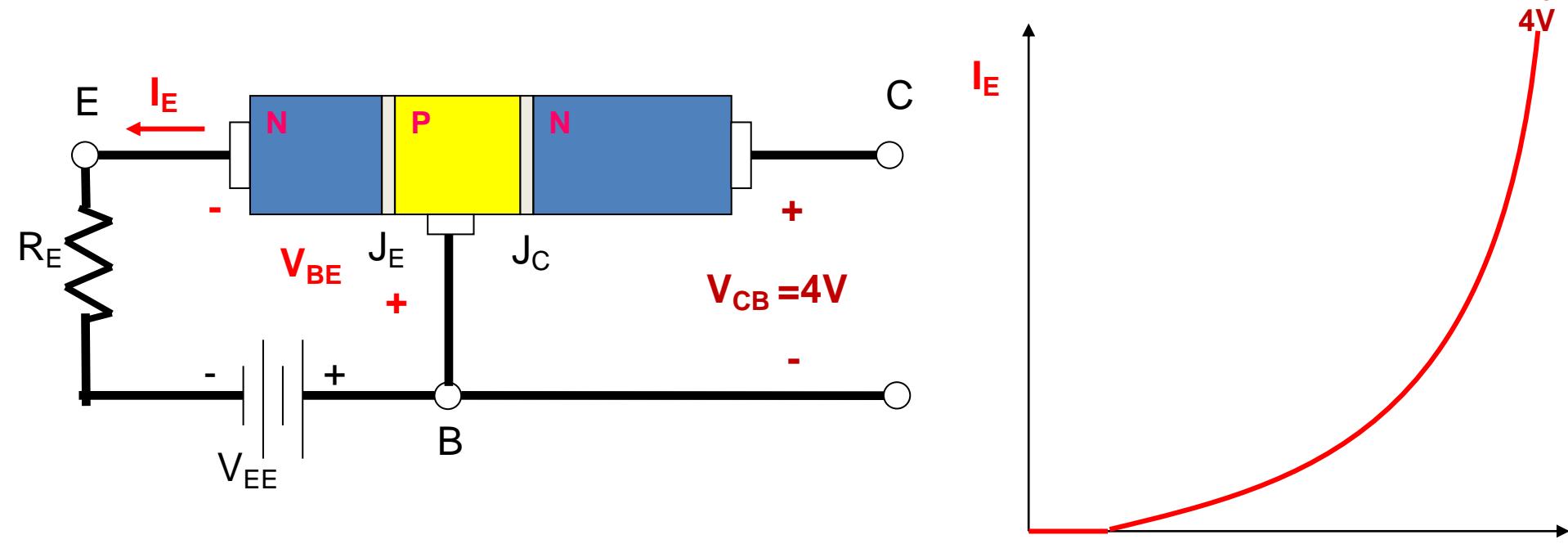
Characteristics of a transistor in CB configuration

Input characteristics



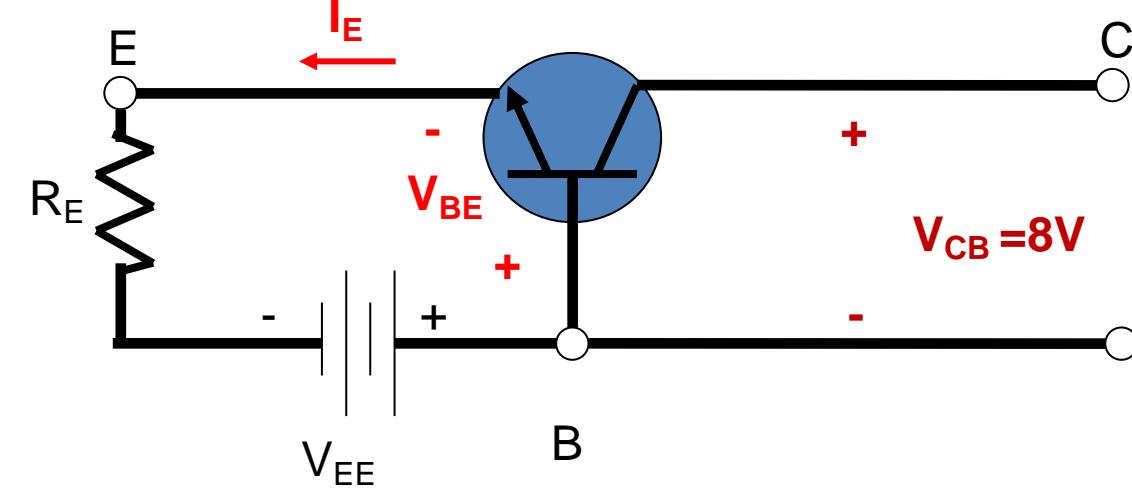
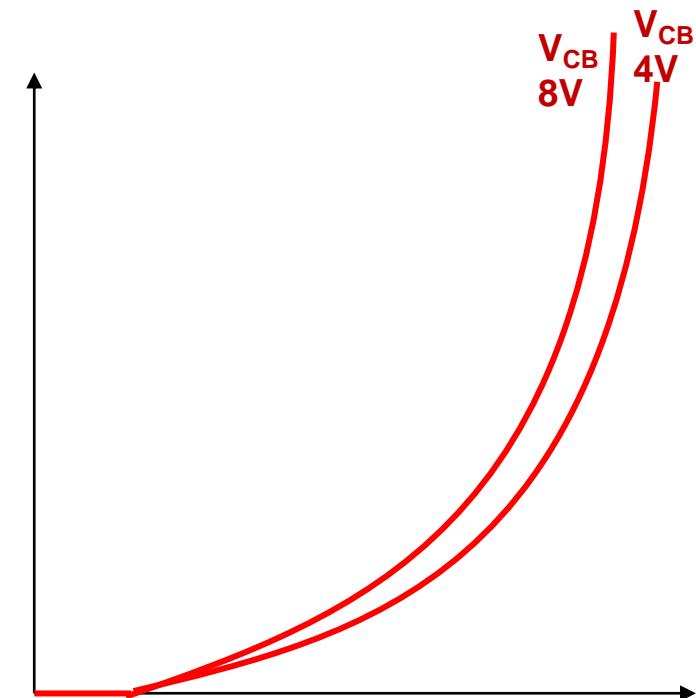
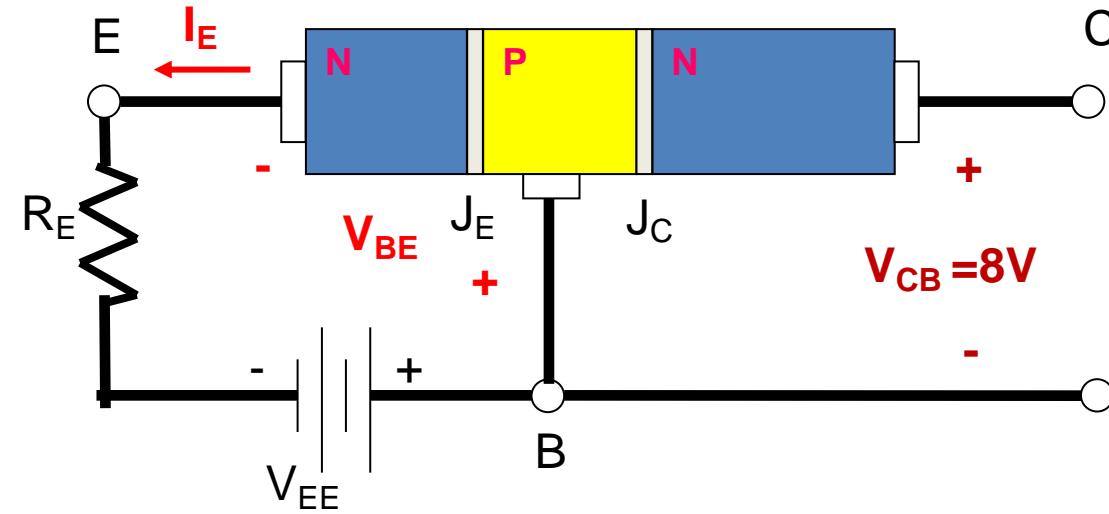
Characteristics of a transistor in CB configuration

Input characteristics



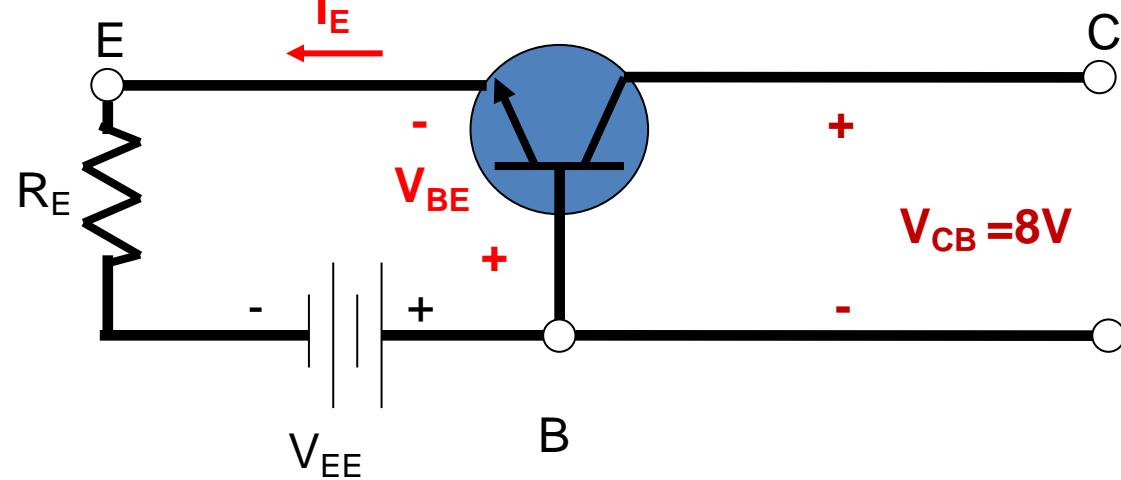
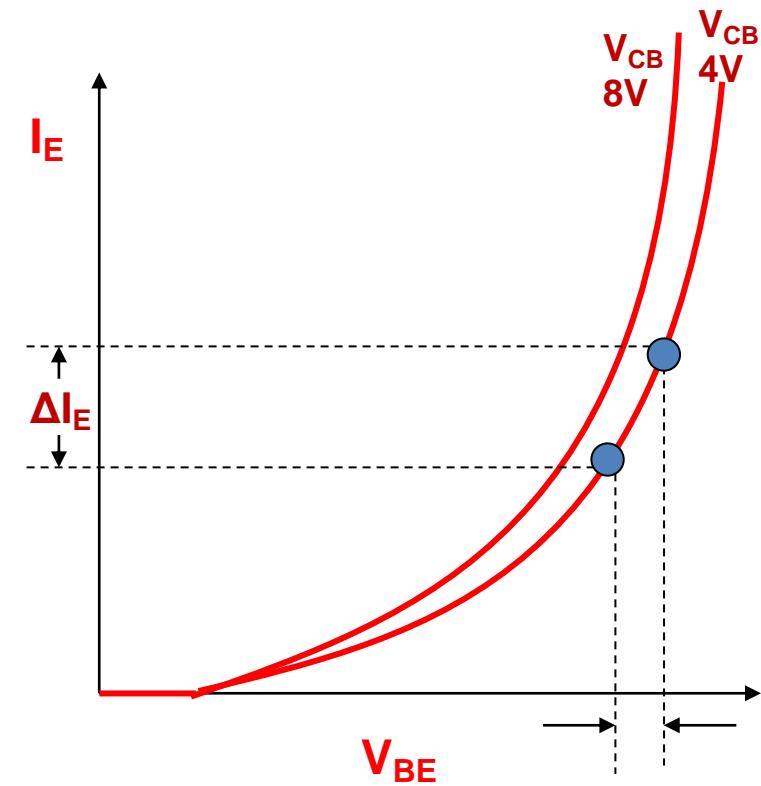
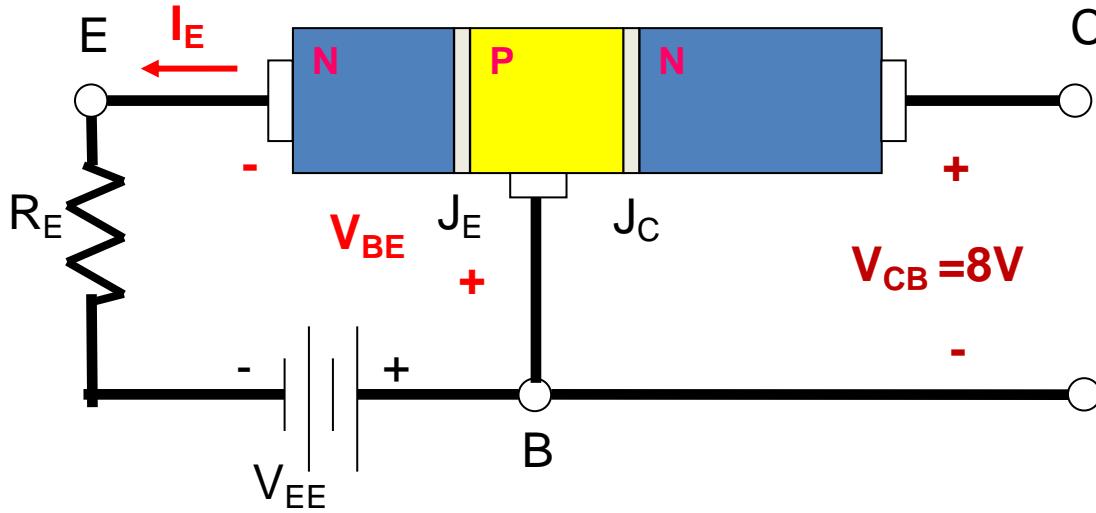
Characteristics of a transistor in CB configuration

Input characteristics



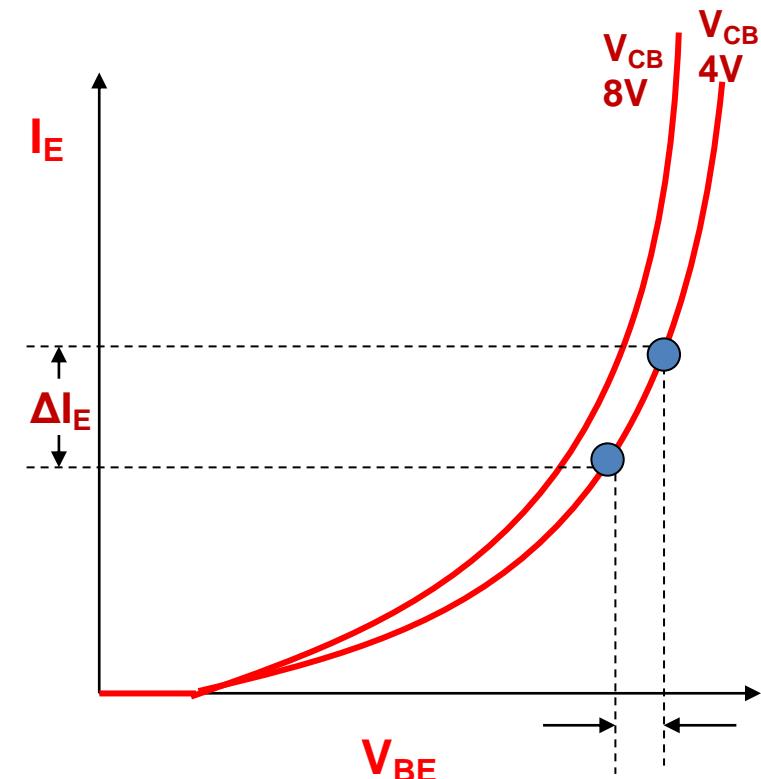
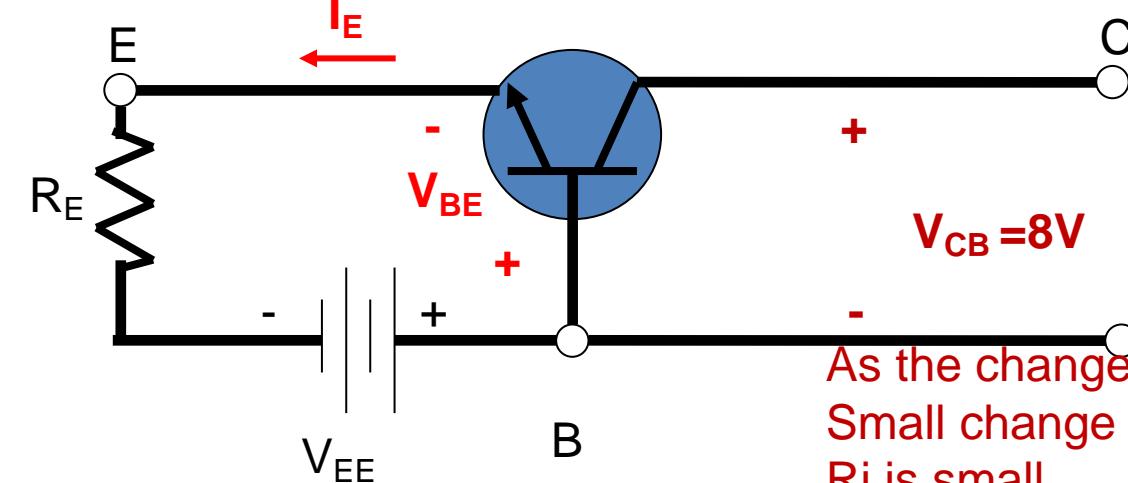
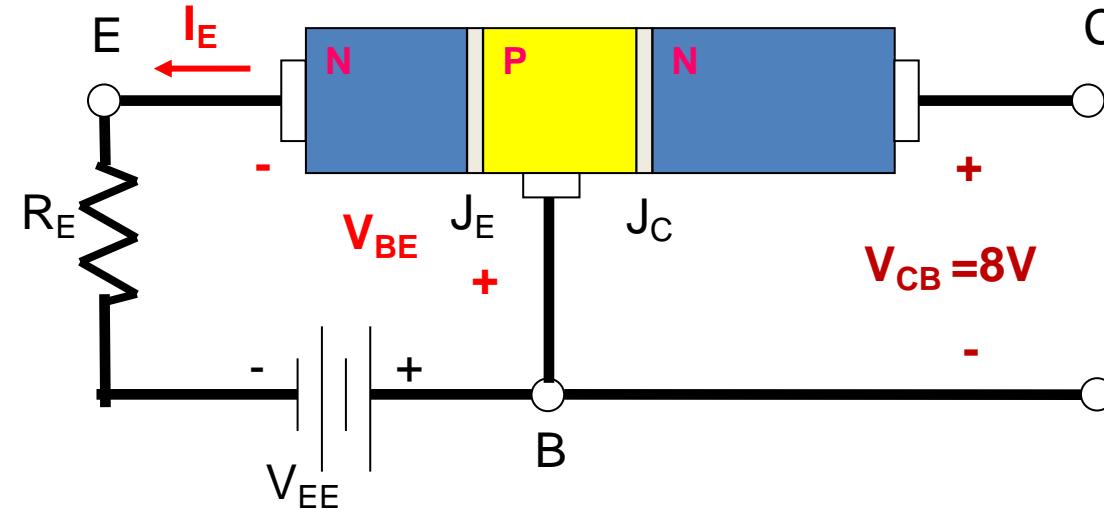
Characteristics of a transistor in CB configuration

Input characteristics



Characteristics of a transistor in CB configuration

Input characteristics



$$\text{Input resistance } R_i = \frac{\Delta V_{BE}}{\Delta I_E}$$

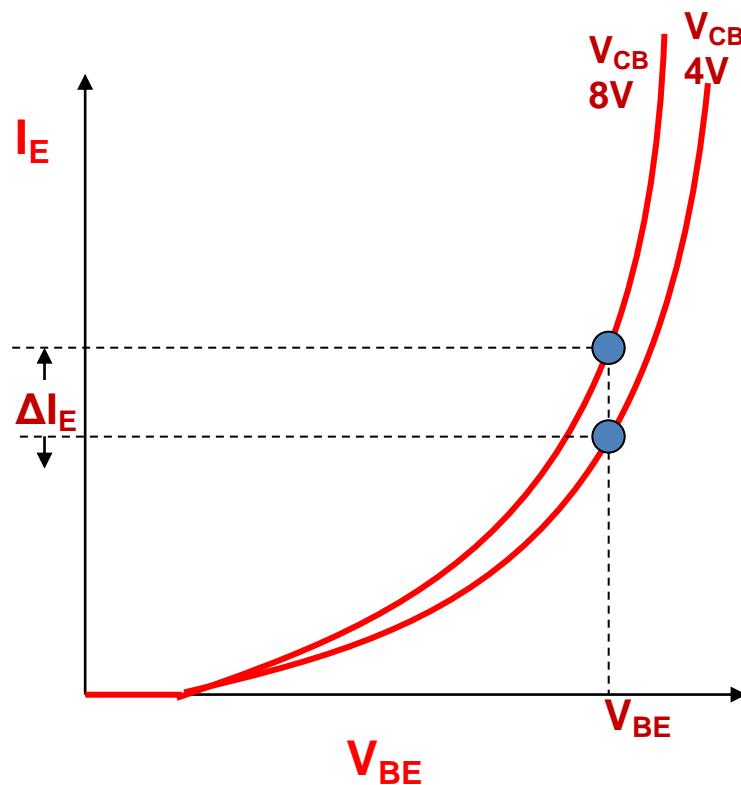
at constant V_{CB}

As the change in emitter current is very large for a small change in input voltage, the input resistance R_i is small

Characteristics of a transistor in CB configuration

Input characteristics

Effect of VCB (output voltage) on the input characteristics :



- As shown in figure the emitter current increases slightly with increase in the output voltage (V_{CB}).
- This happens due to a special phenomenon called “Early effect” or “base width modulation”.

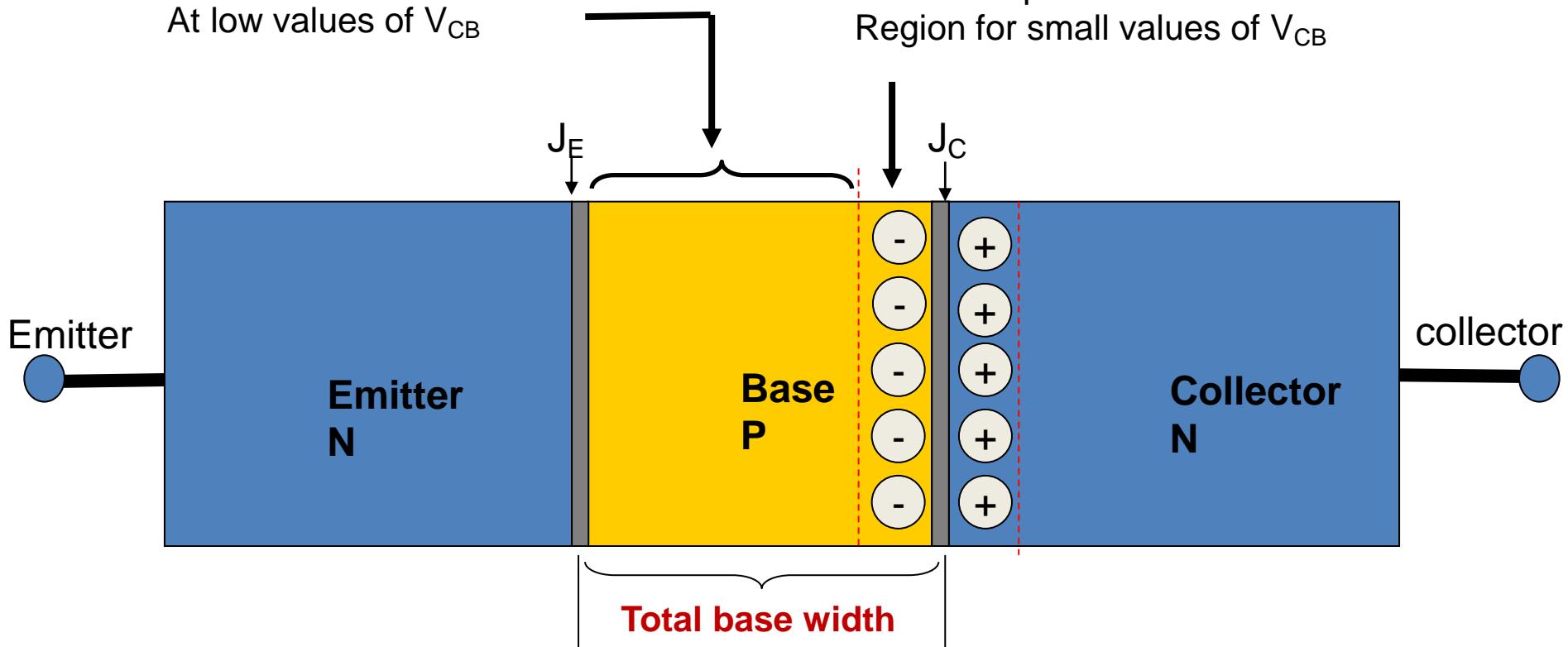
Characteristics of a transistor in CB configuration

Input characteristics

“Early effect” or “base width modulation”.

Larger effective base width
At low values of V_{CB}

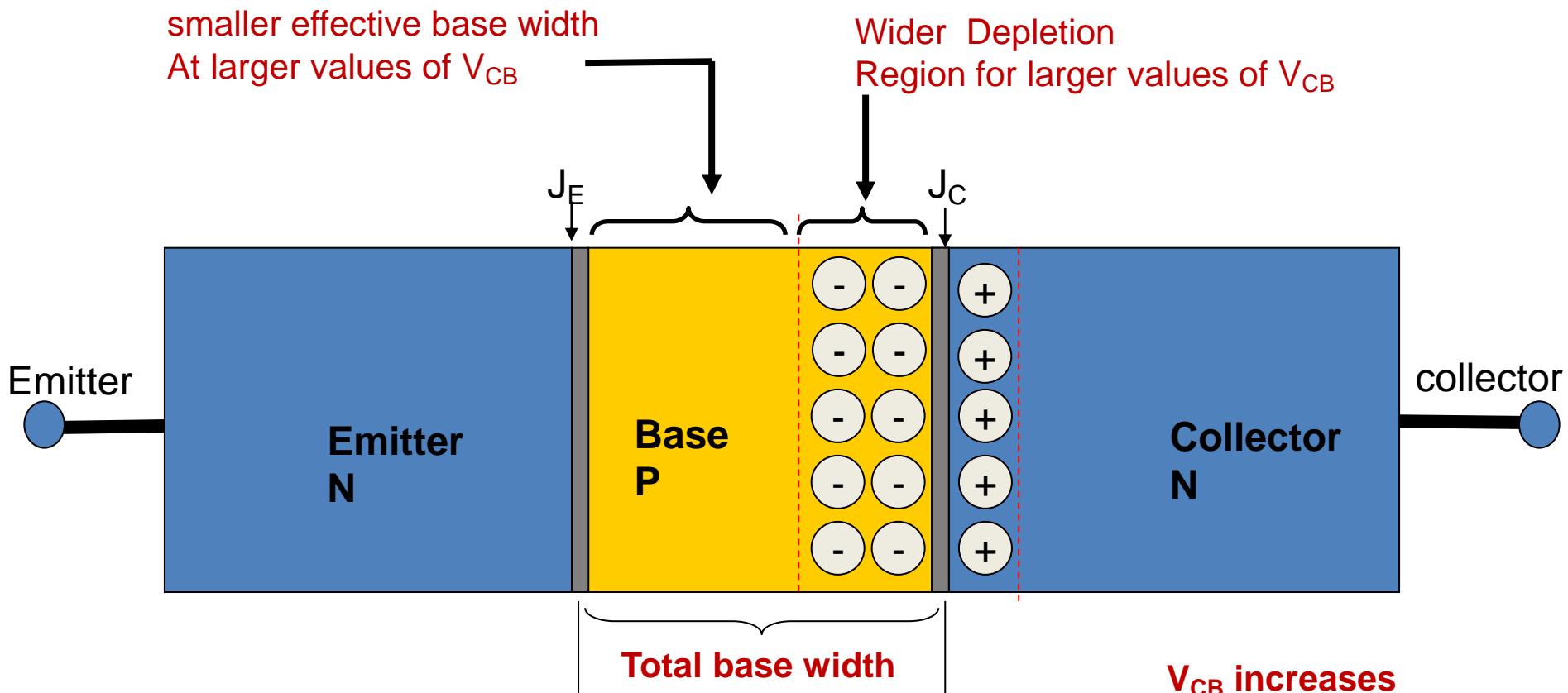
Narrow Depletion
Region for small values of V_{CB}



Characteristics of a transistor in CB configuration

Input characteristics

“Early effect” or “base width modulation”.

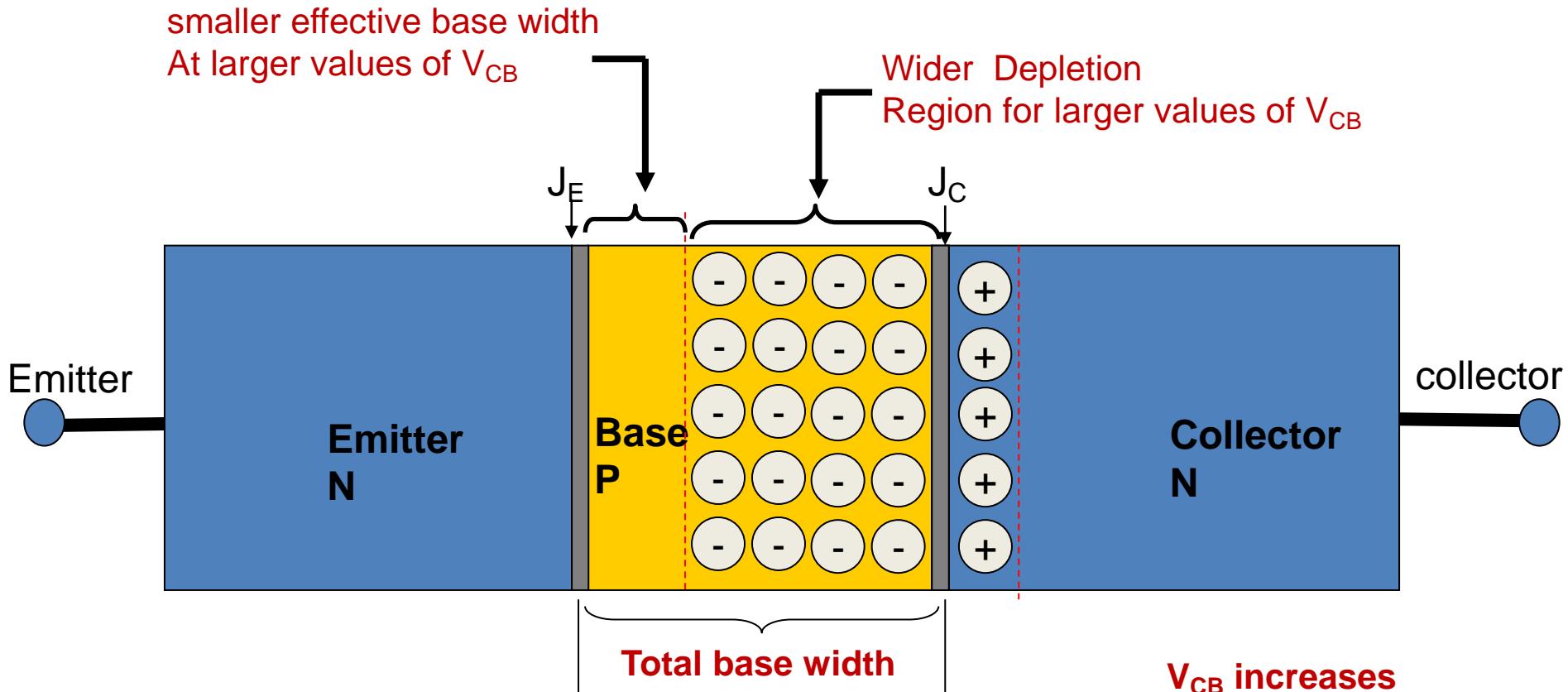


- As V_{CB} is increased, the reverse voltage applied to the CB junction increases.
- This widens the depletion region at the collector junction
- Due to this, effective width of the base region decreases

Characteristics of a transistor in CB configuration

Input characteristics

“Early effect” or “base width modulation”.

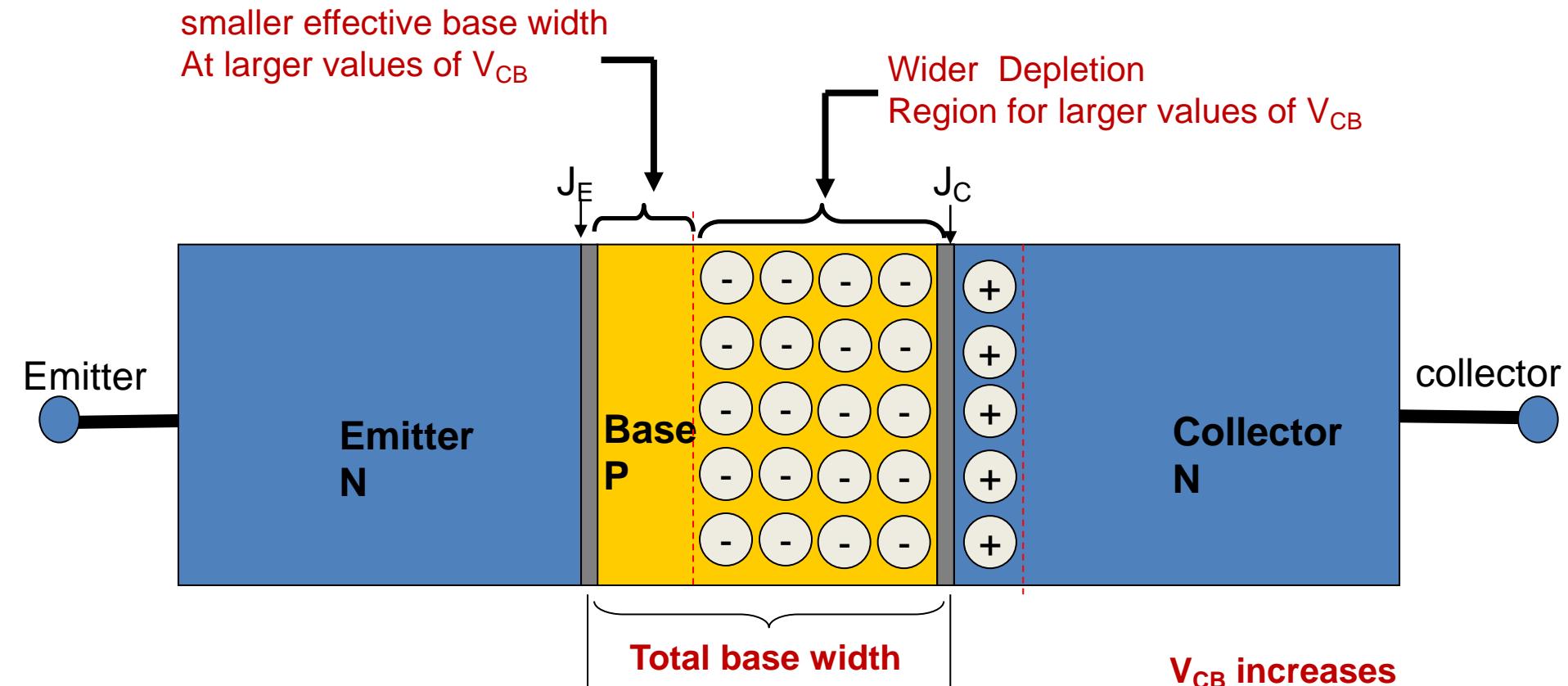


- As V_{CB} is increased, the reverse voltage applied to the CB junction increases.
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Characteristics of a transistor in CB configuration

Input characteristics

“Early effect” or “base width modulation”.

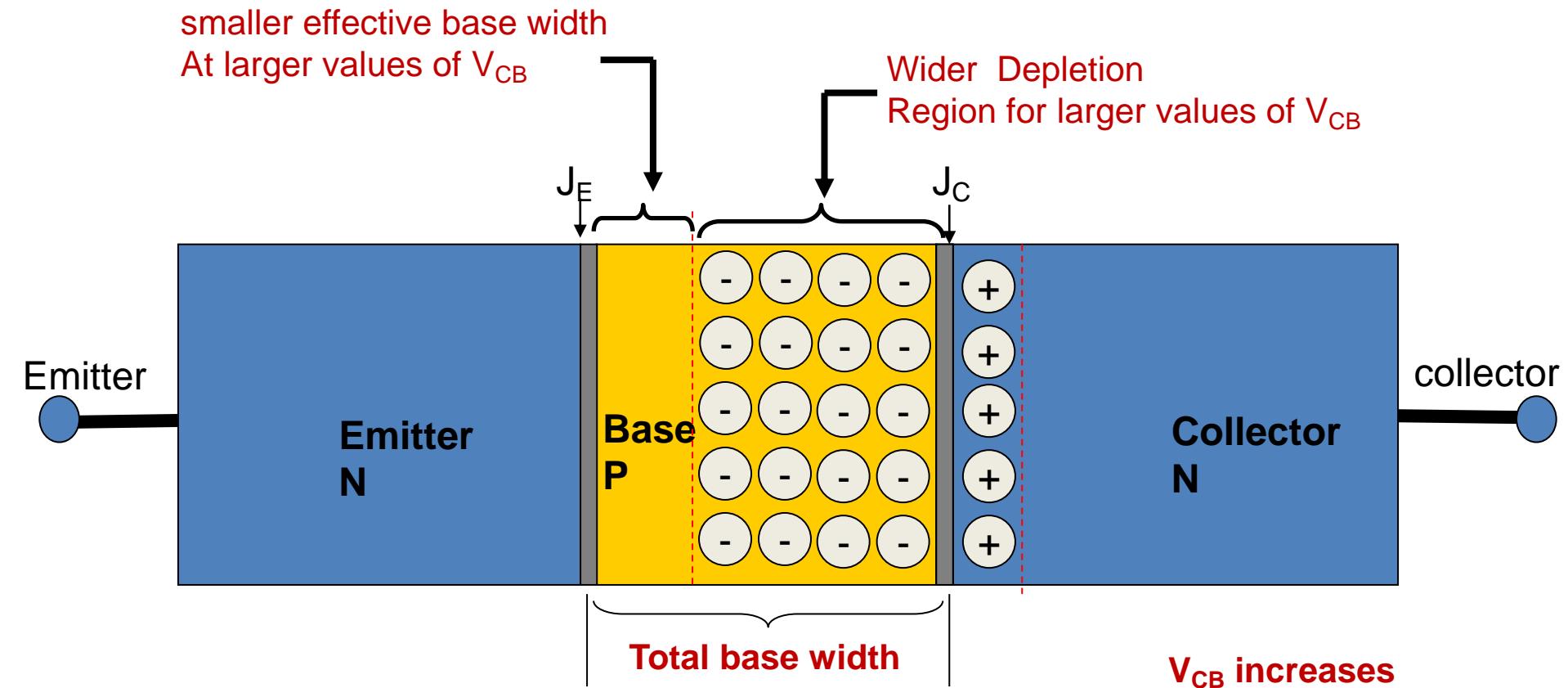


- This will increase the charge concentration gradient in the base region.
- Due to increase in the charge carrier concentration, more number of electrons diffuse from the emitter to the base i.e. emitter current increases.

Characteristics of a transistor in CB configuration

Input characteristics

“Early effect” or “base width modulation”.



- Thus increase in V_{CB} the input I_E increases slightly

Characteristics of a transistor in CB configuration

Input characteristics

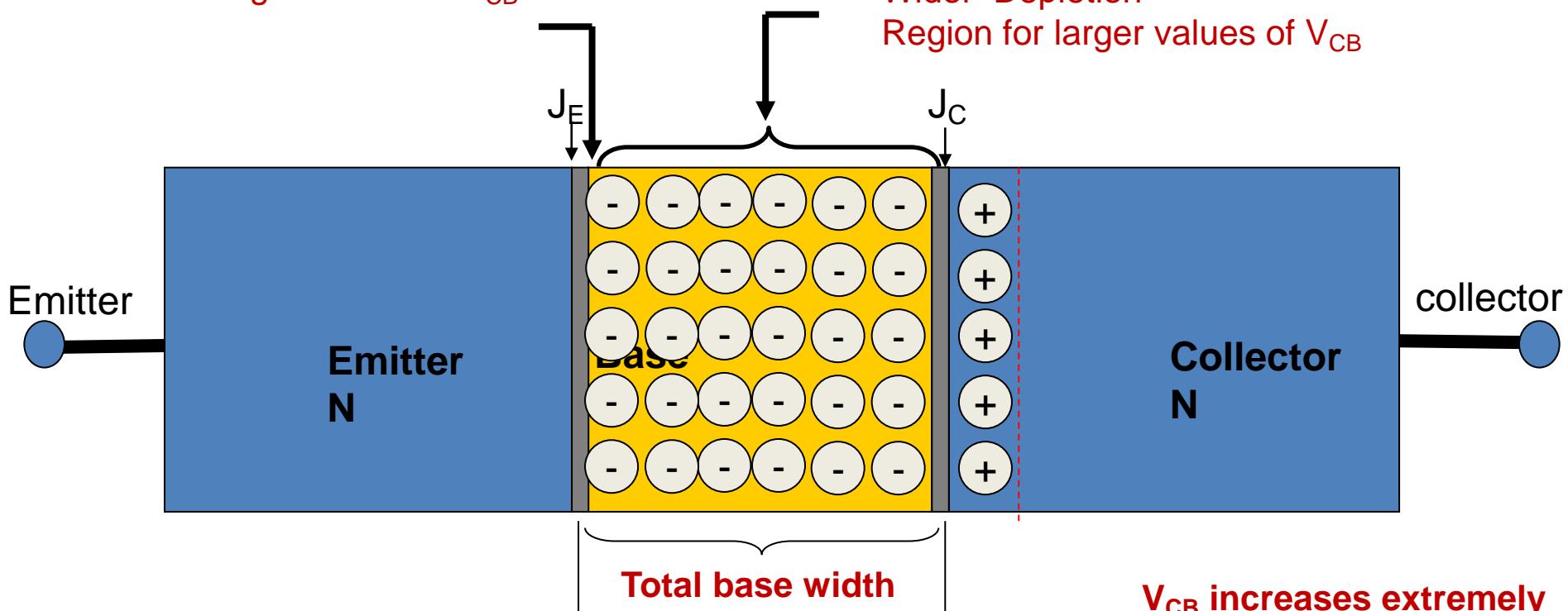
“Early effect” or “base width modulation”.

zero effective base width

At larger values of V_{CB}

Wider Depletion

Region for larger values of V_{CB}

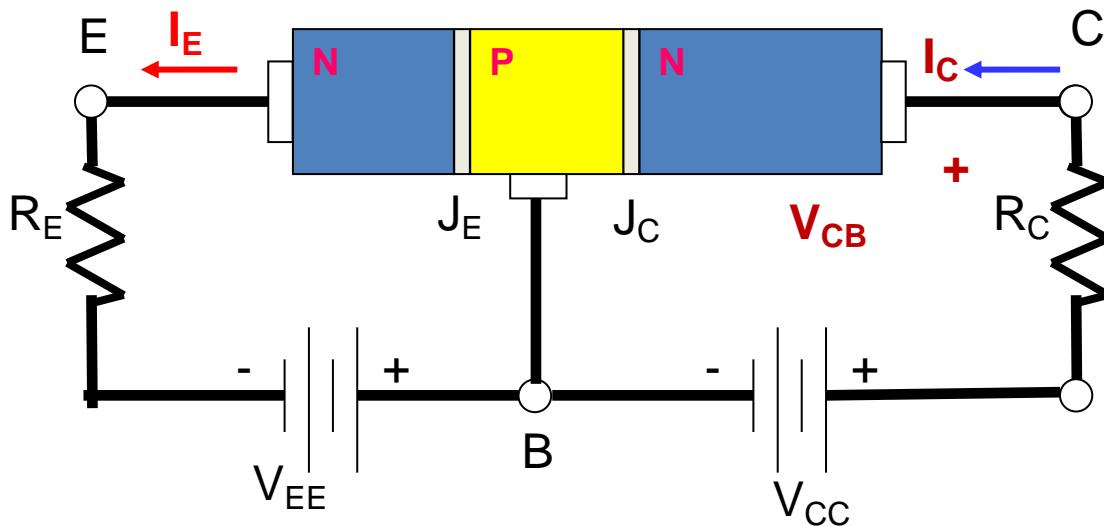


- For extremely large V_{CB} the effective base width may be reduced to zero, causing voltage breakdown of a transistor.
- This phenomenon is known as punch through

Characteristics of a transistor in CB configuration

Output characteristics

Constant

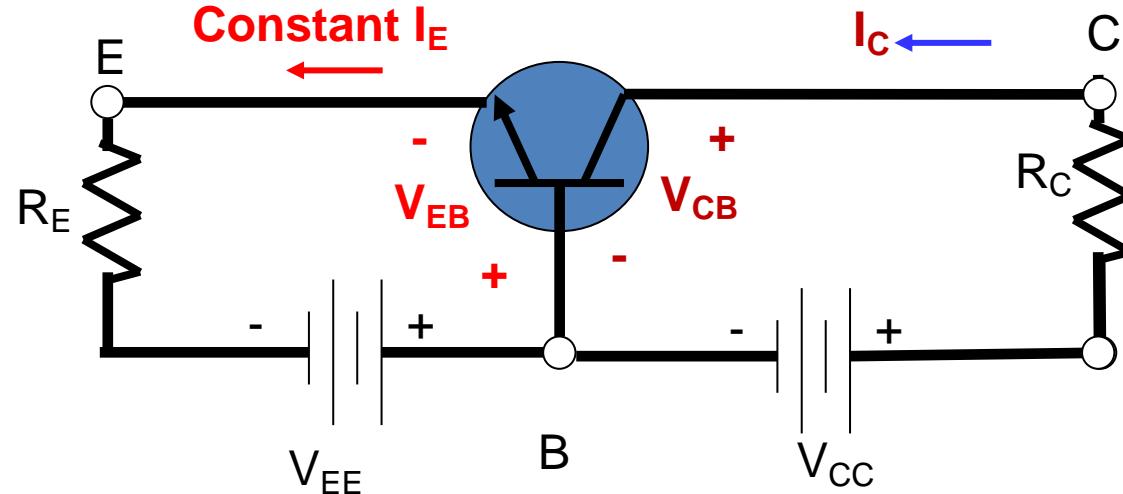


- output characteristics is always A graph of output current versus output voltage.

- For the CB configuration, output Current is I_C and output voltage Is the collector to base voltage V_{CB}

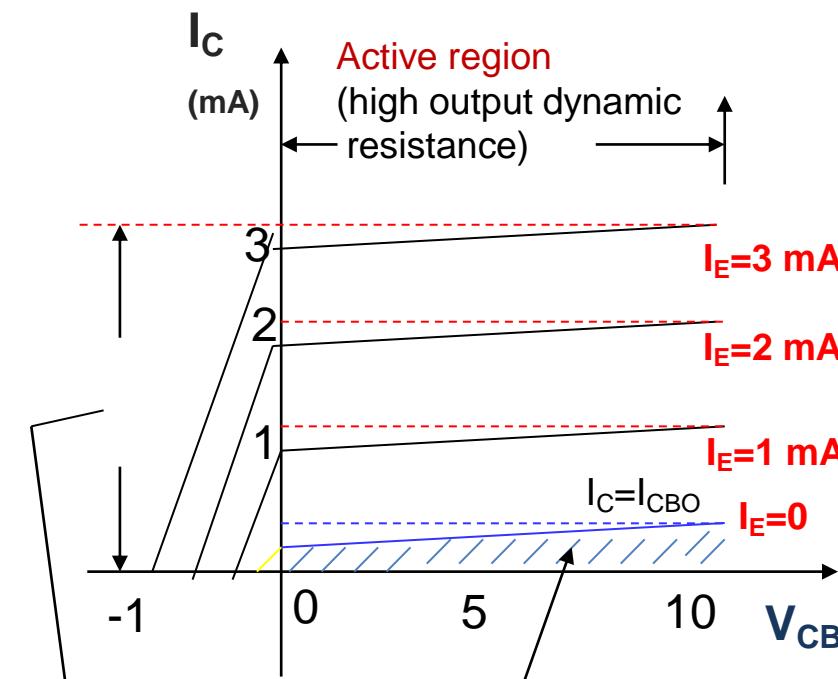
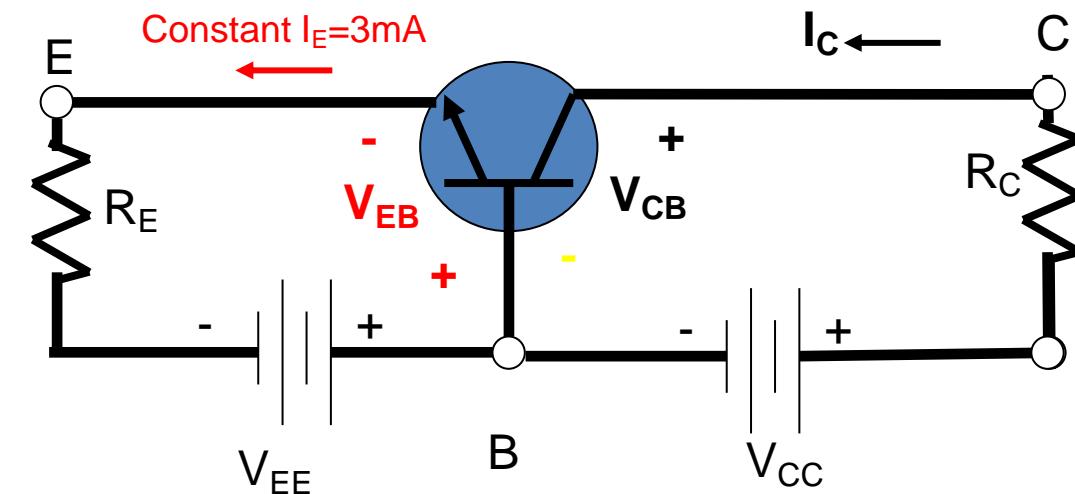
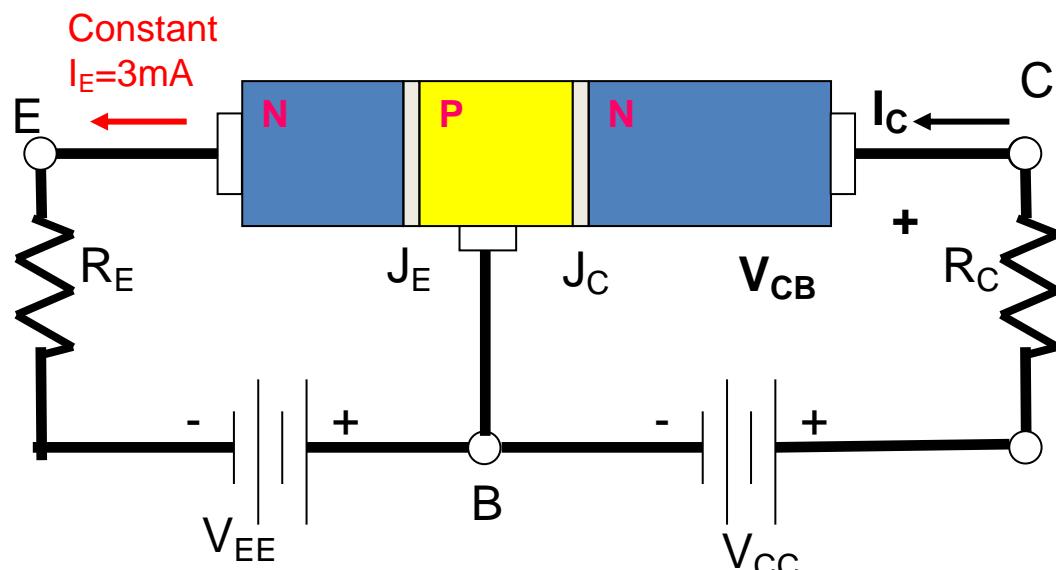
- Input characteristics is plotted at a constant input current I_E

Constant I_E



Characteristics of a transistor in CB configuration

Output characteristics



Cutoff region
Both the junction
Becomes reverse bias

saturation region
Both the junction
Becomes forward bias

Characteristics of a transistor in CB configuration

Output characteristics

Dynamic output resistance of the transistor :

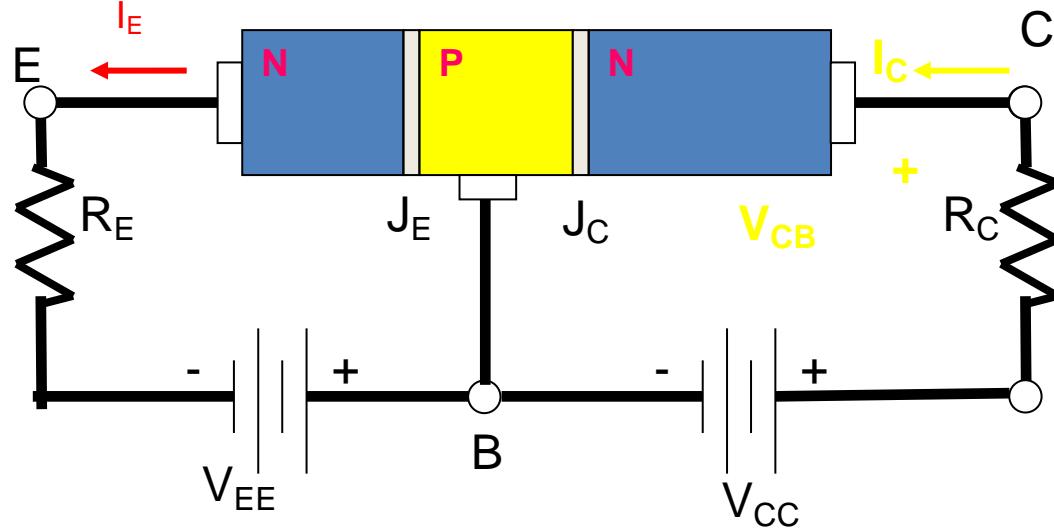
$$R_o = \Delta V_{CB} / \Delta I_C$$

for I_E constant

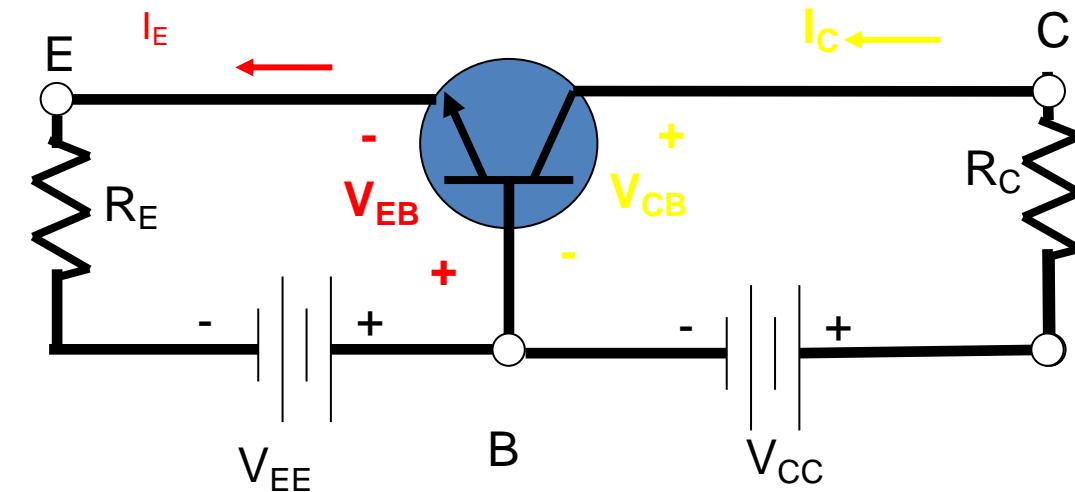
- This is nothing but the reciprocal of the output characteristics in the active region.
- Slope of the output characteristics in the active region is very small.
- Therefore the dynamic resistance R_o in the active region is high.
- That's why the voltage drop across the transistor is very large in active region

Characteristics of a transistor in CB configuration

Transfer characteristics

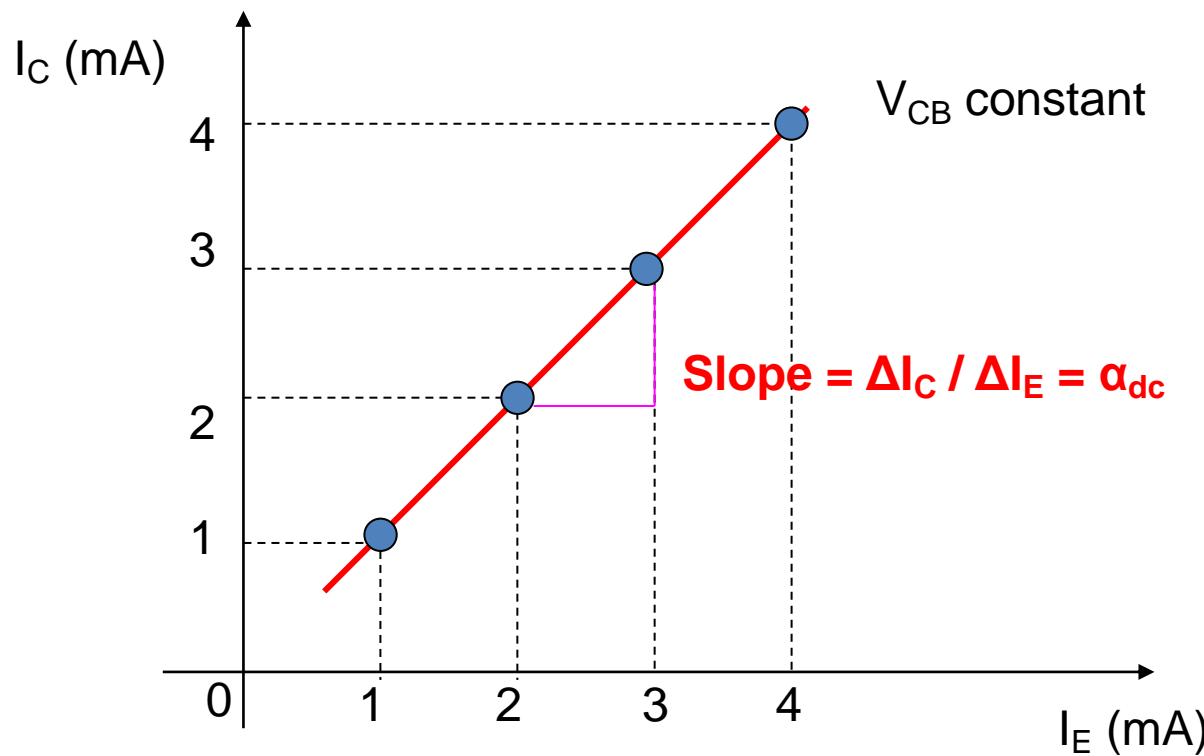


- Transfer characteristics is a graph Of output current (I_C) versus input Current (I_E)
- This characteristics is also called as Current gain characteristics.
- The transfer characteristics is plotted for constant value of V_{CB}



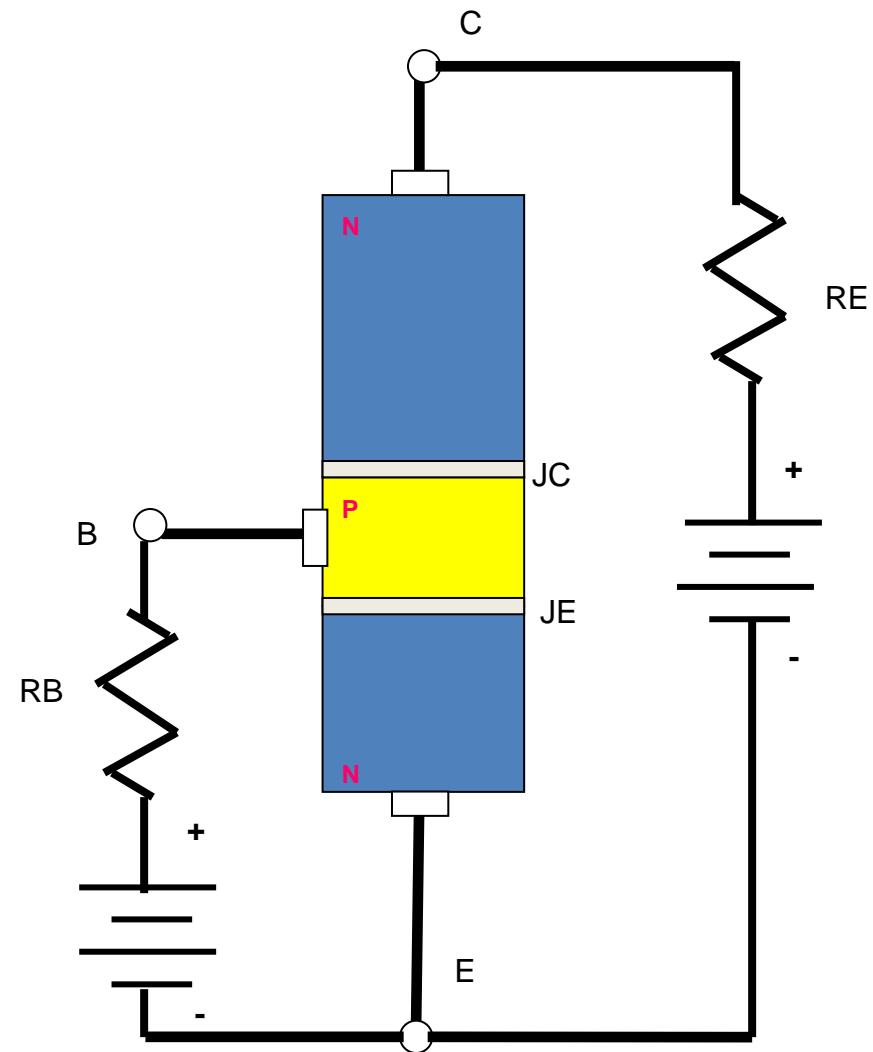
Characteristics of a transistor in CB configuration

Transfer characteristics

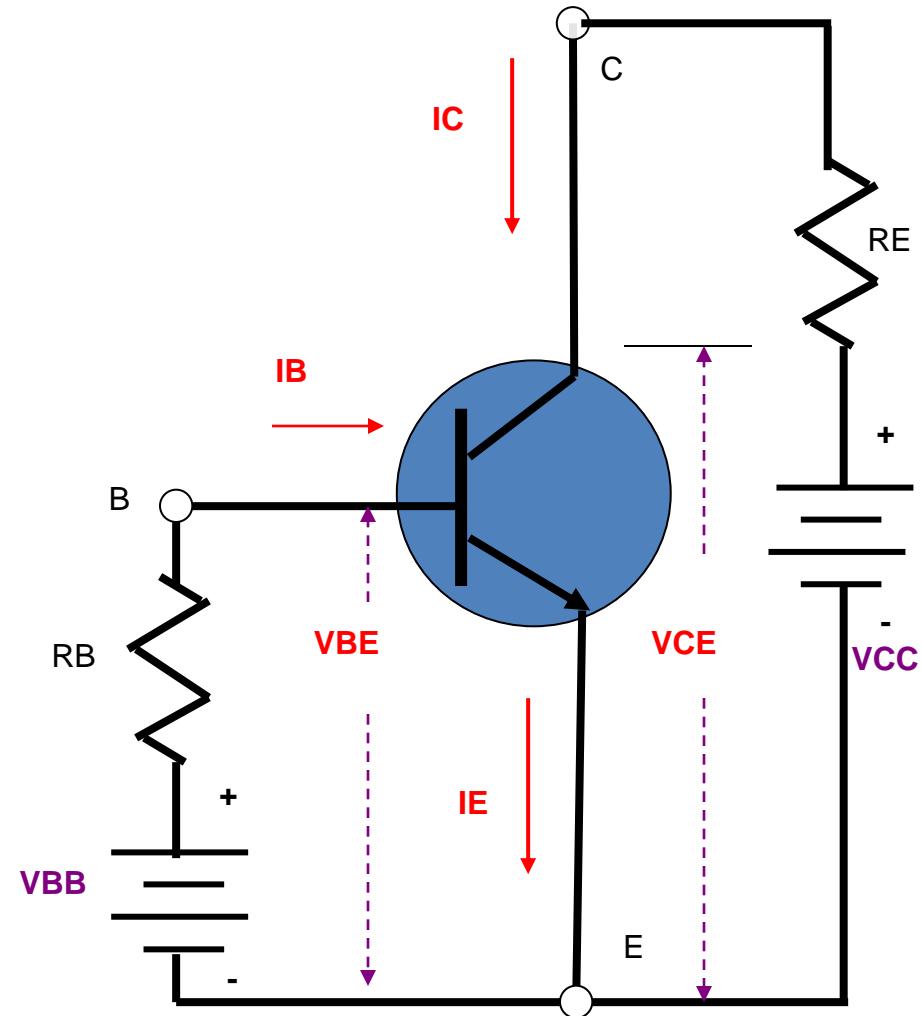


$$\alpha_{dc} = \Delta I_C / \Delta I_E$$

Common emitter configuration



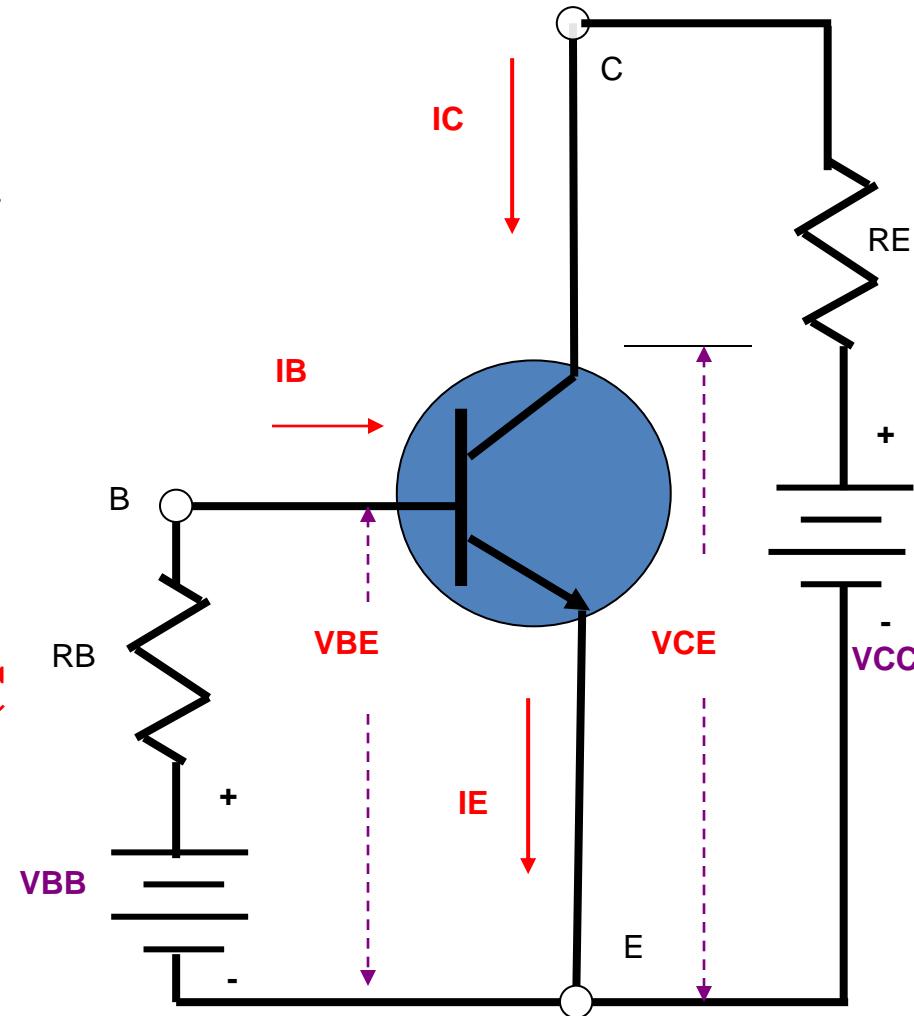
N-P-N Transistor



Common emitter configuration

Emitter acts as a common terminal between input and the output. The input voltage is applied between base and emitter. Hence **V_{BE}** is the input voltage and **I_B** is the input current.

The output is taken between the collector and emitter. Therefore **V_{CE}** is the output voltage and **I_C** is the output current.



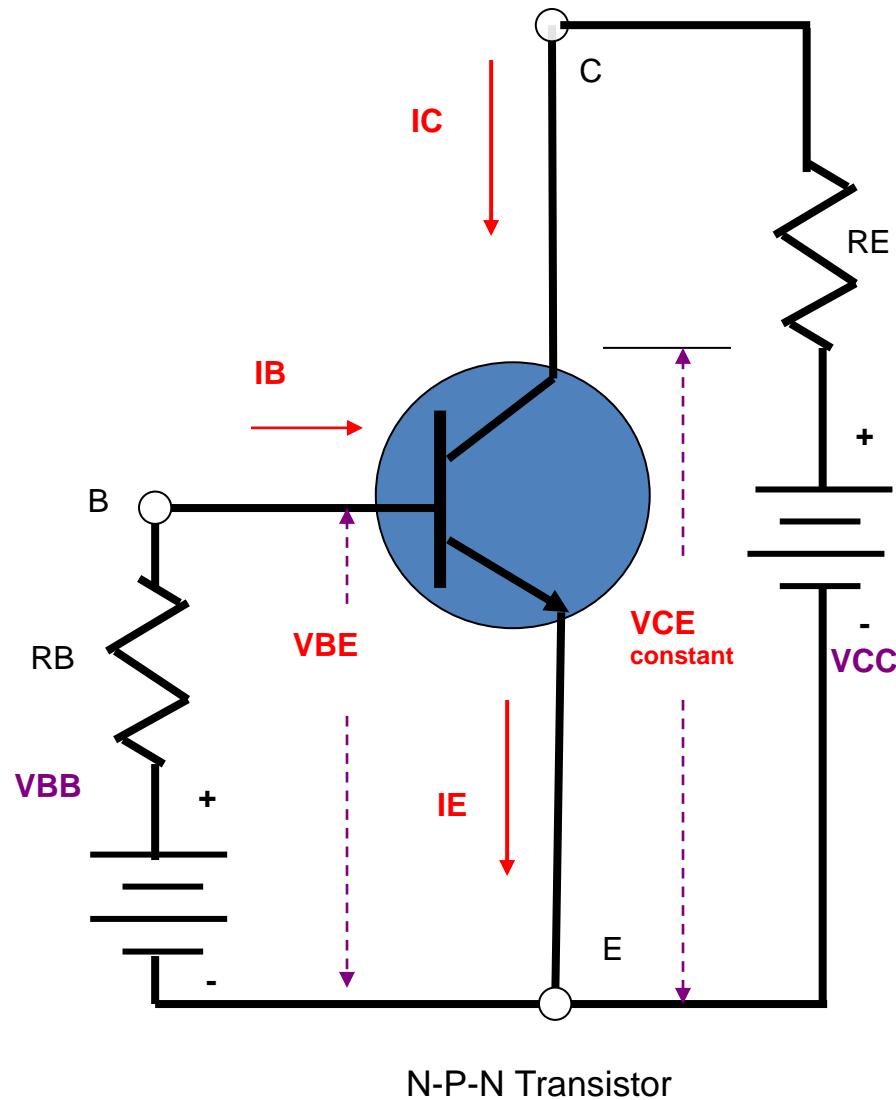
N-P-N Transistor

Characteristics of a transistor in CE configuration

- Input characteristics
- Output characteristics
- Transfer characteristics

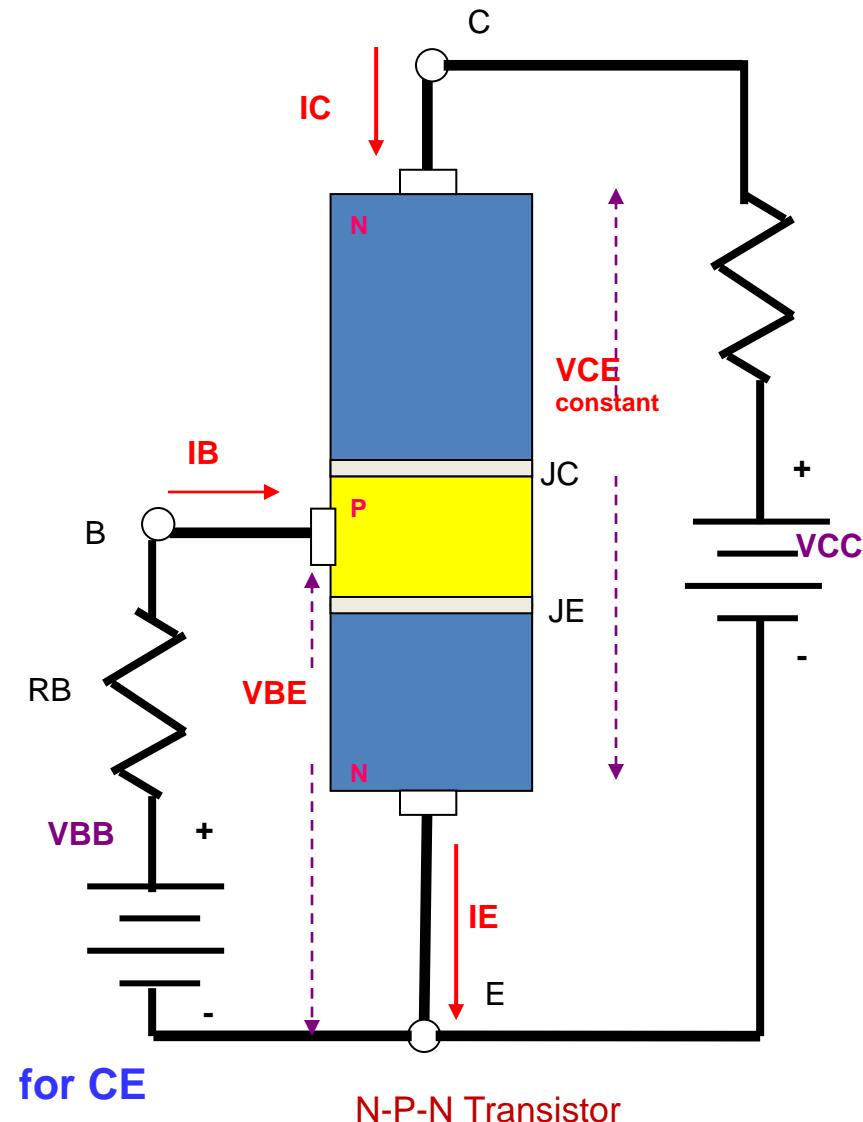
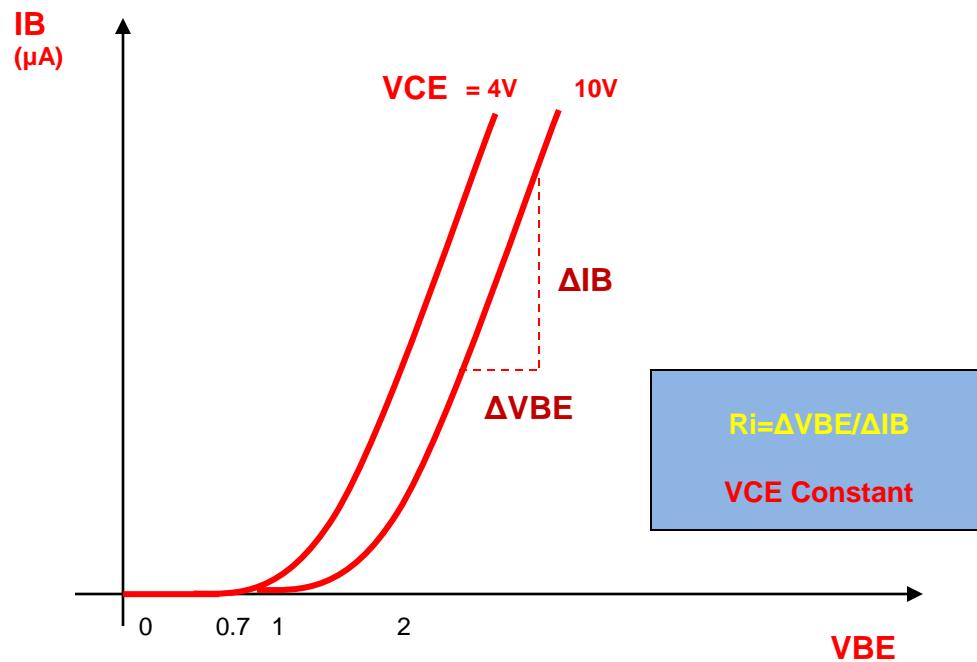
Characteristics of a transistor in CE configuration

- **Input characteristics:**
- It is a graph of input current (I_B) versus input voltage (V_{BE}) at a constant output voltage (V_{CE}).



Characteristics of a transistor in CE configuration

- **Input characteristics:**
- It is a graph of input current (I_B) versus input voltage (V_{BE}) at a constant output voltage (V_{CE}).

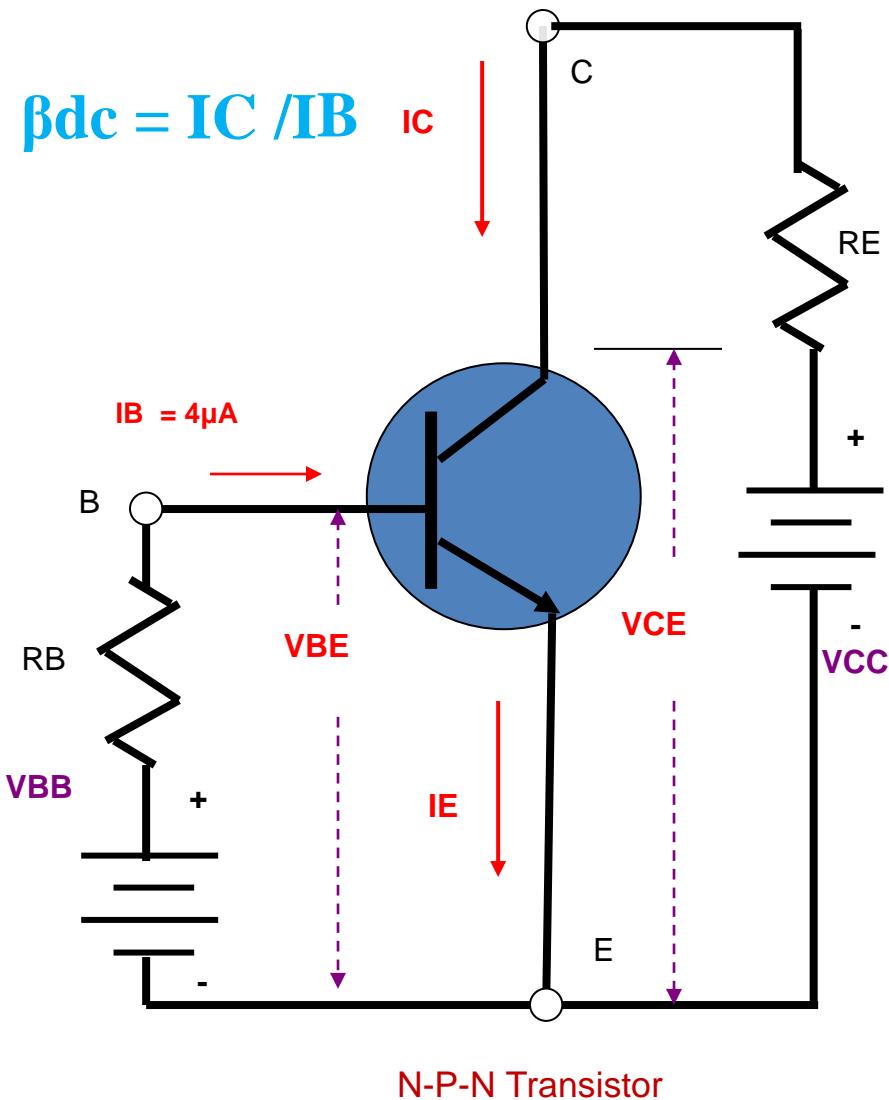
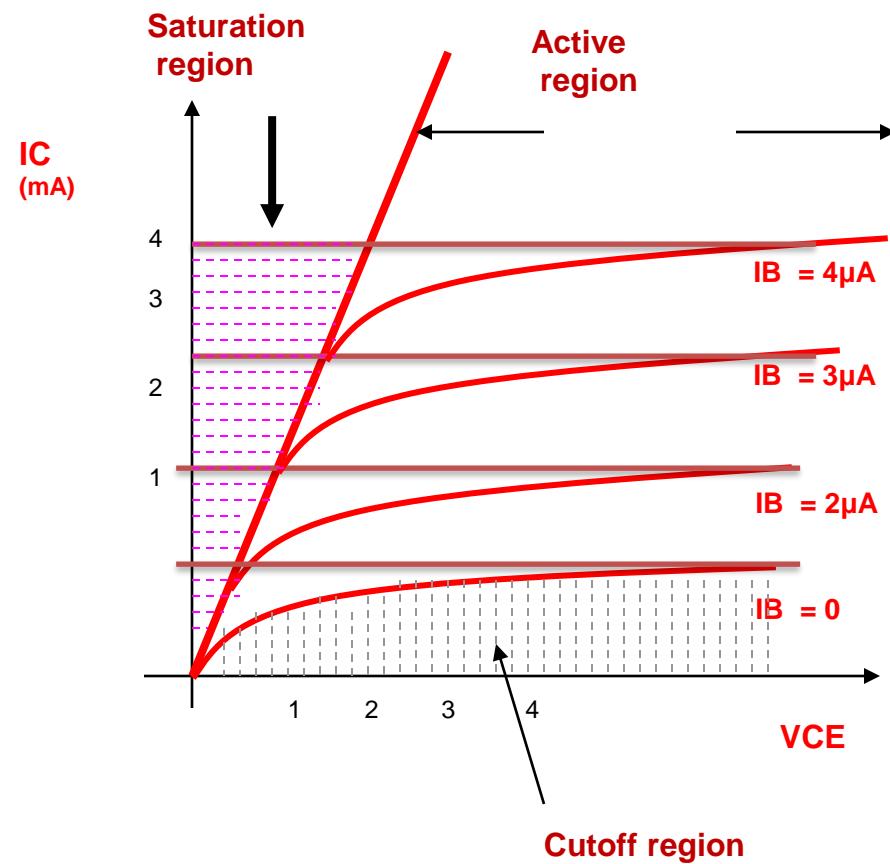


The value of dynamic input resistance “ R_i ” is low for CE

N-P-N Transistor

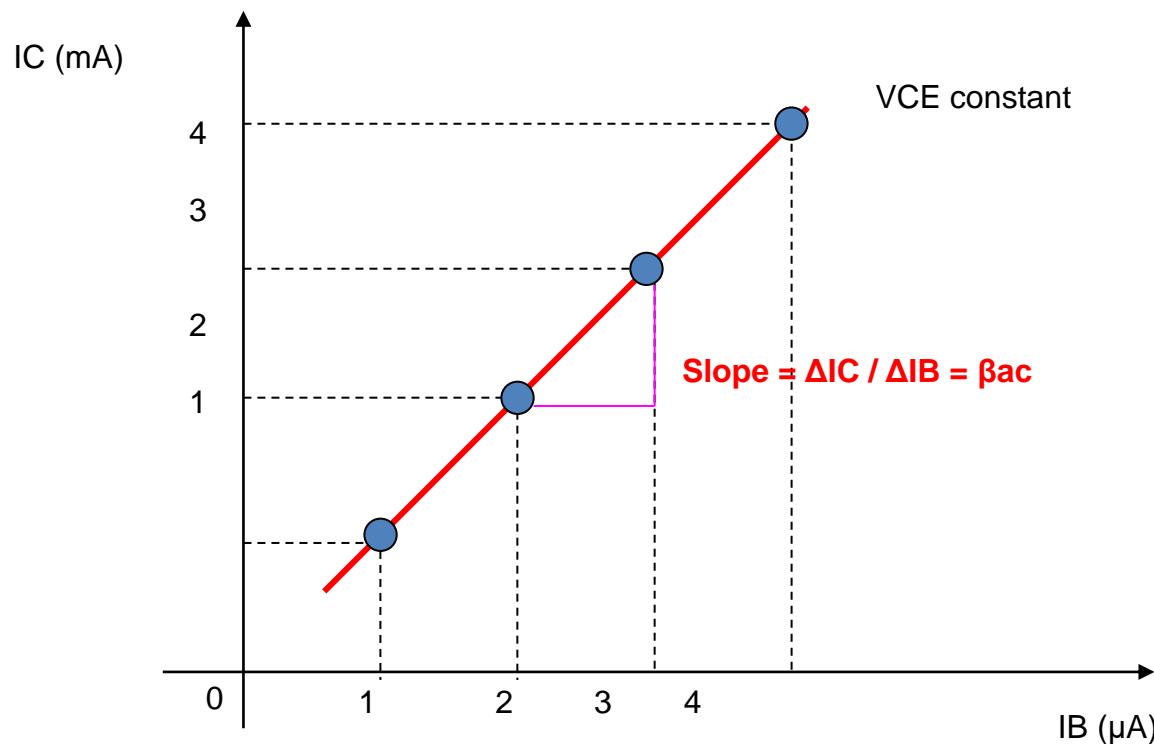
Characteristics of a transistor in CE configuration

- **Output characteristics:**
- It is a graph of output current (I_C) versus output voltage (V_{CE}) at a constant input current (I_B)



Characteristics of a transistor in CE configuration

Transfer characteristics



$$\beta_{ac} = \Delta I_C / \Delta I_B$$

$$\beta_{dc} = I_C / I_B$$

VCE constant

Relation between α_{dc} and β_{dc}

The expression for β_{dc} in terms of α_{dc}

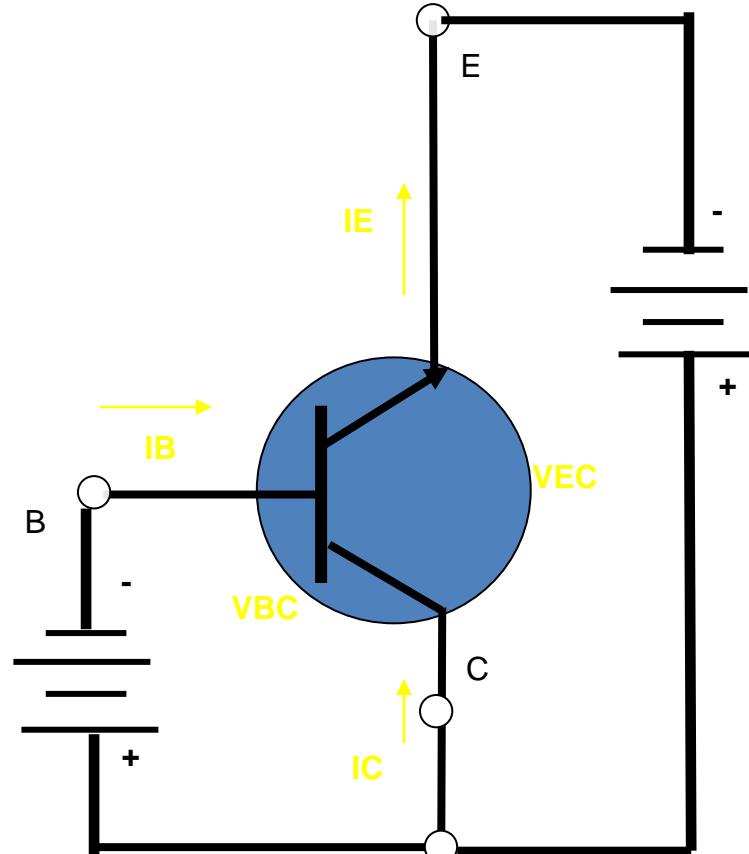
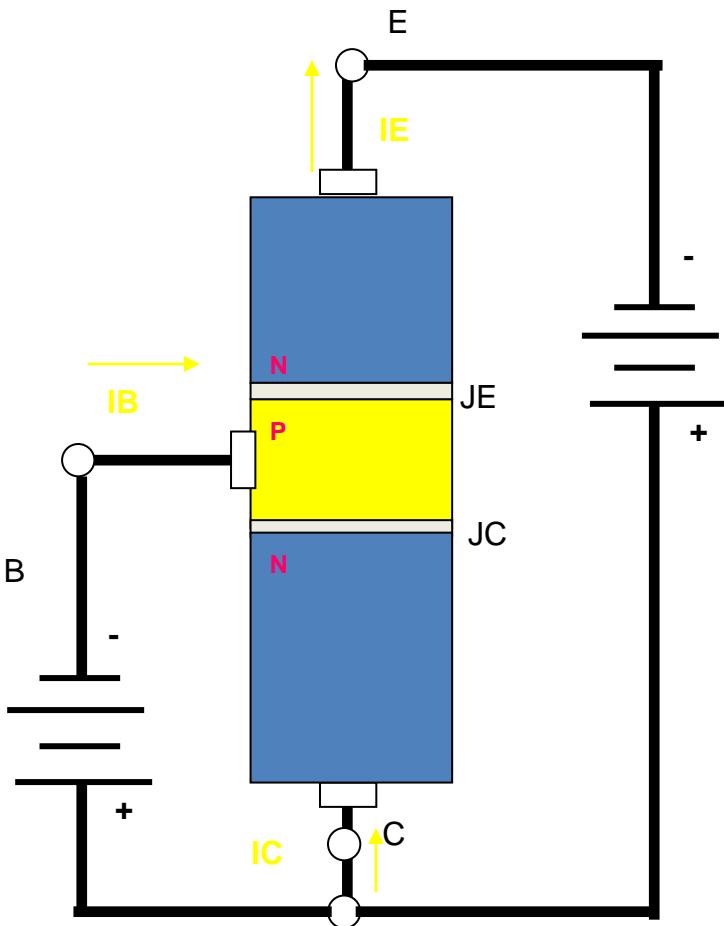
$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

The expression α_{dc} for in terms of β_{dc}

$$\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc} + 1}$$

Common collector configuration

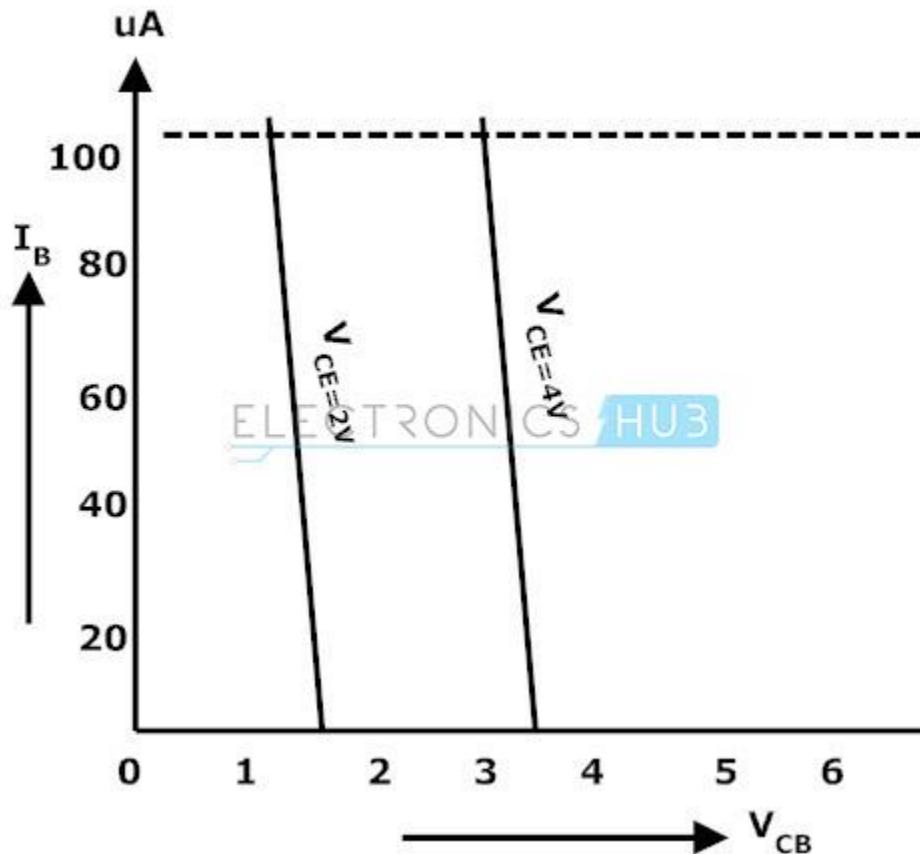
EMITTER FOLLOWER



N-P-N Transistor

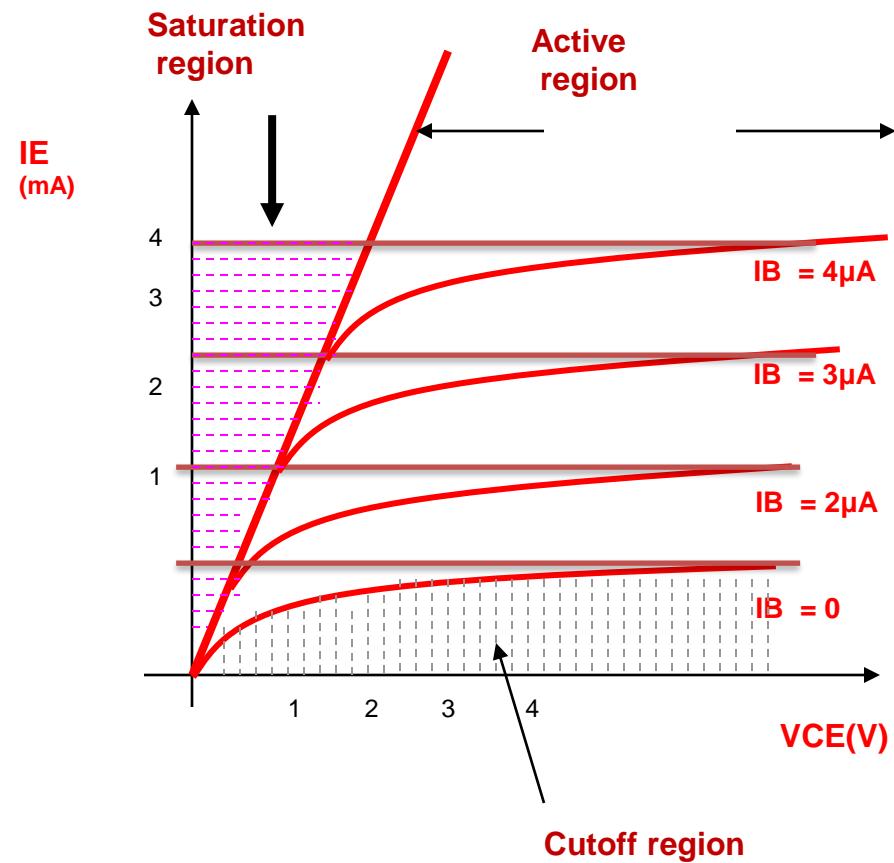
Characteristics of a transistor in CC configuration

Input characteristics:



Characteristics of a transistor in CC configuration

- **Output characteristics:**
- It is a graph of output current (I_c) versus output voltage (V_{CE}) at a constant input current (I_B)



$$\text{Current gain } \gamma = I_E/I_B$$

Current gain of common collector configuration

- The current gain of a transistor in a common collector configuration is denoted by γ (gamma) and is defined as:
- Current gain $\gamma = I_E/I_B$
 $= (I_C + I_B) / I_B$
 $= 1 + \beta_{dc}$ since $\beta_{dc} = I_C/I_B$
 $\gamma \approx \beta_{dc}$

Comparison of configuration

Sr. No.	Parameter	CB	CE	CC
1	Common terminal between input and output	Base	Emitter	Collector
2	Phase Difference/ Conduction angle	0 °	180 °	0 °
3	Input current	I _E	I _B	I _B
4	Output current	I _C	I _C	I _E
5	Current gain	$\alpha_{DC} = I_C/I_E$ Less than one	$\beta_{DC} = I_C/I_B$ High	$\gamma = I_E/I_B$ HIGH
6	Input Voltage	V _{eb}	V _{be}	V _{bc}
7	Output voltage	V _{cb}	V _{ce}	V _{ec}
8	Current gain	Less than unity	High	High
9	Input resistance	Very low (20Ω)	Low (1KΩ)	High(500kΩ)
10	Output resistance	Very high (1M)	High(40kΩ)	Low (50Ω)
11	Application	As preamplifier	Audio amplifier	Impedance matching

Why is CE configuration most preferred configuration ?

- Out of three configurations, the CE configuration is the most popular and widely used configurations. The reasons are as follows :
- **It has high voltage gain as well as a high current gain.**
- **As voltage gain and current gain are high, it has very high power gain.**

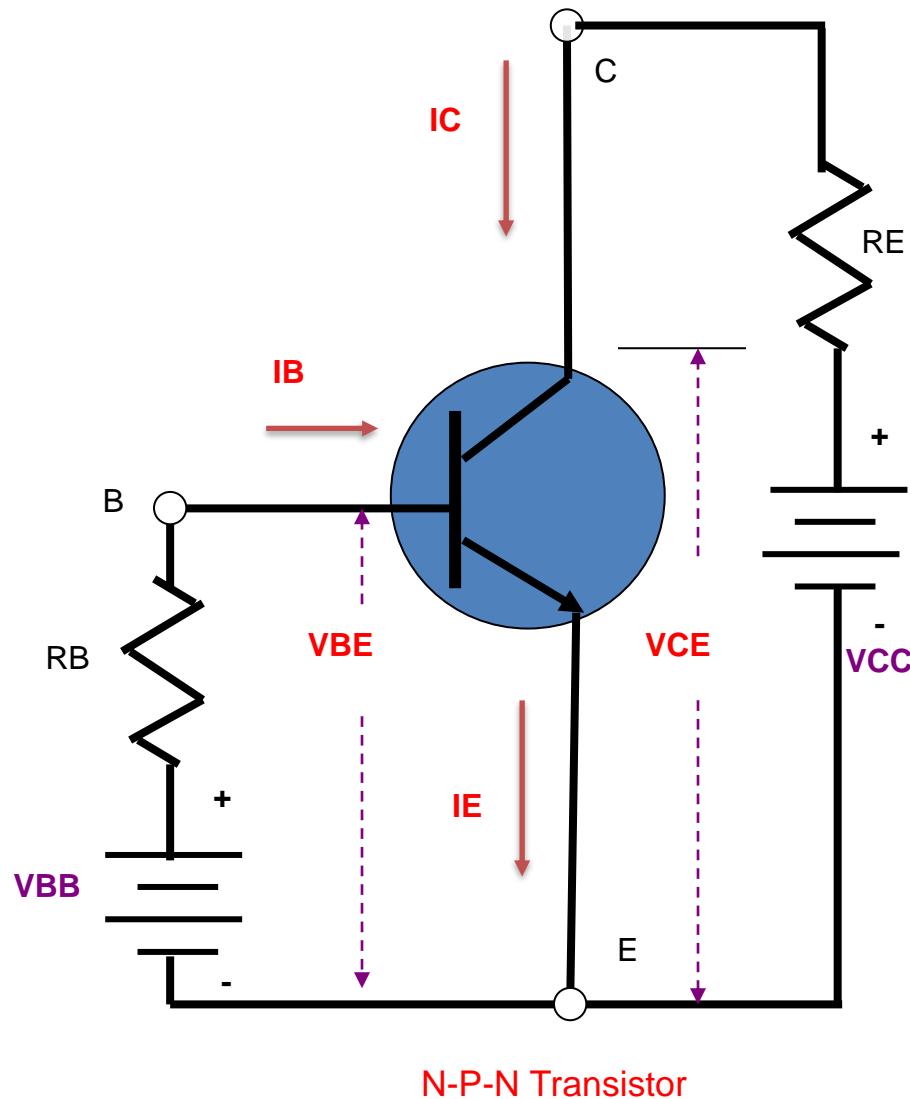
Transistor Biasing

- What is meant by dc biasing of a transistor ?
- Depending on the application, a transistor is to be operated in any of the three regions of operation namely cutoff, active and saturation region.
- To operate the transistor in these regions the two junctions of a transistor should be forward or reverse bias

Q. 2 What is DC Load Line? Derive the equation of CE amplifier and explain criteria for selection of Operating Point (Q Point).

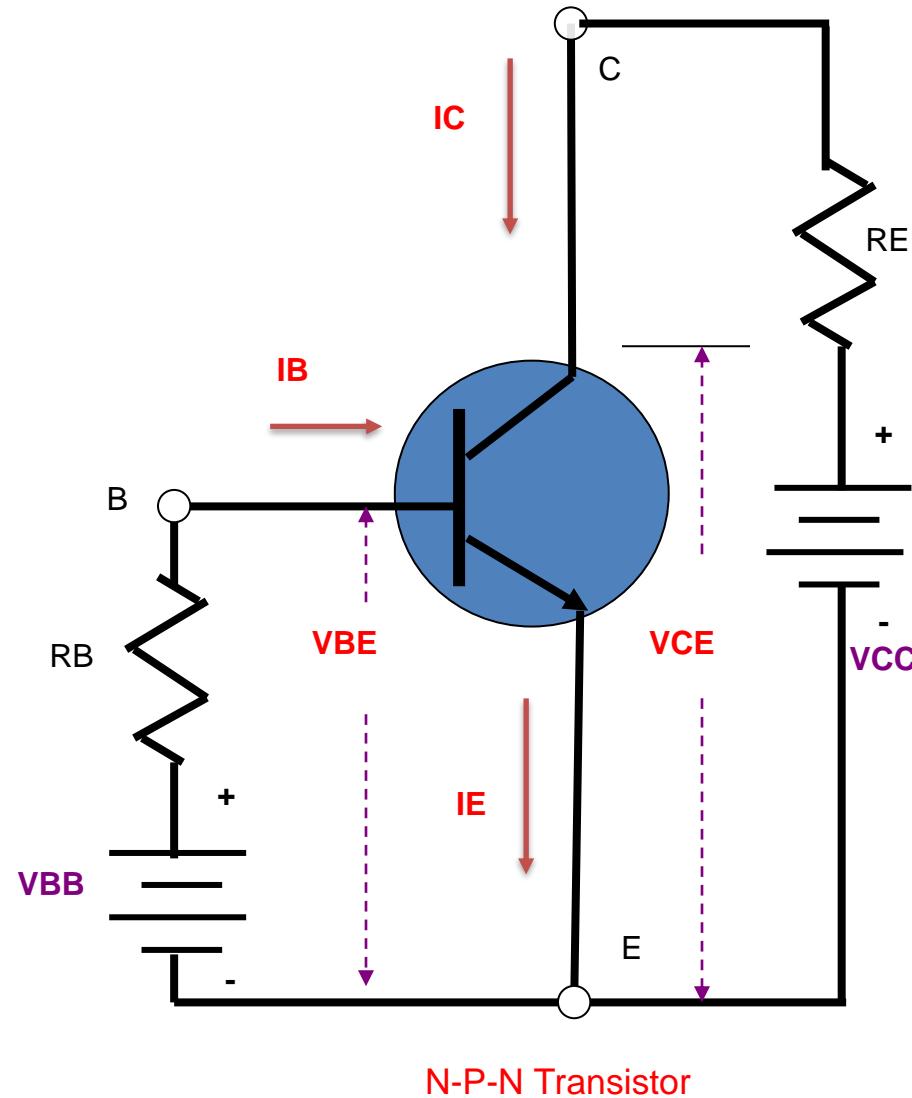
DC Load Line

- Procedure to plot the DC load line



DC Load Line

- Procedure to plot the DC load line
- Refer to the collector circuit of a CE configuration, apply KVL



DC Load Line

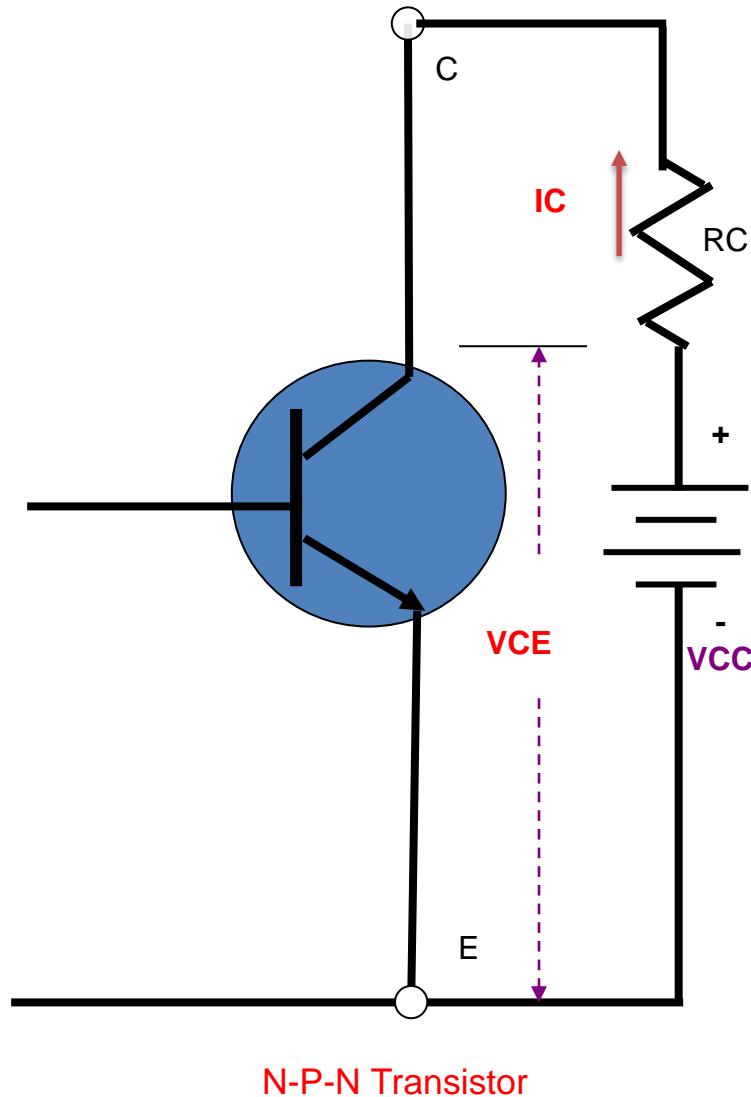
- Procedure to plot the DC load line
- Refer to the collector circuit of a CE configuration, apply KVL

$$V_{CC} - V_{CE} - I_C R_C = 0$$

Rearranging this equation we get

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

Compare this equation with general equation of straight line
i.e. $y = mx + C$



DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

i.e. $y = mx + C$

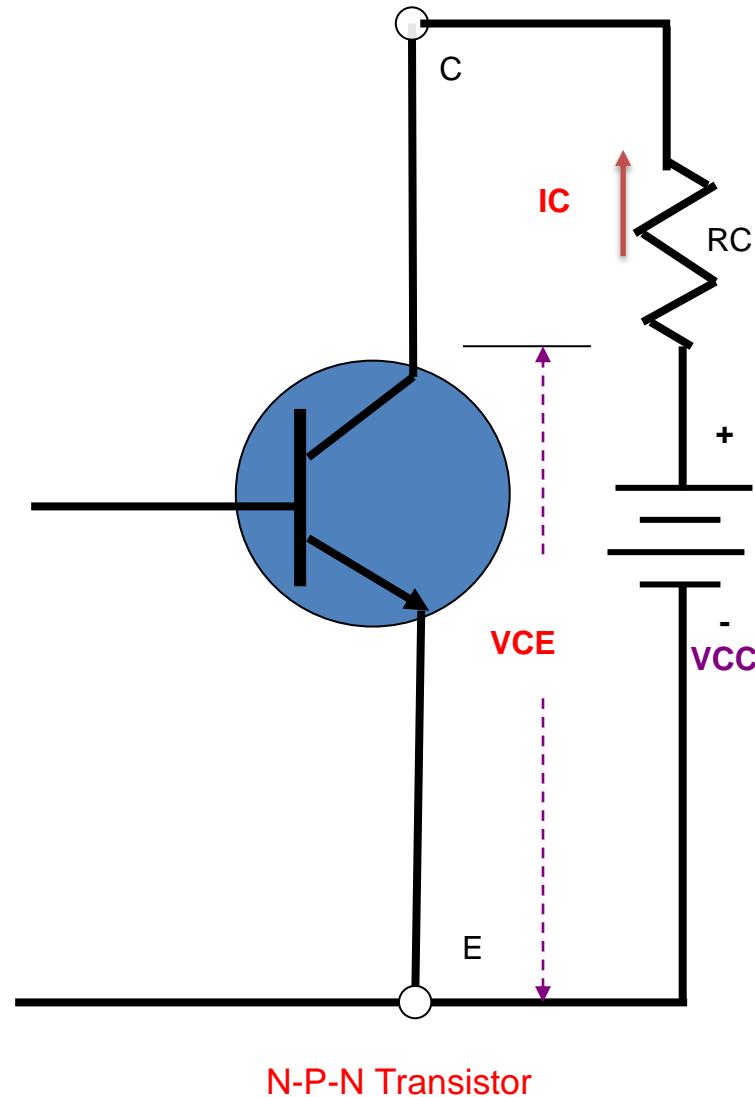
The comparison yields the following results.

$$y = I_C$$

$$m = -1/R_C$$

$$X = V_{CE}$$

$$C = V_{CC}/R_C$$



DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

i.e. $y = mx + C$

The comparison yields the following results.

$$y = I_C$$

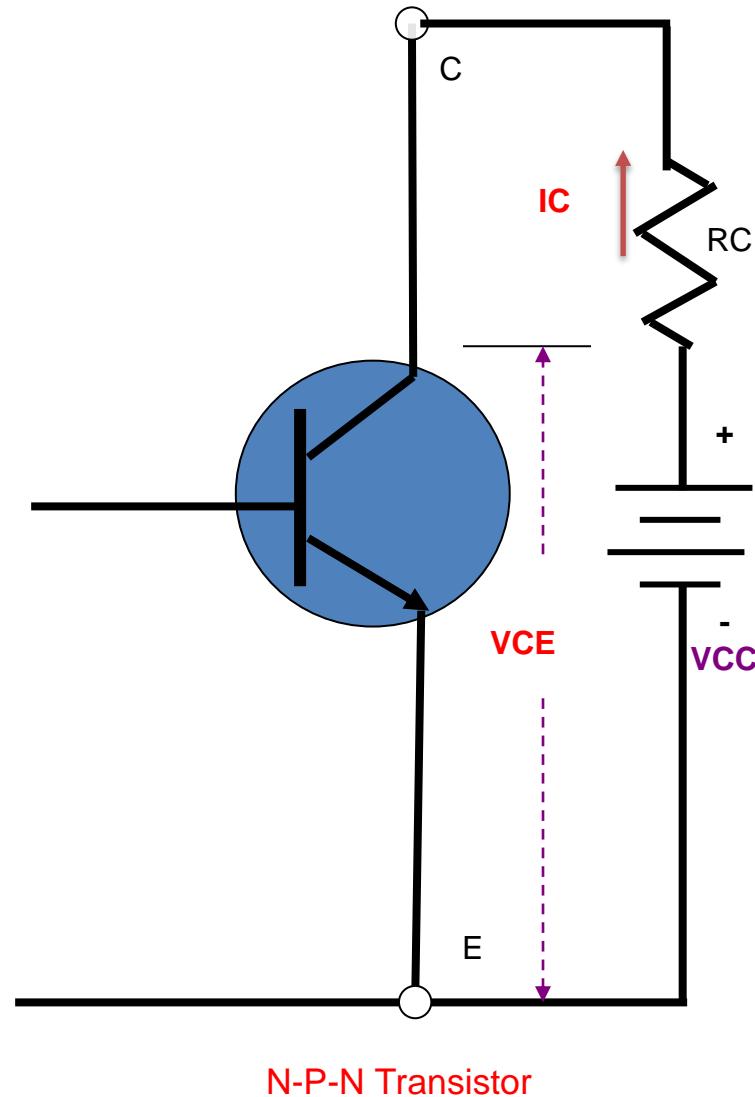
$$m = -1/R_C$$

$$X = V_{CE}$$

$$C = V_{CC}/R_C$$

This comparison shows that above equation represents a straight line.

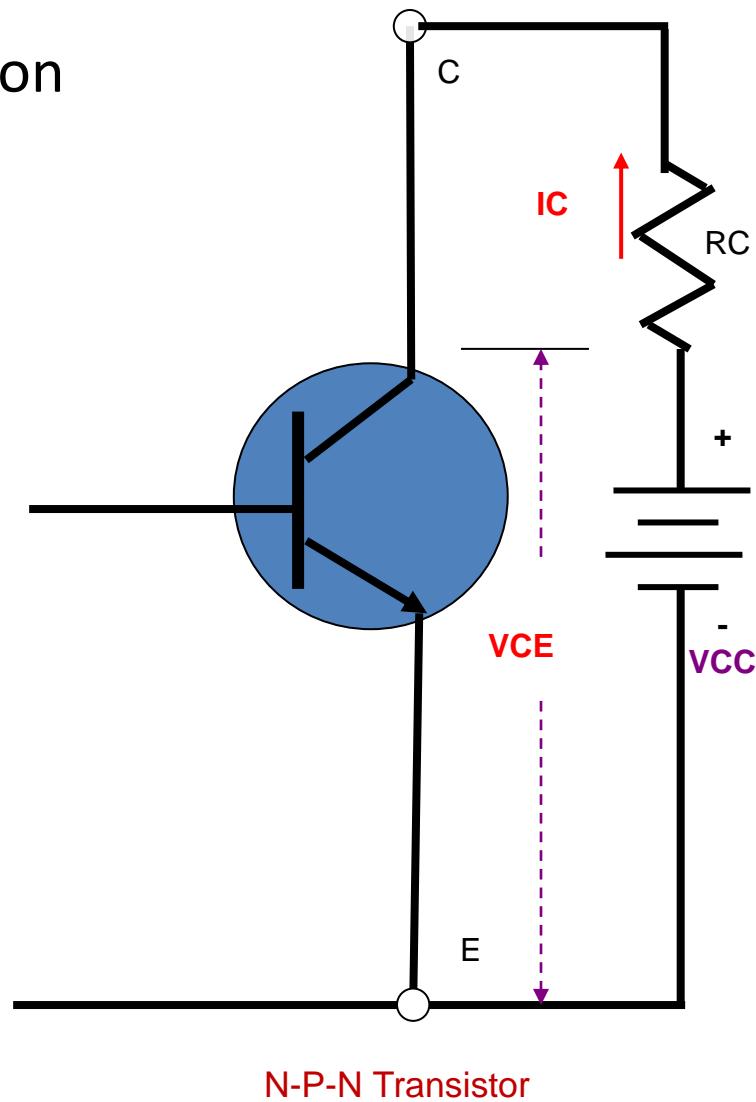
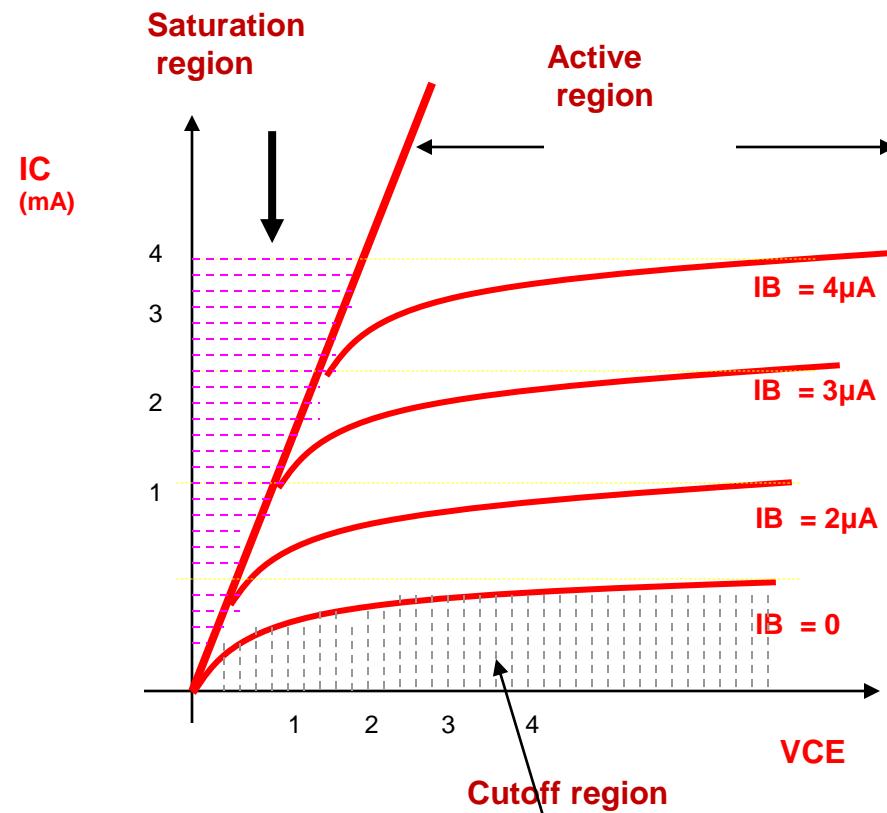
This straight line is called as DC load line



DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

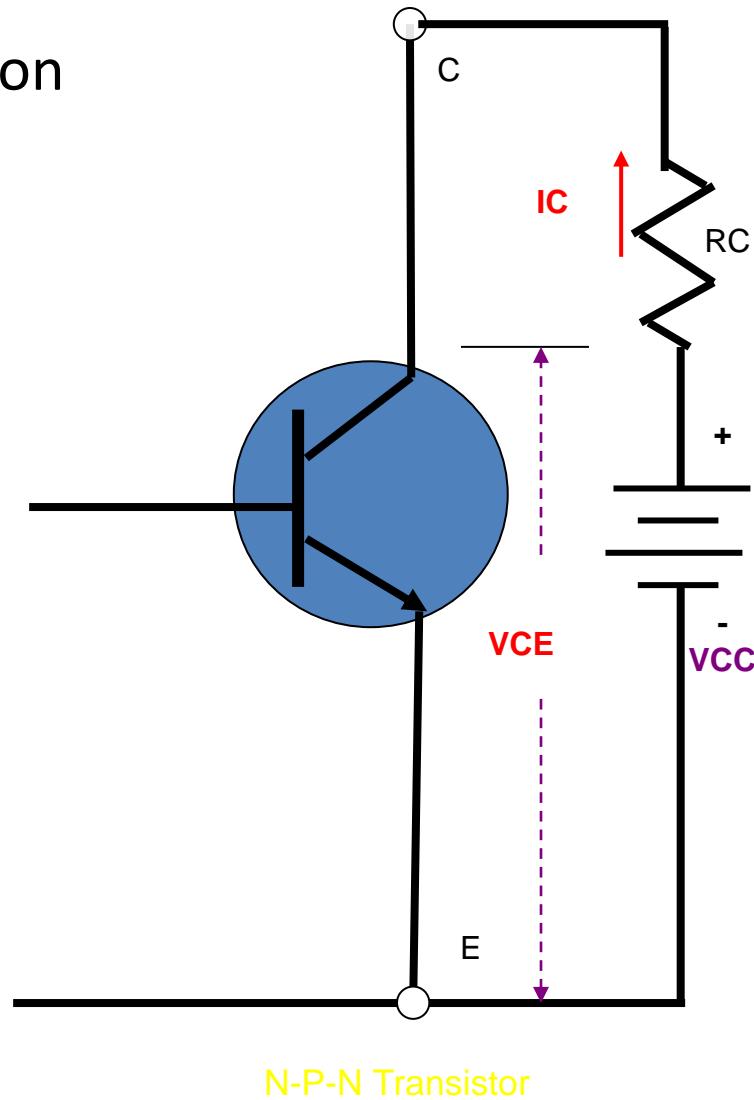
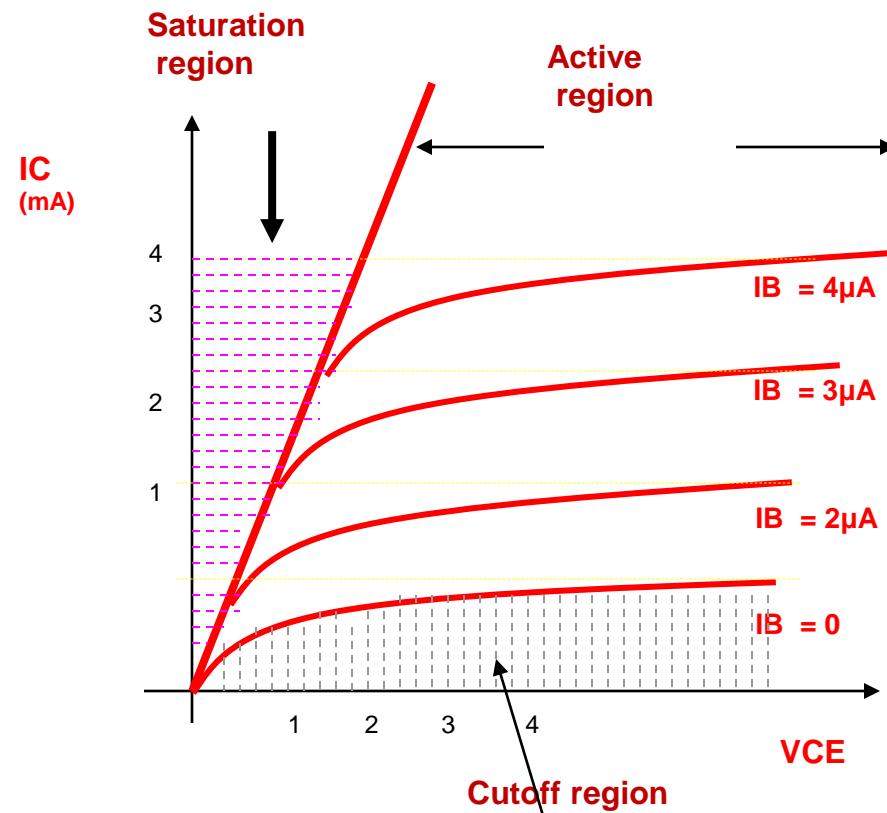
- Now substitute $V_{CE} = 0$ in above equation



DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

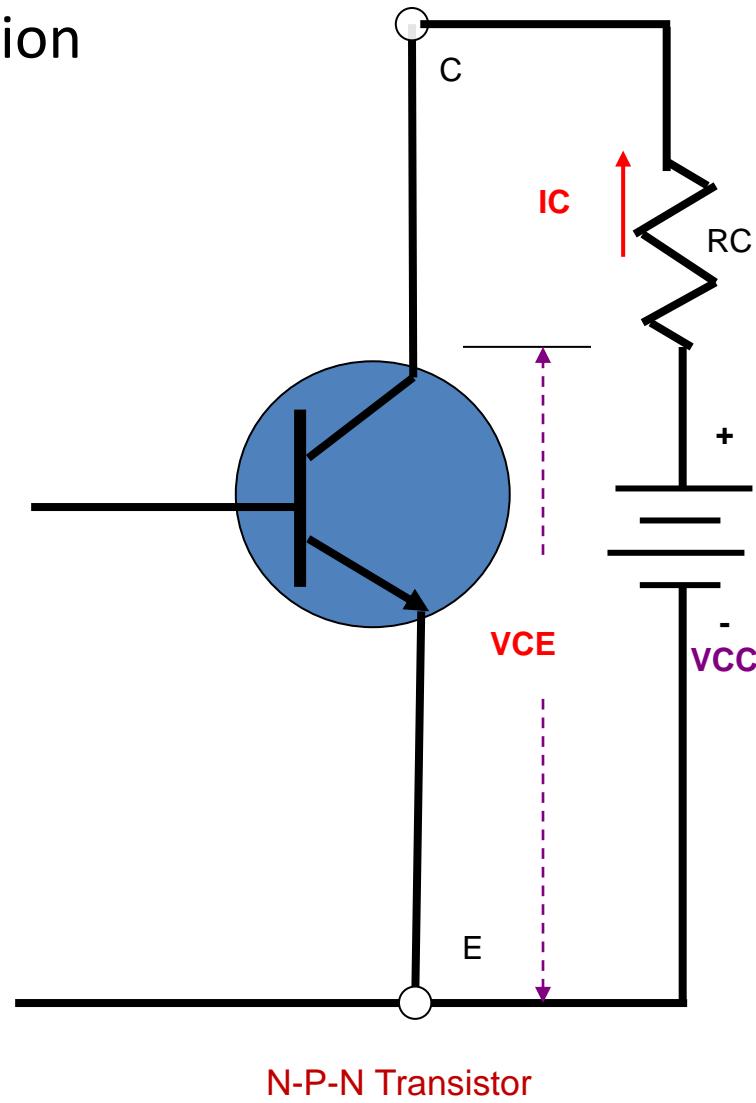
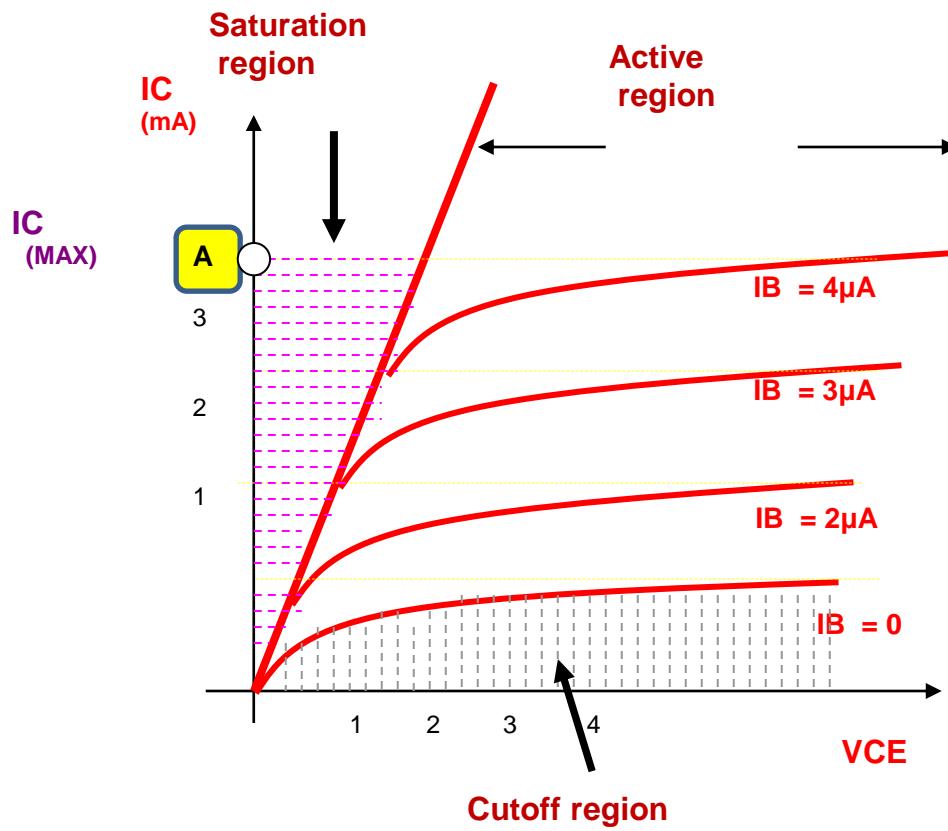
- Now substitute $V_{CE} = 0$ in above equation
- $I_C = V_{CC}/R_C$



DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

- Now substitute $V_{CE} = 0$ in above equation
- $I_C = V_{CC}/R_C$
- Or $I_{C(MAX)} = V_{CC}/R_C$ or point "A"

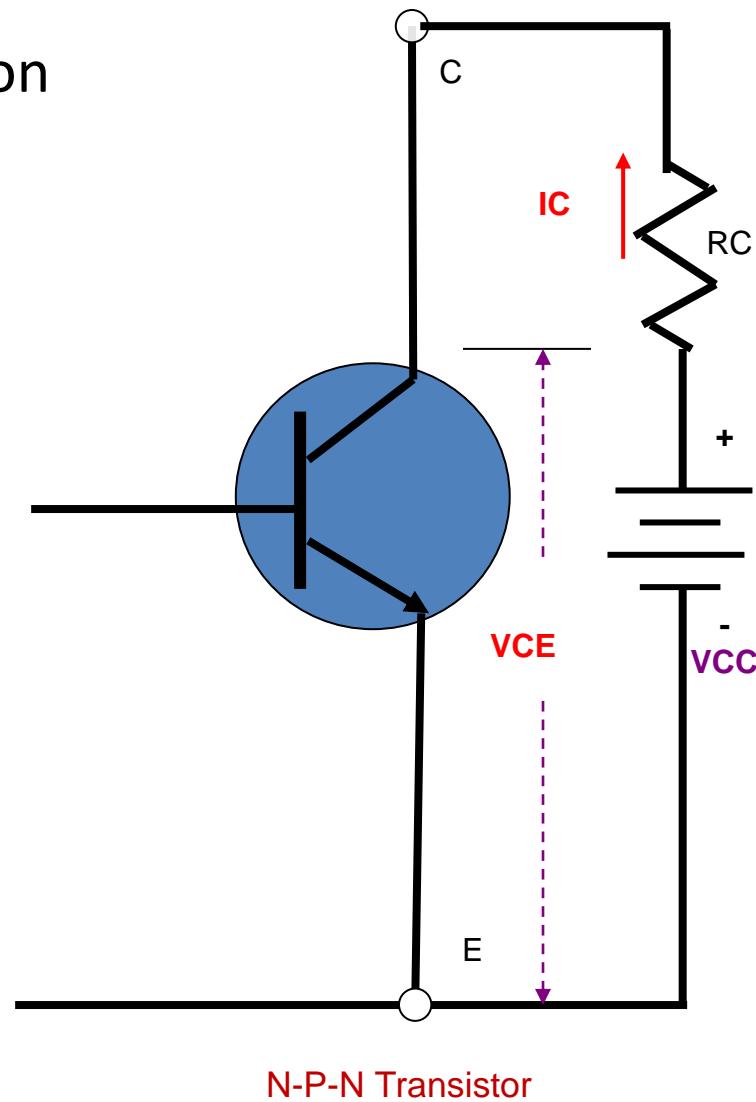
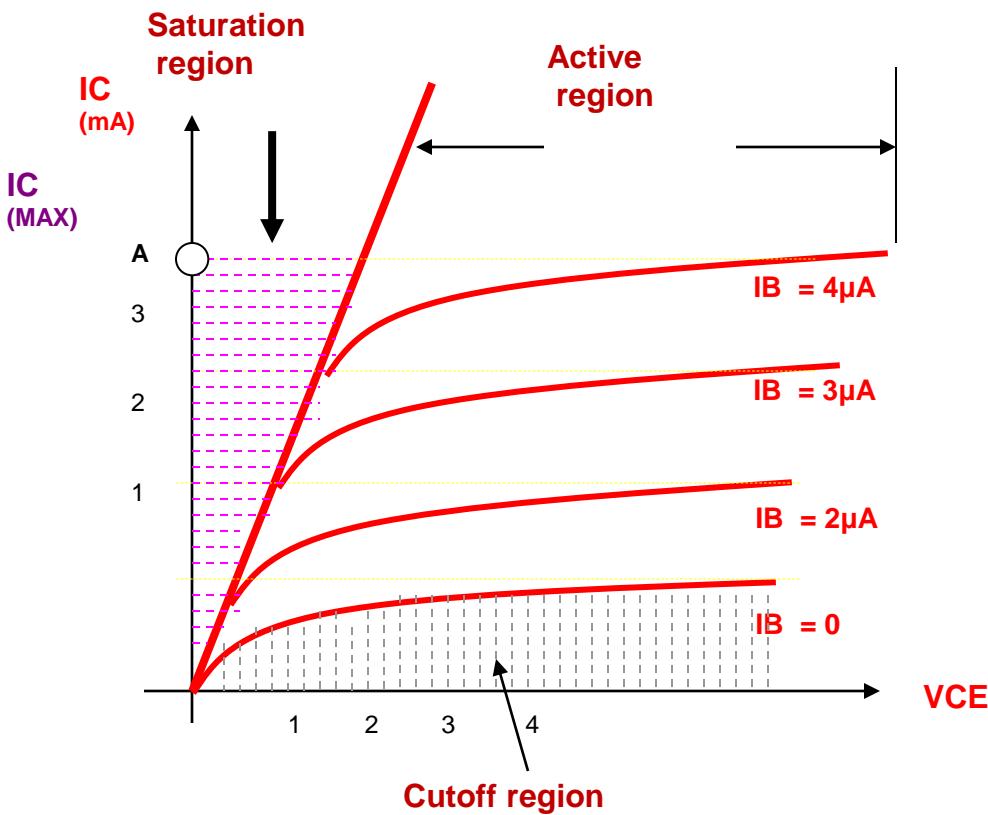


DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

- and substituting $I_C = 0$ in above equation

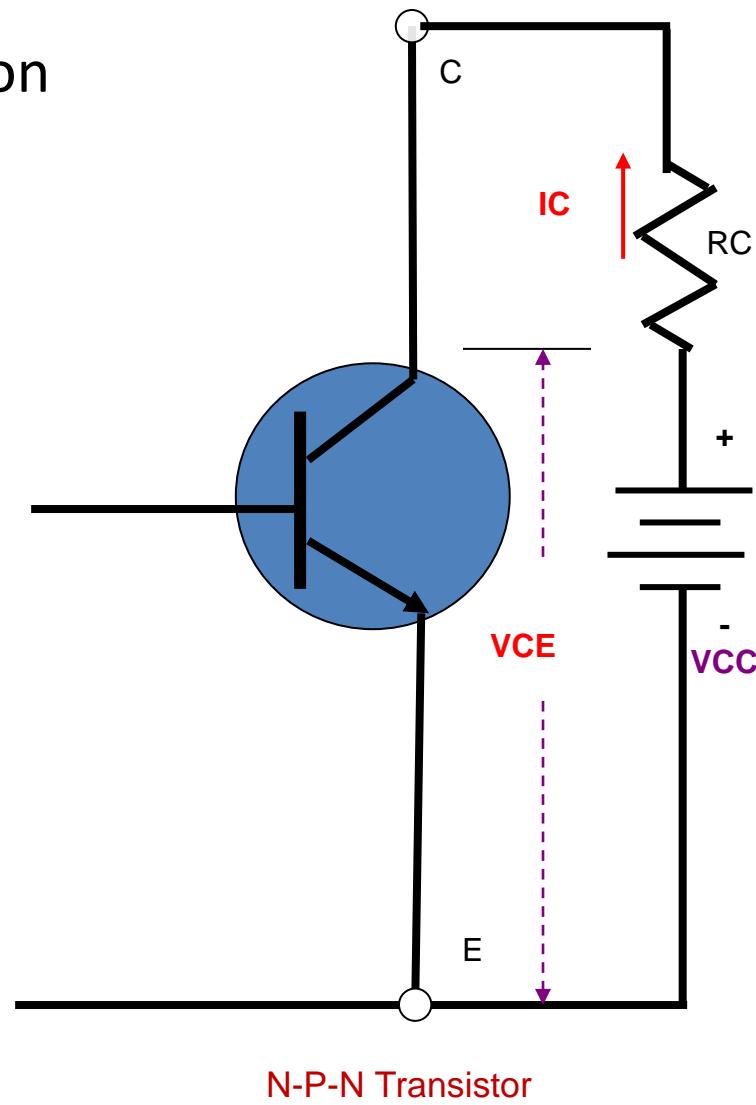
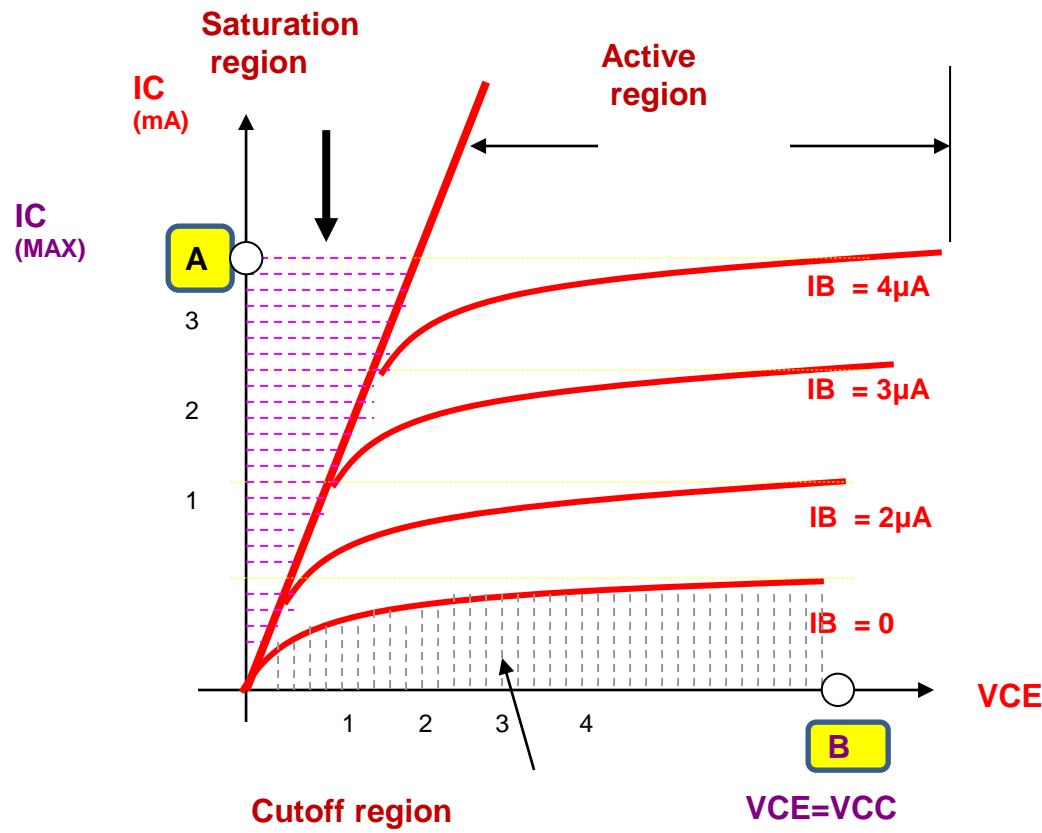
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DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

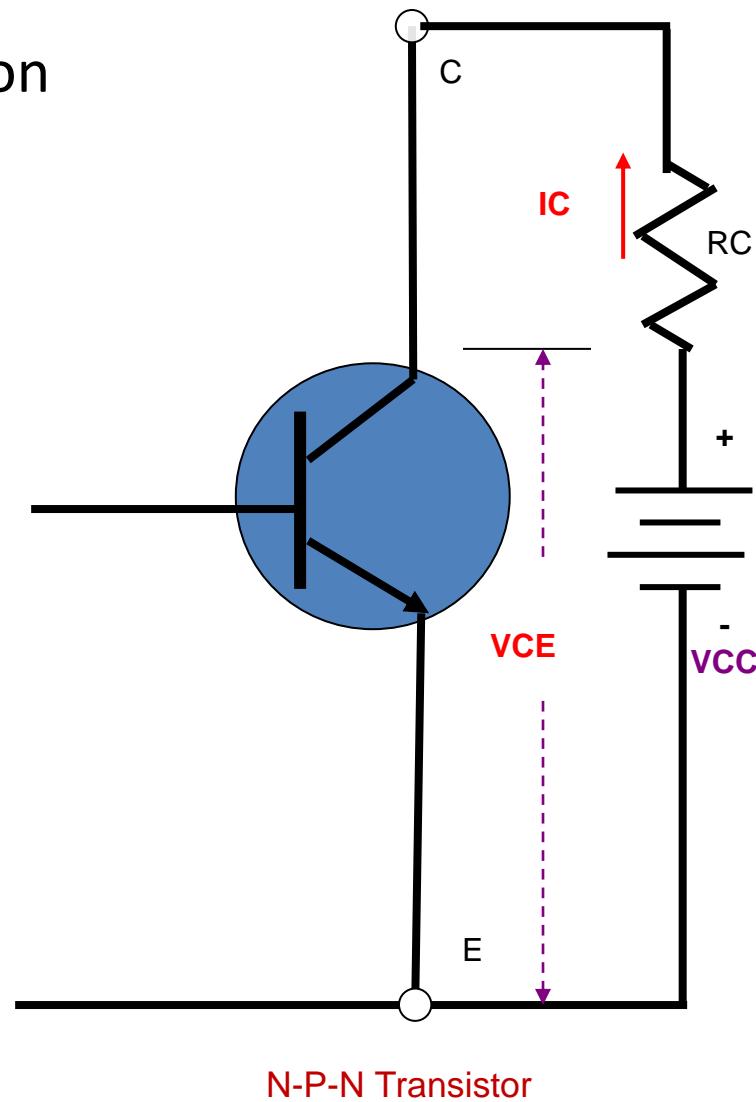
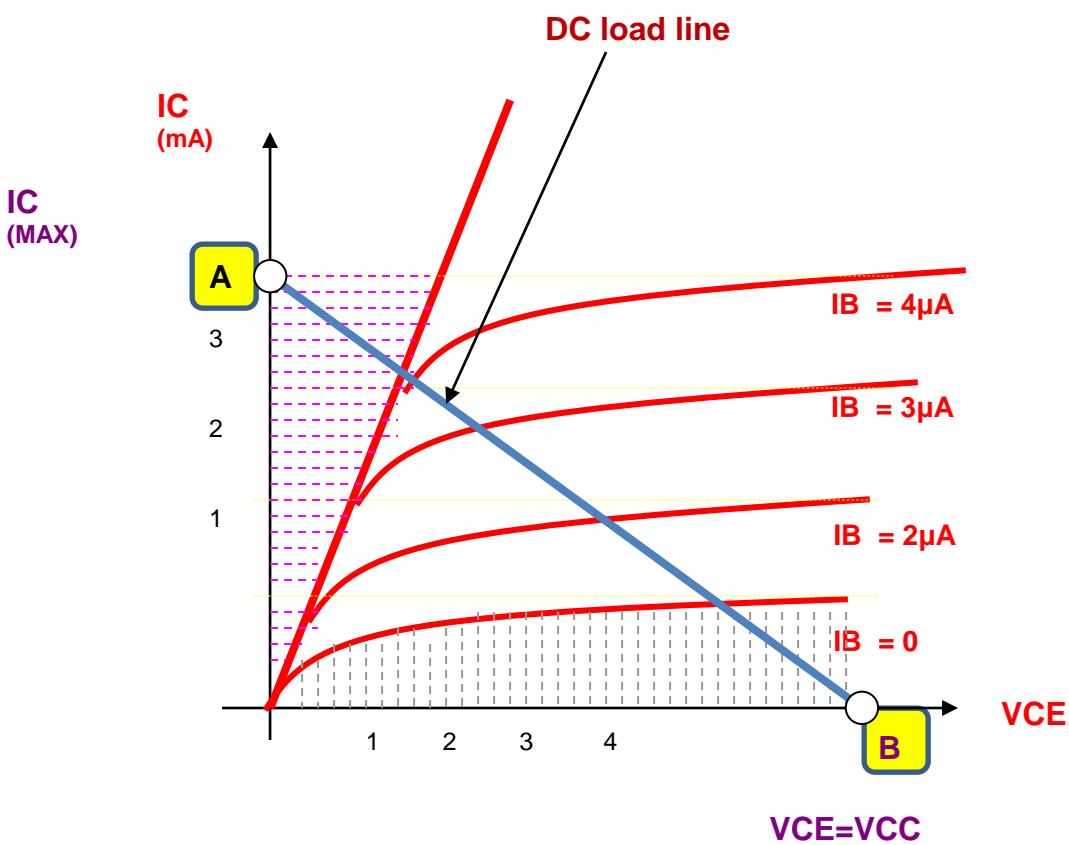
- and substituting $I_C = 0$ in above equation
- $V_{CE} = V_{CC}$ $\rightarrow \rightarrow$ or point "B"

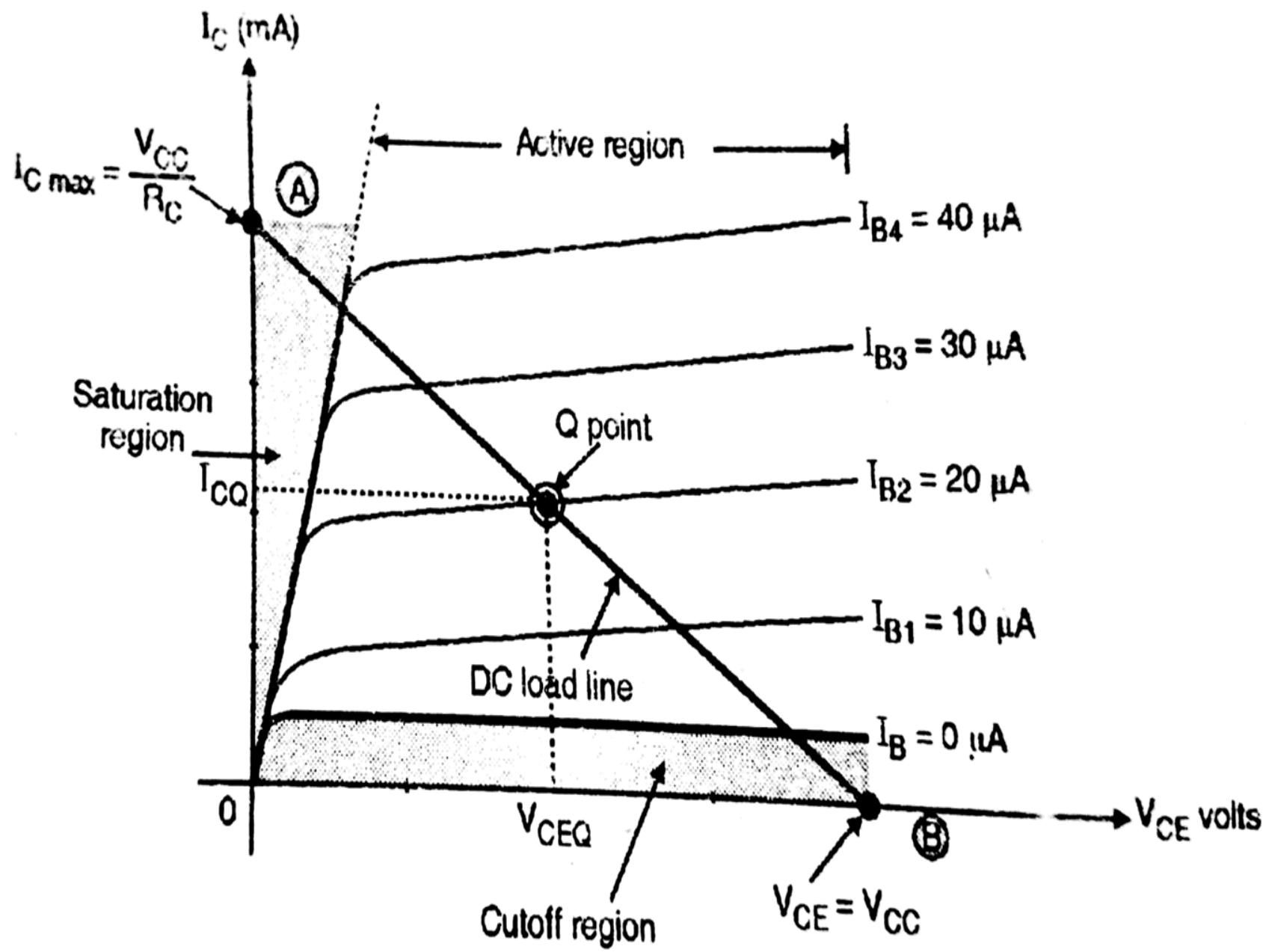


DC Load Line

$$I_C = [-1/R_C] V_{CE} + V_{CC}/R_C$$

- and substituting $I_C = 0$ in above equation
- $V_{CE} = V_{CC}$ → or point "B"



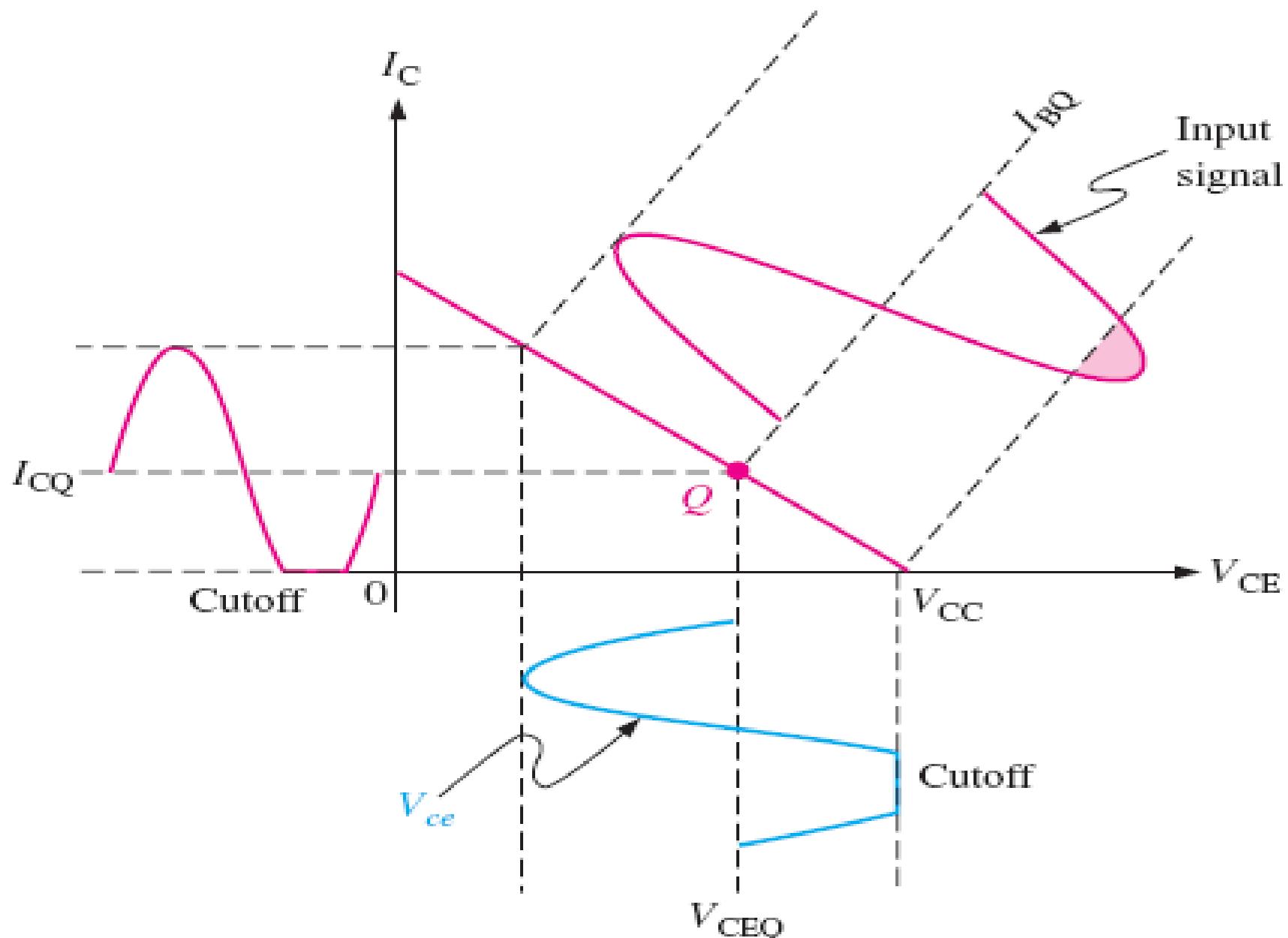


The quiescent point (Q Point)

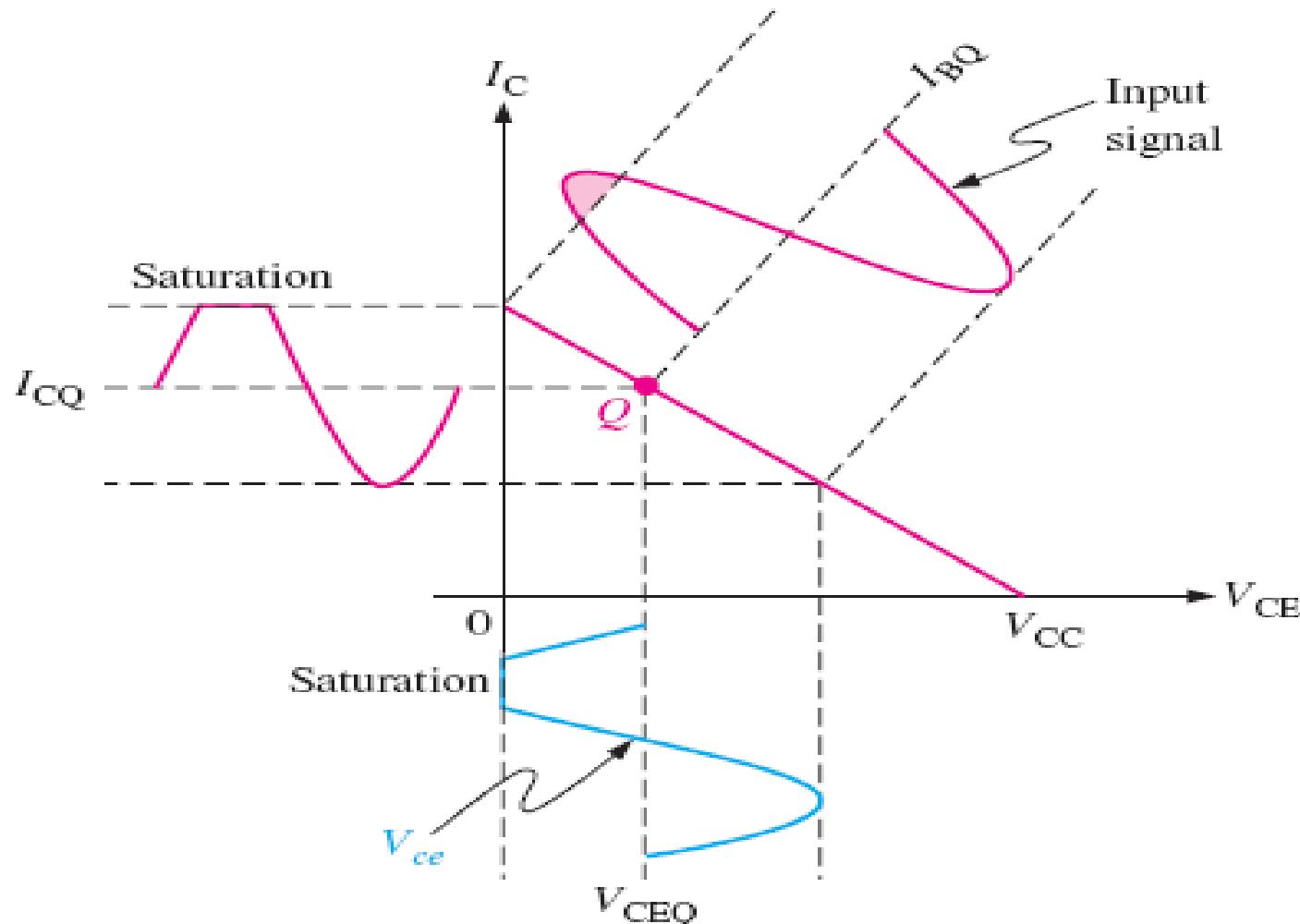
- The term quiescent means quite, still or inactive. The Q point is also called as “operating point” or “bias point”.
- It is a point on a load line which represents the dc current through a transistor (I_{CQ}) and the voltage across it (V_{CEQ}), When no ac signal is applied.
- In short it represents a dc biasing conditions

The quiescent point (Q Point)

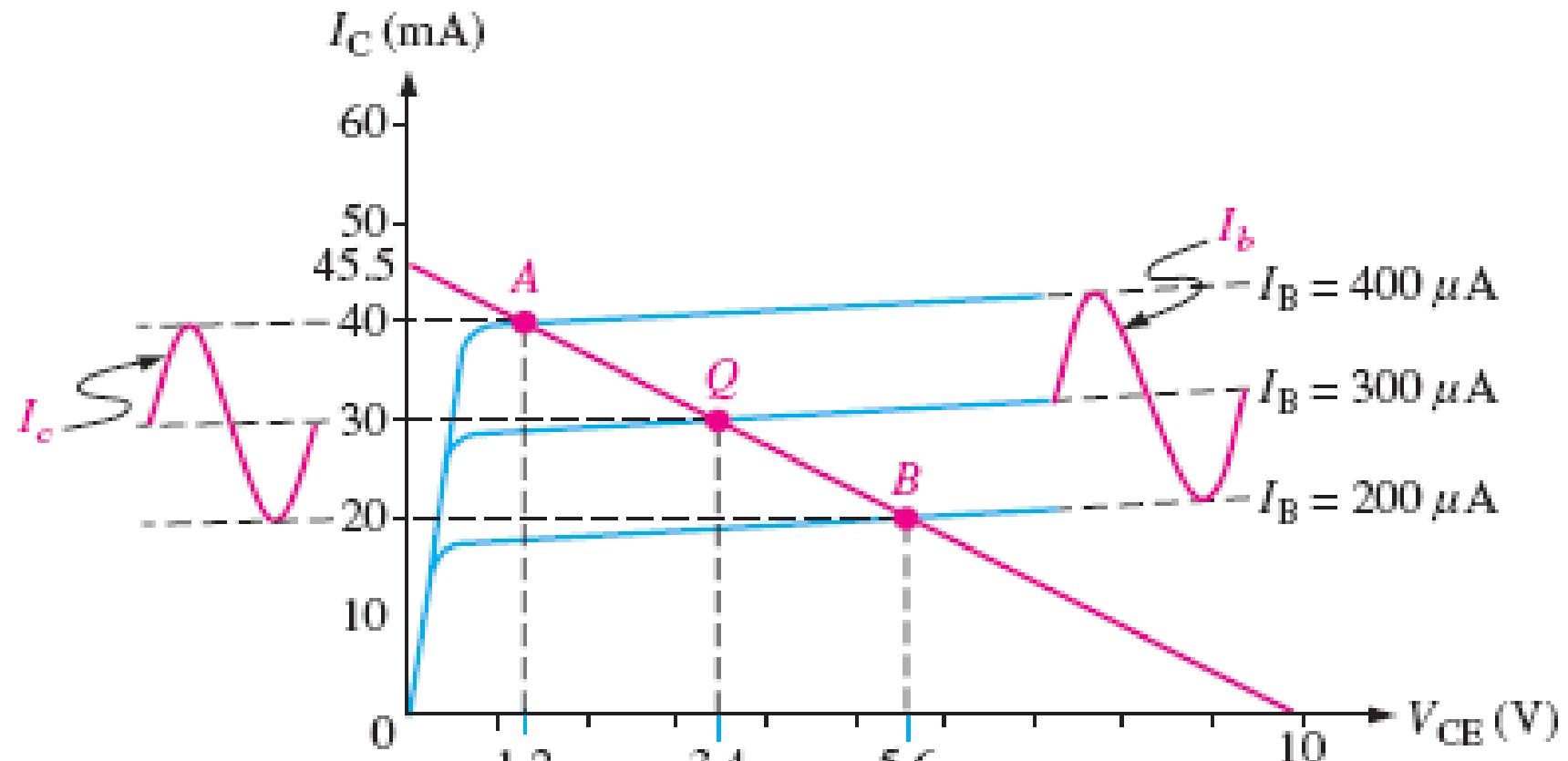
- The dc load line is a set of infinite number of such operating points and the user or designer can choose any point on the dc load line as the operating point.
- The position of operating point on the load line is dependent on the application of transistor.
- If the transistor is being used for **“Amplification”** purpose then the Q point should be at the center of load line.



(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.



- (a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



Q Point Position	Type of Clipping in Output
Q Point Near to Saturation Region	Positive Clipping (The output is clipped in Positive Half Cycle)
Q Point Near to Cut Off Region	Negative Clipping (The output is clipped in Negative Half cycle)
Q Point Exact at Centre Position	No Clipping

Typical Junction Voltages

Voltages	Silicon Transistor	Germanium Transistor
V_{BE} (Cut-off)	0	-0.1V
V_{BE} (Cut-in)	0.5V	0.1V
V_{BE} (Active)	0.7V	0.2V
V_{BE} (Saturation)	0.8V	0.3V
V_{CE} (Saturation)	0.2V	0.1V

To get Maximum Amplification in Active Region

$$V_{CE} = \frac{V_{CC}}{2} \quad \text{and} \quad I_{CQ} = \frac{I_{Cmax}}{2}$$

Factor affecting the stability of Q point

- Parameters of transistor depend on temperature : V_{BE} , I_{CO} , β_{DC}
- Thermal Runaway.

- Current Gain (β)

Factor affecting the stability of Q point

- After establishing the operating point, when input signal is applied, the output signal should not move the transistor either to saturation or to cut-off. However, this unwanted shift might occur due to various reasons outlined below:
- Parameters of transistor depend on temperature. As it increases, leakage current due to minority charge carriers (I_{CBO}) increases. As I_{CBO} increases, I_{CEO} also increases, causing increase in collector current I_C . This produces **heat** at the collector junction. This process repeats, and finally Q-point may shift into saturation region. Sometimes the excess heat produced at the junction may even burn the transistor. This is known as **thermal runaway**.
- When a transistor is replaced by another of the same type, the Q-point may shift, due to change in parameters of transistor such **as current gain (β)** which changes from unit to unit.
- To avoid a shift of Q-point, bias-stabilization is necessary. Various **biasing circuits** can be used for this purpose.

Biasing circuits

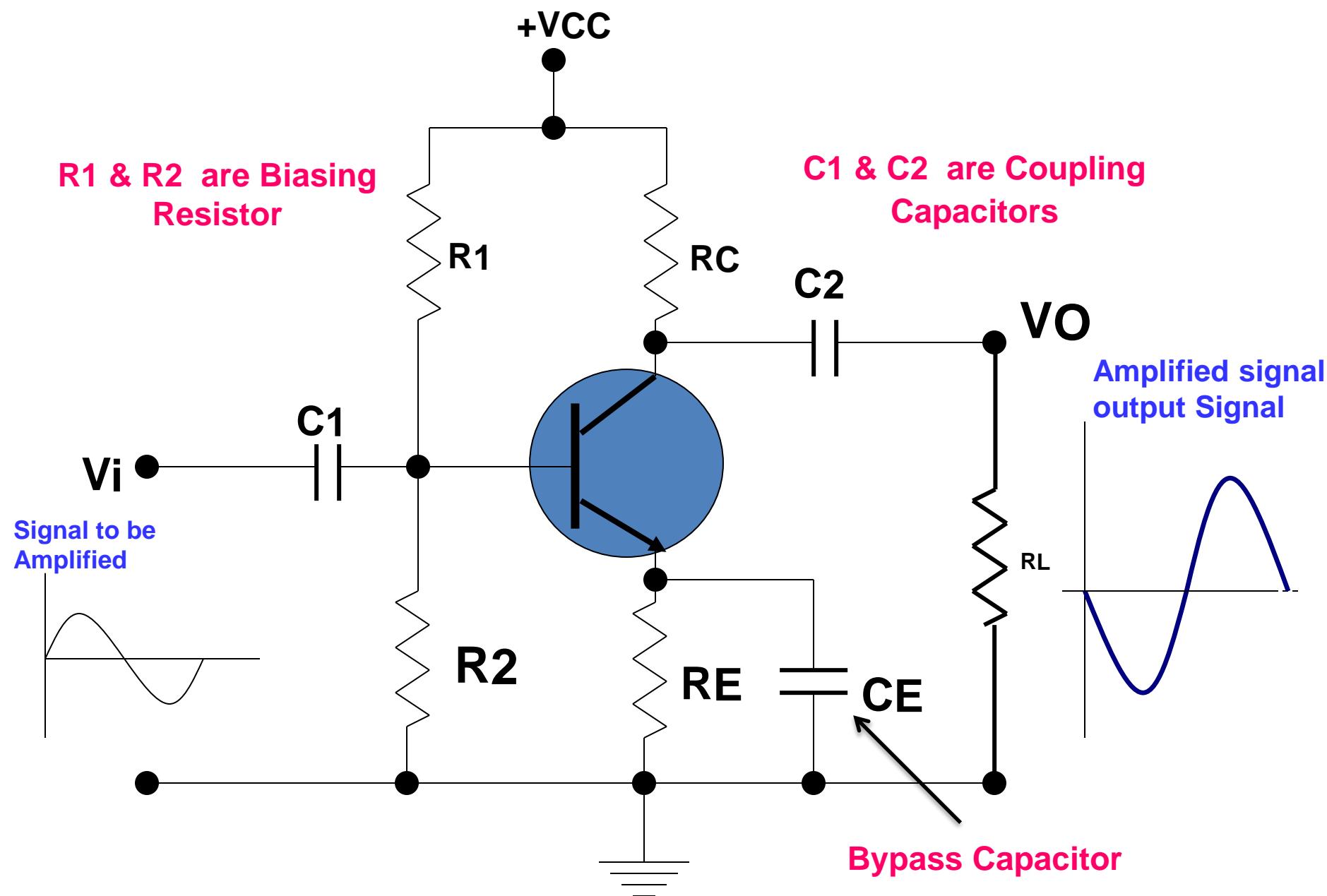
- To avoid a shift of Q-point, bias-stabilization is necessary. Various biasing circuits can be used for this purpose.
- Fixed bias
- Collector-to-base bias
- Self Biased or Voltage divider bias
- Fixed bias with emitter resistor
- Emitter bias

BJT Amplifier

Properties of Ideal Amplifier

- Input Resistance(R_i) : HIGH
- Output Resistance(R_o): ZERO
- Voltage Gain(A_v): HIGH or Large
- Current Gain(A_i): HIGH or Large
- Power Gain(A_p): HIGH
- Bandwidth: INFINITE

Single Stage RC Coupled CE Amplifier



R₁, R₂, R_E form A voltage divider biasing circuit for the CE configuration it sets the Q i.e Operating point of CE amplifier.

The input capacitor C_{c1} is used to block D.C Component present in signal & pass only A.C signal for amplification.

C_E used parallel with R_E is called emitter bypass capacitor. It provide low resistance path to the amplified A.C. Signal. If it is not used the amplified A.C signal that passes through R_E causes a voltage drop it. This will reduce output voltage & also gain of the amplifier.

C_{c2} is used to block D.C and couple A.C output of amplifier to the load.

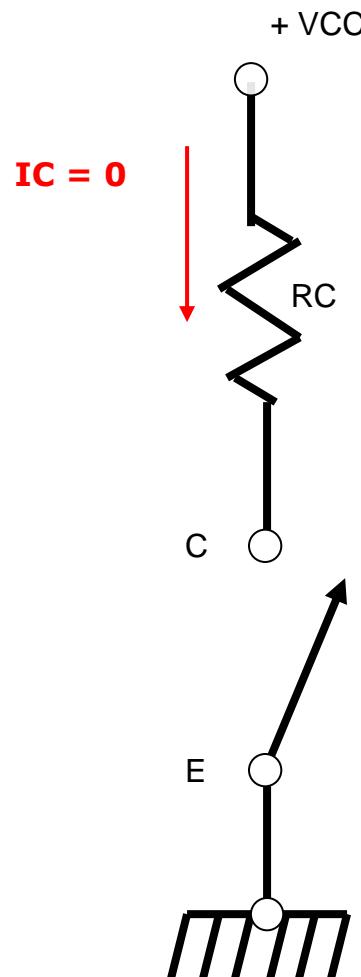
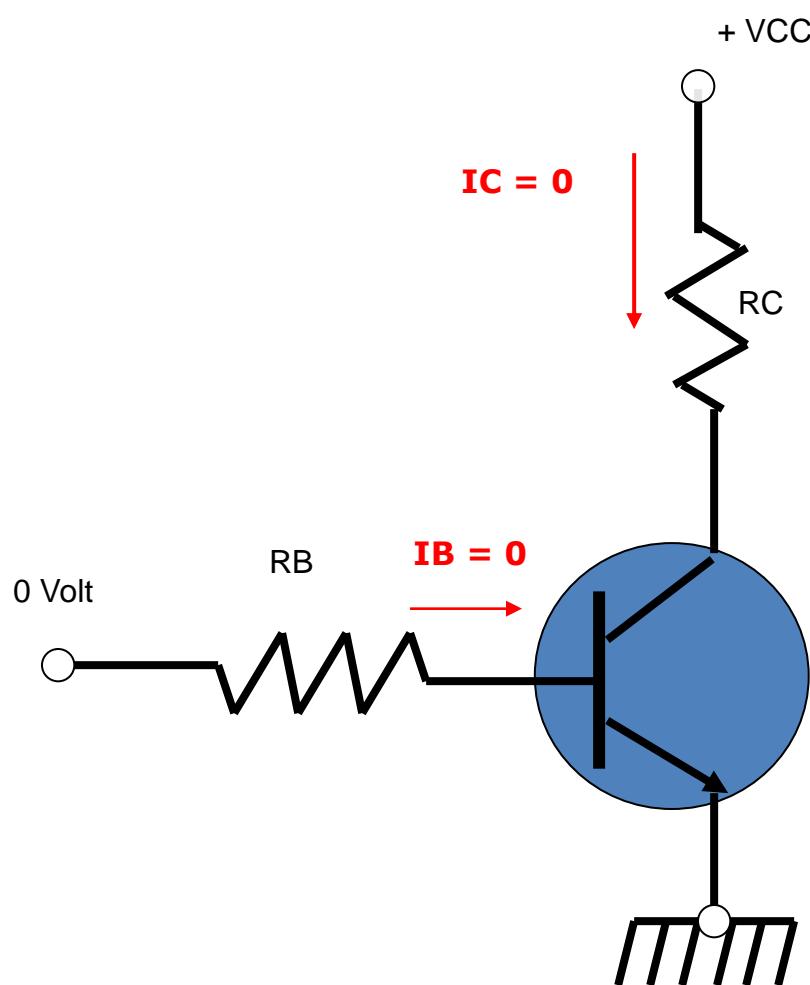
Input voltage & output voltage are is not in phase. The output is 180 degrees out of phase with the input .

Transistor as a switch

- To operate BJT as a switch, it is to be operated in two regions namely cutoff and saturation.
- In cutoff region both the junctions of transistor are reverse biased and only reverse current flows. This current is very small and practically neglected. Thus no current flows through the transistor in cutoff region.
- Hence in this region, it acts as a **open switch**.

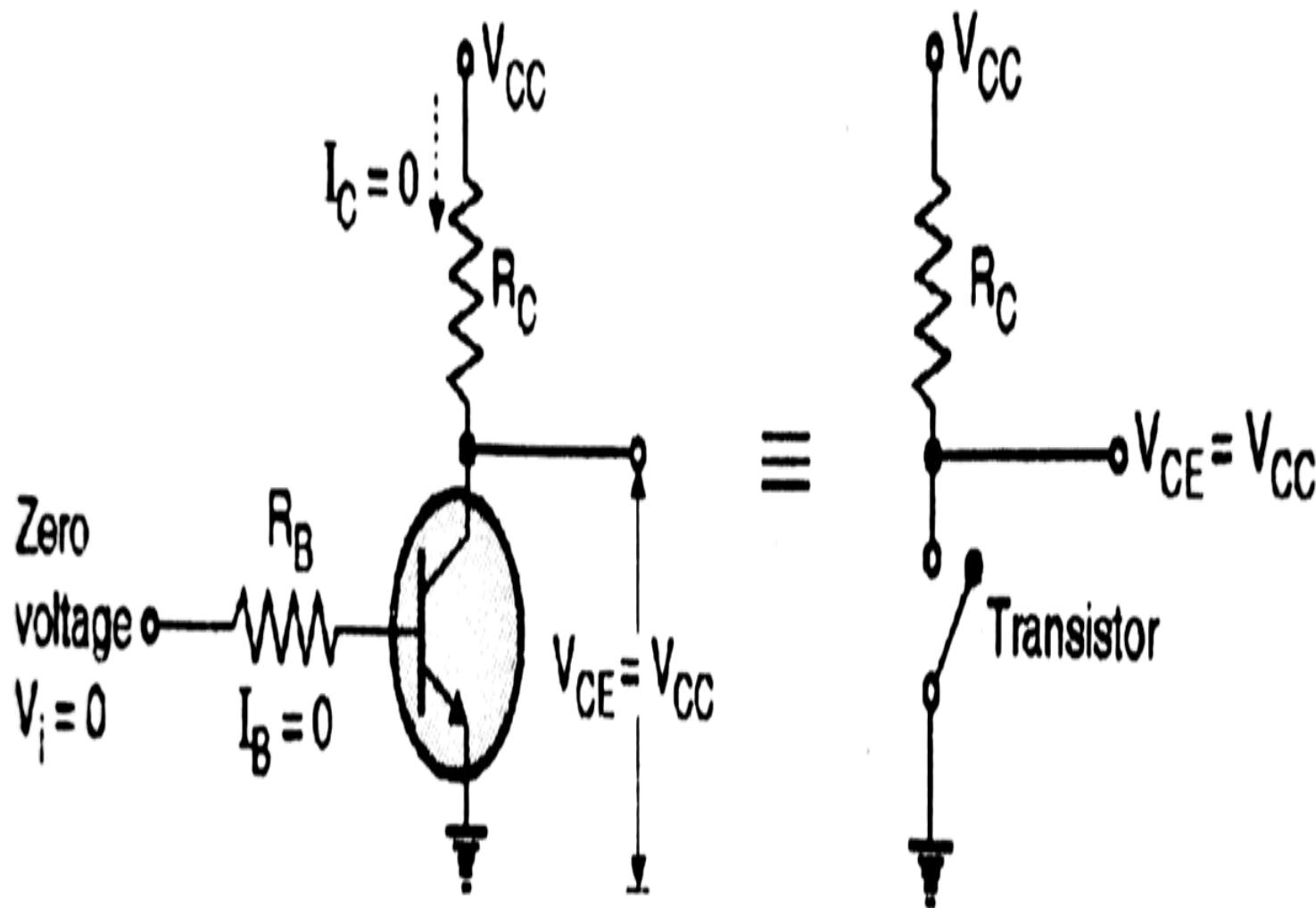
Transistor as a switch

- Cutoff region, it acts as a **open switch**.



N-P-N Transistor

Cutoff region, it acts as a open switch.

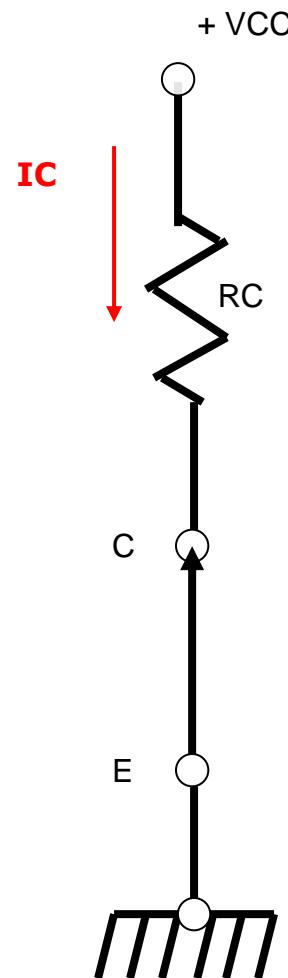
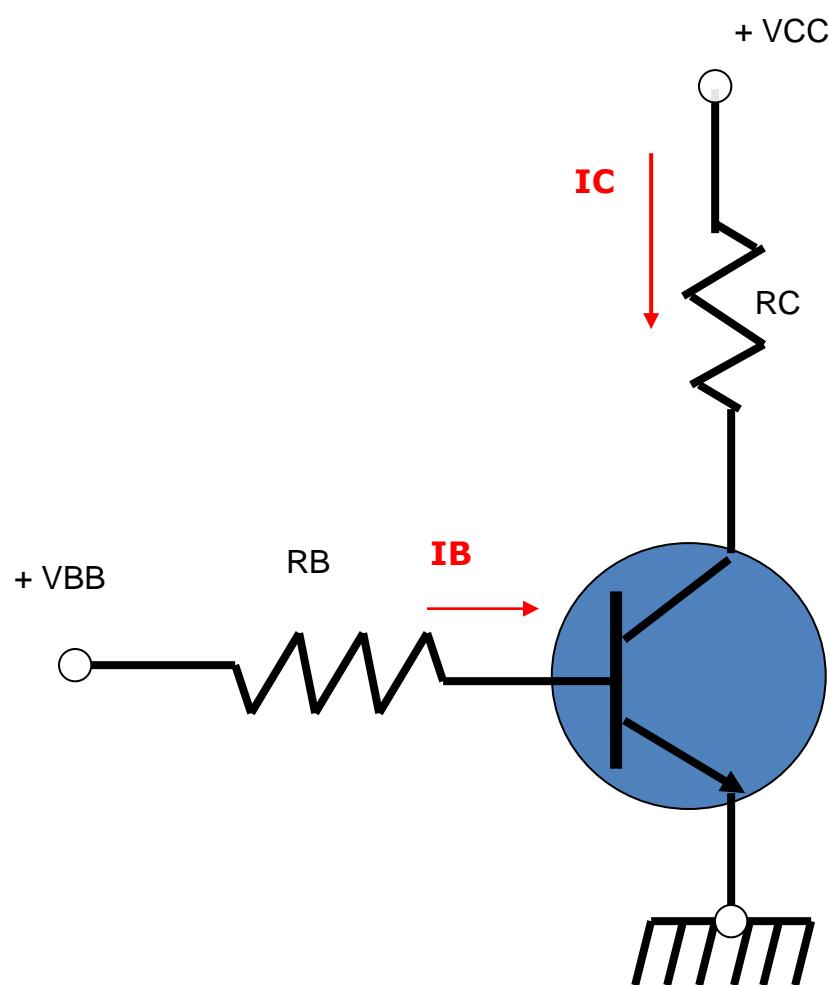


Transistor as a switch

- In the saturation region both the junction are forward biased. The voltage VCE drops to very small value about 0.2 V and 0.3 V. this is denoted as VCE (sat).
- In saturation condition, collector current is large and controlled by external resistance in collector circuit.
- Practically, VCE (sat) can be neglected as it is very small compared to supply voltage hence output voltage which is VCE for CE configuration is zero in saturation region.
- Thus it acts as a **closed switch**

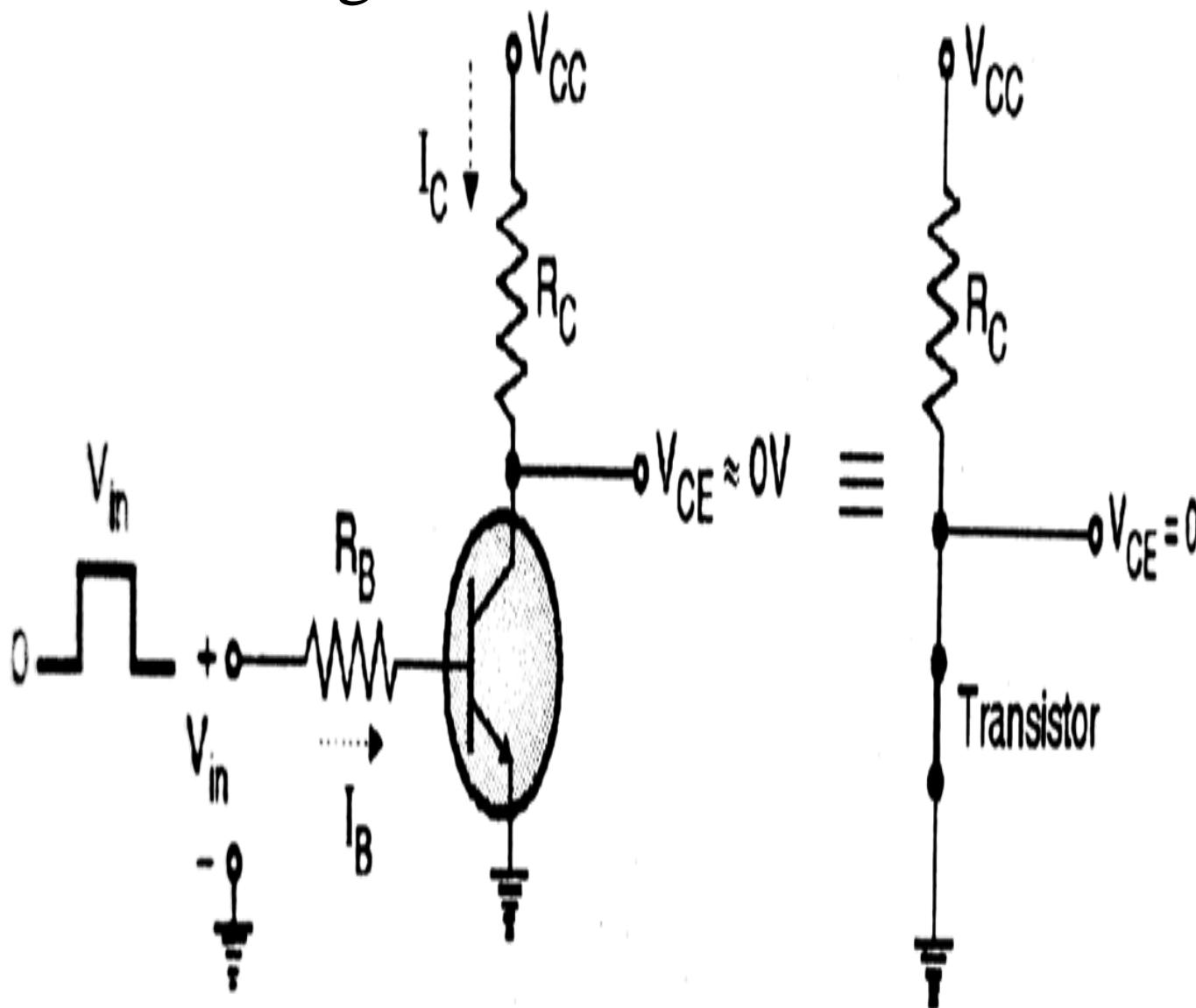
Transistor as a switch

- Saturation region, it acts as a **close switch**.



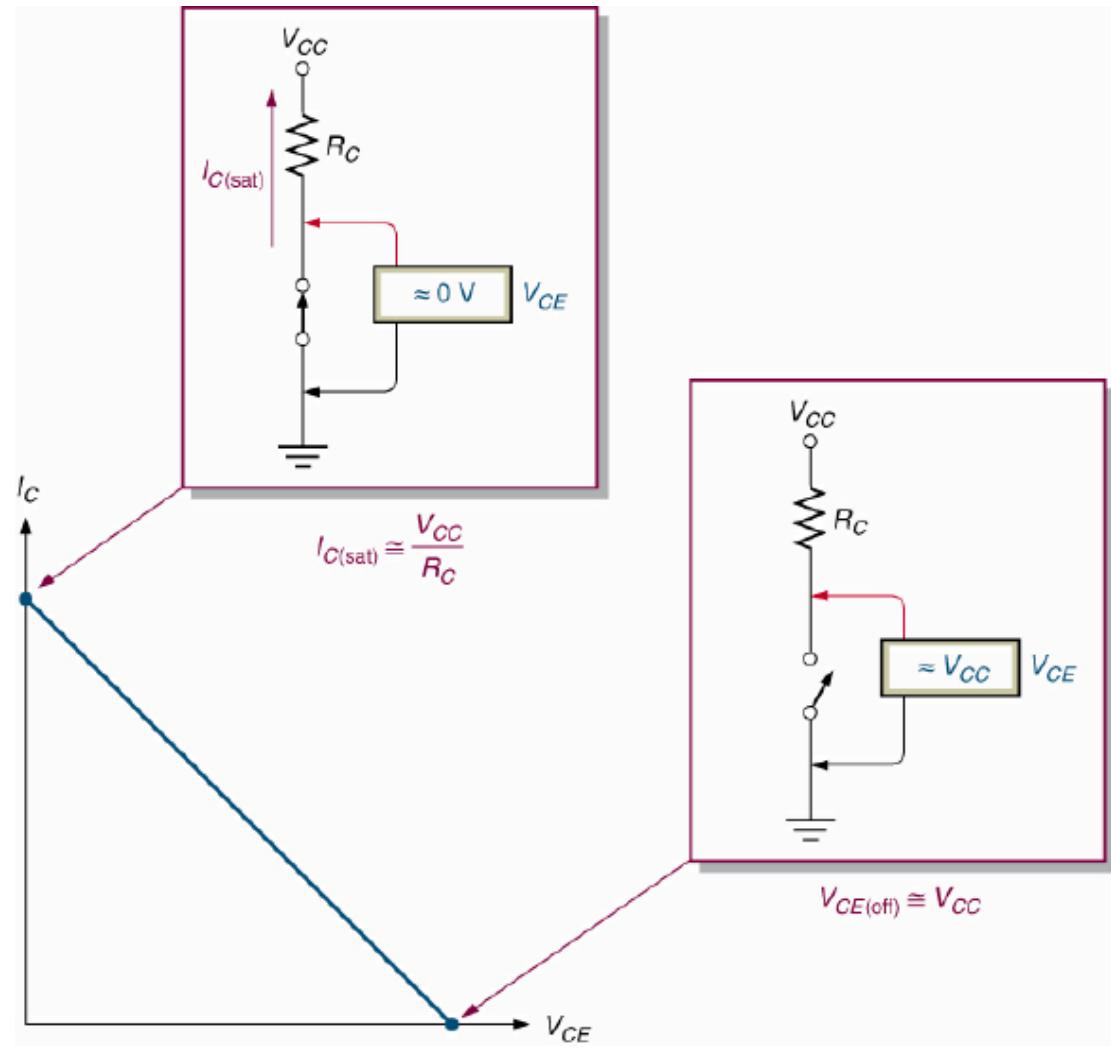
N-P-N Transistor

Saturation region, it acts as a **Closed** switch.



Open and Closed BJT Switch

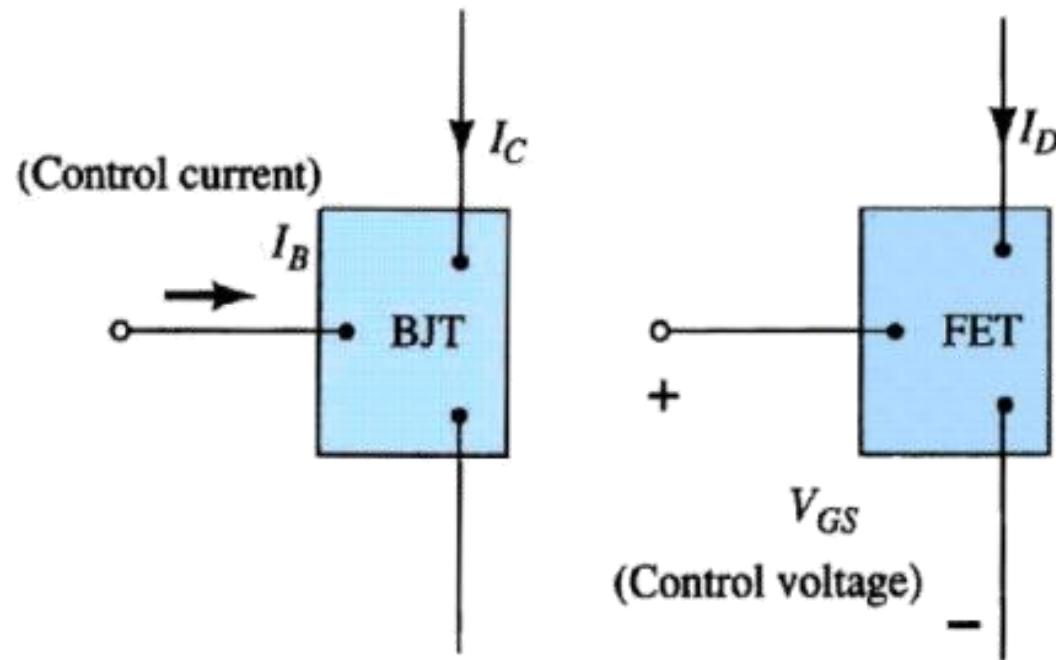
- When operated in **saturation**, the BJT acts as a **closed switch**.
- When operated in **cutoff**, the BJT acts as an **open switch**.



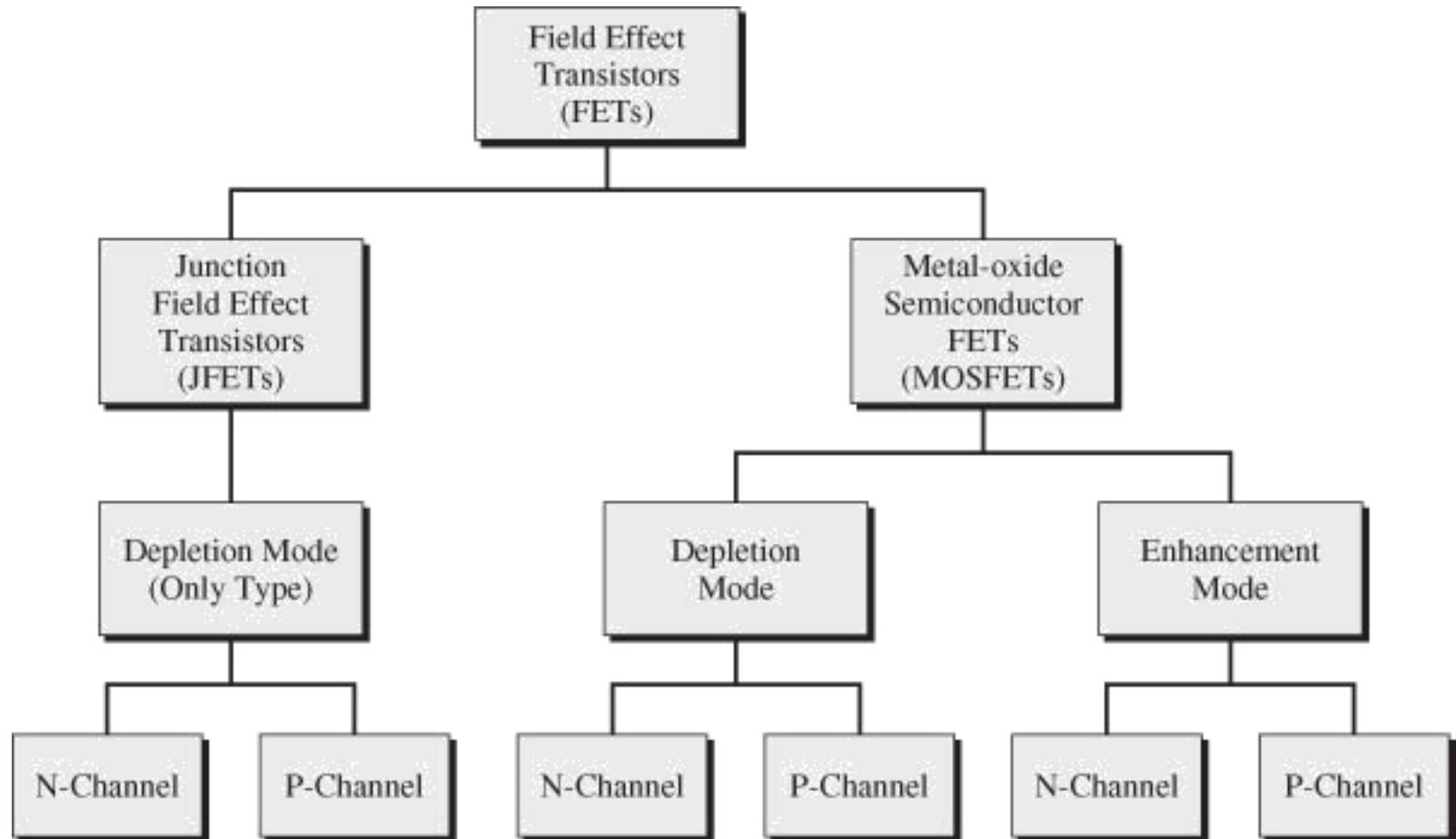
FIELD-EFFECT TRANSISTORS (FET'S)

- FET's are the **uni polar** devices because, unlike BJT's that use both **electron** and **hole** current, they operate only with one type of charge carrier.
- The two main types of FET's are the
- Junction field effect transistor (**JFET**) and
- The metal oxide semiconductor field effect transistor (**MOSFET**)

Current Controlled vs Voltage Controlled Devices



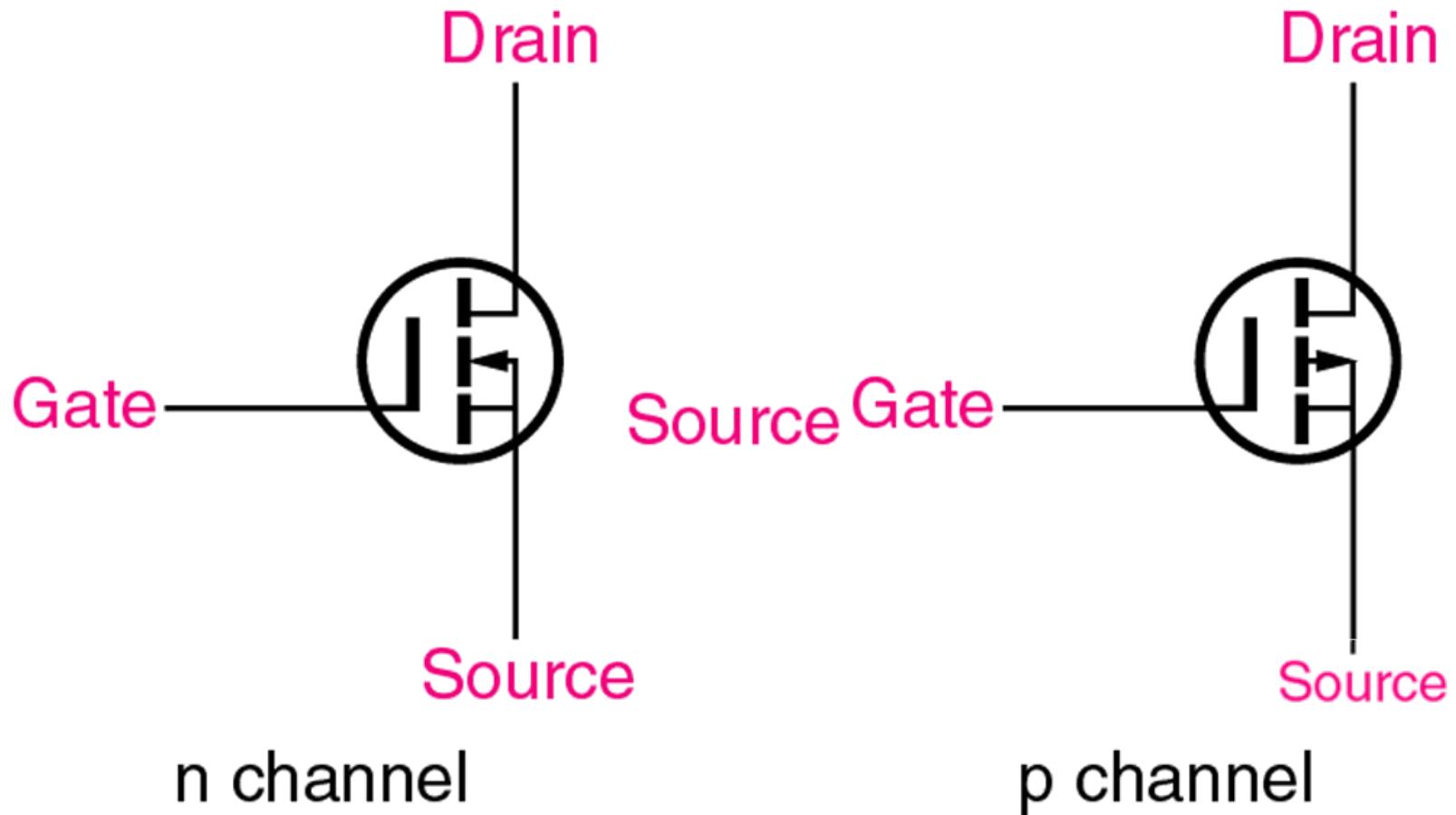
Classification scheme for field effect transistors.



THE MOSFET (IGFET)

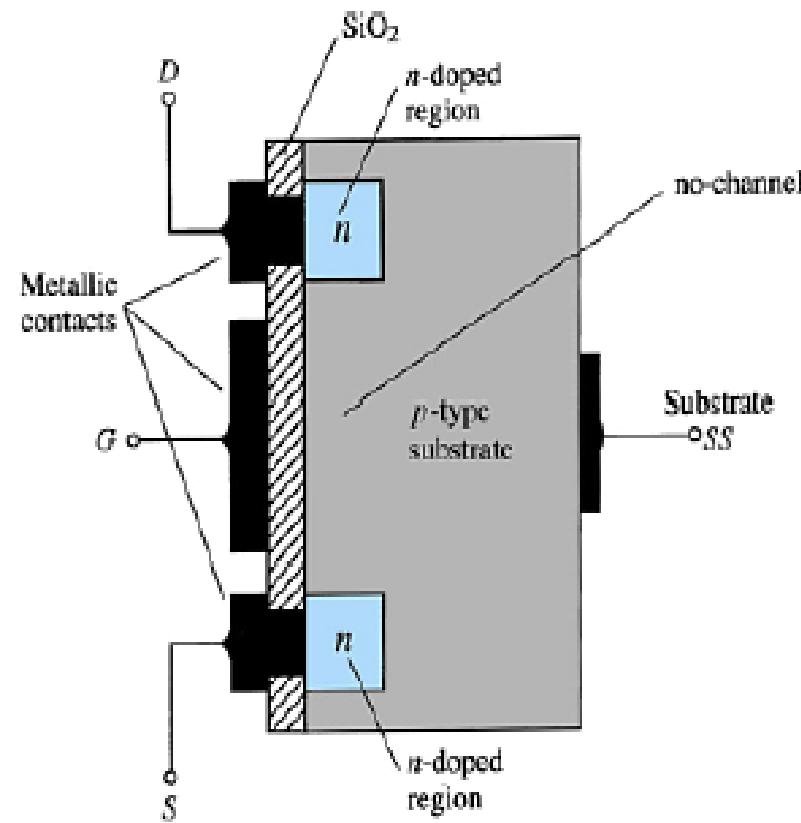
- The MOSFET (metal oxide semiconductor field effect transistor) is the category of FET.
- The MOSFET differs from the JFET in that it has no PN junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer.
- Two basic types of MOSFETS are :
- Depletion (D) MOSFET and
- Enhancement (E) MOSFET
- Because of the insulated gate, these devices are also called **IGFET**.

ENHANCEMENT MOSFET (E-MOSFET) schematic symbol

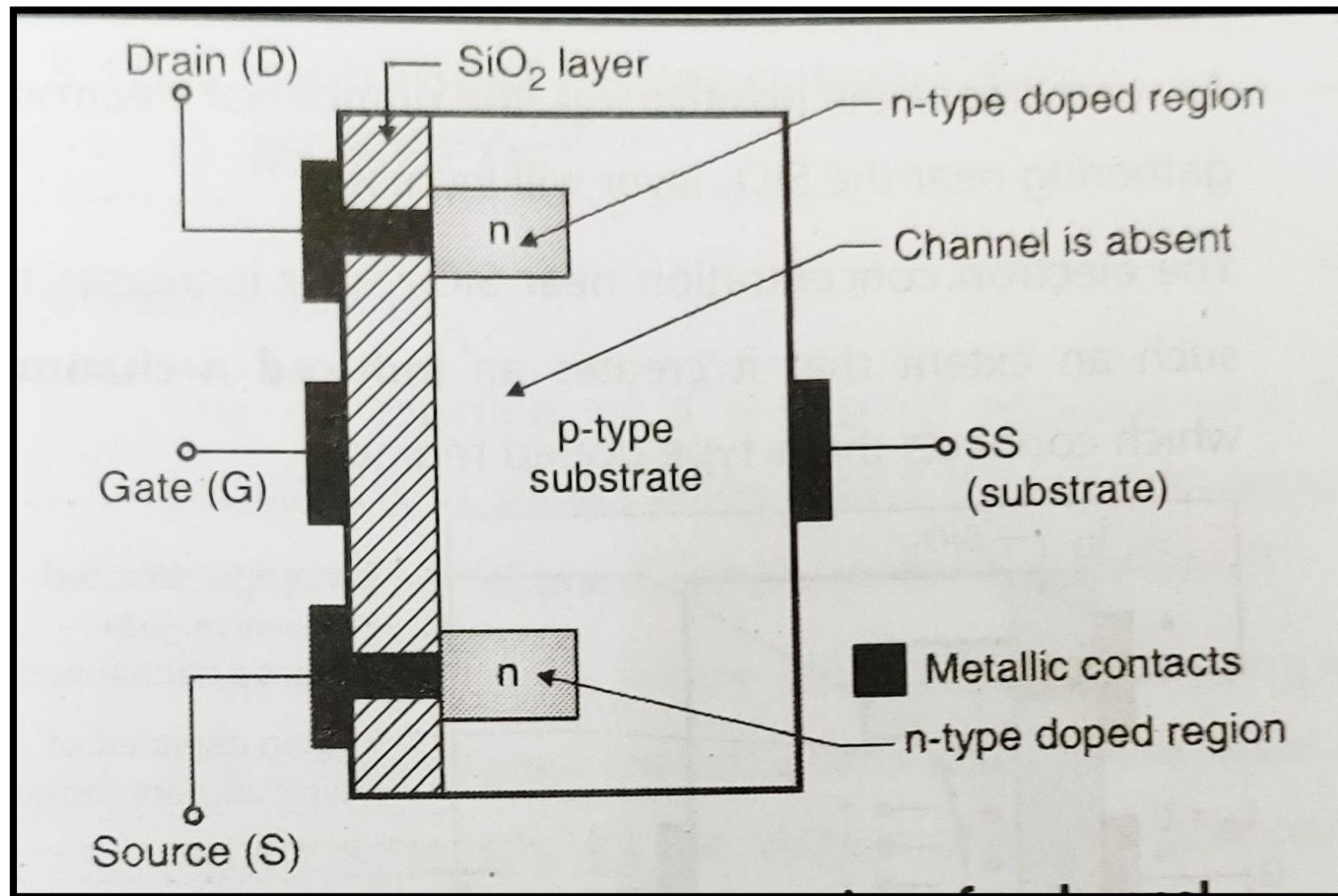


E-Type MOSFET Construction

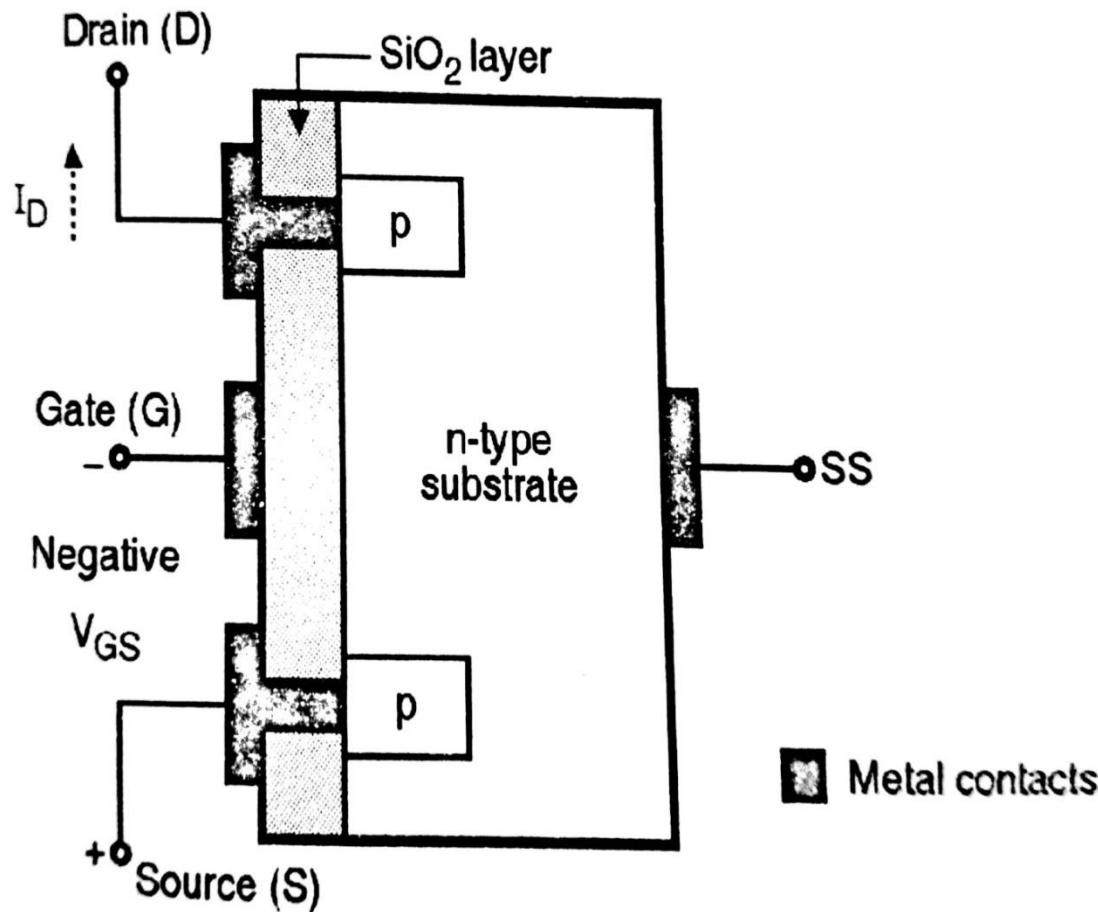
- The **Drain (D)** and **Source (S)** connect to the two *n*-doped regions. These *n*-doped regions are connected via an *n*-channel
- The **Gate (G)** connects to the *p*-doped substrate via a thin insulating layer of SiO_2
- There is no channel
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the **Substrate (SS)**



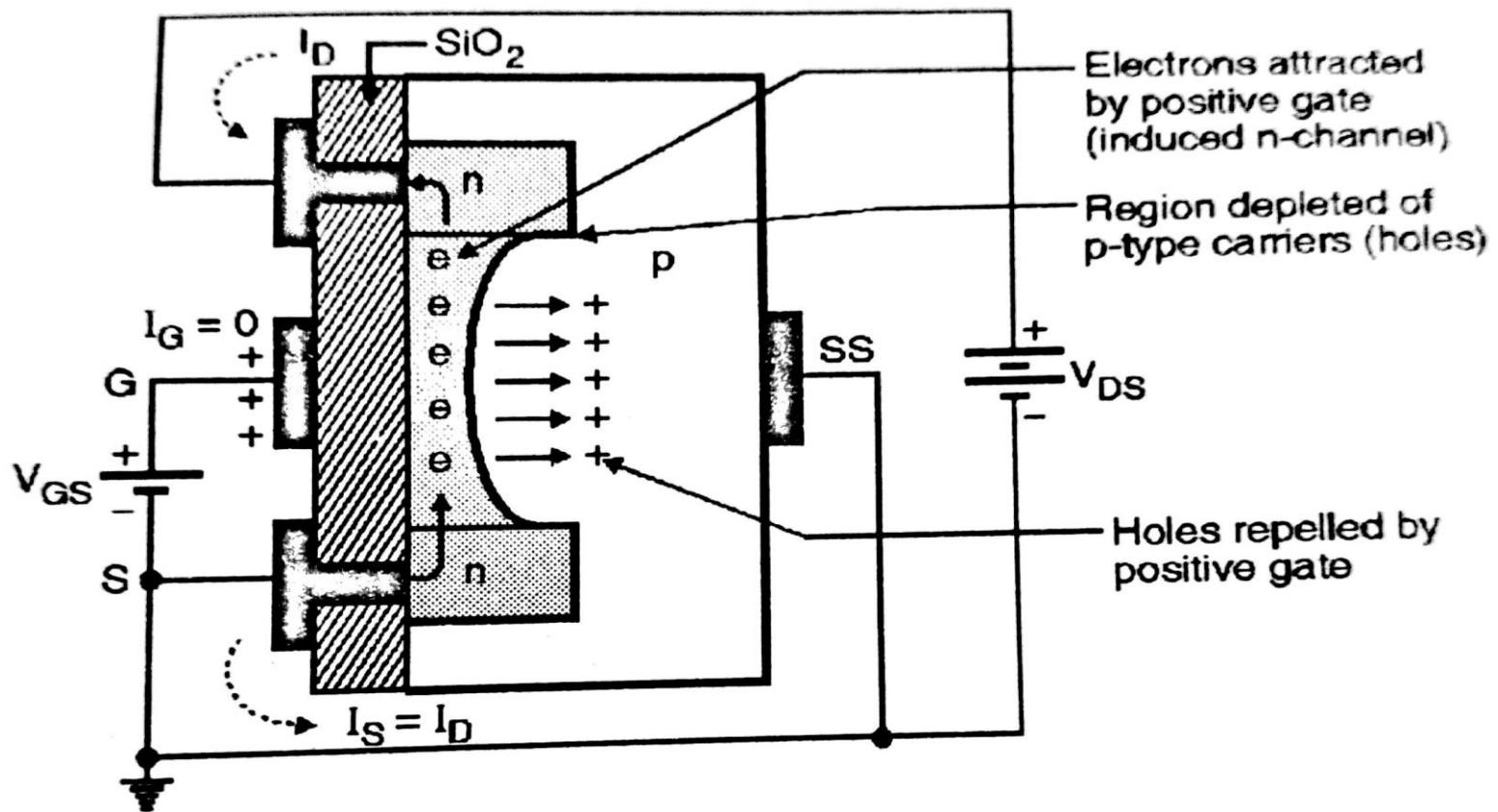
n- Channel MOSFET



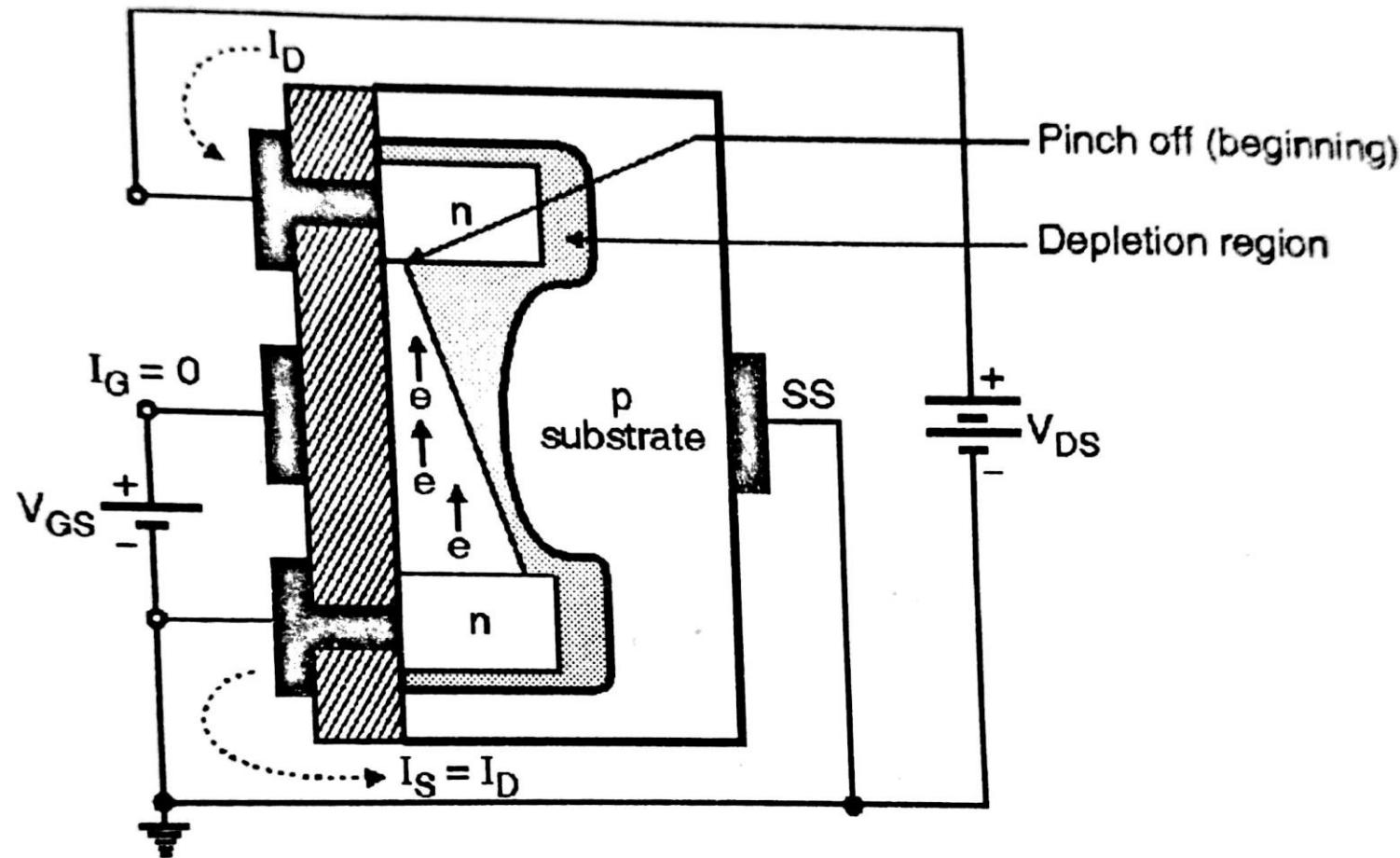
P- Channel MOSFET



Operation when V_{GS} is Positive



Effect of increase in Drain to Source Voltage



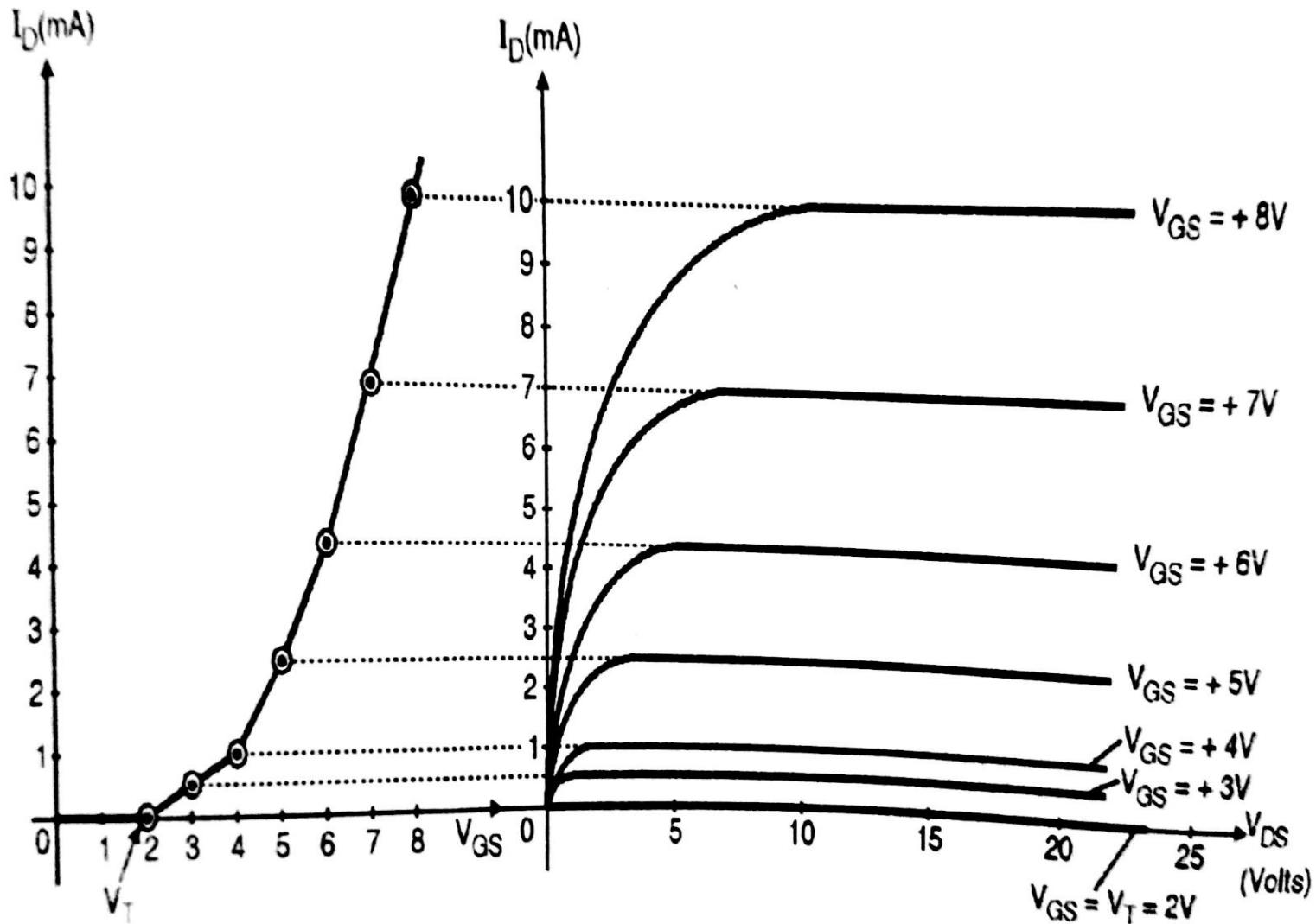
MOSFET Summary

1. Enhancement Type - the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "**Normally Open**" switch

2. Depletion Type - the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "**Normally Closed**" switch.

MOSFET type	$V_{GS} = +ve$	$V_{GS} = 0$	$V_{GS} = -ve$
P-Channel Enhancement	OFF	OFF	ON
N-Channel Enhancement	ON	OFF	OFF

Transfer & Drain Characteristics of N channel



Transfer Characteristics

Drain Characteristics

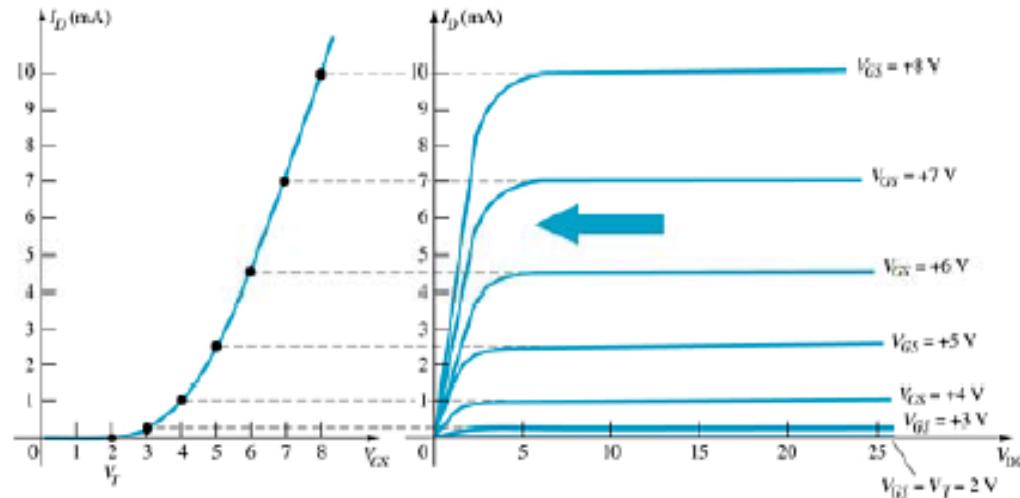
N- Enhancement Mode MOSFETs E-Type MOSFET Transfer Curve

To determine I_D given V_{GS} :

$$I_D = k(V_{GS} - V_T)^2$$

Where:

V_T = threshold voltage
or voltage at which the
MOSFET turns on



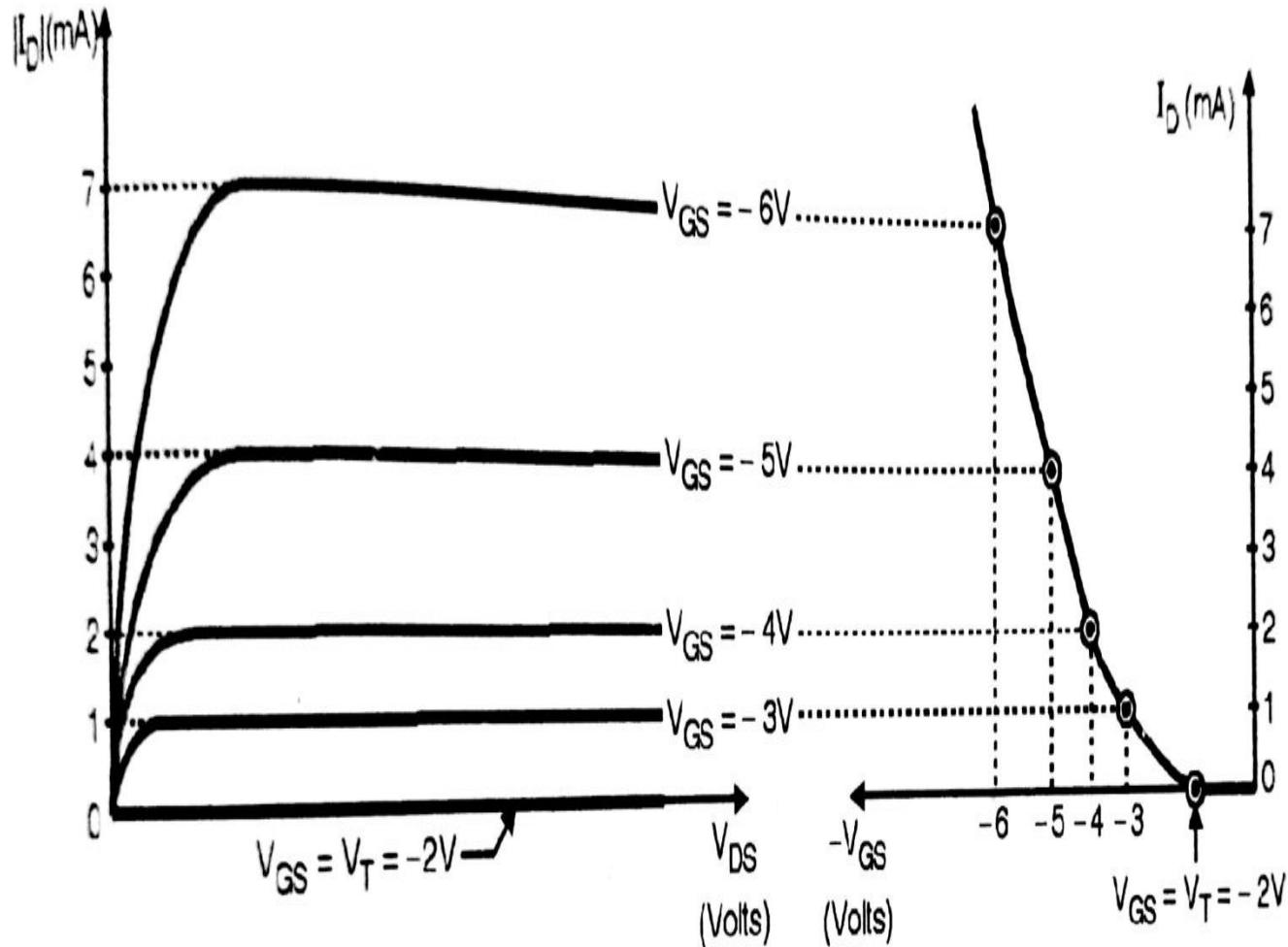
k , a constant, can be determined by using
values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

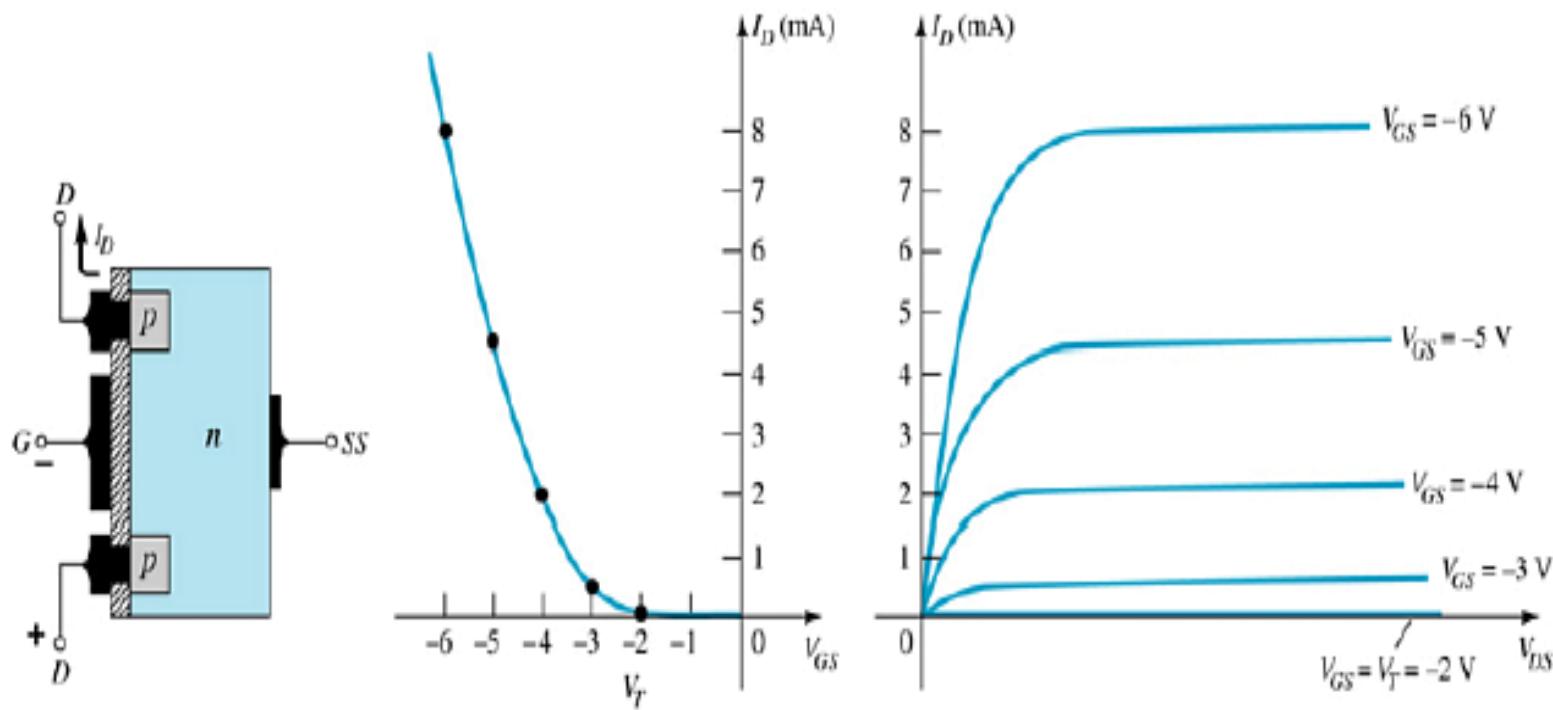
V_{DSsat} can be calculated by:

$$V_{DSat} = V_{GS} - V_T$$

P Channel E-MOSFET



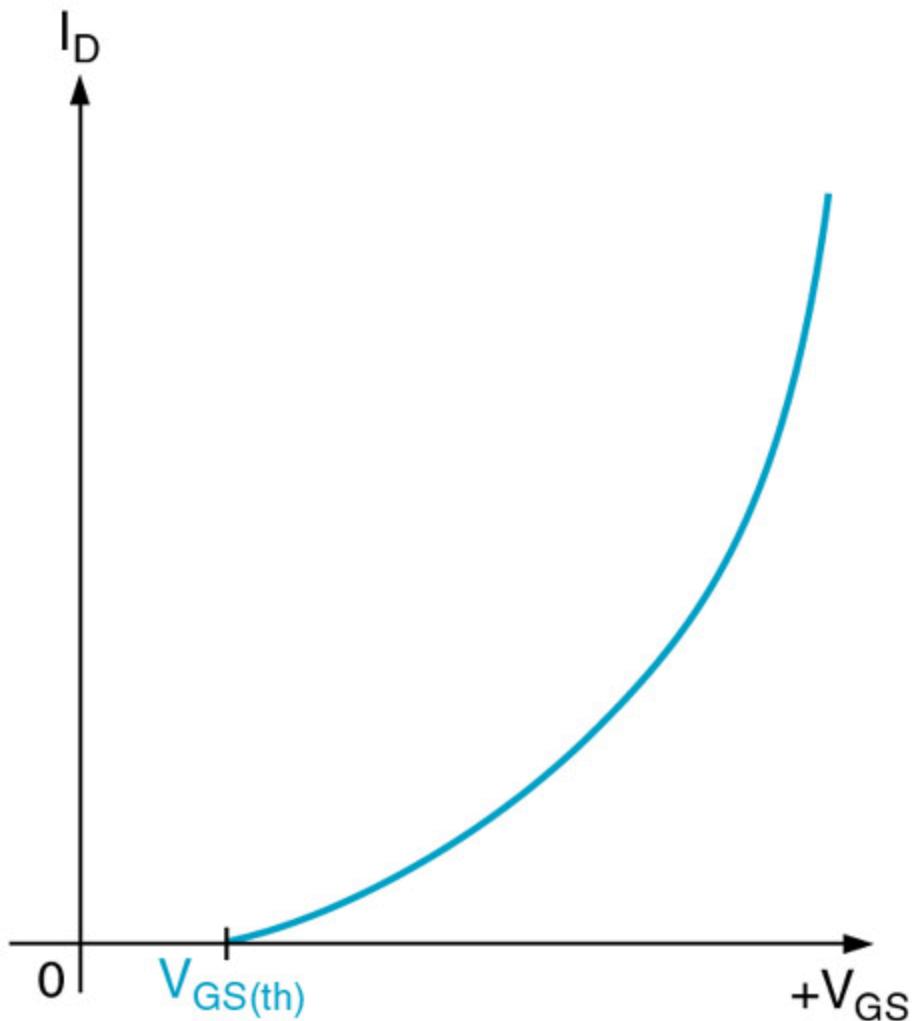
p-Channel E-Type MOSFETs



The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

ENHANCEMENT MOSFET (E-MOSFET)

Transfer characteristics (n – channel)



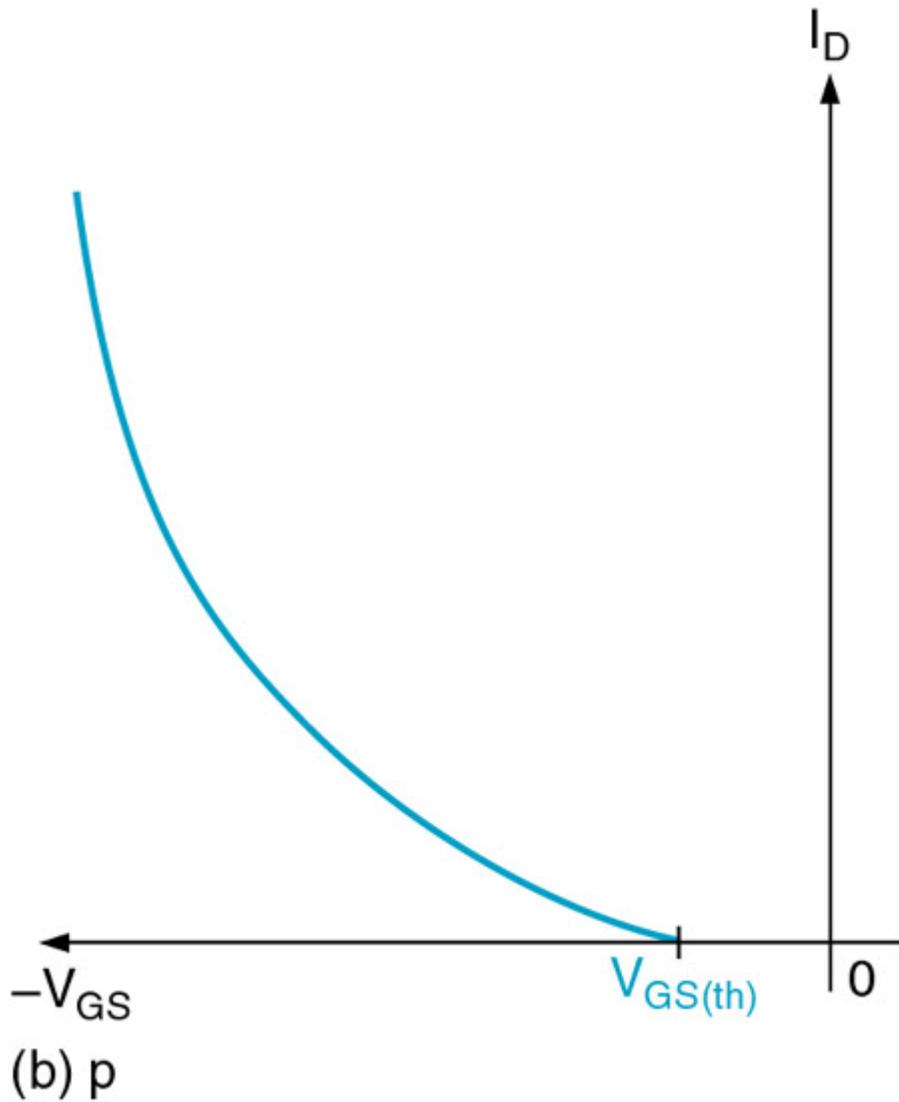
(a) n channel

- The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel area.
- For any gate voltage below the threshold value, there is no channel

FIGURE E-MOSFET general transfer characteristic curves.

ENHANCEMENT MOSFET (E-MOSFET)

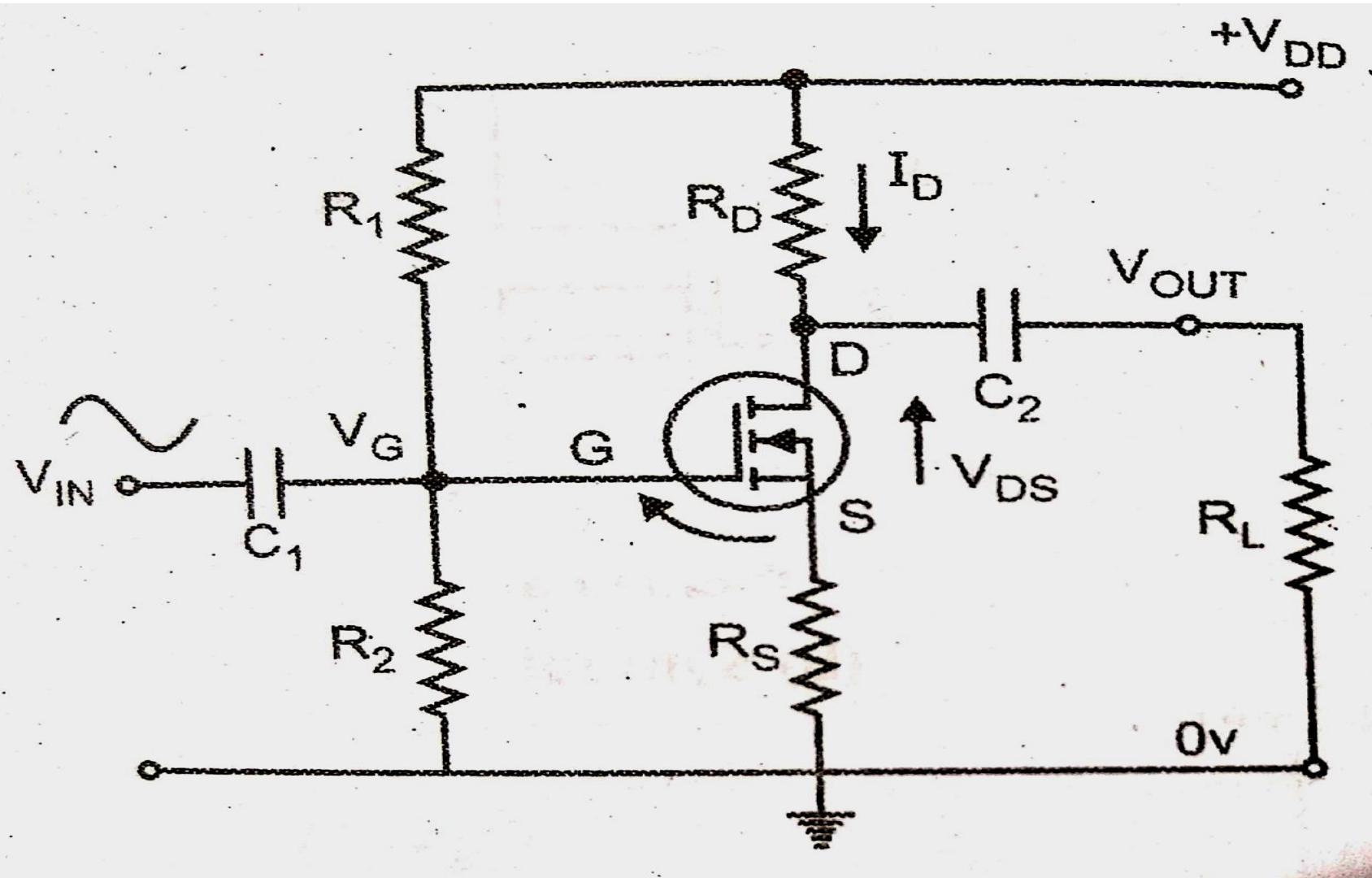
Transfer characteristics (p – channel)



- The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel area.
- For any gate voltage below the threshold value, there is no channel

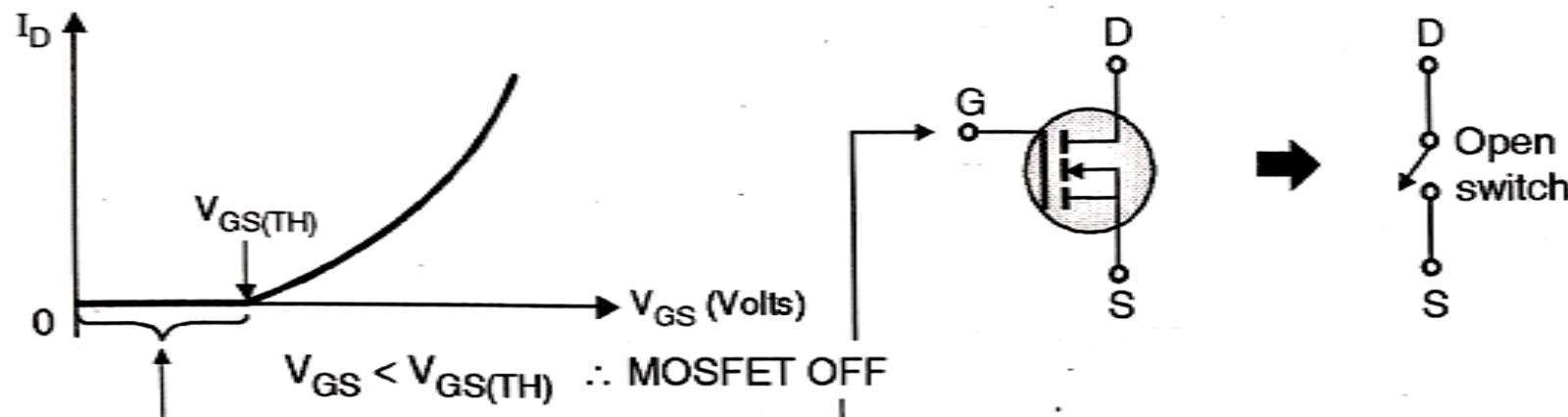
FIGURE E-MOSFET general transfer characteristic curves.

MOSFET as an AMPLIFIER



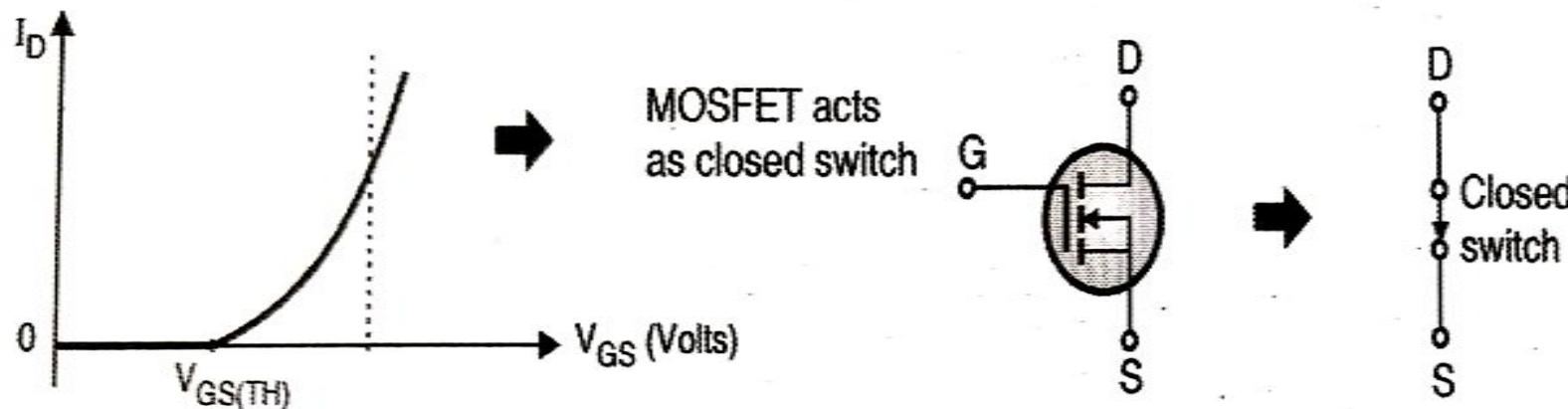
MOSFET as a SWITCH

MOSFET as an open switch



(a) MOSFET in its OFF state

MOSFET as a closed switch



(b) MOSFET in its ohmic region

MOSFET act as SWITCH

- $V_{GS} < V_T$ MOSFET is **OFF** condition so act as **Open Switch**
- V_{GS} grater than or equal to V_T then MOSFET is **ON** condition so act as **Closed Switch**

Parameter	BJT	MOSFET
Current / Voltage Control	Current	Voltage
Device Type	Bipolar	Unipolar
Size	Small	Very Small
Controlling Terminal	Base	Gate
Thermal Runaway	Can take place	Dose not take place
Transfer Characteristics	Linear	Non linear
Types	PNP & NPN	N & P Channel
Sensitivity	High	Less
Thermal noise	More	Low
Switching Speed	Less	More
Gain Bandwidth Product	High	Low
Input Resistance	Less compare to MOSFET	Very high
Voltage Gain	More	Less

Parameter	BJT	MOSFET	
Regions of operation:	Saturation – ON Switch , Cut off – OFF Switch Active – Amplifier	Ohmic – ON Switch ,Saturation – Amplifier , Cut off – OFF Switch	
Configuration	CE, CB, CC	CS,CG,CD	
Thermal Stability	Less	More	
Symbol	<p>n-p-n transistor</p>	<p>p-n-p transistor</p>	<p>Drain</p> <p>Source</p> <p>n channel</p>

Operational Amplifier(Op-Amp)

- Operational amplifier:
Functional block diagram of operational amplifier, ideal operational amplifier, Op-amp as Inverting and Non inverting amplifier

Operational Amplifiers

What is an Op amp?

A multistage high-gain amplifier integrated in analysis as a separate block.

- ⇒ The input of an op amp is a differential amplifier therefore has 2 inputs.
- ⇒ The output is singled ended.
- ⇒ Typically configured for a dual power supply (+/-V)

Op-amp pin diagram

There are 8 pins in a common Op-Amp, like the 741 which is used in many instructional courses.

- Pin 1: Offset null
- ◆ Pin 2: Inverting input terminal
- ◆ Pin 3: Non-inverting input terminal
- Pin 4: $-V_{CC}$ (negative voltage supply)
- Pin 5: Offset null
- ◆ Pin 6: Output voltage
- Pin 7: $+V_{CC}$ (positive voltage supply)
- Pin 8: No Connection

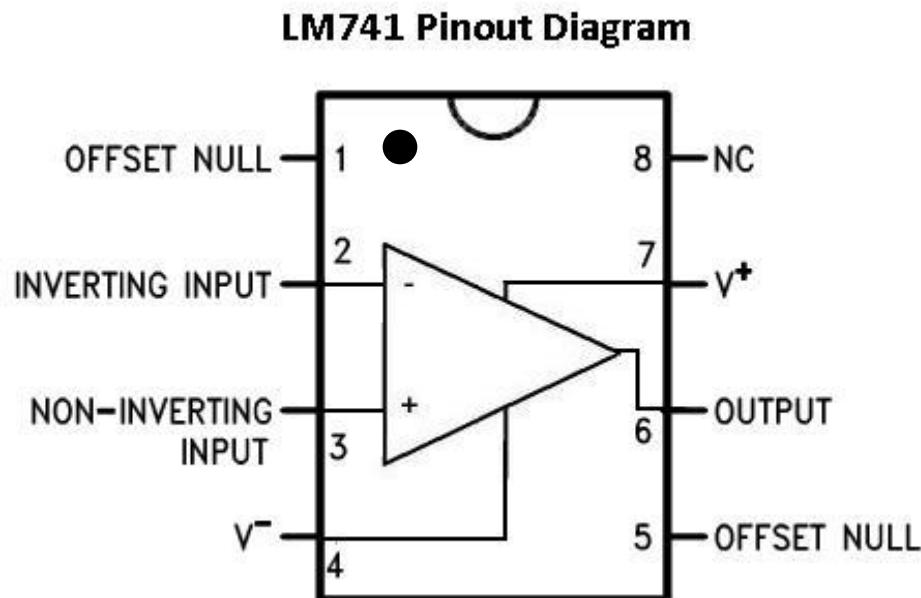
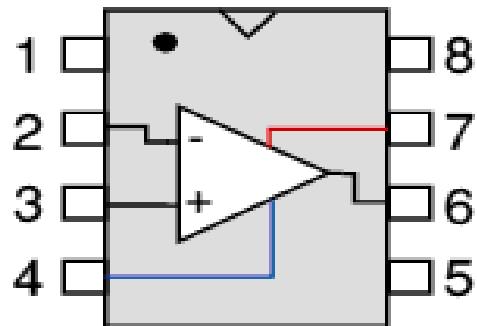


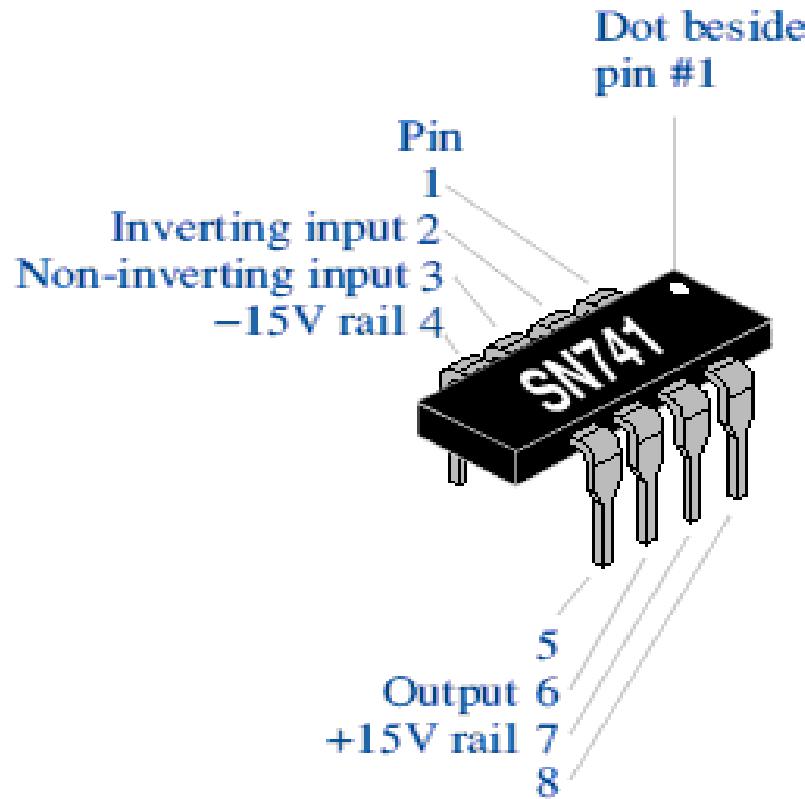
Figure : Pin connection, LM741.

Pin configuration of OP-AMP IC 741

741 Op Amp
8-pin DIP

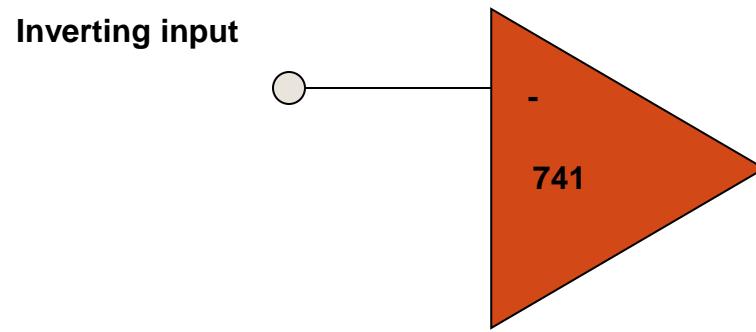


Top view

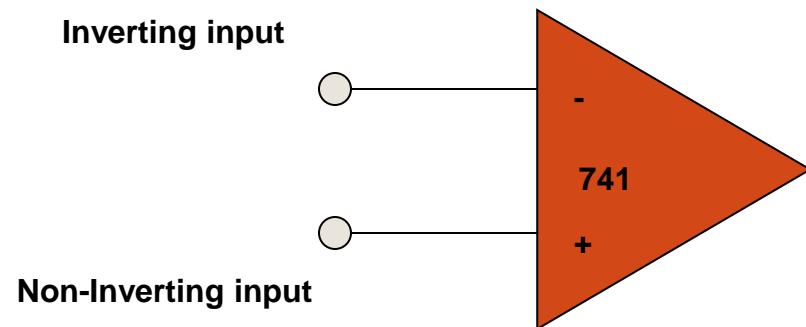


The most usual 741 package

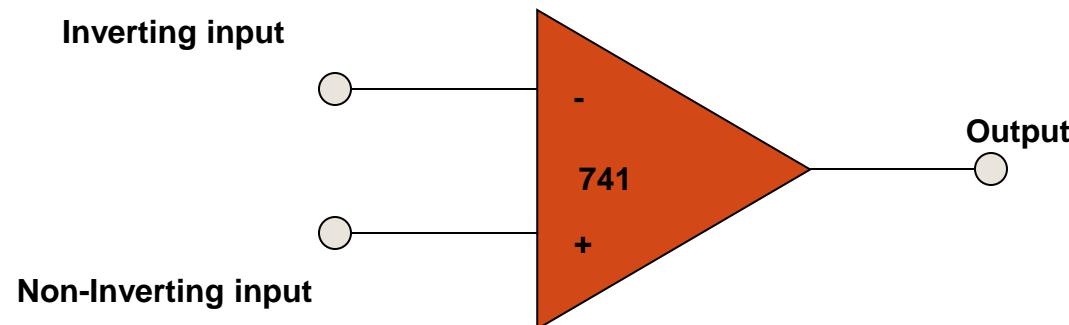
Symbol and terminal



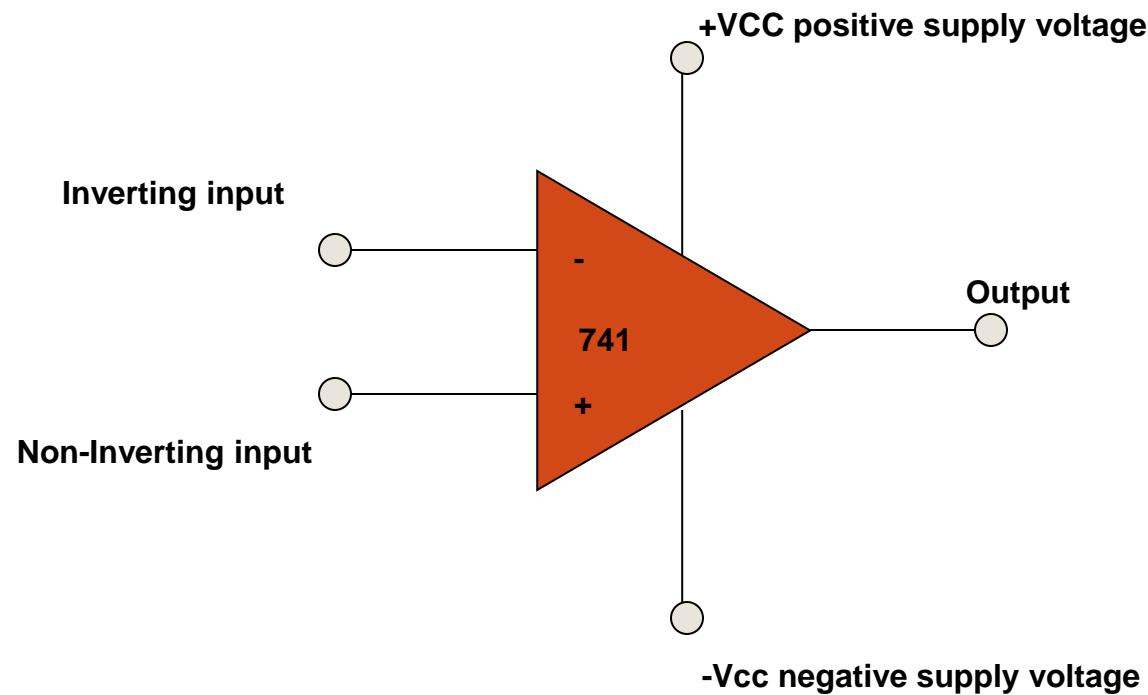
Symbol and terminal



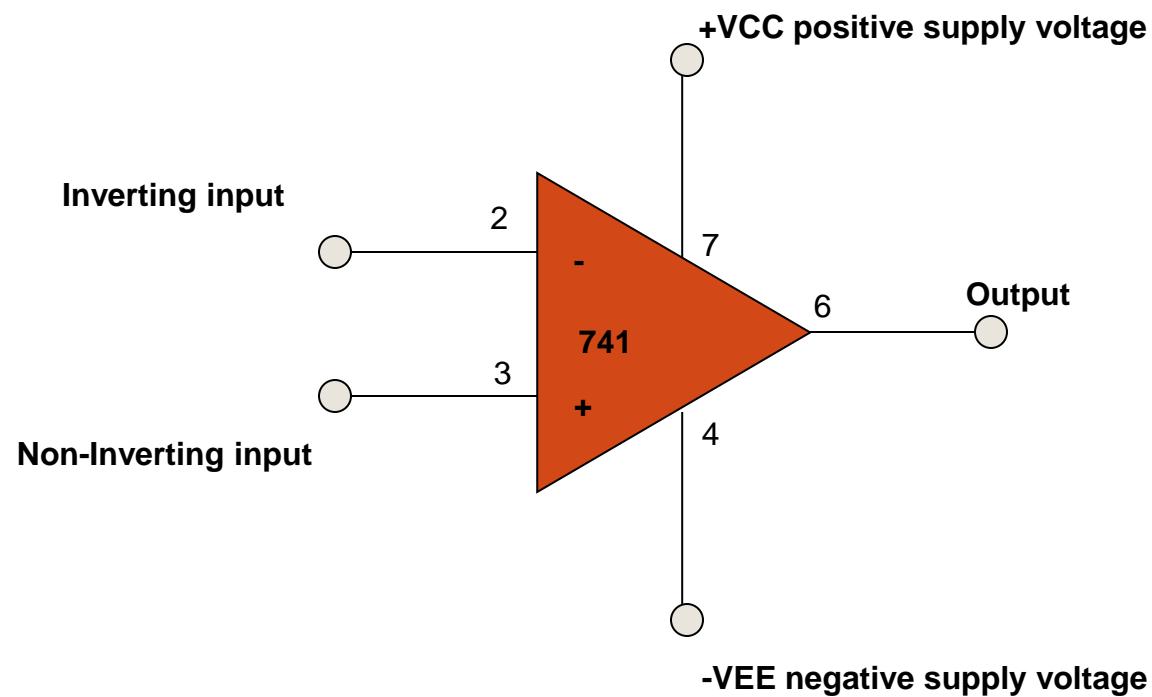
Symbol and terminal



Symbol and terminal



Symbol and terminal



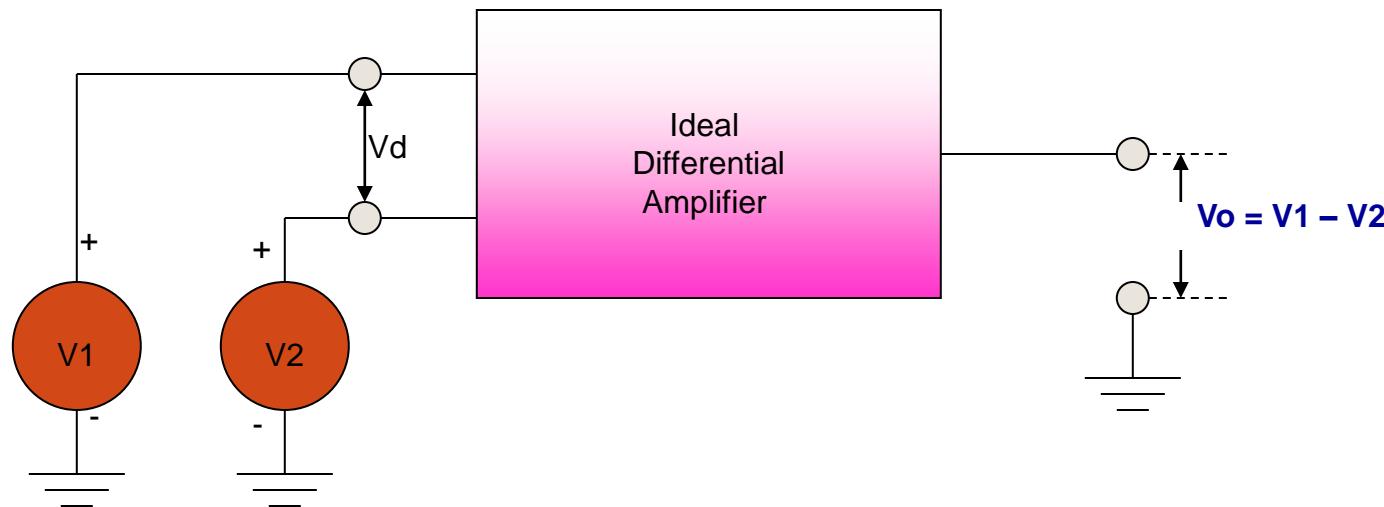
The OP-AMP IC 741

- The most common and most famous op-amp is the just 741, which is packaged in an 8-pin mini-DIP. The integrated circuit contains **20 transistors and 11 resistors**. Introduced by Fairchild in 1968, the 741 and subsequent IC op-amps including FET-input op-amps have become the standard tool for achieving amplification and a host of other tasks.

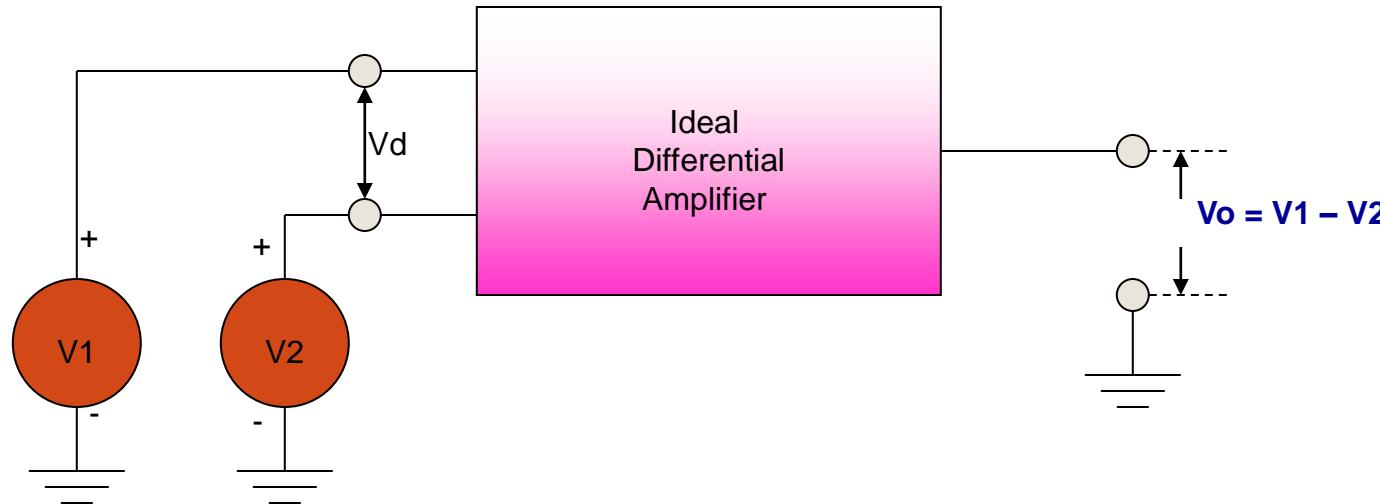
Manufactures of OP-AMP IC 741

- The manufactures of Op-amp ICs are companies like Fairchild, National semiconductor, Motorola, Texas Instruments and signetics.
- The identifying initials for some other companies are as follows:
 1. National semiconductors : LM 741
 2. Motorola : MC 741
 3. RCA : CA 741
 4. Texas instruments : SN 52741
 5. Signetics : N 5741

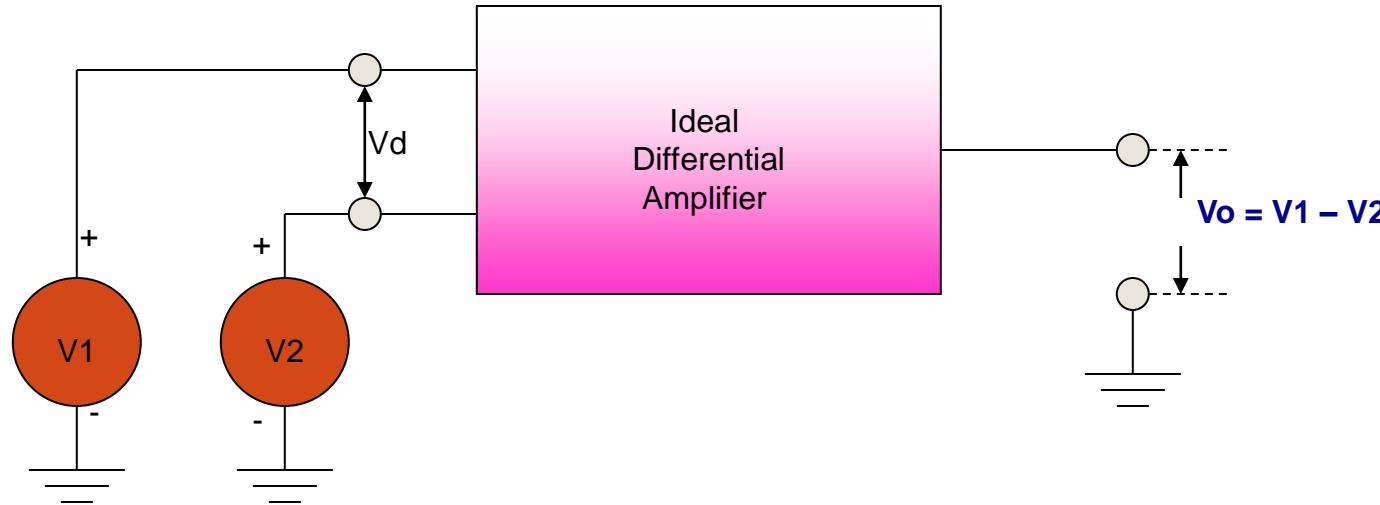
- Ideal differential amplifier
- An ideal differential amplifier is expected to amplify the differential signal present between its two input signal.
- It is also the basic stage of an integrated Op-amp with differential input.



Block diagram of an ideal differential amplifier

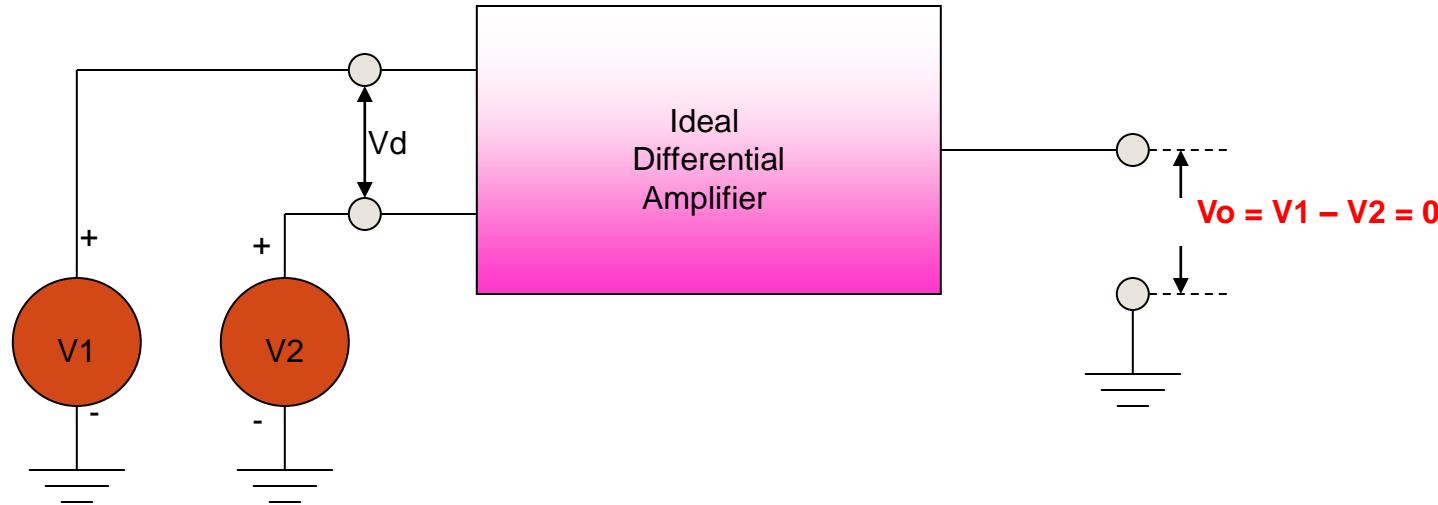


- **Differential input signal :**
- The difference between the input signals V_1 and V_2 is called as the differential signal V_d
- Differential signal $V_d = V_1 - V_2$
- From the equation it is clear that the amplifier output will be non-zero if and only if the differential signal is non-zero value



Differential gain :

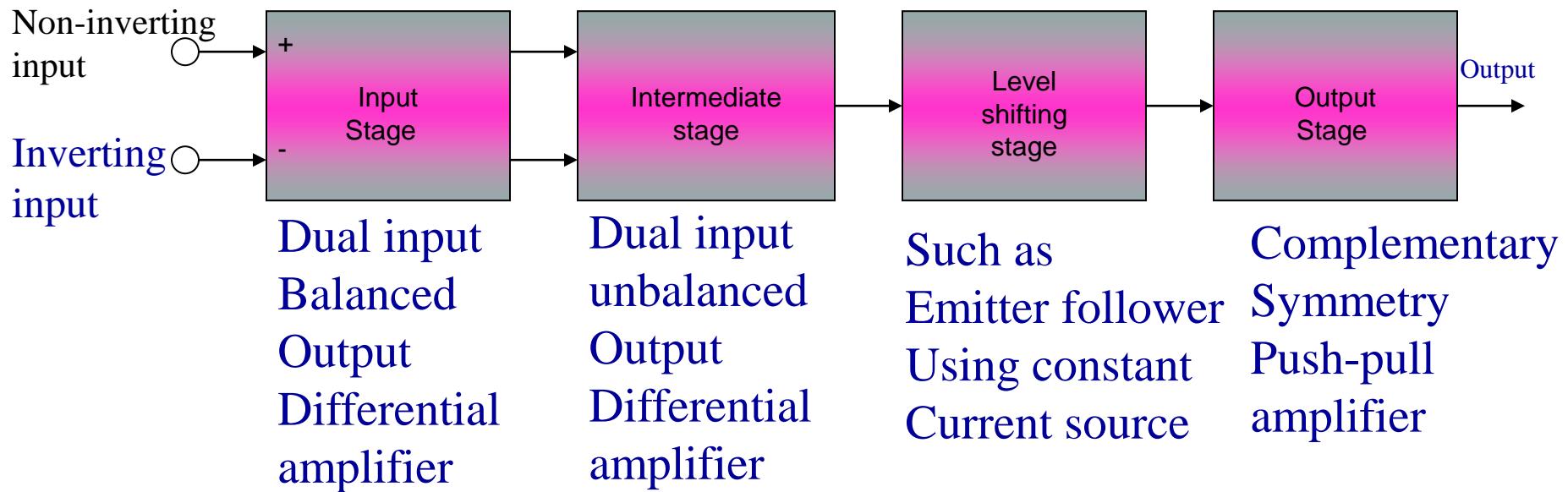
- $V_o = A_d (V_1 - V_2)$
- Where A_d is called as the differential gain.
- The differential gain can be defined as the gain with which the differential amplifier amplifies the differential signal.
- $V_o = A_d V_d$ as $V_d = V_1 - V_2$
- Therefore the expression for the gain $A_d = V_o / V_d$
- In decibels $A_d (\text{dB}) = 10 \log_{10} [V_o / V_d]$



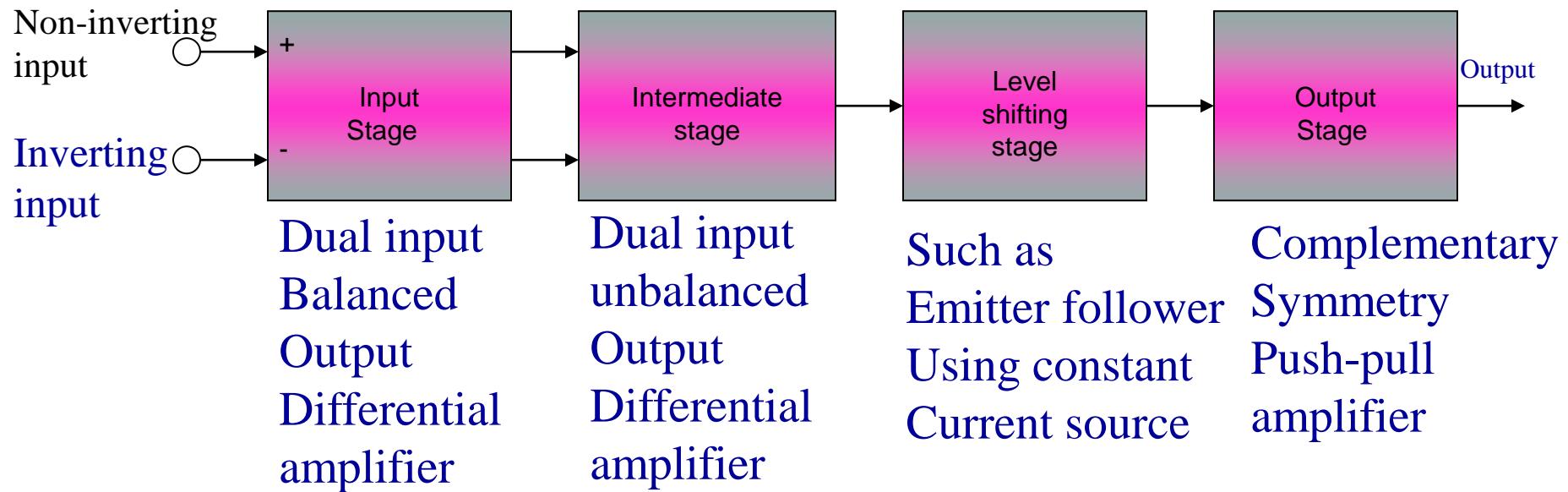
Common mode signal :

- A common signal to both the input terminals (i.e. $V_1=V_2=V$) is called as common mode signal.
- The output voltage produced by an ideal differential amplifier is zero for the common mode signal.

Block diagram of a typical OP-AMP



Block diagram of a typical OP-AMP

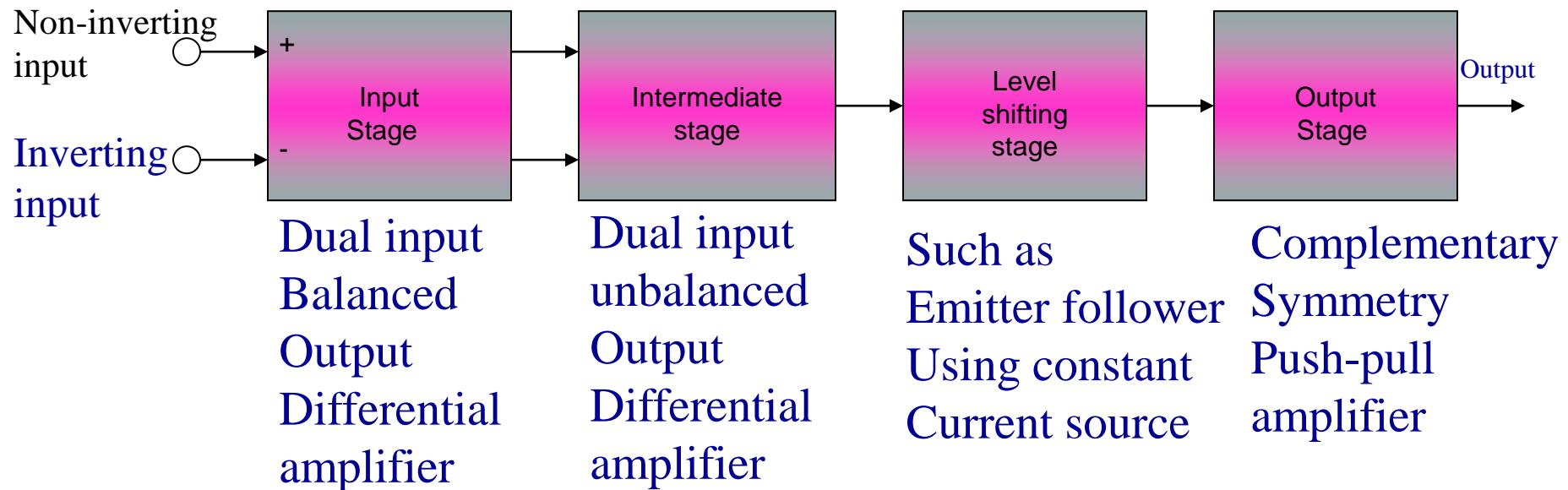


Input Stage : The input stage is A dual-input balanced output differential amplifier. The two inputs are inverting and non-inverting input terminals.

This stage provides most of the voltage gain of the op-amp and decides the input resistance value R_i .

It provide high input impedance.

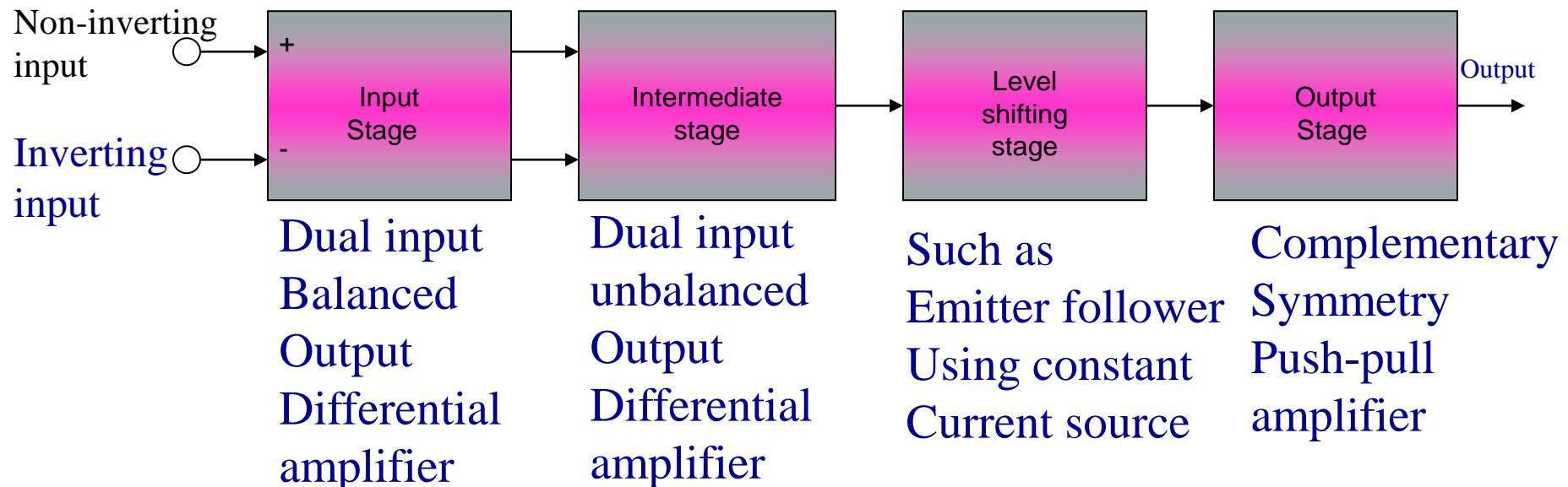
Block diagram of a typical OP-AMP



Intermediate Stage :

This is usually another differential amplifier.
It is driven by output of input stage.
This stage is a dual input unbalanced output (single ended output) differential amplifier.

Block diagram of a typical OP-AMP

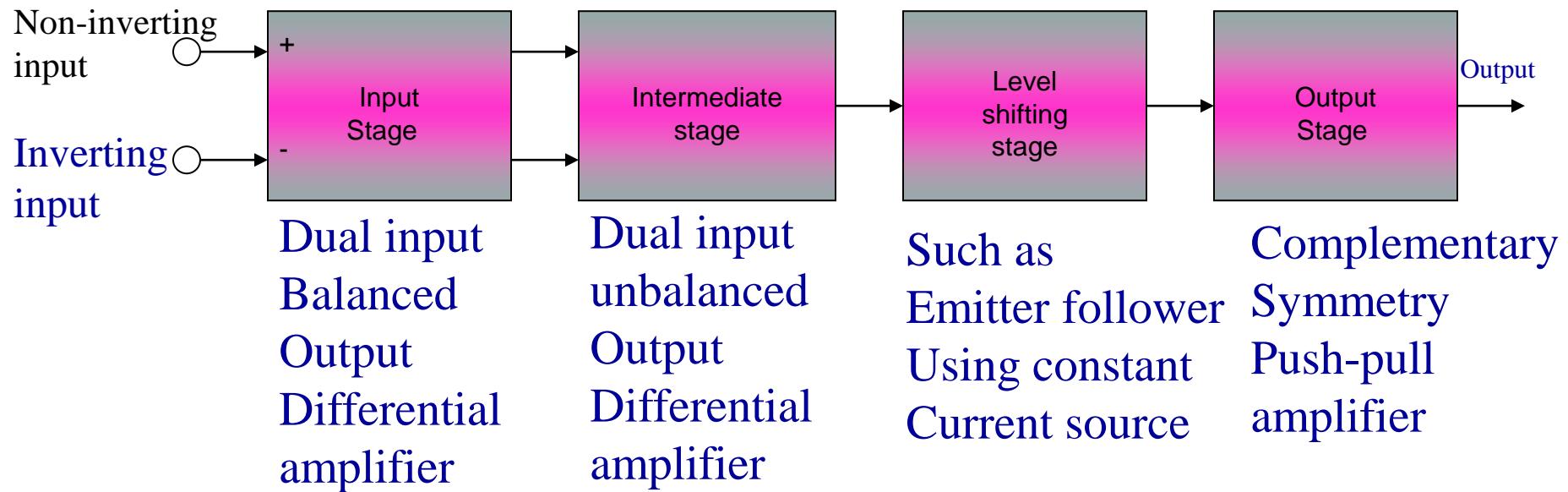


Level shifting Stage :

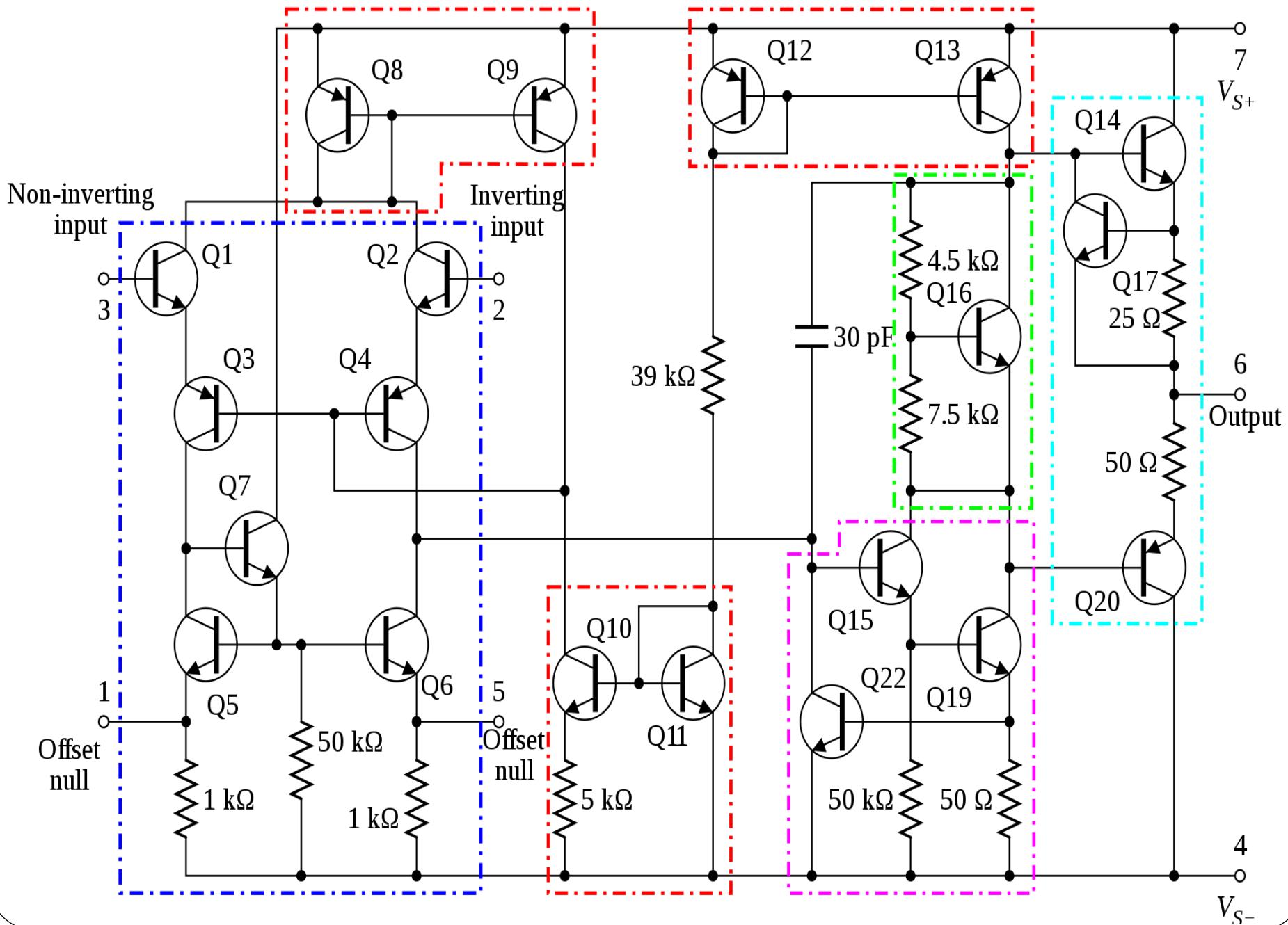
Due to the direct coupling between the first two stages, the input of level shifting stage is an amplified signal with some non-zero dc level.

Level shifting stage is used to bring this dc level to zero volts with respect to ground.

Block diagram of a typical OP-AMP

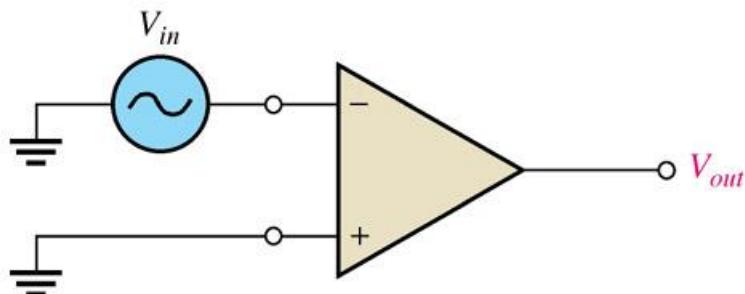


Output Stage : This stage is normally a complementary output stage. It increases the magnitude of voltage and raises the current supplying capability of the op-amp. Its also provides the low output resistance.

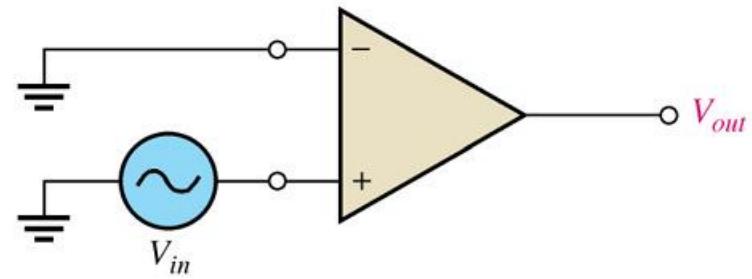


Modes of Operation

1. Single-ended input mode.

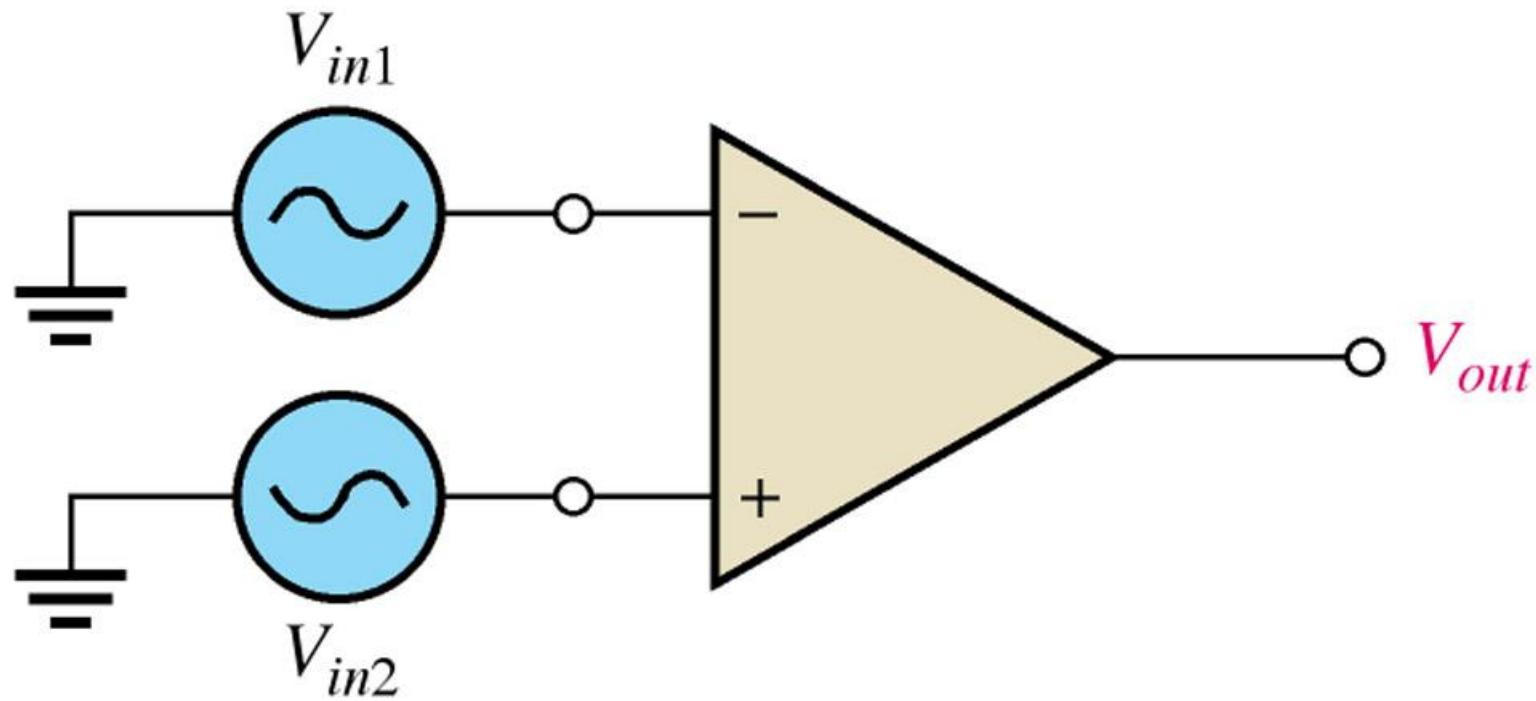


(a)

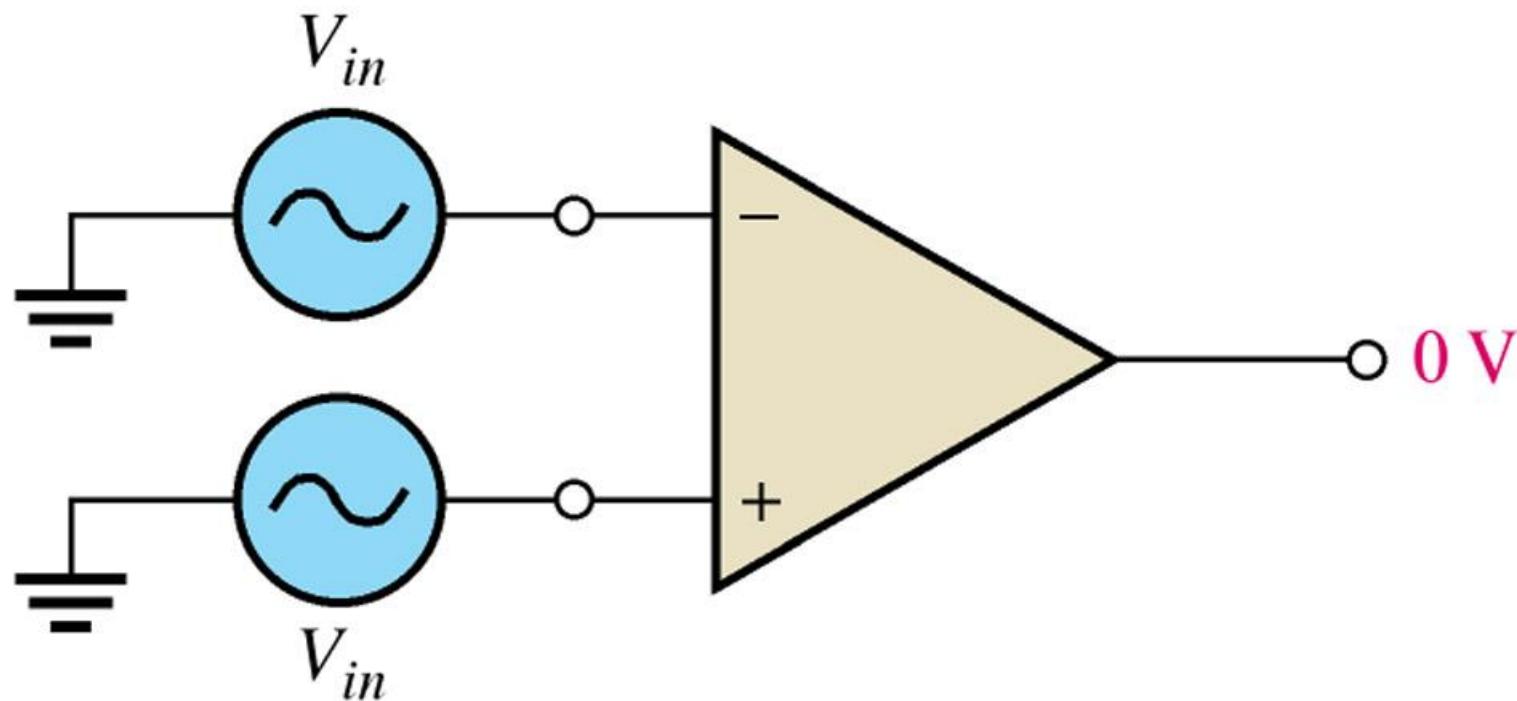


(b)

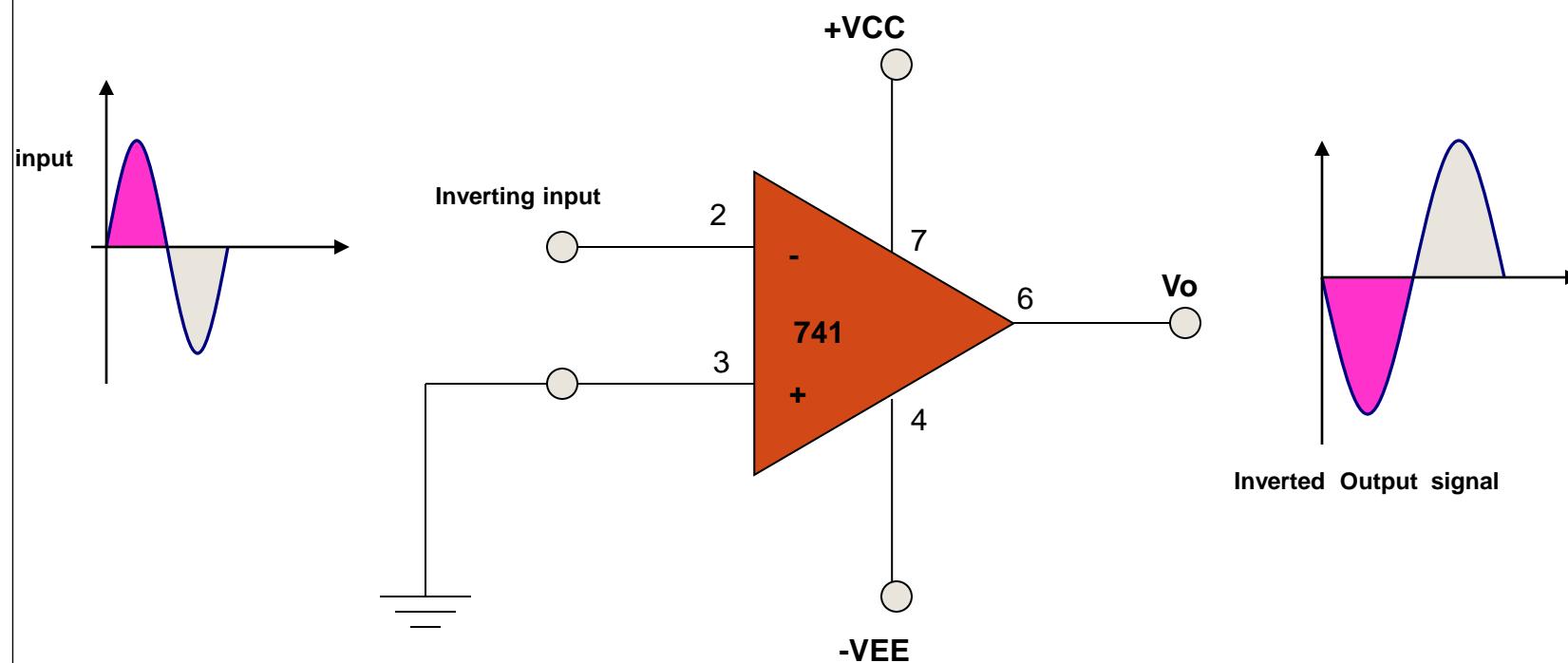
2. Differential input mode.



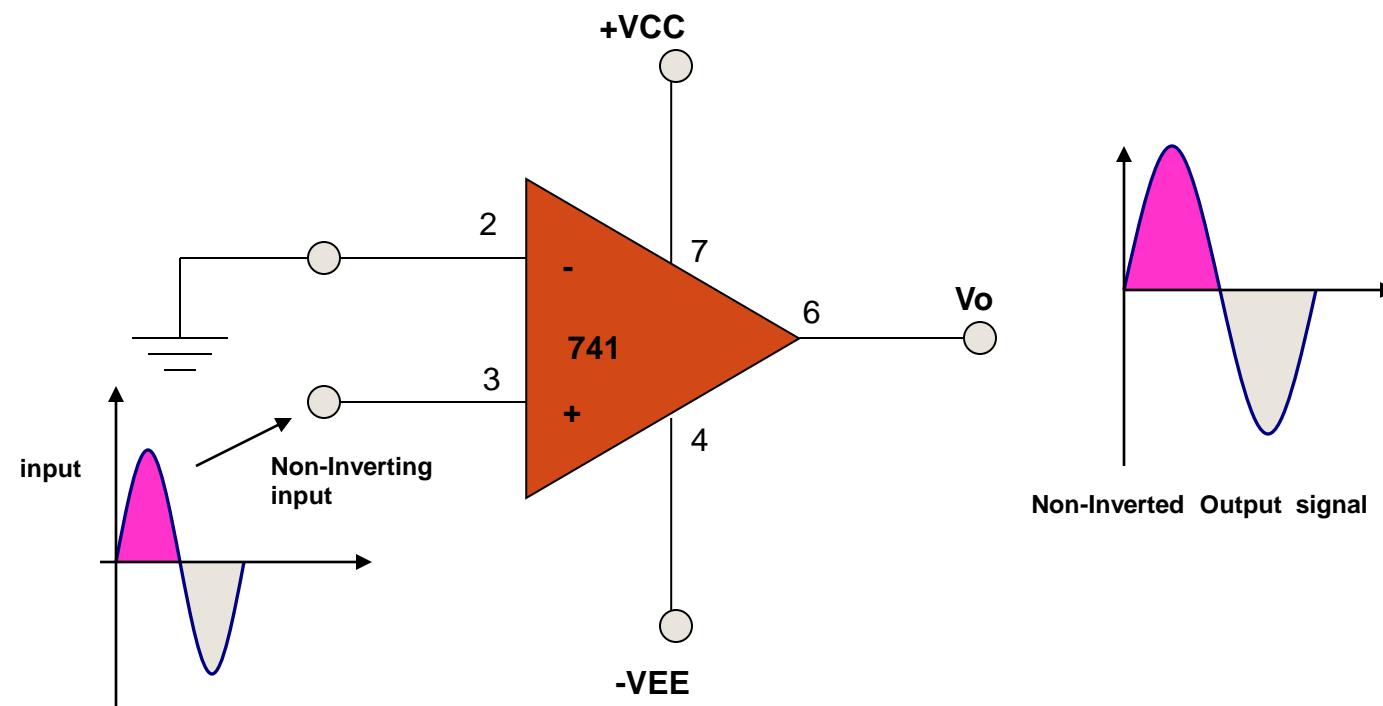
3. Common-mode operation.



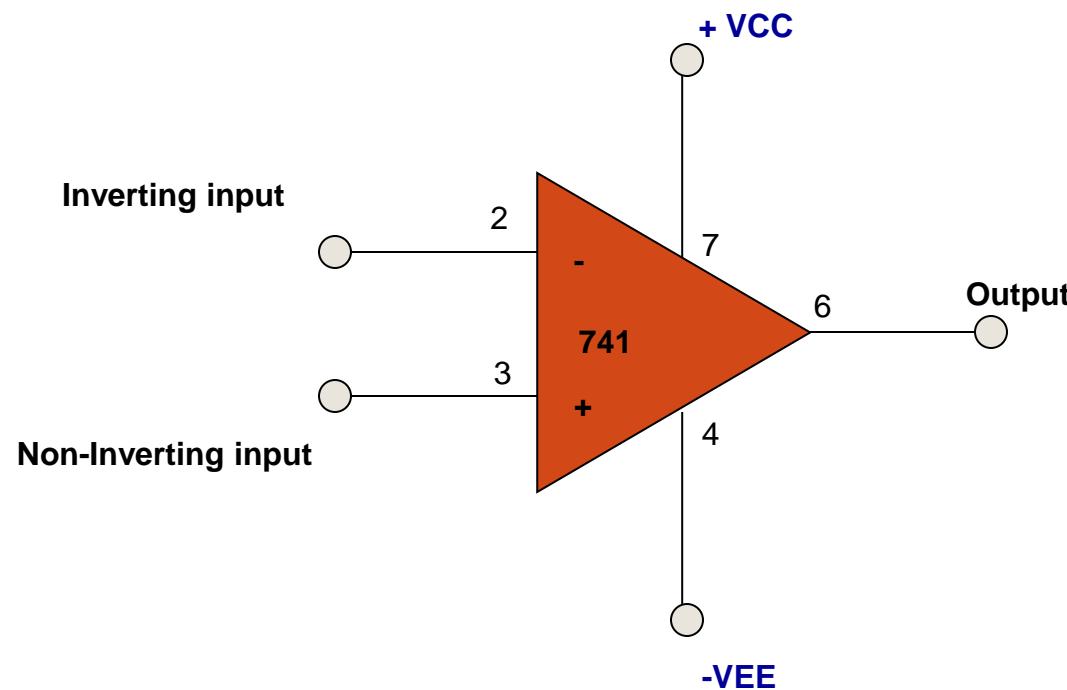
Input and output signals 180° phase shift when the input signal is applied to the inverting (-) terminal



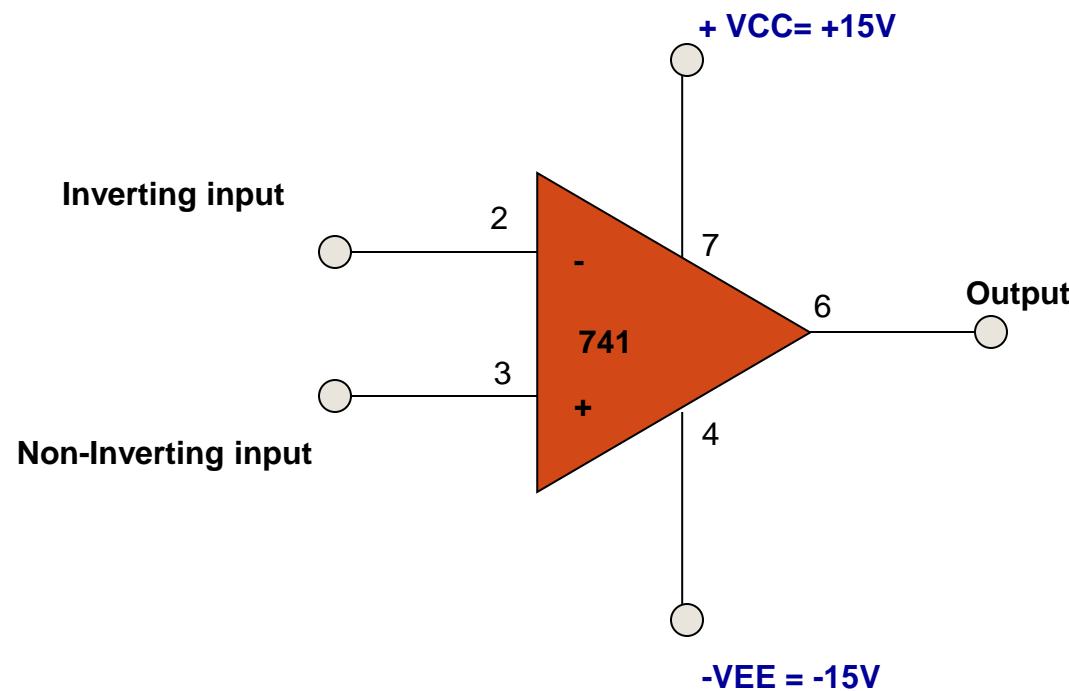
Input and output signals 0^0 phase shift when the input signal is applied to the Non-inverting (+) terminal



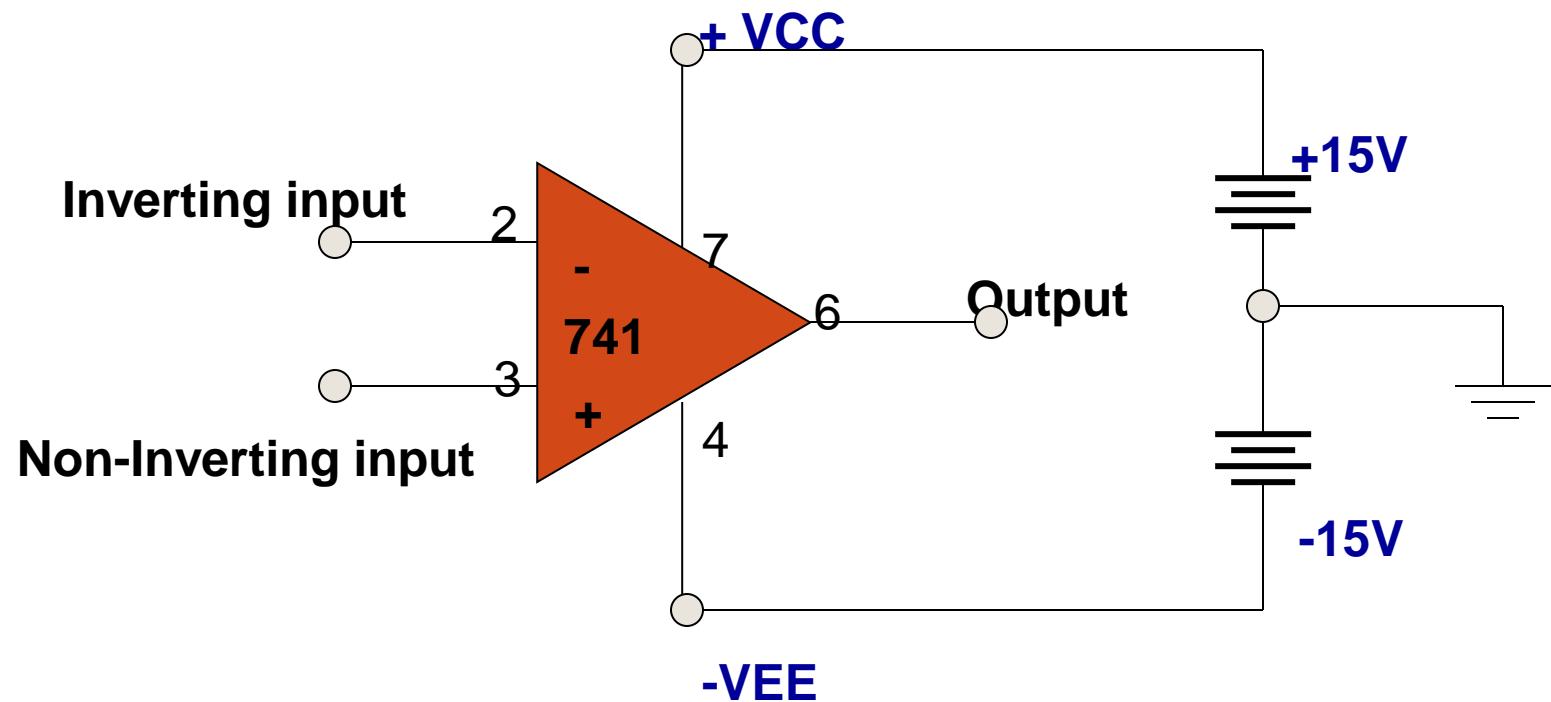
DC power supply for an OP-AMP



DC power supply for an OP-AMP

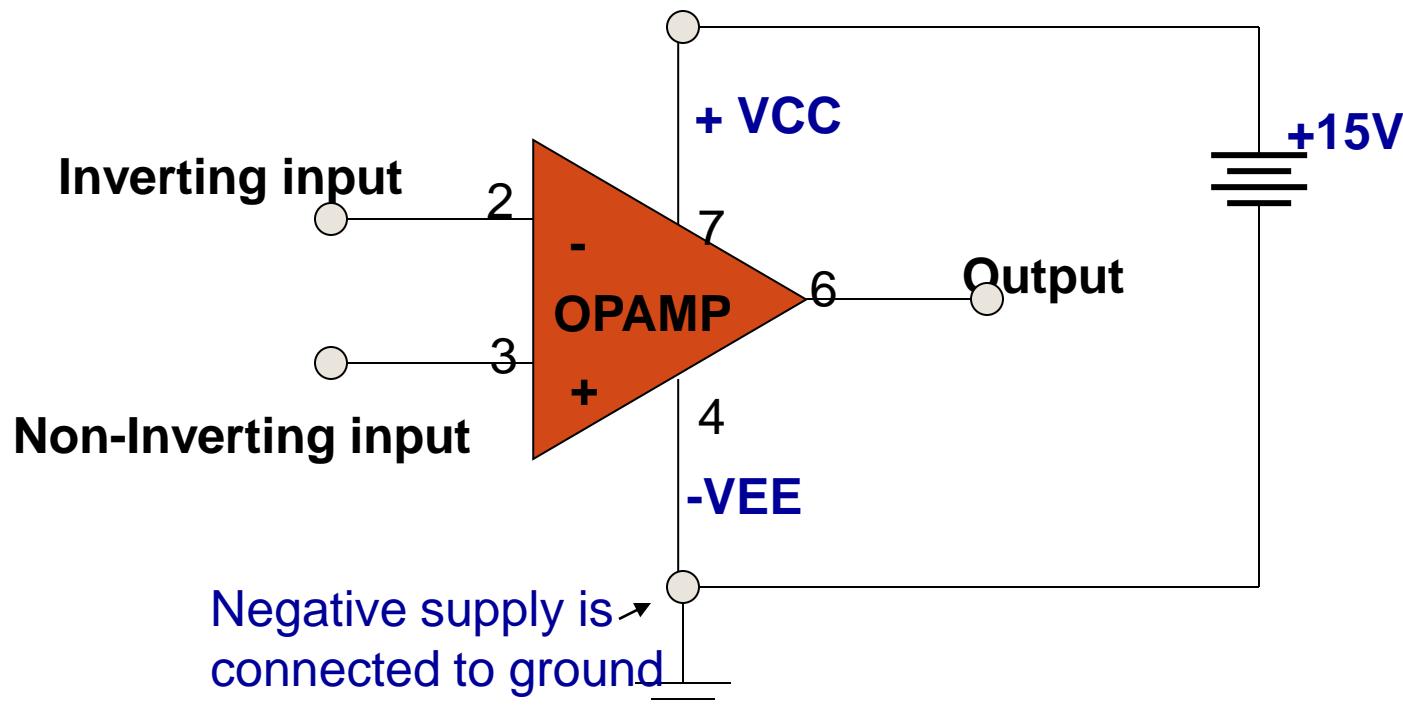


DC power supply for an OP-AMP

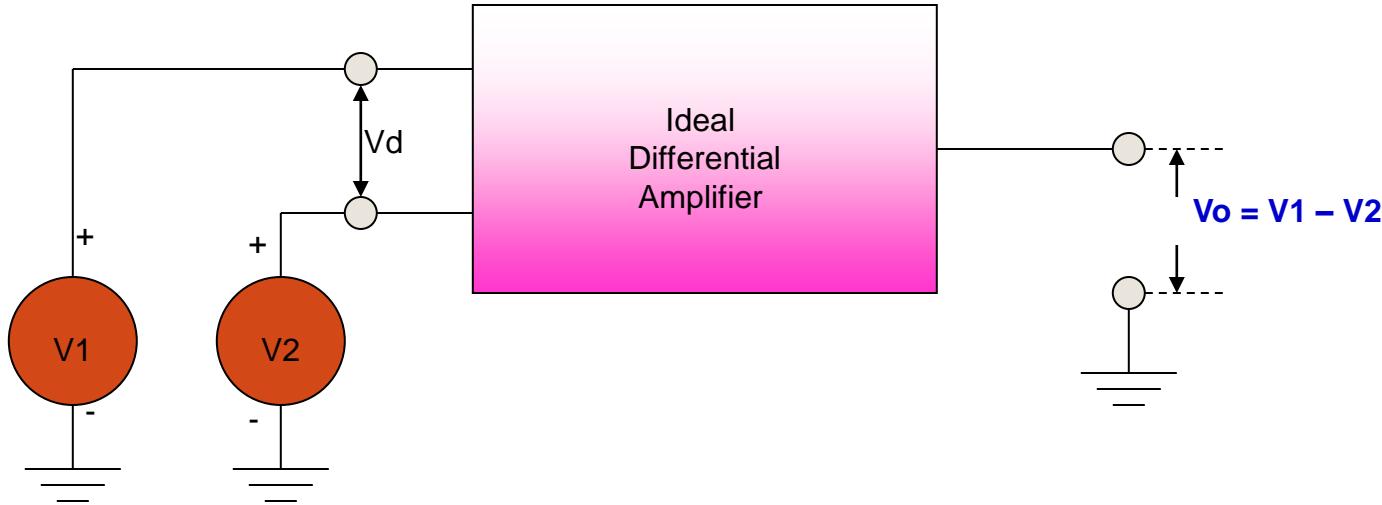


Dual polarity supply

DC power supply for an OP-AMP

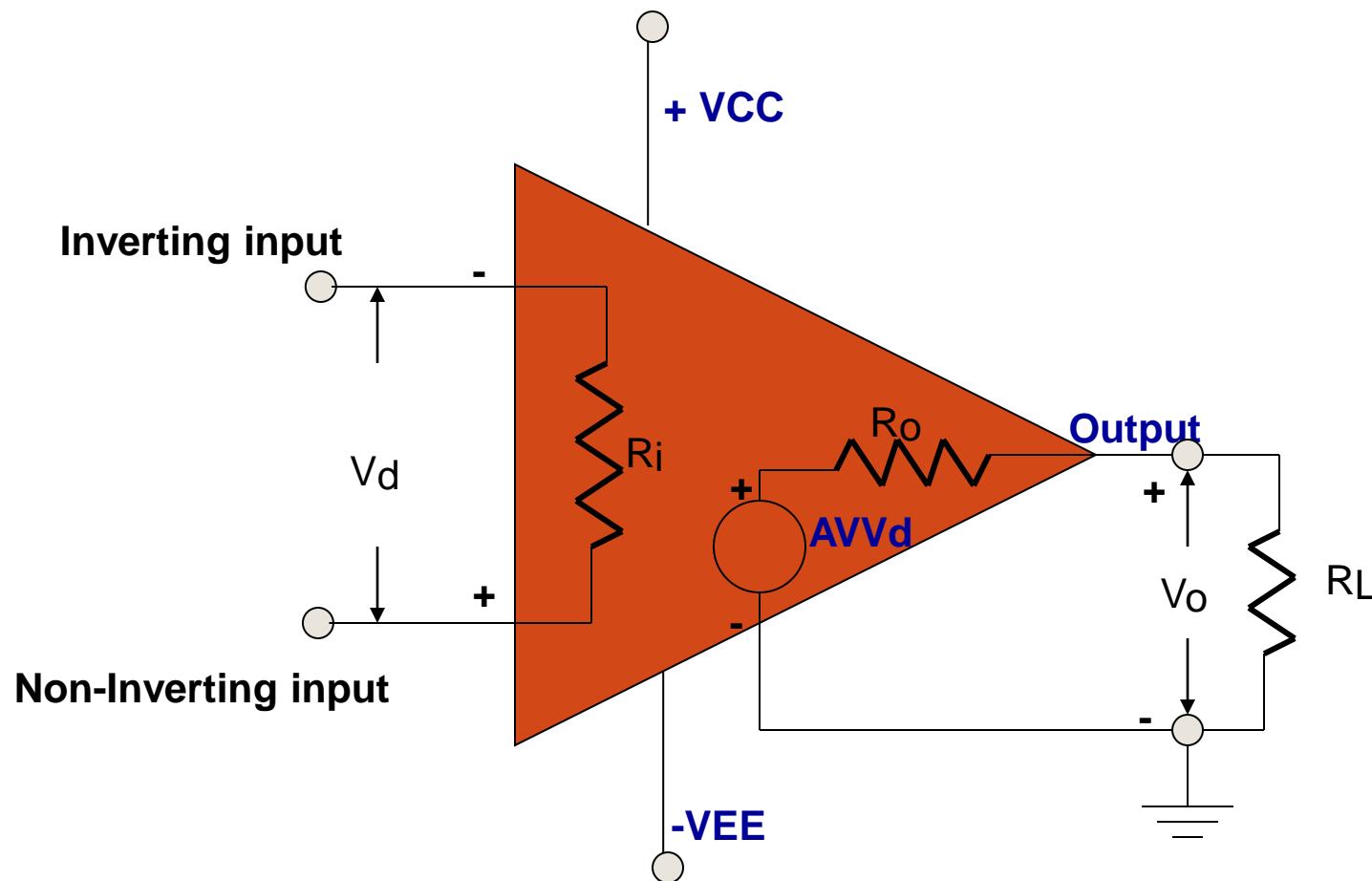


Single polarity supply



- **Common mode rejection ratio (CMRR) :**
- Common mode rejection ration (CMRR) is the ability of a differential amplifier to reject the common mode signal successfully.
- CMRR is defined as the ratio of differential gain \$A_d\$ and common mode gain \$A_c\$. It is denoted by letter “\$\rho\$”
- $$\text{CMRR} = \rho = |A_d / A_c|$$
- Ideally CMRR should be infinite and practically it should be as high as possible.

Equivalent circuit of an OP-AMP

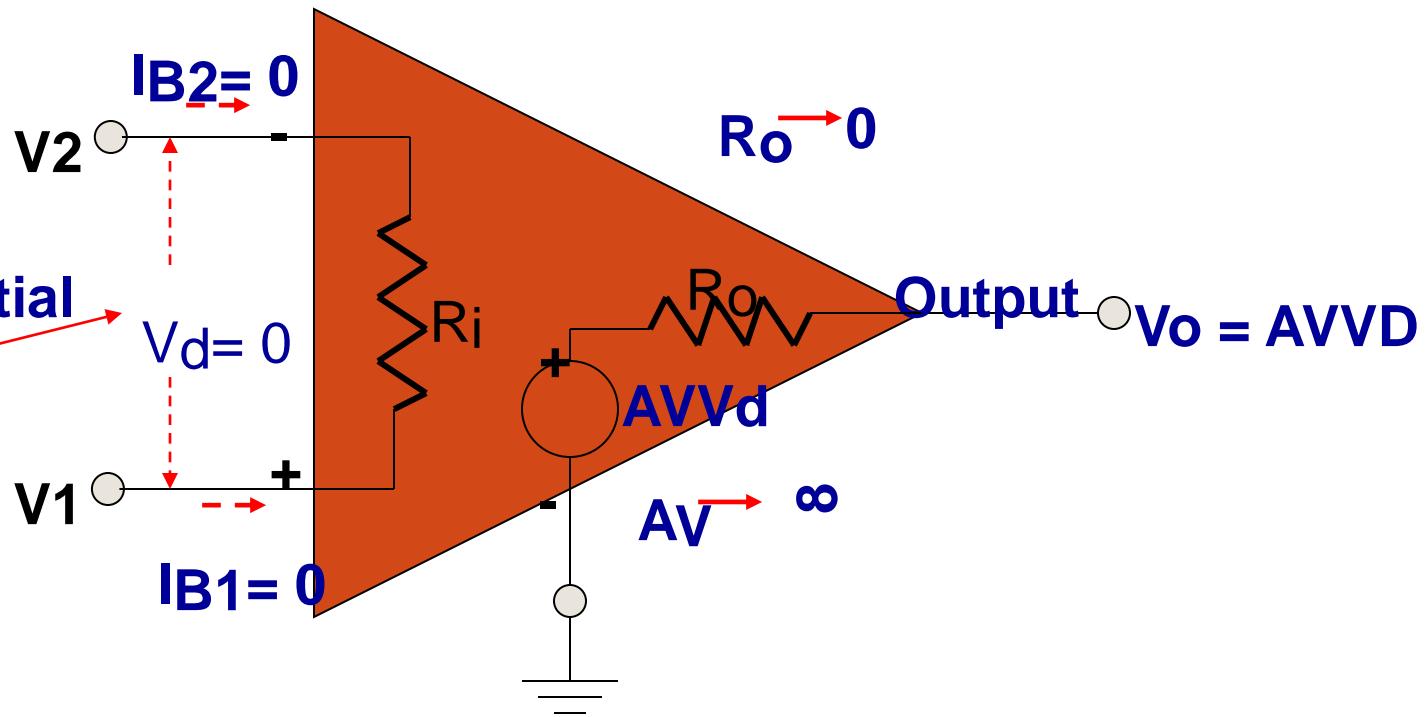


The ideal OP-AMP Parameters

$$R_i \rightarrow \infty$$

$$I_{B2} = 0$$

Zero differential
Input voltage



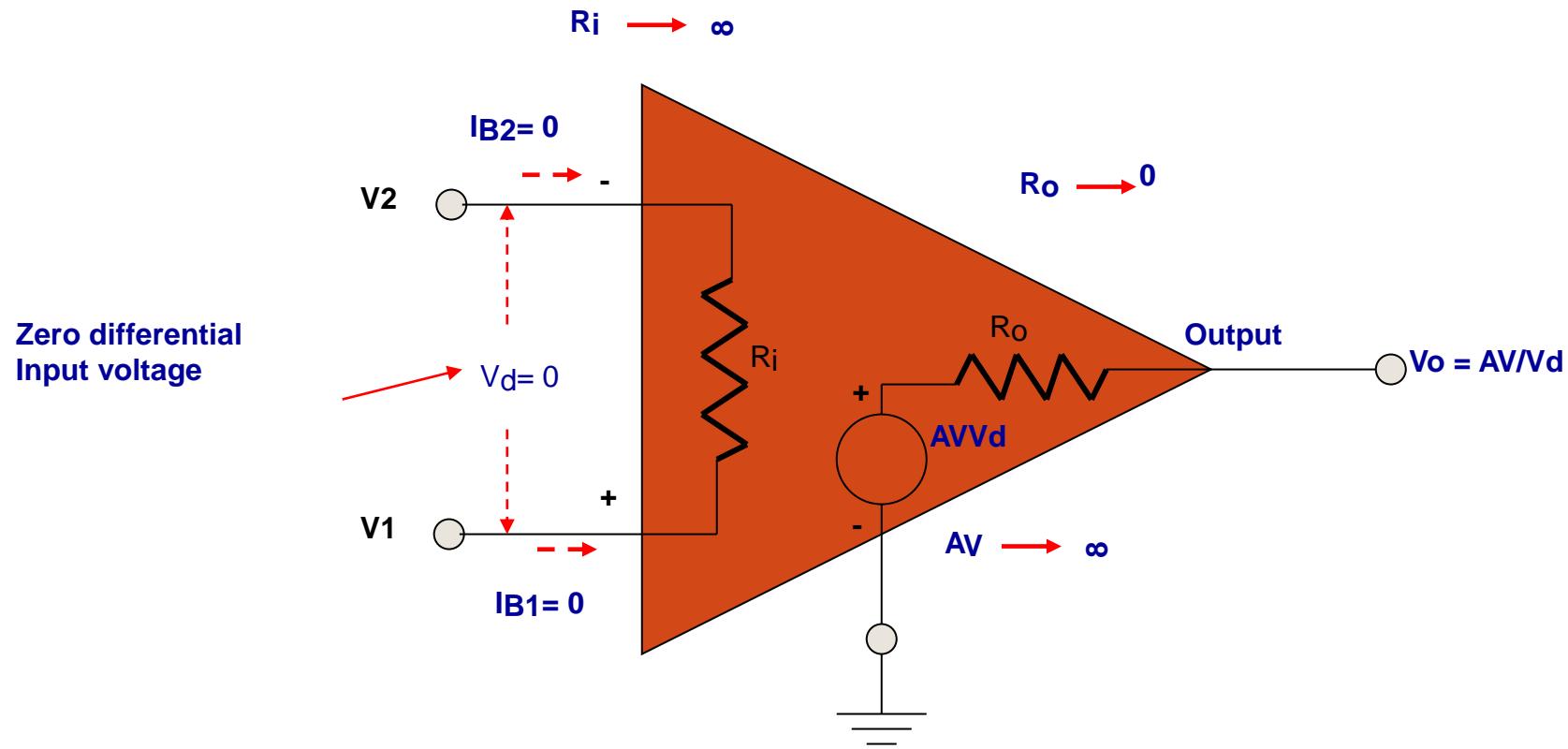
Important characteristics of Op-Amp

1. Infinite voltage gain ($A_v \rightarrow \infty$)

the open loop gain of an ideal OP-AMP is denoted by A_v . It is the differential voltage gain and its value for an ideal OP-AMP is infinite.

$$V_o = A_v * V_d$$

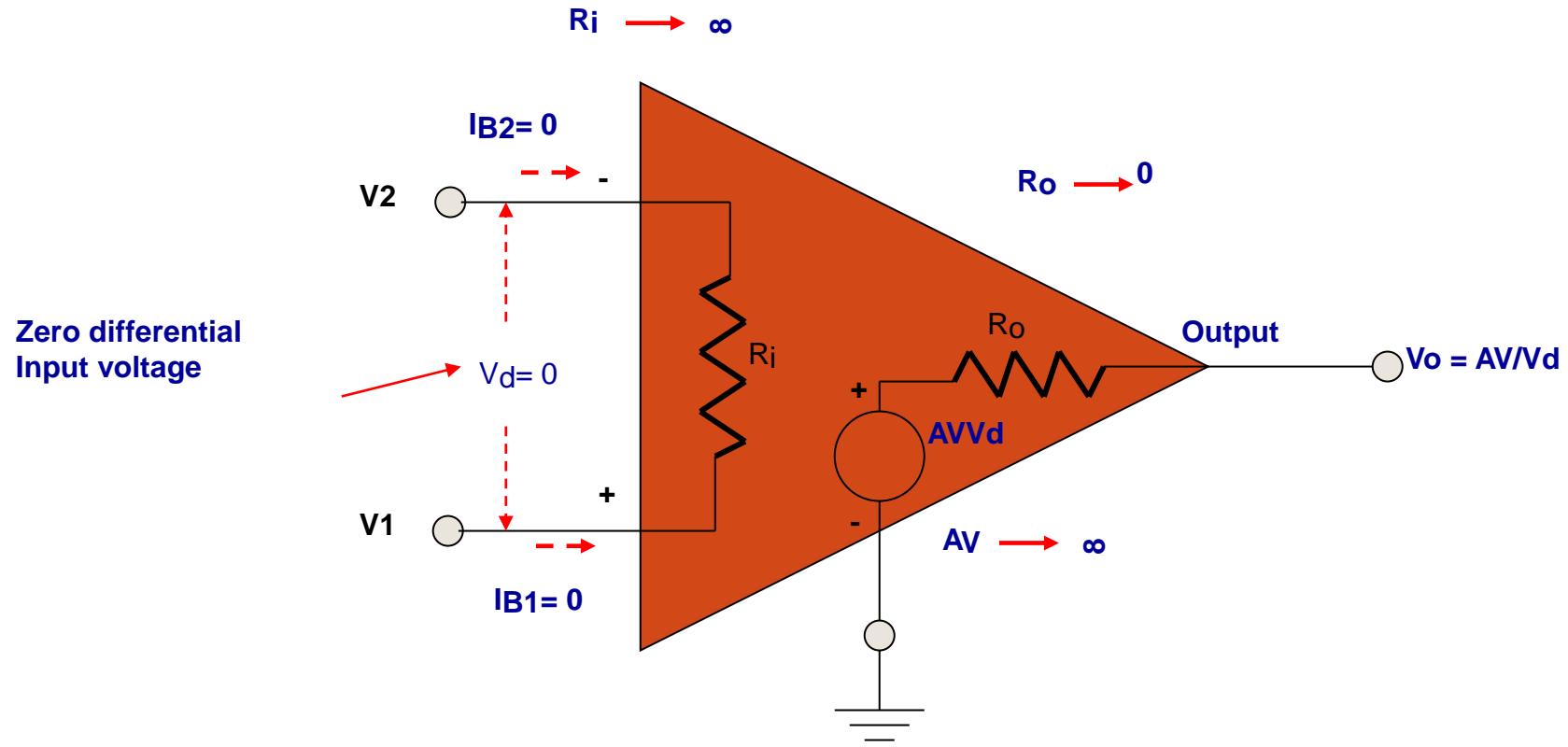
The ideal OP-AMP



2. Infinite input resistance ($R_i \rightarrow \infty$)

the input resistance R_i of an ideal OP-amp is infinite. Due to this, the current flowing in each input terminal will be zero. **$I_{B1}=0$ $I_{B2}=0$** due to infinite input resistance, almost any source can drive it and there is no loading of the source.

The ideal OP-AMP

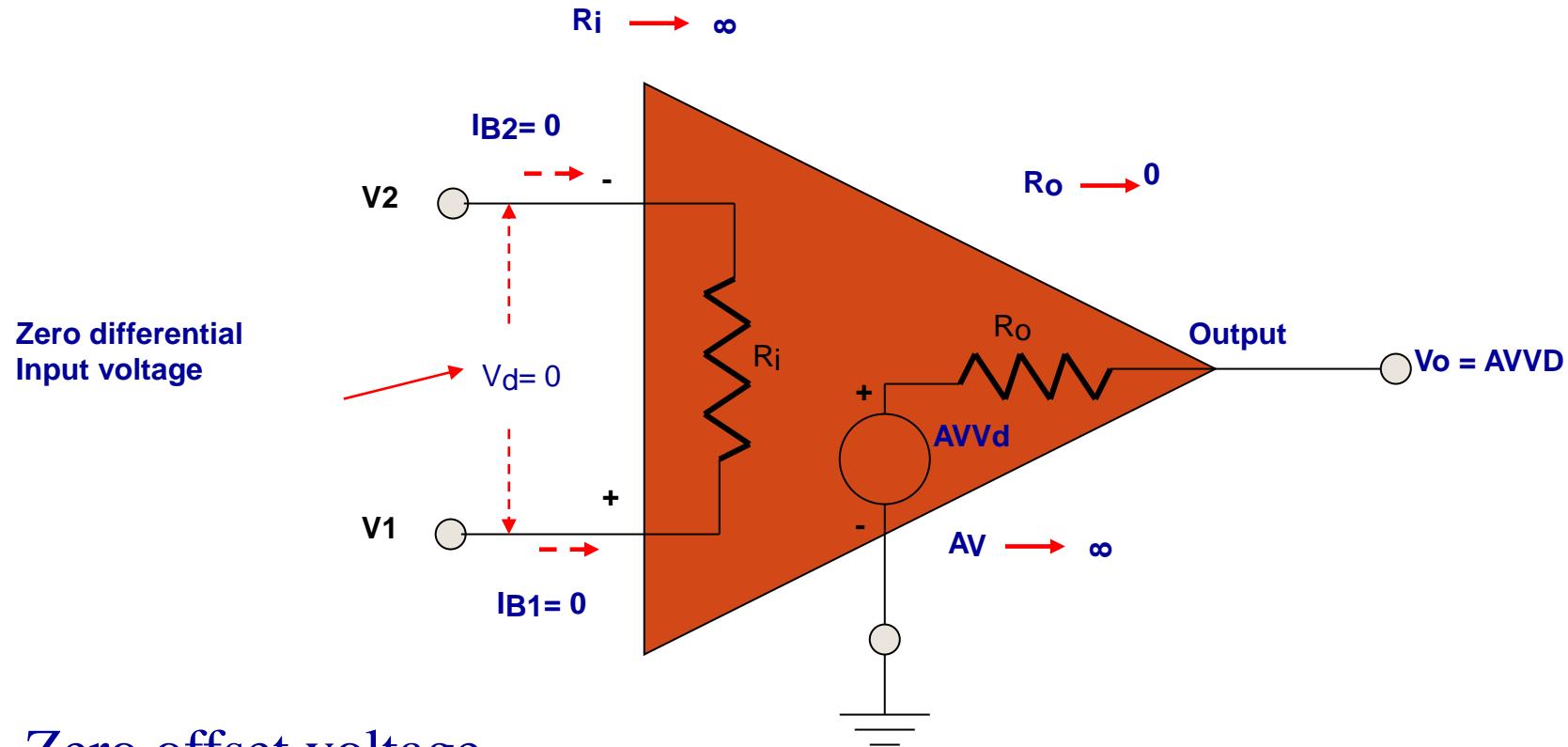


3. Zero output resistance ($R_o = 0$)

the output resistance R_o of an ideal OP-amp is zero.

Due to this, the ideal Op-amp can handle infinite number of other devices.

The ideal OP-AMP



4. Zero offset voltage

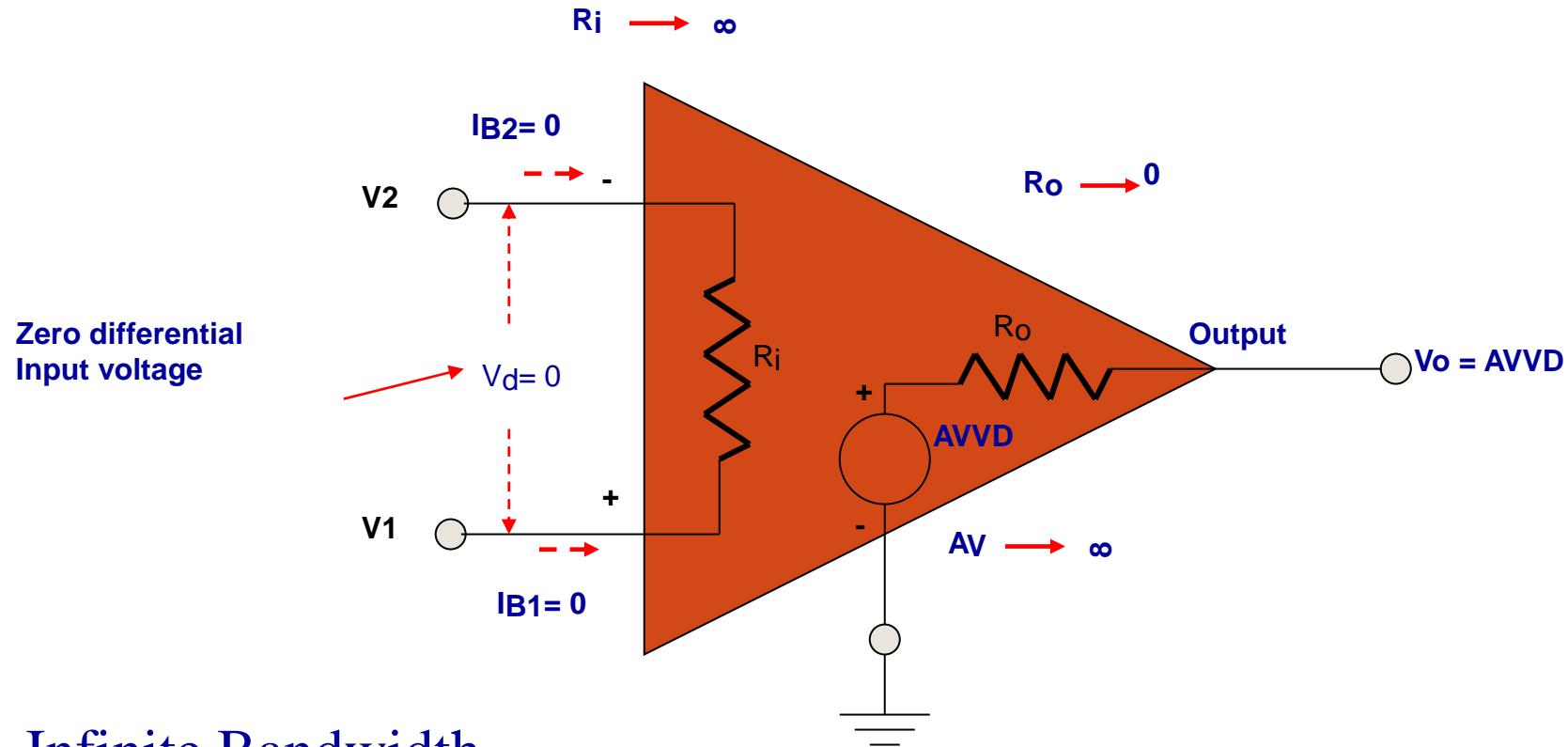
in practical Op-amps a small output voltage is present even though both the inputs V_1 ad V_2 are having a zero value.

This voltage is called as the offset voltage.

for ideal Op-amp the offset voltage is zero.

That means output voltage is zero when input voltage is zero.

The ideal OP-AMP



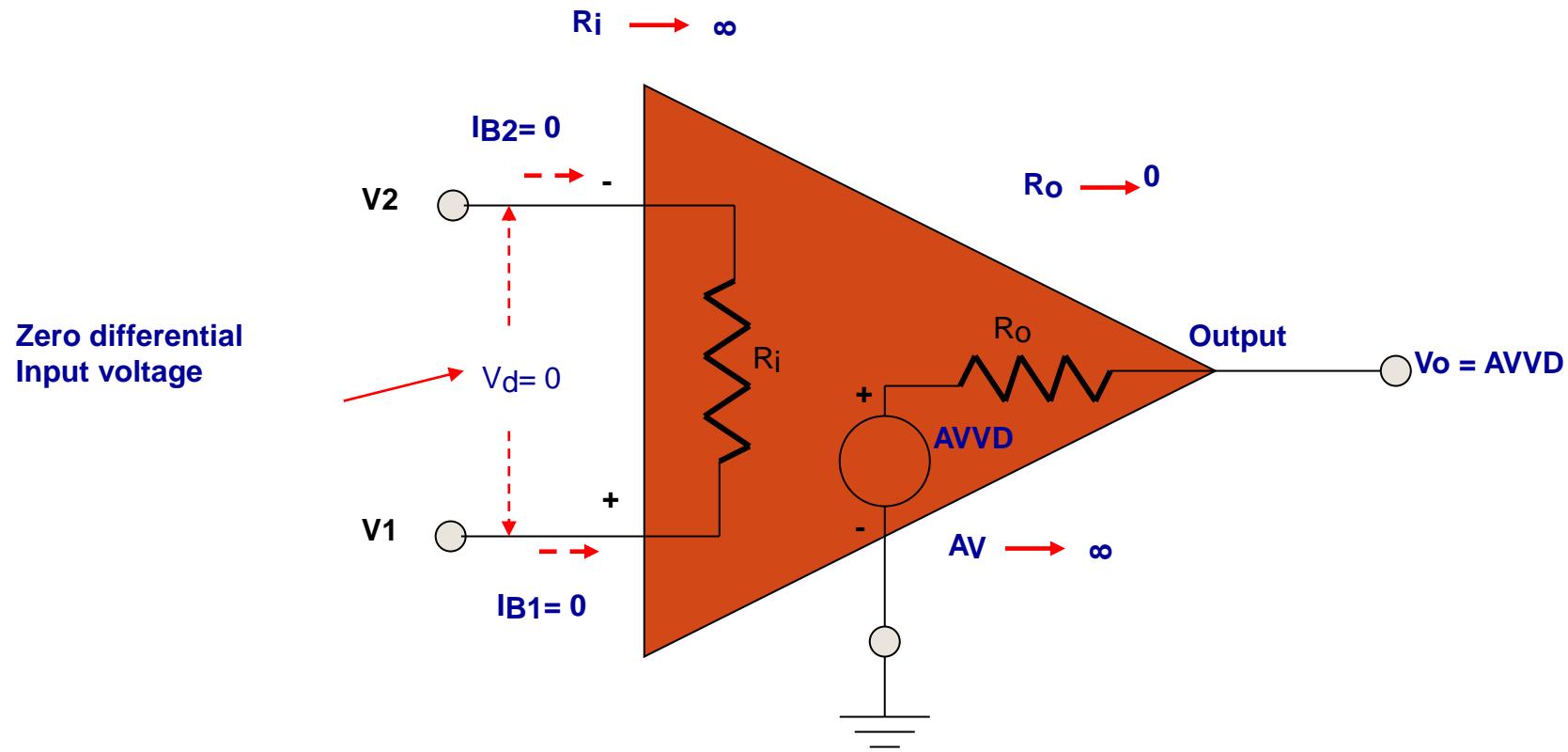
5. Infinite Bandwidth

Bandwidth of an amplifier is the range of frequencies over which all the signal frequencies are amplified almost equally.

The bandwidth of an ideal Op-amp is infinite. So it can amplify any frequency from zero to infinite hertz.

Thus the gain of an ideal amplifier is constant from zero to infinite hertz.

The ideal OP-AMP

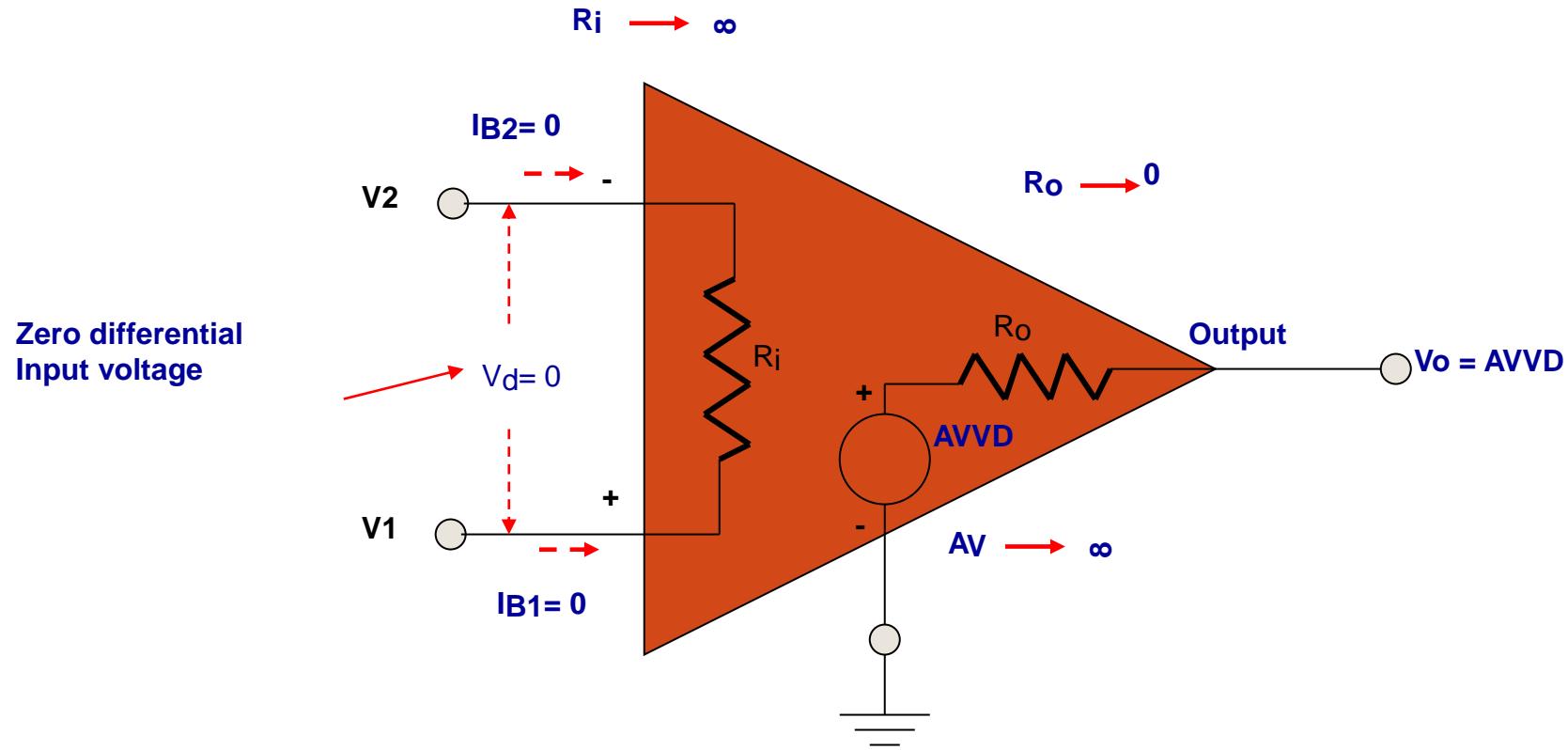


6. Infinite CMRR

for an Op-amp, the common mode rejection ratio (CMRR) is defined as the ratio of differential gain to common mode gain. CMRR is infinite for the ideal Op-amp.

Thus the output voltage corresponding to the common mode noise is zero.

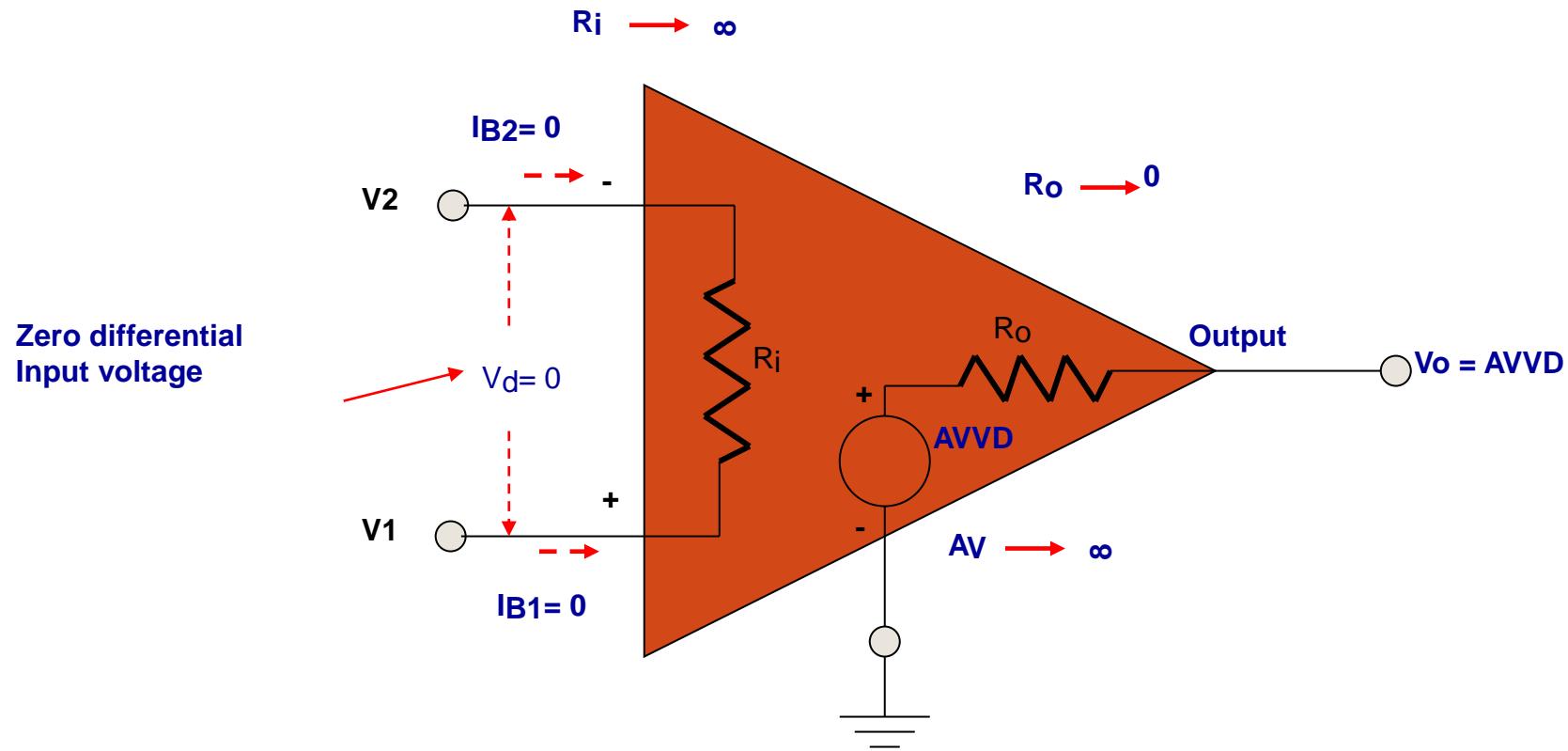
The ideal OP-AMP



7. Infinite slew rate.

the slew rate of an ideal Op-amp is infinite so that the output voltage changes occur simultaneously with the input voltage changes.

The ideal OP-AMP



8. Zero power supply rejection ratio (PSRR).

PSRR is a parameter which specifies the degree of the dependence of the Op-amp output on the changes in power supply output. For an ideal Op-amp, $PSRR = 0$. that means the output voltage does not change due to fluctuation in supply voltage

The practical characteristics of OP-AMP

- Input offset voltage (V_{IOS}) :
- Ideally, for a zero input voltage, the Op-amp output voltage should be zero.
- But practically it is not so. This is due to the unavoidable unbalances inside the Op-amp, specially the unbalances in its differential input stage.
- So we have to apply a small differential voltage at the input of the Op-amp to make the output voltage zero, which is called **input offset voltage**.
- The input offset voltage is denoted by V_{ios} .
- This input offset voltage is normally in a few mV range.
- The value of input offset voltage is temperature dependent.

The practical characteristics of OP-AMP

- Input bias current (I_B) :
- Input bias current I_B is the average of the currents flowing into the two input terminals of the Op-amp.
- Ideally the currents I_{B1} and I_{B2} must be zero.
- But for practical Op-amp they do exist due to the finite value of input resistance R_i . Due to slight difference in the characteristics of the transistors used in the input stage of an Op-amp, the two currents I_{B1} and I_{B2} are not equal.
- The maximum value of I_B is 50nA for IC 741.
- It can reduced to pA level using FET Op-amps.
- The value of input bias current is temperature dependent.

The practical characteristics of OP-AMP

- Input offset current (I_{IOS}) :
- The algebraic difference between the currents flowing into the inverting and non-inverting terminals of Op-amp is called as “input offset current”.
- $$I_{IOS} = \left| I_{B1} - I_{B2} \right|$$
- Ideally, the input offset current must be zero and practically it should be as small as possible.
- The input offset current exists due to the unequal currents I_{B1} and I_{B2} flowing into the input terminals of the Op-amp.
- The input offset currents for the Op-amp is few tens or hundreds of nA.
- For IC 741 the maximum input offset current is 6 nA.

The practical characteristics of OP-AMP

- Common mode rejection ratio (CMRR) :
- CMRR of a practical Op-amp is not infinity.
- However it is very high.
- For IC 741 the CMRR is 90 dB or 31622.
- Such high CMRR is helps to reject the common mode signals such as noise successfully.

The practical characteristics of OP-AMP

- Power supply rejection ratio (PSRR) :
- The change in the Op-amps input offset voltage caused by variation in the supply voltage is called as power supply rejection ratio (PSRR).
- It is also called as supply voltage rejection ratio (SVRR) .
- PSRR is expressed either in microvolt per volt or in decibels.

- For IC 741, $\text{PSRR} = 150 \mu\text{V/V}$

- **Slew rate :**
- Slew rate is defined as the maximum rate of change of output voltage per unit time and it is expressed in volts/microseconds.
- **Importance of Slew rate :**
- Slew rate decides the capability of Op-amp to change its output rapidly, hence it decides the highest frequency of operation of a given Op-amp.
- Slew rate changes with change in voltage gain. Therefore it is generally specified at unit gain.
- Slew rate should be ideally infinite and practically as high as possible.
- Slew rate of IC 741 op-amp is only **0.5 V/ μ S**

Important characteristics of OP-AMP IC 741

Sr. No.	Characteristics	Value for IC 741	Ideal value
1	Input resistance R_i	$2 \text{ M}\Omega$	∞
2	Output resistance R_o	75Ω	0
3	Voltage gain A_v	2×10^5	∞
4	Bandwidth BW	1 MHz	∞
5	CMRR	90 dB	∞
6	Slew rate S	$0.5 \text{ V}/\mu\text{s}$	∞
7	Input offset voltage	2 mV	0
8	PSRR	$150 \mu\text{V}/\text{V}$	0
9	Input bias current	50 nA	0
10	Input offset current	6 nA	0

Close loop configuration of OP-AMP

- In the closed loop configuration some kind of “feedback” is introduced in the circuit.
 - A part of output is returned back or fed back to the input.
-
- **Types of feedback**
 - Positive feedback or Regenerative feedback
 - Negative feedback or Degenerative feedback.

Positive feedback or regenerative feedback

- If the feedback signal and the original input signal are in phase with each other then it is called as the positive feedback.
- Positive feedback is used in the application such as **“Oscillators” and Schmitt triggers or regenerative comparators.**

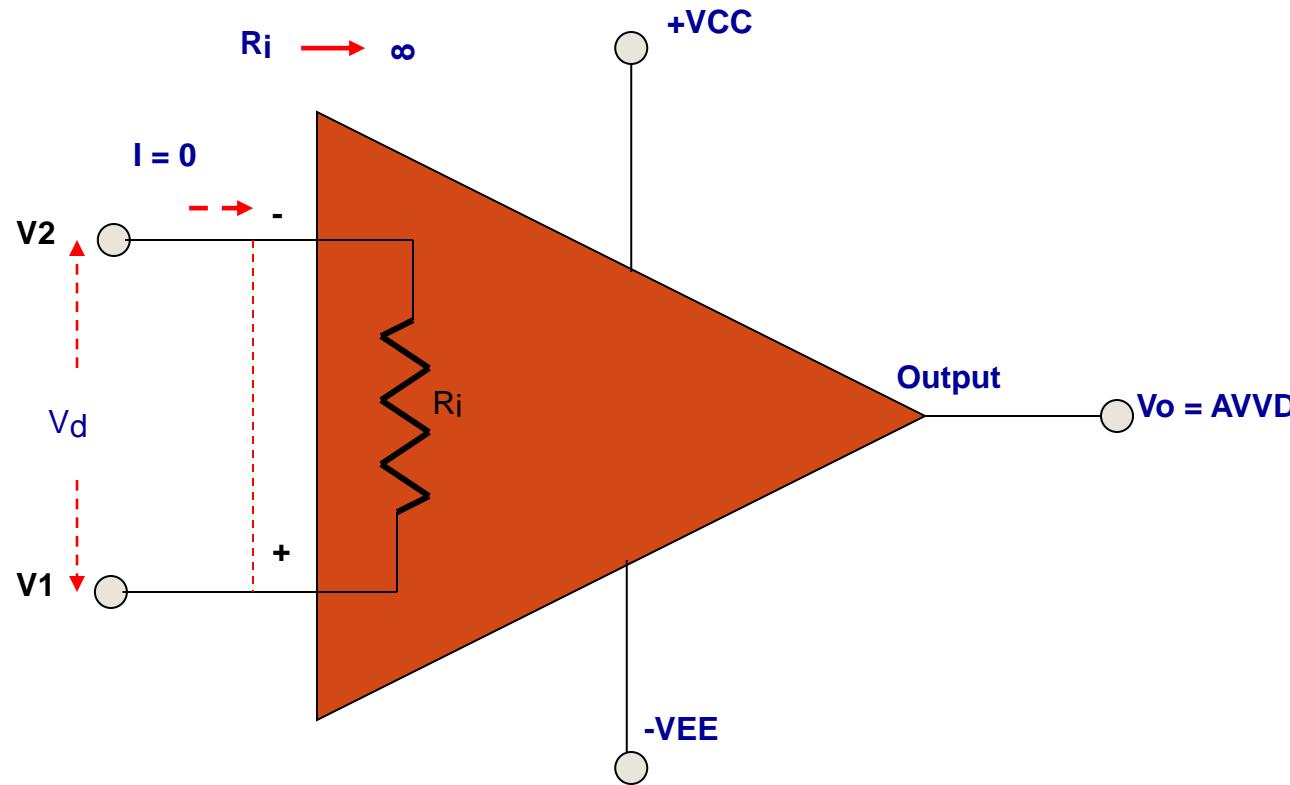
Negative feedback or Degenerative feedback

- If the signal is fed back to the input and the original input signal are 180^0 out of phase, then it is called as the negative feedback.
- In the application **of Op-amp as an amplifier**, the negative feedback is used.

Concept of virtual short and virtual ground

- According to **virtual short** concept, the **potential difference** between the two input terminals of an OP-amp is almost zero.
- Both the input terminals are approximately at the same potential.

Virtual short

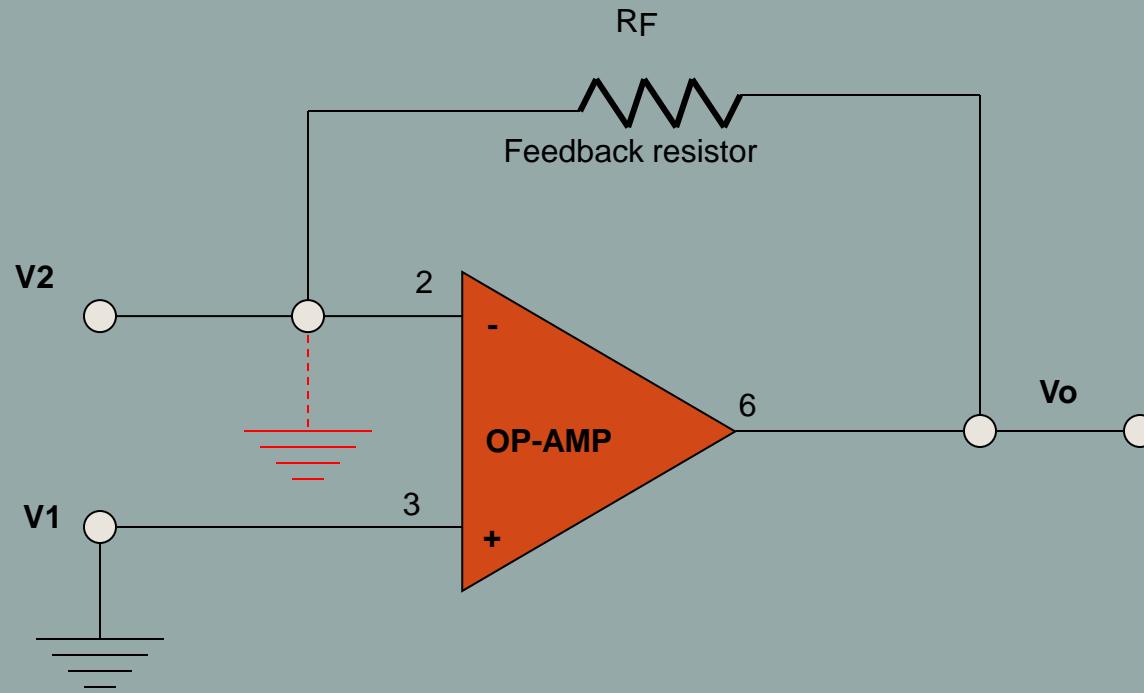


The input impedance R_i of an Op-amp is ideally infinite.

Hence current “I” flowing from one input terminal to the other will be zero.

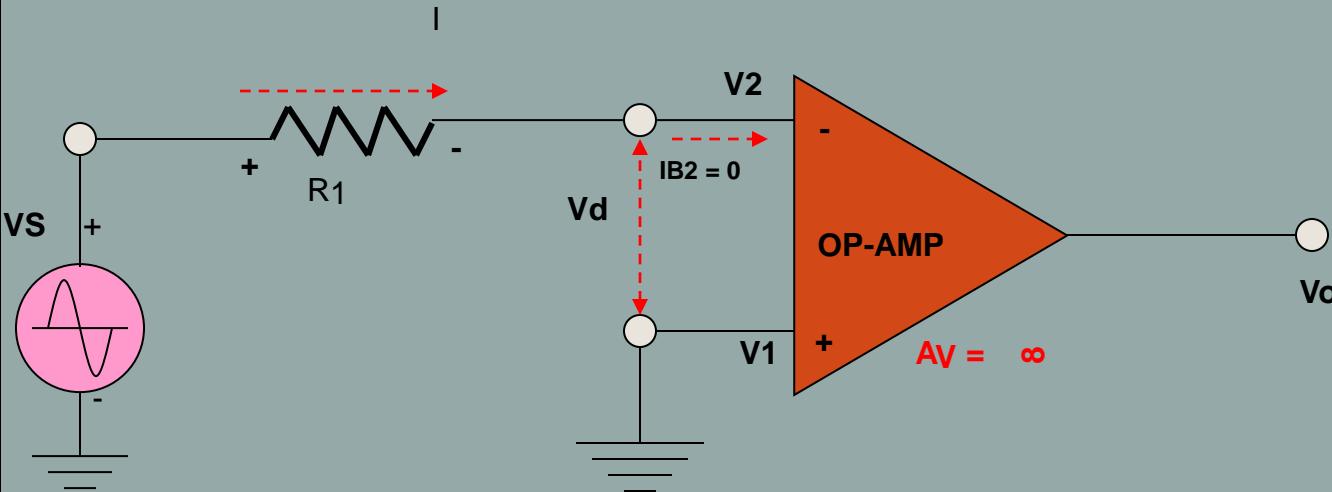
Thus the voltage drop across R_i will be zero and both the input terminals will be at same potential, in other words they are virtually shorted to each other.

Virtual ground

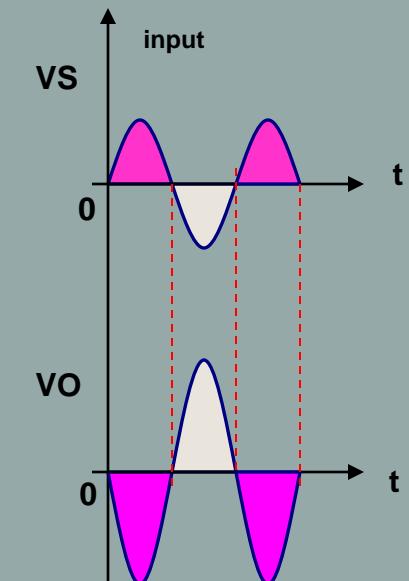
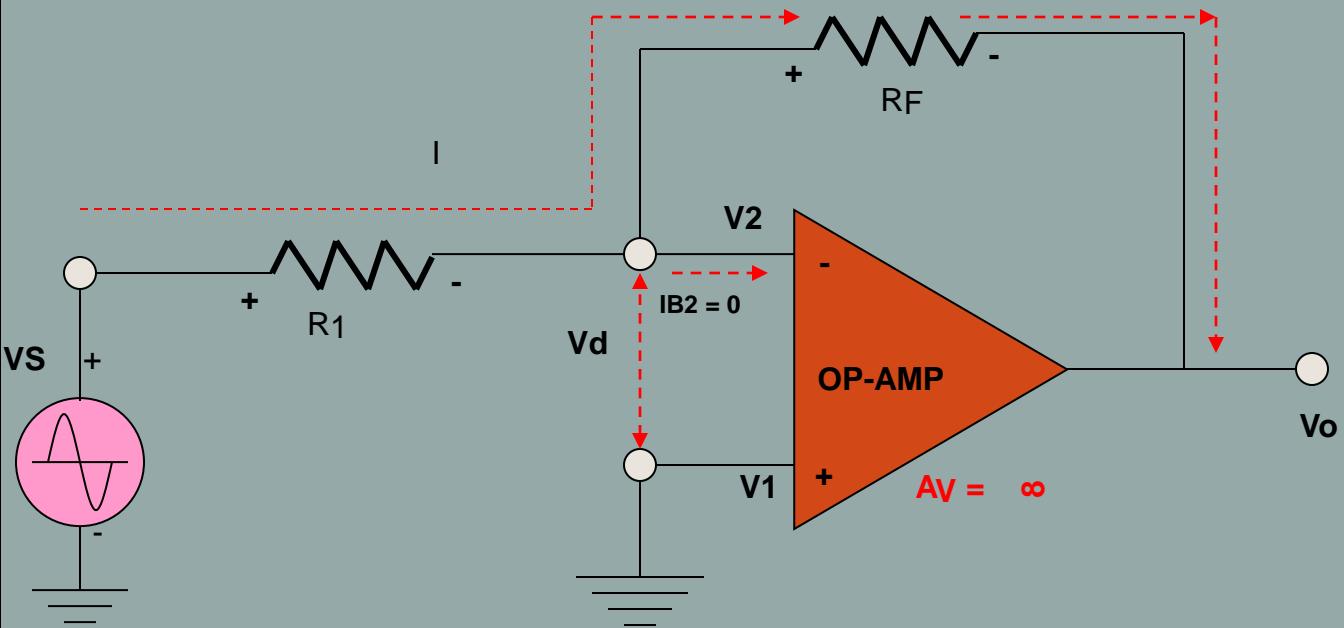


If non inverting terminal (+) of Op-amp is connected to ground as shown in figure, then due to “virtual short” existing between the two input terminals, the inverting terminal will also be at ground terminal.
Hence it is said to be “ virtual ground”

The Inverting Amplifier



The Inverting Amplifier



$$V_o = A_V \cdot V_d$$

$$V_O = A_v \times V_d$$

$$\text{therefore } V_d = V_O / A_v$$

Where A_v = open loop gain of Op-Amp

As we know A_v of an open loop Op-Amp ∞

$$\text{therefore } V_d = V_O / \infty = 0$$

$$V_d = 0$$

$$\text{But } V_d = V_1 - V_2$$

$$V_1 - V_2 = 0$$

$$V_1 - V_2 = 0$$

As the non inverting terminal is connected to ground,

V1 = 0 substituting this Value in above equation we get **V2 = 0**

Thus V2 is at virtual ground

Since the input resistance $R_i = \infty$, the current flowing into the Op-amp will be zero. Therefore the current “I” that passes through R_1 will also pass

As voltage $V_2 = 0$,

The input voltage V_S is voltage across R_1 and Voltage across R_F is output voltage.

The input voltage V_S is given by

$$V_S = I \times R_1 \text{ and}$$

Expression for the closed loop voltage gain (AVF)

The input voltage V_S is given by

$$V_S = I \times R_1 \text{ and}$$

And the output voltage V_O given by

$$V_O = - I \times R_F$$

Closed loop gain AVF is given by

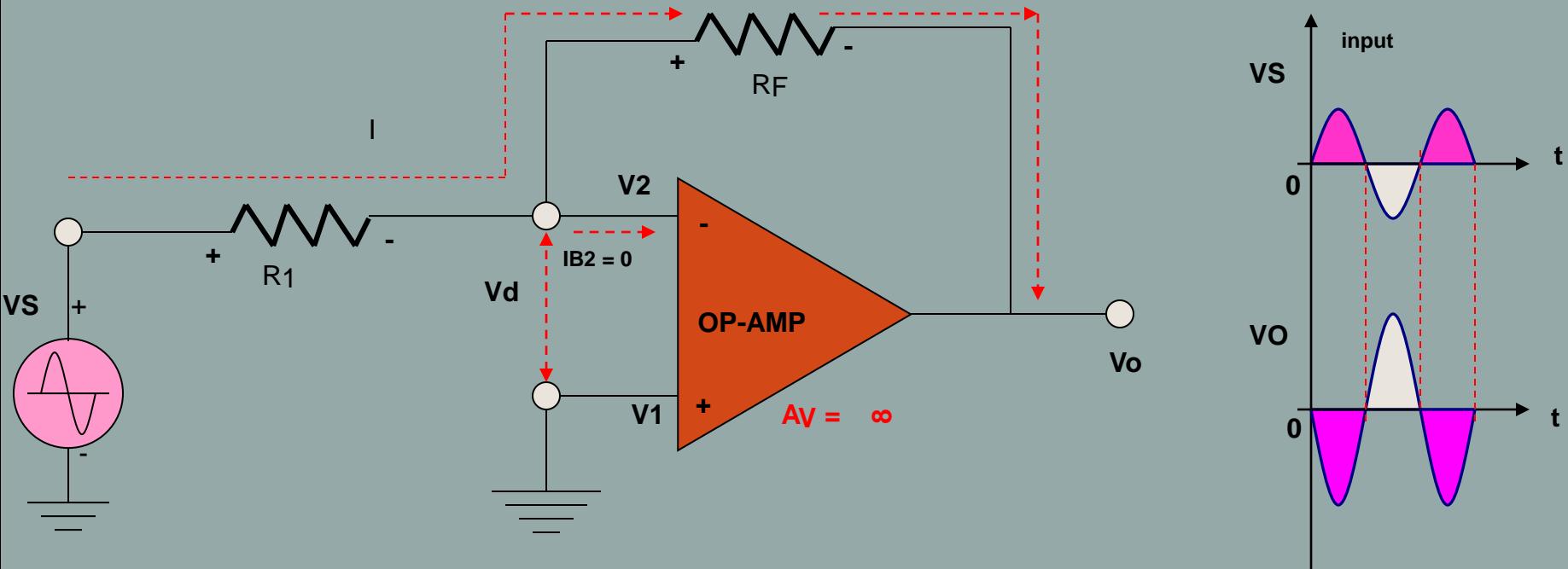
$$AVF = V_O / V_S$$

Substituting the expression for V_O and V_S we get

$$AVF = - R_F / R_1$$

$$AVF = - R_F / R_1$$

The Inverting Amplifier



Expression for the closed loop voltage gain (AVF)

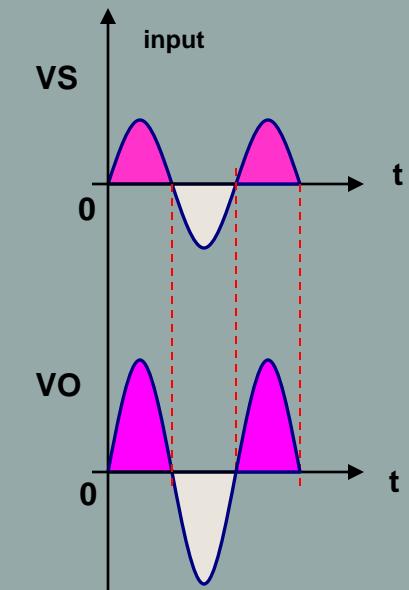
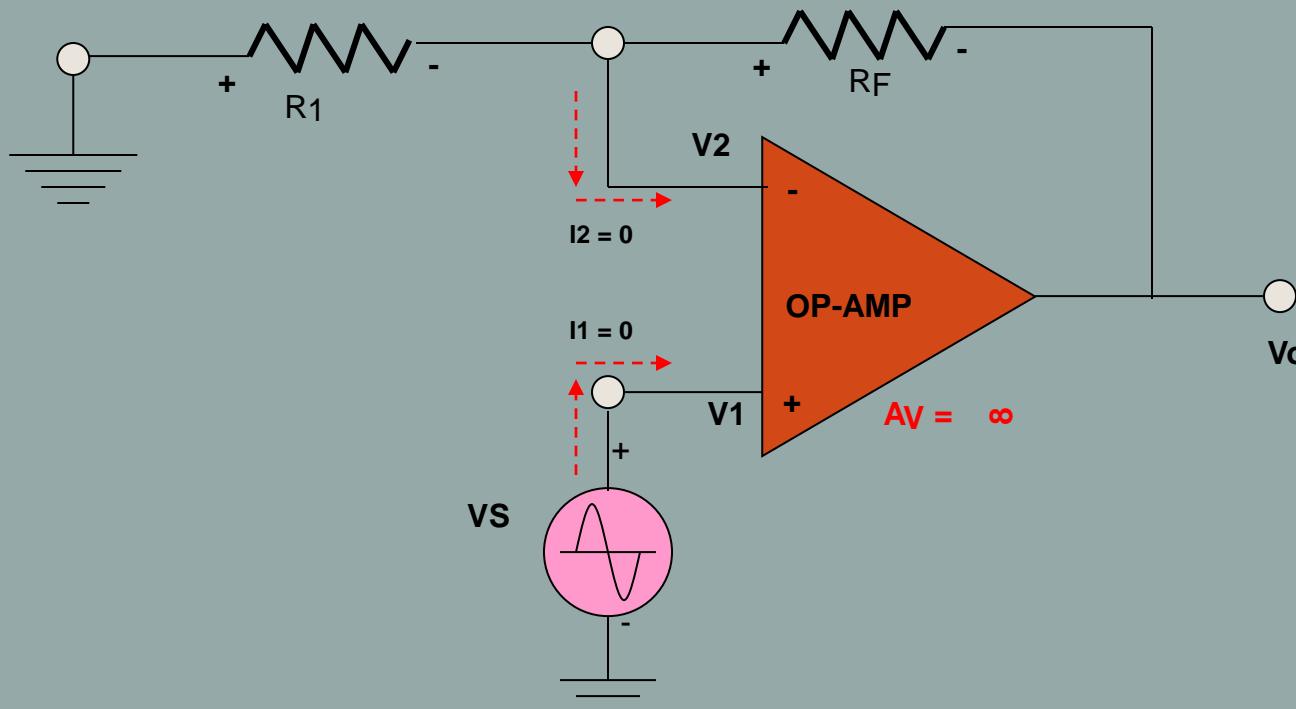
$$\text{AVF} = - \frac{R_F}{R_1}$$

The negative sign indicates that there is a phase shift of 180° between the input and output voltages.

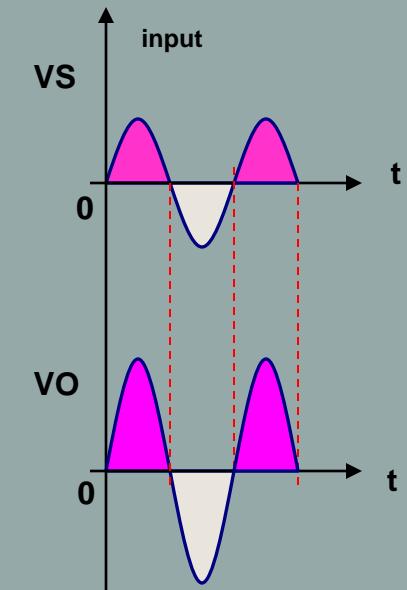
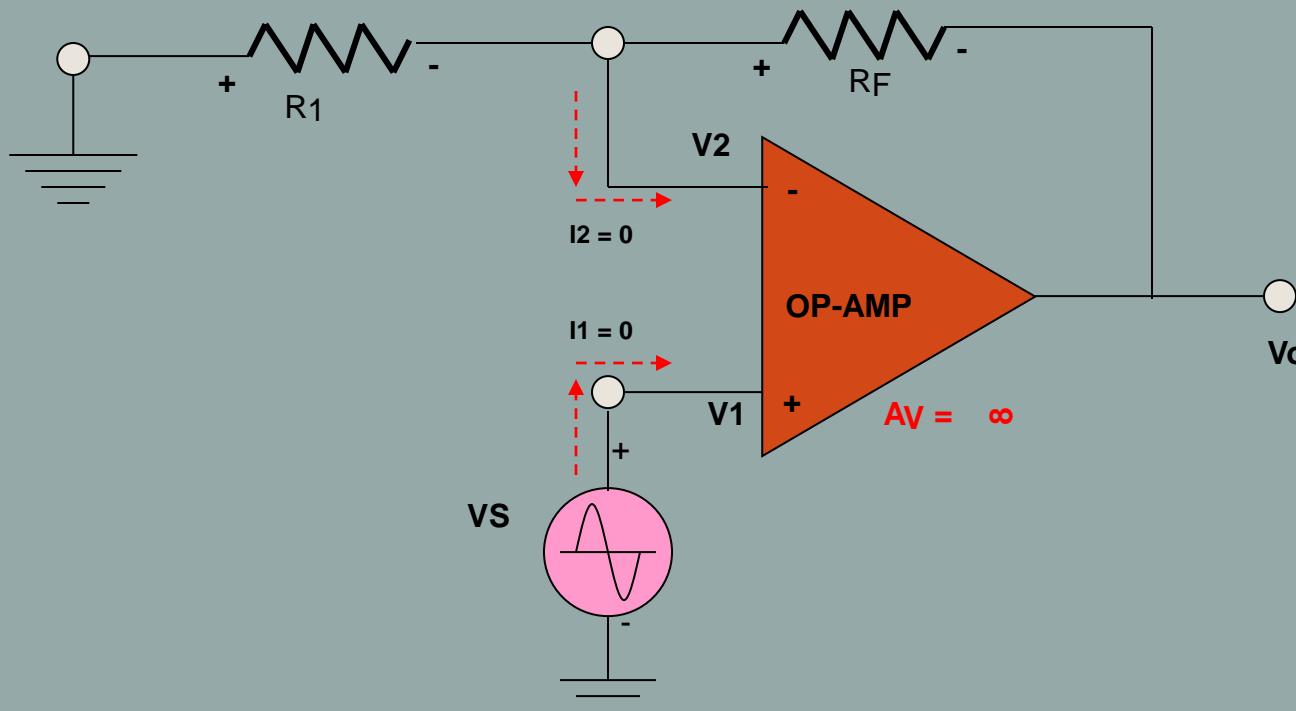
Conclusion from the expression for A_{VF}

- The value of closed loop voltage gain A_{VF} does not depend on the value of open loop voltage gain A_v .
- Value of A_{VF} can be very easily adjusted by adjusting the values of the resistors R_F and R_1 .
- Generally the feedback resistor R_F is a potentiometer to adjust the gain to its desired value.
- The output is an amplified inverted version of input.

The Non-Inverting Amplifier



The Non-Inverting Amplifier



As input impedance of ideal Op-amp is infinite
Therefore the current entering into both the input terminals
of Op-amp will have zero values. ($I_1 = I_2 = 0$)

Expression for the closed loop voltage gain (AVF)

As input impedance of ideal Op-amp is infinite

Therefore the current entering into both the input terminals of Op-amp will have zero values. ($I_1 = I_2 = 0$)

Therefore voltage across R_1 is given by

$$V_2 = \frac{R_1}{R_F + R_1} \times V_o$$

As per the virtual concept

$$V_1 = V_2 = V_S$$

Therefore

$$V_S = \frac{R_1}{R_F + R_1} \times V_o$$

Therefore the closed loop voltage gain AVF is given as :

$$AVF = \frac{V_o}{V_S} = \frac{R_1 + R_F}{R_1}$$

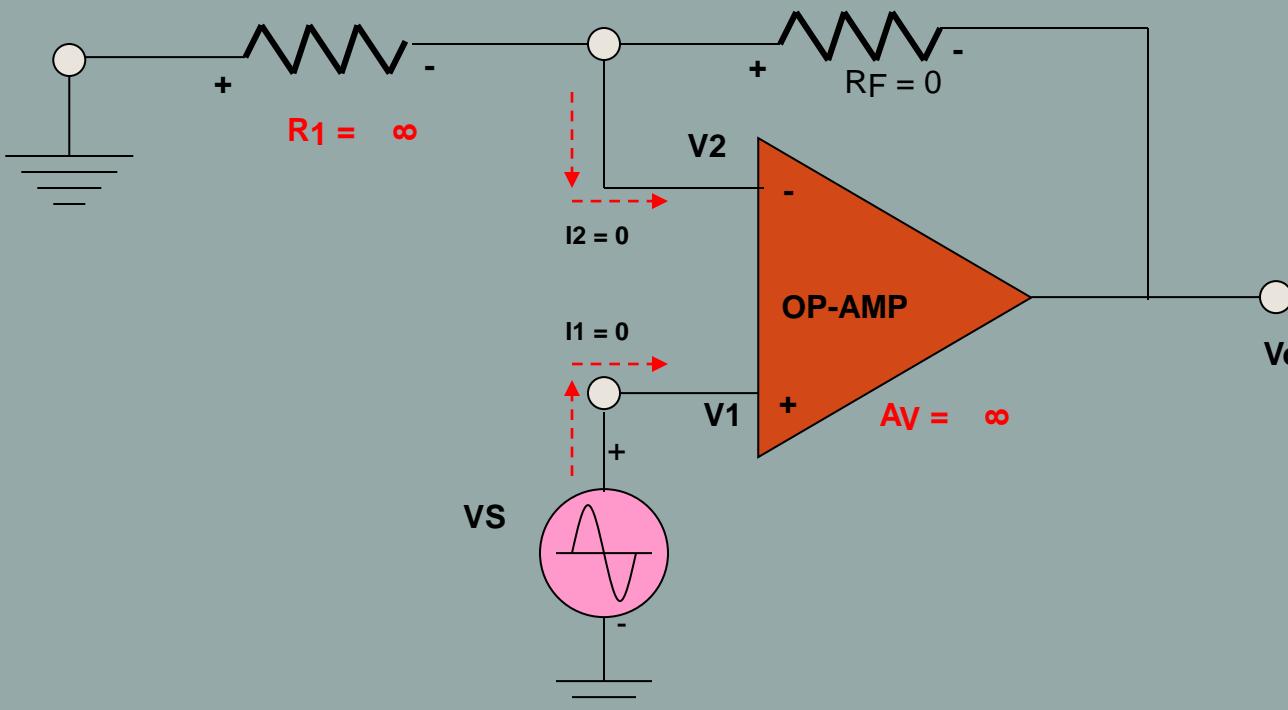
$$AVF = 1 + R_F / R_1$$

Conclusion from the expression for A_{VF}

- The positive sign of equation indicates that the input and output are in phase with each other.
- The closed loop control gain is always greater than unity.
- A_{VF} is adjustable and its value can be adjusted by varying the values of R_F and R_1 .
- Generally a variable resistor is used in place of R_F to adjust the closed loop gain to its desired value.
- A_{VF} is independent of the open loop gain of Op-amp. It depends only on the values of R_F and R_1

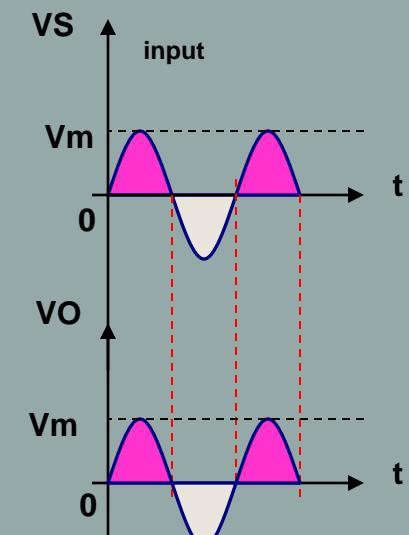
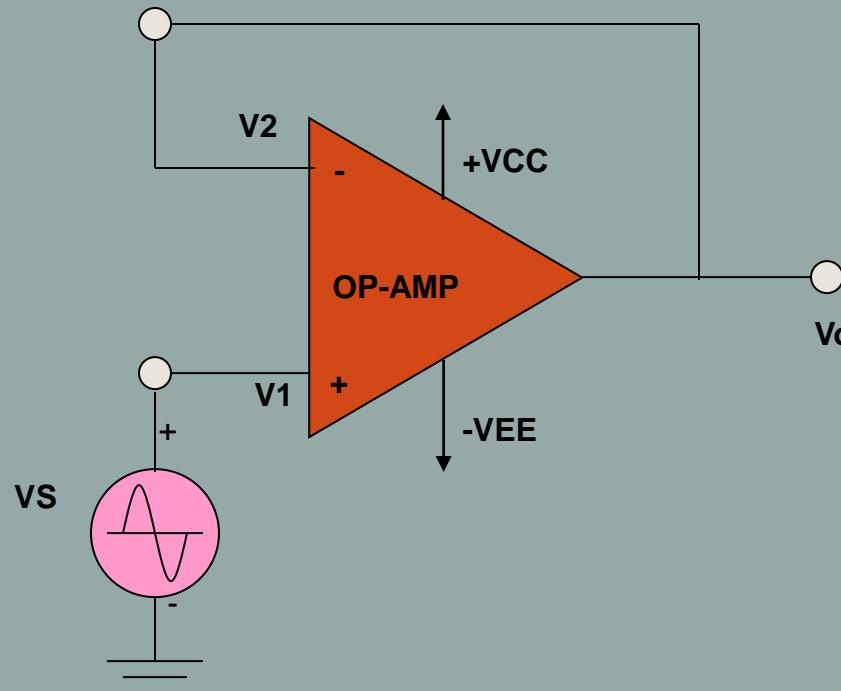
Parameter	Inverting Amplifier	Non Inverting Amplifier
Voltage Gain	$A_{VF} = -R_F/R_I$	$A_{VF} = 1 + \frac{R_F}{R_I}$
Phase Relation between input and output	180° out of phase	In Phase
Value of Voltage Gain	Can be Greater than, Less than or equal to unity	Always greater than or equal to unity
Input Resistance	Very large	Equal to R _i
Application	Summing amplifier ,Inverter , Integrator, Differentiator ,	Voltage Follower
Diagram		

The Voltage follower (unity gain buffer)



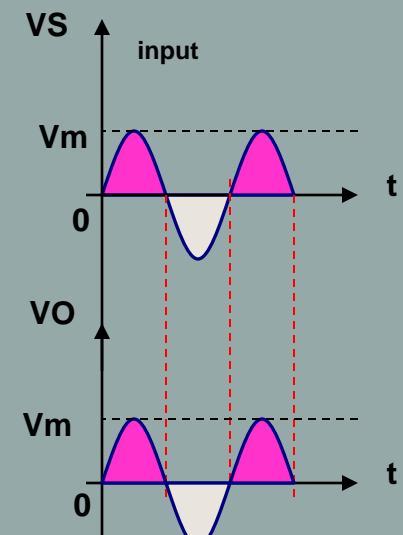
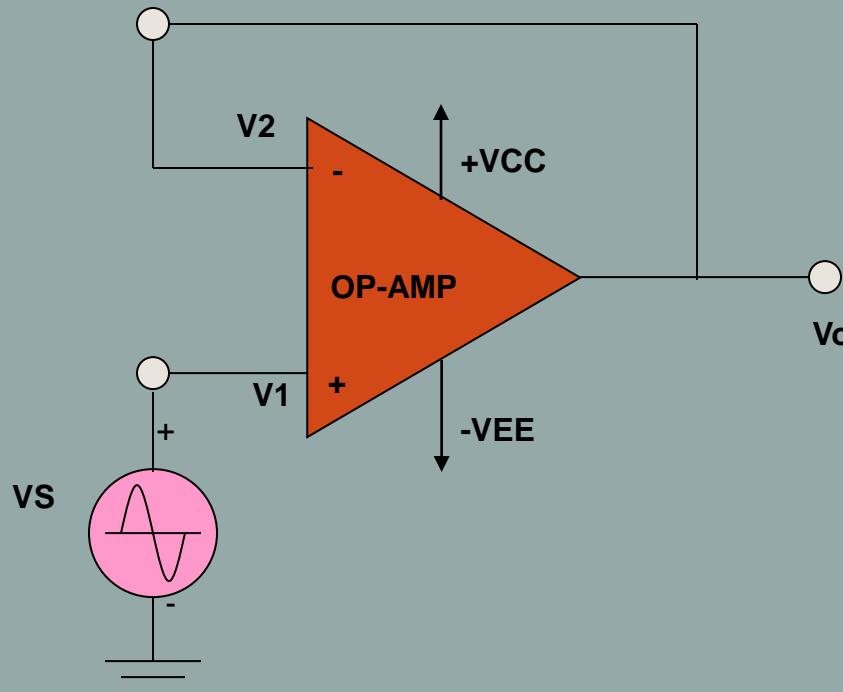
When R_1 is infinite and $R_F = 0$ the non-inverting amplifier gets converted into a voltage follower or unity gain.

The Voltage follower (unity gain buffer)



When R_1 is infinite and $R_F = 0$ the non-inverting amplifier gets converted into a voltage follower or unity gain.

The Voltage follower (unity gain buffer)



Expression for the closed loop voltage gain (AVF)

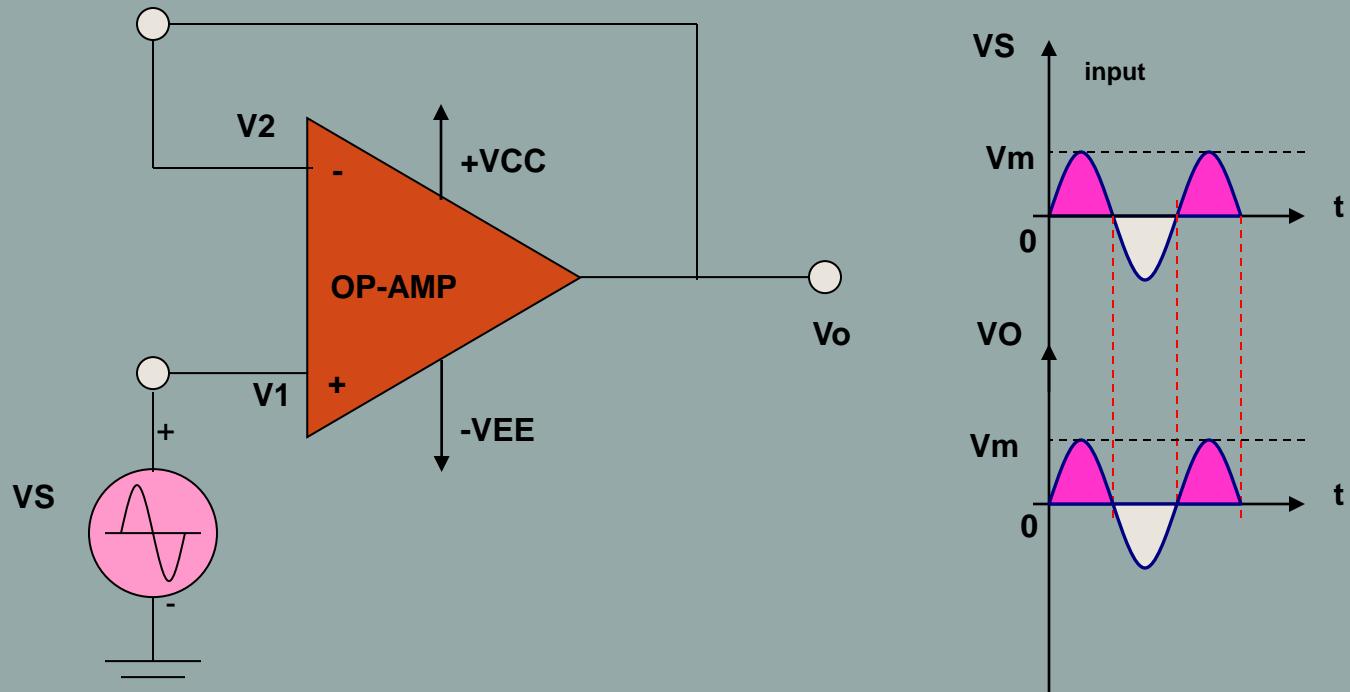
Therefore the closed loop voltage gain AVF is given as :

$$AVF = 1 + RF / R1$$

Substitute the values of $RF = 0$ and $R1 = \infty$

$$AVF = 1$$

The Voltage follower (unity gain buffer)

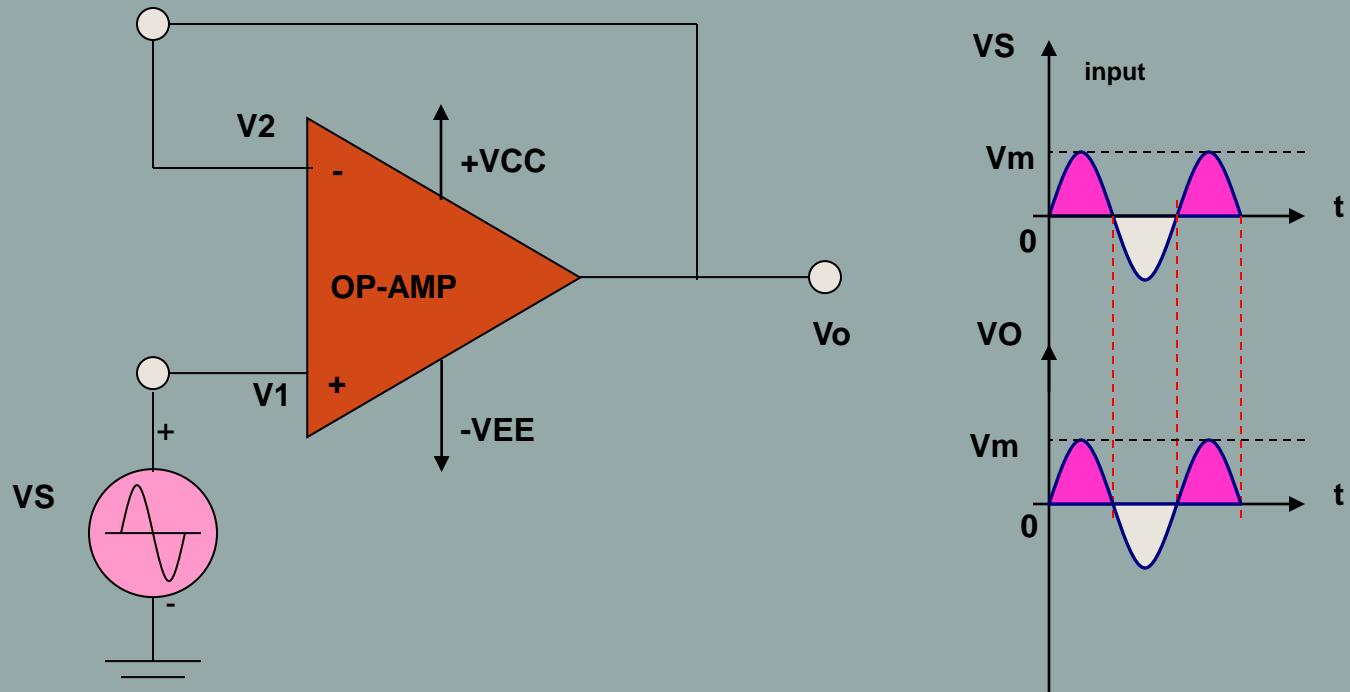


Expression for the closed loop voltage gain (AVF)

$$AVF = 1$$

Therefore the output voltage will be equal to and in phase with the input voltage, as shown in figure. Thus the voltage follower is a non-inverting amplifier with a voltage gain of unity.

The Voltage follower (unity gain buffer)

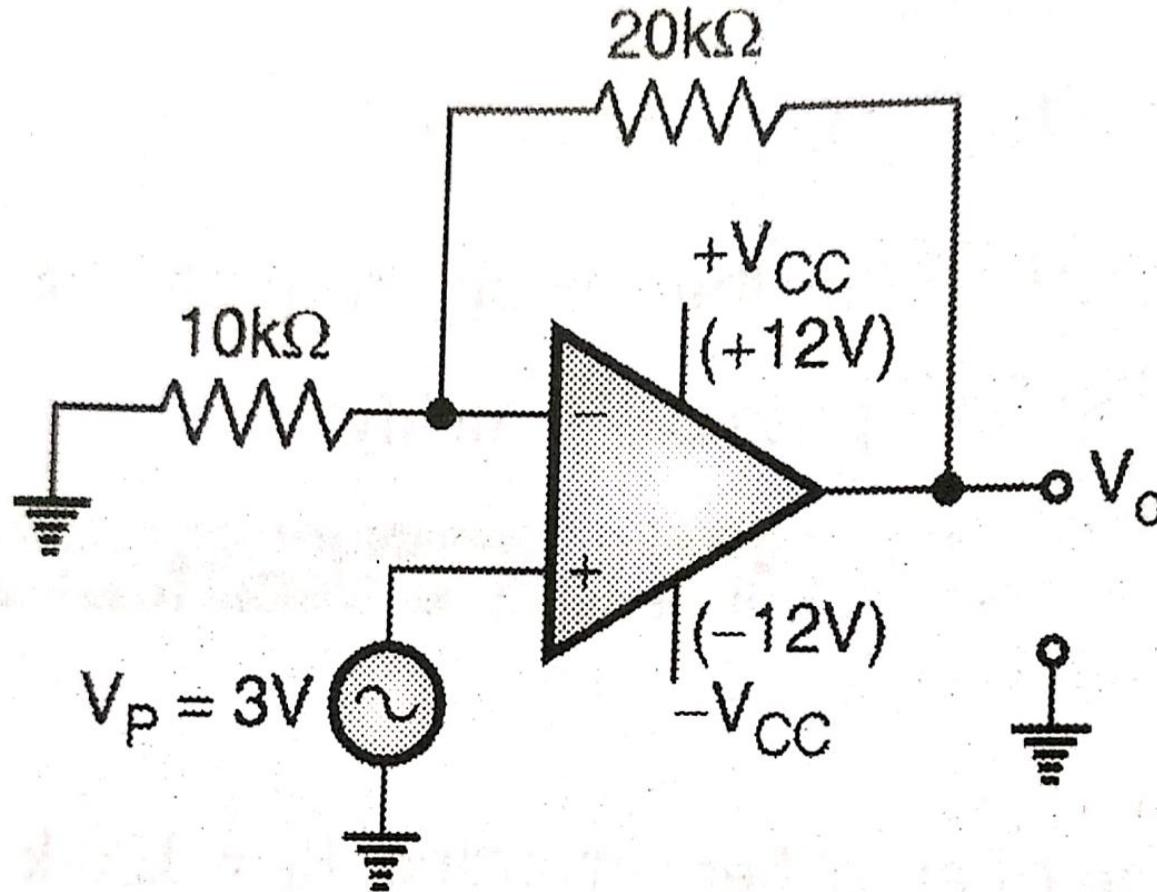


Features of voltage follower circuit

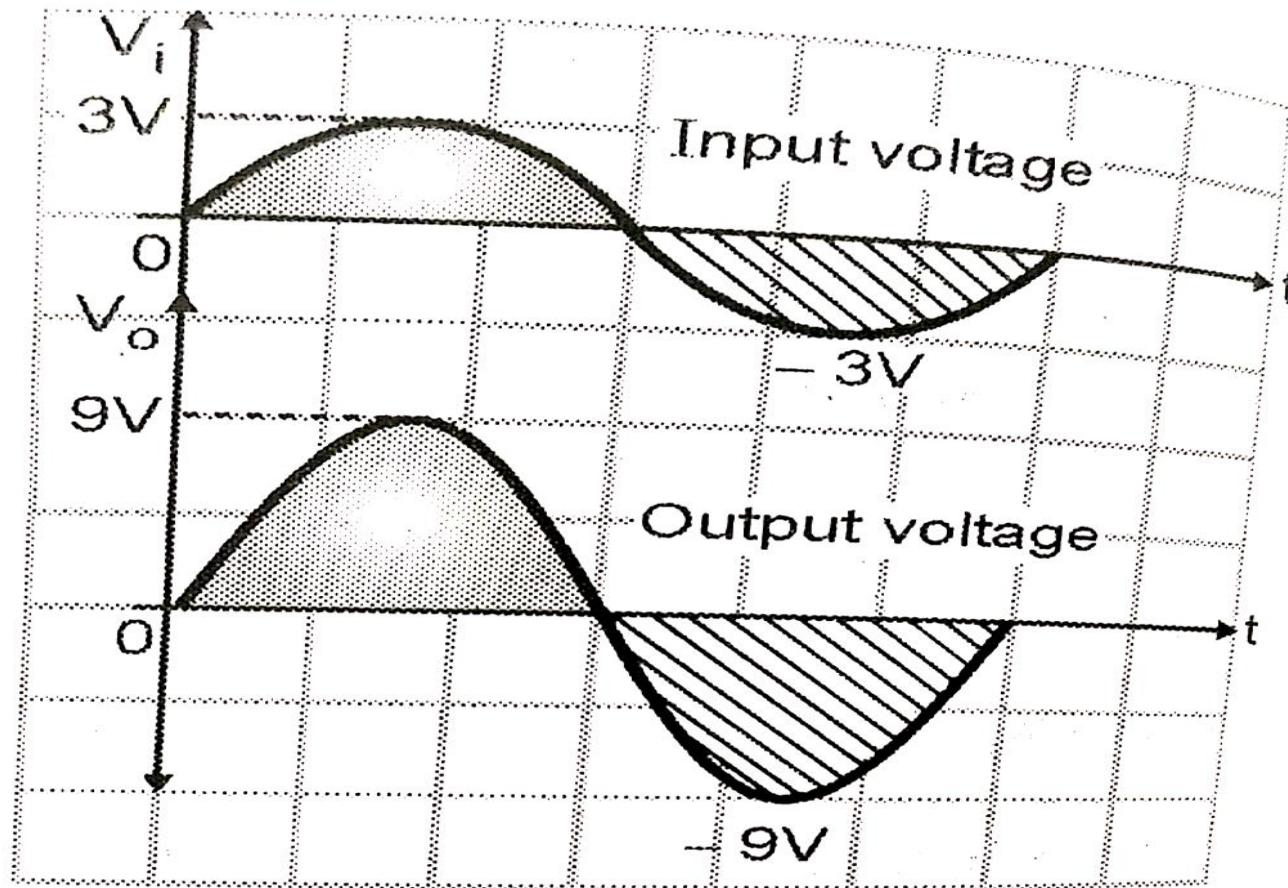
- Closed loop gain equal to 1 i.e. output is equal to input with no phase shift.
- Very high input impedance
- Very low output impedance
- Large bandwidth.

Numerical 1.

Calculate output voltage V_o of Op-amp circuit shown in fig.
Draw Input & output waveforms.



SOLUTION



Numerical 2.

An op-amp is used in non-inverting mode with $R_1 = 1 \text{ k}\Omega$, $R_F = 10 \text{ k}\Omega$, $V_{CC} = \pm 12 \text{ V}$.

Calculate the output voltage for the following inputs : 1. $V_{in} = 100 \text{ mV}$ 2. $V_{in} = 5 \text{ V}$.

Solution

Soln. :

1. Gain of the non-inverting amplifier is $A_{VF} = 1 + \frac{R_F}{R_I}$

$$\therefore A_{VF} = 1 + \frac{10}{1} = 11$$

2. Output for $V_{in} = 100 \text{ mV}$

$$V_o = A_{VF} \times V_{in} = 11 \times 100 \text{ mV} = 1100 \text{ mV or } 1.1 \text{ V}$$

3. Output for $V_{in} = 5 \text{ V}$

$$V_o = A_{VF} \times V_{in} = 11 \times 5 = 55 \text{ V}$$

But V_o cannot be higher than $+V_{CC}$.

$$\therefore V_o = \pm 12 \text{ V}$$

Numerical 3.

An op-amp is used in inverting mode with

$R_1 = 1 \text{ k}\Omega$, $R_F = 15 \text{ k}\Omega$, $V_{CC} = \pm 15 \text{ V}$.

Calculate the output voltage for the following

inputs : 1. $V_{in} = 150 \text{ mV}$ 2. $V_{in} = 2 \text{ V}$.

Solution

Output voltage

1. Gain of the amplifier

$$A_{VF} = \frac{-R_F}{R_I} = \frac{-15 \text{ k}\Omega}{1 \text{ k}\Omega} = -15$$

2. Output voltage for $V_{in} = 150 \text{ mV}$

$$V_o = A_{VF} \times V_{in} = -15 \times 150 \times 10^{-3} = -2.25 \text{ Volts}$$

3. Output voltage for $V_{in} = 2\text{V}$

$$V_o = A_{VF} \times V_{in} = -15 \times 2 = -30 \text{ V}$$

But V_o can never be higher than $\pm V_{sat}$ hence V_o will be restricted to $-V_{sat}$

Assuming $-V_{sat} = 0.9 \times -V_{CC} = 0.9 \times -15 = -13.5 \text{ V}$

The output voltage

$$V_o = -13.5 \text{ V}$$

- END OF UNIT 2