DESIGN OF TWO STAGE CMOS OPERATIONAL AMPLIFIERS.

PROJECT REPORT BY:

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COMMON MODE DIFFERENTIAL AMPLIFIER (FIRST STAGE):

Common Mode Gain Stage Transistors M1, M2, M3, and M4 constitute the first stage of the op amp the differential amplifier. The gate of M1 and M2 is the non-inverting input. A common mode signal is applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of this stage is the trans-conductance of M1 times the total output resistance seen at the drain of M2. The main resistances that contribute to the output resistance are that of the input transistors themselves and the output resistance of the load transistors, M4 and M2. In this, the single ended output is achieved by using a current mirror (M4 and M3). The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. Finally, the current from M1 and M2 multiplied by the output resistance of the input stage gives the single-ended output voltage, which is the part of the input to the next stage.

COMMON SOURCE AMPLIFIER (SECOND STAGE):

The second stage is a current sink load inverter. The motive of the second gain stage is to provide additional gain consisting of transistors M6 and M7. This stage receives the output from the drain of M2 and amplifies it through M6 by common source configuration. This stage employs an active device, M7, which serve as the load resistance for M6. The gain of this stage is the trans-conductance of M6 times the equivalent load resistance seen at the output of M6 and M7. M6 is the driver while M7 acts as load. Resistor R1 plays an important role for Miller pole splitting. Cc capacitance is used to introduce a zero in the system to make the non-dominant pole move further away.

BIASING CIRCUIT:

Transistors M8 and a reference current source form a simple current mirror biasing network that provides a voltage between the gate and source of M5 and M7. Transistors M5 and M7 sink a current based on their gate to source voltage which is controlled by the bias network.

DESIGN OF THE 2 STAGE OP-AMP:

The first aspect considered in the design was to meet the desired specifications. Based on a clear understanding of the specifications, we have chosen the standard CMOS op-amp circuit topology in our design.

CALCULATIONS:

First stage Gain (Av1) = gm1* (rds2||rds4)

Second Stage Gain (Av2) =gm2*(rds6||rds7)

Total Gain (Av total) = Av1*Av2 =

[gm1* (rds2||rds4)]*[gm2*(rds6||rds7)]

GBW = (gm1)/((2*pi*Cc))

Vov= Vgs-vth= 0.2V

IDs = (gm* Vov)/2

$\mathbf{(W/L)_{Pmos}}$= (2*IDs)/(Kn*$(Vov)^2$)

$\mathbf{(W/L)_{Pmos}}$ = 2* $\mathbf{(W/L)_{Nmos}}$

For a chosen Cc= 3.498pF

gm1=2*pi*Cc*GBW (1/gm2) < **R1** < (1/3gm1) **R1**~(1/3gm1)ohms + (+/- 60%)

gm2=2*pi*C_L*4GBW Therefore, **R1= 1.6k**

The assumptions we have taken that all transistors are in saturation. In this project a two-stage op amp with an p-channel input pair is designed. The op amp uses a dual polarity power supply (VDD and VSS) for ac signals to swing above and below ground and also be centered at ground.

TABLE 1: (REQUIRED and SIMULATION SPECIFICATIONS)

Parameters	**Required**	**Simulated.**
Load capacitance	5pF	5pF
Power supply	Vdd = 0.9V, Vss = -0.9V	Vdd = 0.9V, Vss = -0.9V
Open loop gain	≥ 65dB	67.89 dB
Phase margin	≥ 60◦	63^o
Unity gain frequency	≥ 15MHz	17.48MHz

TABLE 2: Values of **W** for the respective transistors:

Transistors.	**Values of (W/L) L= 1um for all the transistors.**
M1, M2 (PMOS)	**340.8um**
M3, M4 (NMOS)	**170.4um**
M5, M8 (PMOS)	**681.6um**
M6 (NMOS)	**730.1um**
M7 (NMOS)	**1400 um**

CONCLUSION:

The report presented the full design and analysis of a two stage CMOS Op-Amp. The results show that the amplifier designed has successfully satisfied all the design specification given in advance.

REFERENCES:

Willy M.C. Sansen, — “Analog Design Essentials”, 2007

B. Razavi, —Design of Analog CMOS Integrated Circuits‖, New York: Mc-Graw Hill,2001.

APPENDIX 1:

NETLIST FILE:

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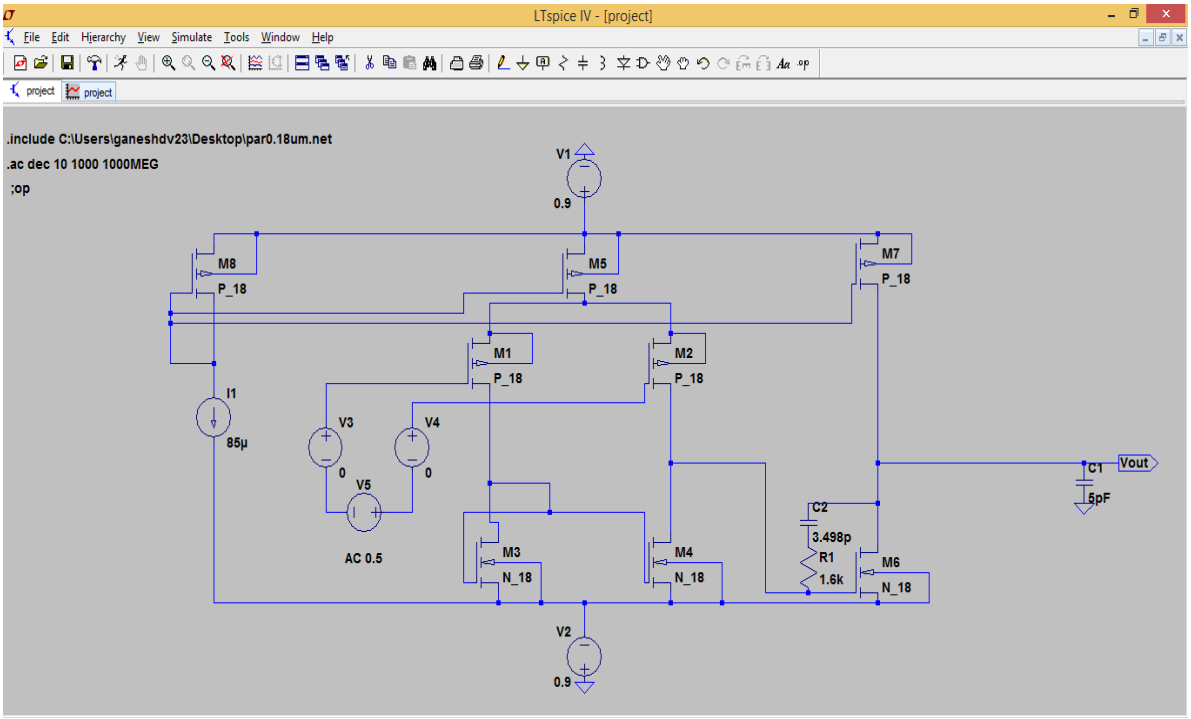
M1 N003 N004 N007 N003 P_18 l=1u w=340.8u ad=204.48p as=204.48p pd=342u ps=342u
M2 N003 N005 N006 N003 P_18 l=1u w=340.8u ad=204.48p as=204.48p pd=342u ps=342u
M3 N007 N007 N010 N010 N_18 l=1u w=170.4u ad=102.24p as=102.24p pd=171.6u
ps=171.6u
M4 N006 N007 N010 N010 N_18 l=1u w=170.4u ad=102.24p as=102.24p pd=171.6u
ps=171.6u
M8 N001 N002 N002 N001 P_18 l=1u w=681.6u ad=408.96p as=408.96p pd=682.8u
ps=682.8u
M5 N001 N002 N003 N001 P_18 l=1u w=681.6u ad=408.96p as=408.96p pd=682.8u
ps=682.8u
M7 N001 N002 Vout N001 P_18 l=1u w=1400u ad=840p as=840p pd=1401.2u ps=1401.2u
M6 Vout N006 N010 N010 N_18 l=1u w=730u ad=438p as=438p pd=741.2u ps=741.2u
I1 N002 N010 85µ
V1 N001 0 0.9
V2 0 N010 0.9
V3 N004 N008 0
V4 N005 N009 0
V5 N009 N008 AC 0.5
C1 Vout 0 5pF
R1 P001 N006 1.6k
C2 Vout P001 3.498p
.model NMOS NMOS
.model PMOS PMOS
.ac dec 10 1000 1000MEG
.op
.end
```

APPENDIX 2:

SIMULATION:



AC ANALYSIS:

In AC analysis, we examine the Gain, Phase Margin and Gain band width product.

Start frequency = 1KHz

Stop frequency = 1GHz