Quadrature O/P, Low Power, Wide Tuning Range PLL Design

Hariharan Nagarajan, Lun-Hao Chang, Ganesh Vhatkar

***Abstract*—A Supply controlled Differential I, Q 8-Stage Inverter based Ring Oscillator(RO) VCO for a K_{VCO} of 3GHz/V and a Phase Noise of -107dBc/Hz at 1MHz offset is followed by a 50MHz BW AC Coupled Buffer. Ratioed Logic TSPC Divide by 8 circuit is embedded in the feedback. Type II, 3^{rd} order Charge Pump PLL(CPPLL) is designed for 60^o phase margin for a Constant UGB of 6MHz for a REF Frequency from 62.5MHz to 125MHz with I_{CP}=106 uA, f_{Z1}=1.6MHz and f_{P3}=22.5MHz for REF Ripple Suppression with worst case lock time of 1us. All NTFs are analyzed in MATLAB and PLL is optimized for an integrated (from 10KHz to 100MHz) jitter of 932 fs at 1 GHz O/P Clock in 1.2V TSMC 65nm RF CMOS Process.**

I. Introduction

PLLs are circuits commonly used in a wide variety of applications, such as clock generation and skew compensation in microprocessors, clock and data recovery systems, and communication devices. They can be found in all kind of communication systems. The two main PLL types are LC tank-based VCO and Ring-VCO PLLs. LC tank-base VCOs offer inherent low phase-noise, Ring-VCOs have more compact size, wider tuning range, multiple clock phases and are easier to implement. The need of multiple clock phases discards the use of LC tank VCO.

A. Type I PLL

PLL type is the number of ideal integrators in the loop transmission. The VCO acts as one integrator (voltage to phase). So the lowest value for the Type is 1 since there is no PLL without a VCO.

The input and feedback have equal frequencies but a finite phase difference, $\Delta\phi_1$, and the PD generates pulses whose width is equal to $\Delta\phi_1$. These pulses are low-pass filtered to produce the dc voltage that enables the VCO to operate at a frequency equal to the input frequency, ω_1. The residual disturbance on the control line is called the ripple. A lower LPF corner frequency further attenuates the ripple, but at the cost of system stability.

$$H(s) = \frac{\phi_{out}}{\phi_{in}}(s) = \frac{K_{PD}K_{VCO}}{R_1Cs^2 + s + K_{PD}K_{VCO}}$$

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}; \omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$

B. Type II PLL

CP in CPPLL is second integrator, So Type II.

$$LG(s) = \frac{K_{VCO}I_{cp}}{2\pi}\frac{s + \omega_z}{C_2 s(s + \omega_{p_3})N}$$

Geometric Mean: $\omega_{ugb} = \sqrt{\omega_z * \omega_{p_3}}$

$$\omega_z = \frac{1}{R_{C_1}}; \omega_{p_3} = \frac{1}{R(\frac{C_1C_2}{C_1+C_2})}$$

$$\frac{C_1}{C_2} = 2(tan^2\phi_m + tan\phi_m\sqrt{(tan^2\phi_m + 1)})$$

$$I_{cp} = \frac{2\pi C_2 N}{K_{VCO}}\omega_{ugb}^2\frac{\sqrt{\omega_{p_3}^2 + \omega_{ugb}^2}}{\sqrt{\omega_z^2 + \omega_{ugb}^2}}$$

C. Compare & Contrast

Modern RF synthesizers rarely employ the Type I PLL. This is for three reasons. First, $\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$ Type I imposes a tight relation between the loop stability and the corner frequency of the low-pass filter. The ripple on the control line modulates the VCO frequency and must be suppressed by the choosing a low value for ω_{LPF}.

But a small ω_{LPF} leads to a less stable loop. Type II PLL topology that does not exhibit this trade-off.

Second, the Type I PLL suffers from a limited acquisition range, if the VCO frequency and the input frequency are very different at the startup, the loop may never acquire lock. However, Type II PLL always locks.

While not directly relevant to RF synthesizers, the finite static phase error and its variation with the input frequency also prove undesirable in some applications. This error can be driven to zero by means of an infinite loop gain in Type II PLL.

II. Phase-Locked Loop Block Design

A. Phase/Frequency Detector

The problem of limited acquisition range is solved by introducing a frequency detector is added to the loop. PFD operates as an FD if its input frequencies are not equal and as a PD if they are.

The circuit consists of two edge-triggered, reset-table D flipflops with their D inputs tied to logical ONE. Signals A and B act as clock inputs of DFFA and DFFB, respectively, and the AND gate resets the flipflops if $Q_A = Q_B = 1$.We note that a transition on A forces Q_A to be equal to D input, i.e., a logical ONE. Subsequent transitions on A have no effect. When B goes high, so does Q_B, activating the reset of the flipflops. Thus, Q_A and Q_B are simultaneously high for a duration given by the total delay through the AND gate and the reset path of the flipflops. If A and B are exactly in-phase, both Q_A and Q_B exhibit these narrow reset pulses.

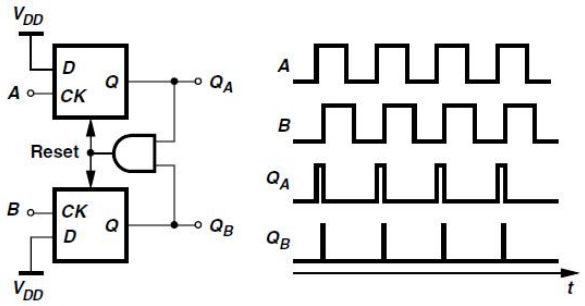

Fig. 1. PFD implementation.

B. Charge Pump

A Source Switched CP sinks or sources current for a limited period of time. Depicted in Fig. 2 is an example, where M1 and M4 act as switches and controlled by the inputs Down and UP, respectively. A pulse of width ΔT on Up turns M4 on for ΔT seconds, allowing I_{M3} to charge C1. Consequently, Vc goes up by an amount equal to ΔT * I_{M3}/C1. Similarly, a pulse on Down yields a drop in Vc. Nominally, I_{M3}=I_{M2}=Ip. Thus, if Up and Down are asserted simultaneously, I_{M3} simply flows through M3 and M2, creating no change in Vc.

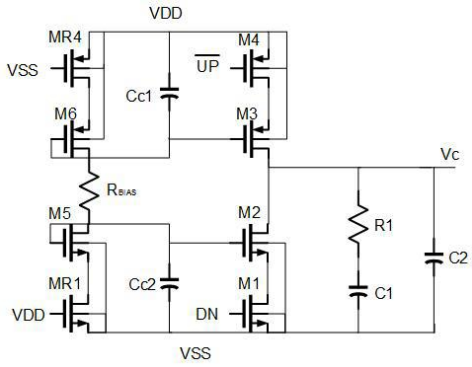

Fig. 2. Charge Pump.

C. TSPC Divider

The first stage of ratioed logic TSPC Fig. 3 operates as the master D latch and the last two as the slave D latch. The slave latch is designed as ratioed logic, i.e., both NMOS devices are strong enough to pull down B and QZ even if M_4 or M_6 is on. When CK is high, the first stage reduces to an inverter, the second stage forces a ZERO at B, and the third stage is in the store mode. When CK goes down, B remains low if A is high, or it rises if A is low, with QZ tracking B because M_7 and M_6 act as a ratioed inverter.

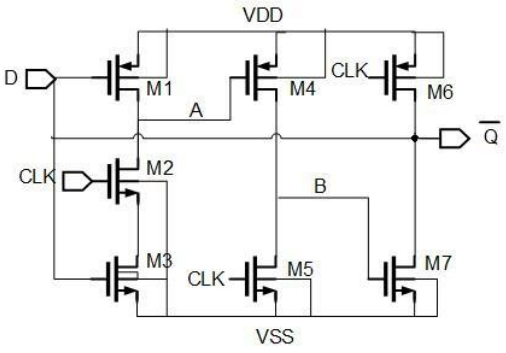

Fig. 3. TSPC circuit using ratioed logic.

D. RO based VCO

The propagation delay of an inverter is t_p. The time period of oscillation is $T_o = 2 * t_p * 4$. PMOS in Supply Controlled RO-VCO is kept in Deep Saturation for Linearizing K_{VCO} from 530mV(1GHz) to 700mV(0.5GHz).

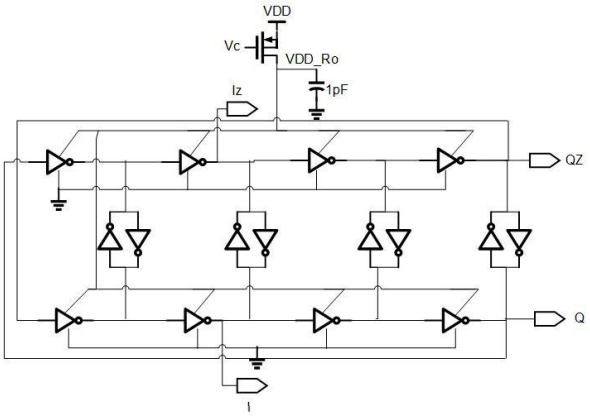

Fig. 4. Supply Controlled RO-VCO.

E. VCO Buffer

$$\frac{OUT}{IN} = (1 - 2gmR_f)\frac{s}{s + \frac{2gm}{Cc}}$$

The 3dB BW is 50MHz which is $(\frac{1}{10})^{th}$ of the lowest frequency of operation for Cc = 1pF and Gain = 20.

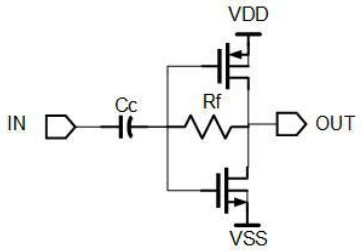

Fig. 5. VCO Buffer.

III. NTF

- Noise Transfer Function

$$NTF_{IN}(s) = NTF_{DIV}(s) = \frac{\phi_{OUT}(s)}{\phi_{IN}(s)} = \frac{N * LG(s)}{1 + LG(s)}$$

$$NTF_{CP}(s) = \frac{\phi_{OUT}(s)}{i_{CP}(s)} = \frac{2\pi}{I_{CP}} NTF_{IN}(s)$$

$$NTF_R(s) = \frac{\phi_{OUT}(s)}{v_R(s)} = \frac{\frac{K_{VCO}}{s}}{1 + LG(s)}$$

$$NTF_{VCO}(s) = \frac{\phi_{OUT}(s)}{\phi_{VCO}(s)} = \frac{1}{1 + LG(s)}$$

IV. Design Choice

PM ϕ_m	60^o	45^o
R	1KΩ	
K_{VCO}	3.078GHz/v	
ω_{ugb}	6MHz	
ω_z	1.6MHz	2.5MHz
ω_{p3}	22.5MHz	14.4MHz
C_1	100pF	64pF
C_2	7.7pF	13.25pF
I_{cp}	106.6uA	117.5uA

V. Simulation

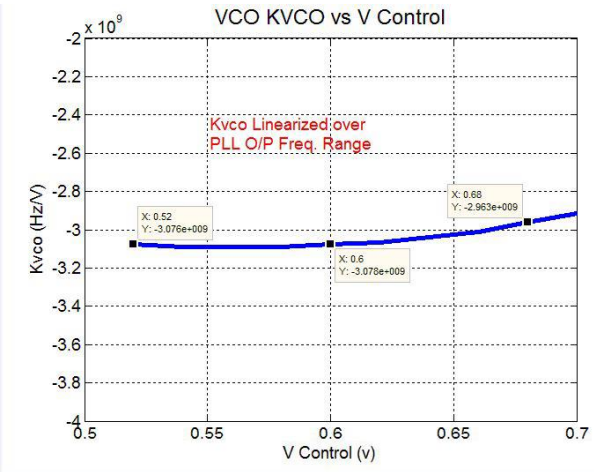

Fig. 6. KVCO vs. V Control.

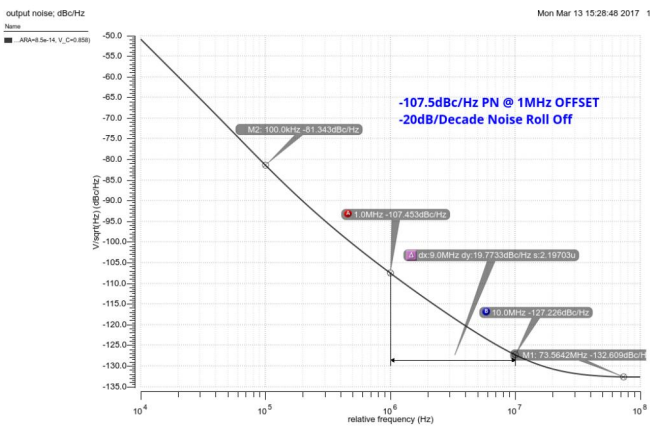

Fig. 7. RO-VCO phase noise profile.

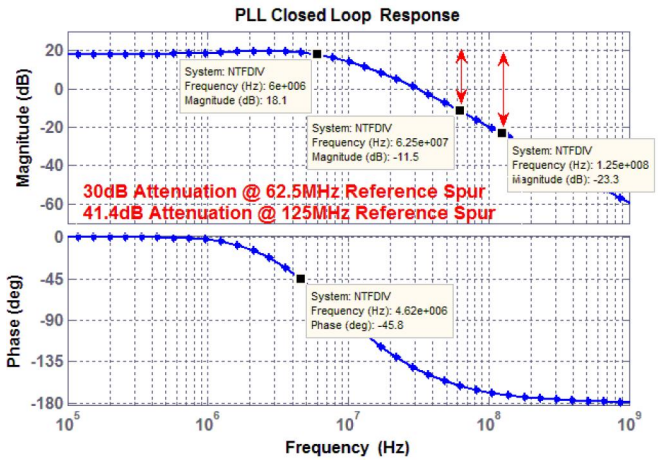

Fig. 8. PLL Closed-Loop Response.

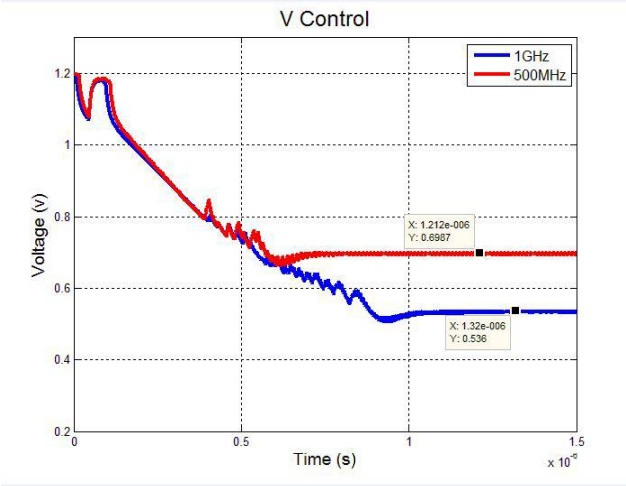

Fig. 9. V Control settling profile at 500MHz and 1GHz.

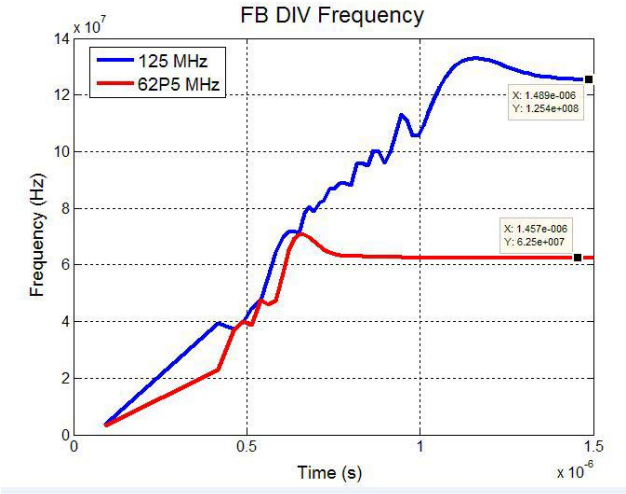

Fig. 10. FB Divider frequency settling profile at 62.5MHz and 125MHz.

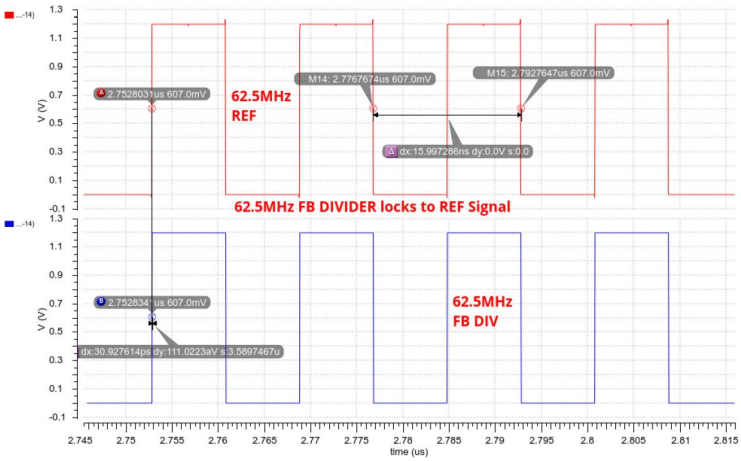

Fig. 11. FB divider locks at 62.5MHz.

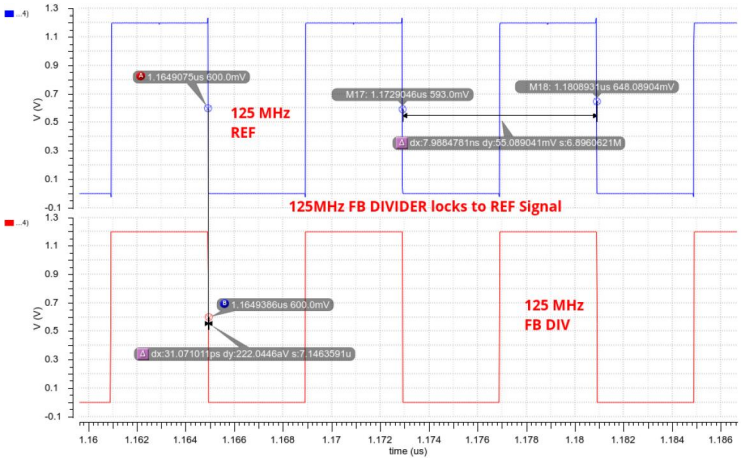

Fig. 12. FB divider locks at 125MHz.

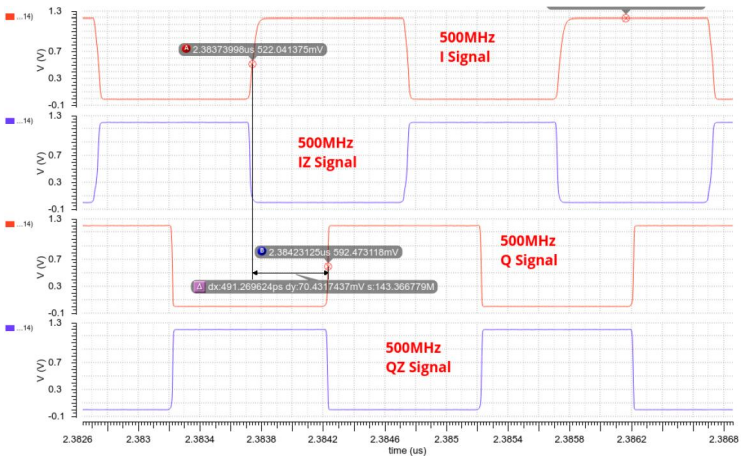

Fig. 13. VCO 500MHz I,Iz,Q,Qz Clocks.

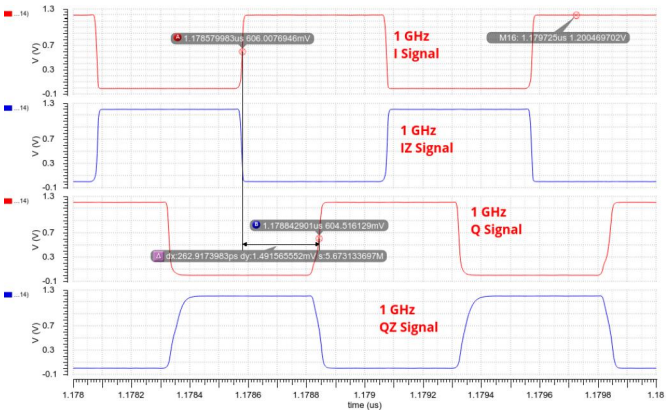

Fig. 14. VCO 1GHz I,Iz,Q,Qz Clocks.

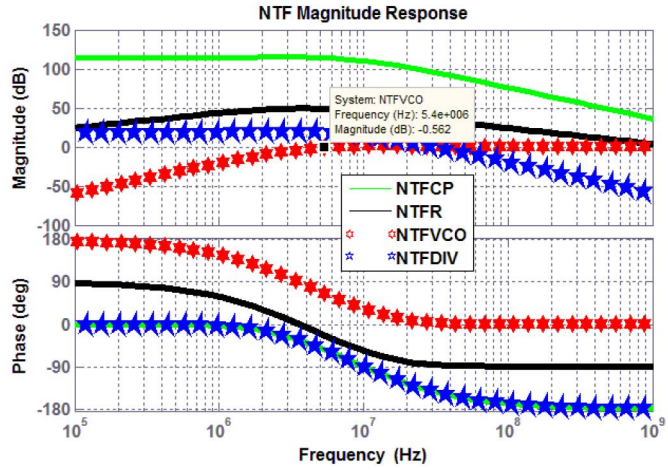

Fig. 15. NTF vs. Frequency.

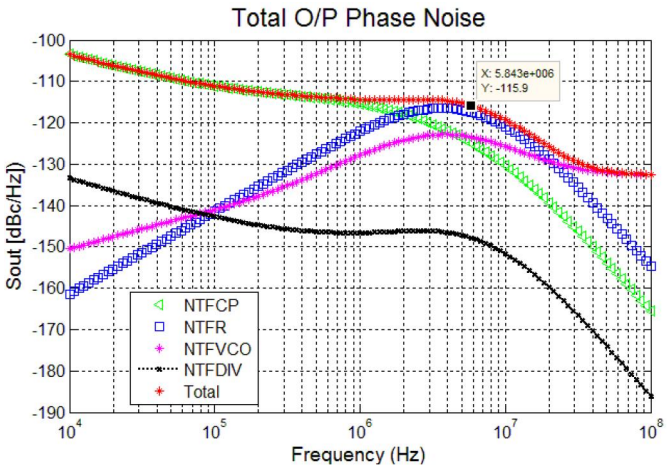

Fig. 16. $S_{\phi_{OUT}}$ vs. Frequency.

TABLE I
PLL POWER CONSUMPTION 1.2V & JITTER

	1GHz Mode (uA)	0.5GHz Mode (uA)	Jitter (fS)
VCO + Buffer	1623	633	520
Divider	1540	1540	34
Charge Pump	17	11	53
Resistor	0	0	567
PFD	2.5	1.2	
Total	3182	2185	772

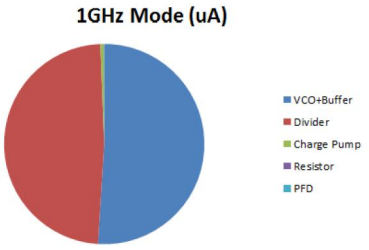

Fig. 17. 1GHz PLL Power Consumption 1.2V.

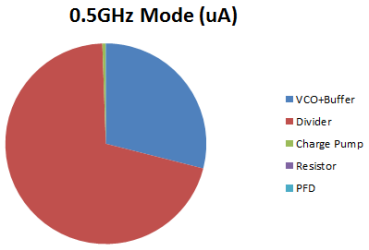

Fig. 18. 0.5GHz PLL Power Consumption 1.2V.

VI. CONCLUSION

A Supply controlled Differential I, Q 8-Stage Inverter based Ring Oscillator(RO) VCO followed by an AC Coupled Buffer. Ratioed Logic TSPC was used as Divide by 8 circuit in the feedback. Type II, 3^{rd} order Charge Pump PLL(CPPLL) is designed for 60^{o} phase margin for a Constant UGB of 6MHz for a REF Frequency from 62.5MHz to 125MHz and achieved a worst case lock time of 1us. All NTFs are analyzed in MATLAB and PLL is optimized for an integrated (from 10KHz to 100MHz) jitter of 932fs at 1GHz O/P Clock in 1.2V TSMC 65nm RF CMOS Process.

REFERENCES

[1] A. Hajimiri and T. H. Lee, A General Theory of Phase Noise in Electrical Oscillators, IEEE J. of Solid-State Circuits, vol. 33, pp. 179194, Feb. 1998.