RF FRONT END RECEIVER DESIGN

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ABSTRACT :
2.4GHz, 80 MHz RF BW LNA is designed with 50 fF C_{PAD}, 40 nH L_G for an S_{11} < -12 dB, Gain of 17 dB, NF of 4 dB across RF BW, 1nH Bond-Wire Inductor as Source Degeneration and an IIP_3 > -30 dBm within 0.4 mA, 1.2 V Supply. 10 KΩ series resistor biasing from low power NMOS diode-mirror and Cascode NMOS Gate biased at V_{DD}. NMOS Cross-Coupled LC VCO and AC Coupled Buffers are designed for a Phase Noise of -125 dBc/Hz at 1 MHz offset in Current-Limited regime for an f_c of 4.8 GHz within 0.8 mA, 1.2 V Supply. Phase Noise $1/f^2$ skirt optimization at 1 MHz offset by Wide NMOS devices for an LC Tank Quality Factor of 21 at 4.8 GHz with L_{TANK} = 1.9 nH and C_{TANK} = 450fF. Onchip 1:1 Balun interfaces single ended LNA O/P to differential I/P of passive-quadrature Mixer with a coupling coefficient of 0.8. TSPC Ratioed Logic Divider drives the mixer gates at 2.4GHz LO frequency in this low power RX frontend in TSMC 65nm RF CMOS Process.

DESIGN INTRODUCTION:

LNA:

As the first active stage of receivers, LNAs play a critical role in the overall performance. We must employ active devices to provide a 50Ω input resistance without the noise of a 50 Ω resistor. One such method employs a **CS stage with inductive degeneration**. We first compute the input impedance of the circuit while neglecting C_{gd} and C_{sb}.

$$\boldsymbol{Z_{in} = L_s S + \frac{1}{C_{gs} S} + \frac{g_m L_s}{C_{gs}}}$$

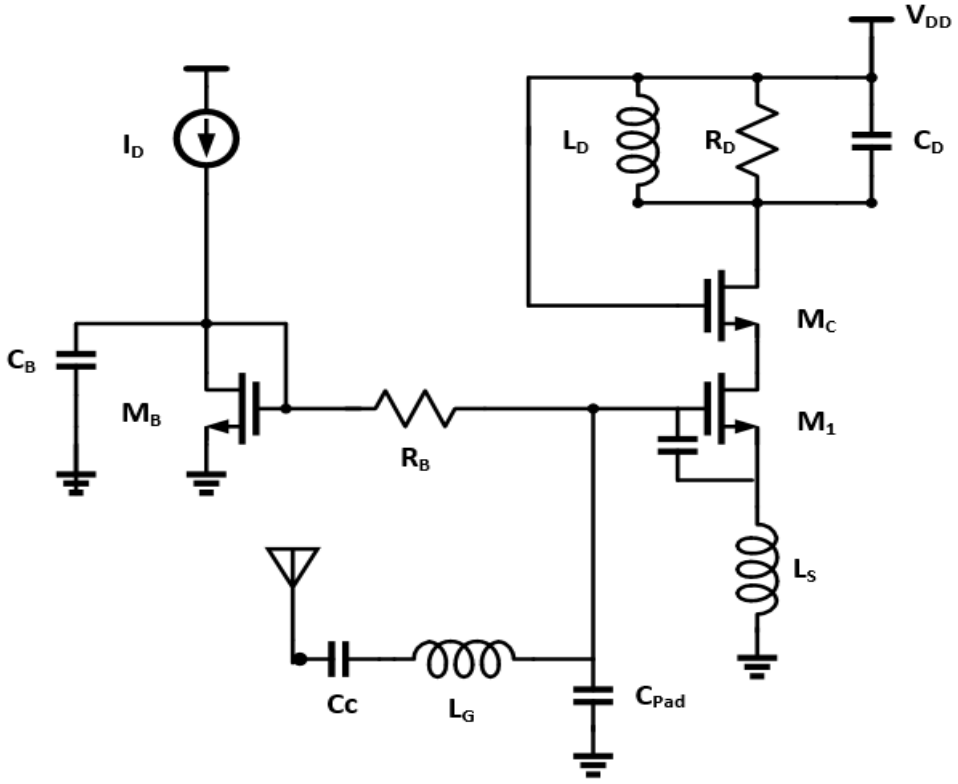
In practice, the degeneration inductor is often realized as a bond wire with the reasoning that the latter is inevitable in packaging and must be incorporated in the design. To minimize the inductance, a "downbond" can directly connect the source pad to a ground plane in the package, but even this geometry yields a value in the range of 0.5 to 1 nH. That is, the input resistance provided by modern MOSFETs tends to be substantially higher than 50 Ω if a bond wire inductance is used. In addition to $\boldsymbol{C_{gd}}$, the input pad capacitance of the circuit also lowers the input resistance.

$$\boldsymbol{R_{eq} = \left(\frac{C_{gs}}{C_{gs} + C_{pad}} \right)^2 * \frac{g_m L_s}{C_{gs}}}$$

$$\boldsymbol{C_{eq} = C_{gs} + C_{pad}}$$

$$\omega_o = \frac{1}{\sqrt{(C_{gs} + C_{pad}) * (L_g + L_s)}}$$

We can now make two observations. First, the effect of the gate-drain and pad capacitance suggests that the transistor f_T need not be reduced so much as to create$R_s = 50\Omega$. Second, since the degeneration inductance necessary for Re{Z_{in} }=50 Ω is insufficient $C_{gs} + C_{pad}$ to resonate with, another inductor must be placed in series with the gate where it is assumed L_g is off-chip.



Trans-Conductance gain of the circuit:

$$G_m = \frac{\omega_T}{2\omega_o} * \frac{1}{R_s} \qquad R_s = \frac{g_m L_s}{C_{gs}} \qquad \omega_T = \frac{g_m}{C_{gs}}$$

The voltage gain is equal to the product of the circuit's trans-conductance and the load resistanceR_D,

$$A_v = \frac{\omega_T}{2\omega_o} * \frac{R_D}{R_s}$$

Noise figure of the Cascode CS stage:

$$NF = 1 + g_m R_s \gamma * \left(\frac{\omega_o}{\omega_T}\right)^2 + \frac{4R_s}{R_D} * \left(\frac{\omega_o}{\omega_T}\right)^2$$

MIXER:

Mixers perform frequency translation by multiplying two waveforms (and possibly their harmonics). As such, mixers have three distinctly different ports. In the receive path, the down conversion mixer senses the RF signal at its "RF port" and the local oscillator waveform at its "LO port." The output is called the "IF port" in a heterodyne RX or the "baseband port" in a direct-conversion RX. Similarly, in the transmit path, the up conversion mixer input sensing the IF or the baseband signal is called the IF port or the baseband port, and the output port is called the RF port. The input driven by the LO is called the LO port.

GAIN:

The first harmonic of this waveform has a peak amplitude of $\frac{4}{\pi}$ and can be expressed as $\frac{4}{\pi}\cos(\omega_{LO}t)$. In the frequency domain, this harmonic consists of two impulses at $\mp\omega_{LO}$, each having an area of $\frac{2}{\pi}$. Thus, the convolution of an RF signal with these impulses creates the IF signal with a gain of $\frac{2}{\pi}$ The conversion gain is therefore equal to $\frac{2}{\pi}$ for abrupt LO switching. We call this topology a "return-to-zero" (RZ) balanced mixer because the output falls to zero when the switch turns off.

OUTPUT NOISE:

Vout is equal to the noise of RS for half of the LO cycle and equal to zero for the other half, we expect the output power density to be simply equal to half of that of the input, i.e., Vn^2 =2kTRS. It is important to note that the power spectral density of the square wave has a $sinc^2$, envelope, exhibiting an impulse with an area of 0.5^2, at f=0, two with an area of $\frac{1}{\pi^2}$ at f =±f_{LO}, etc. The output spectrum consists of

(a) 2kTRS*0.5^2,

(b) 2kTRS shifted to the right and to the left by ±f_{LO} and multiplied by $\frac{1}{\pi^2}$,

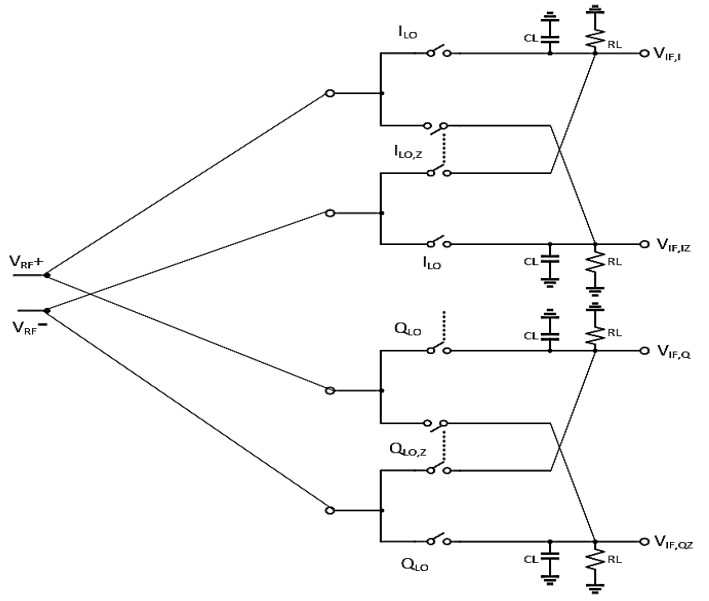
(c) 2kTRS shifted to the right and to the left by ±3 and multiplied by $\frac{1}{9\pi^2}$, etc.

$$Vn^2 = 2kTR_s * \left(\frac{1}{2^2} + \frac{2}{\pi^2} + \frac{2}{9\pi^2} + \frac{2}{25\pi^2} + \cdots\right)$$

$$Vn^2 = 2kTR_s$$

DOUBLY BALANCED MIXER:

V_{out1} is equal to V_1 RF for one half of the LO cycle and equal to V_2 RF for the other half, i.e., R_1 and R_2 can be omitted because the outputs do not "float." We observe that V_{out1} V_{out2} can be decomposed into two return-to-zero waveforms, each having a peak amplitude of $2V_o$. Since each of these waveforms generates an IF amplitude of $\frac{\mathbf{1}}{\boldsymbol{\pi}}$*$2V_o$ and since the outputs are 180 out of phase, we conclude that $\boldsymbol{V_{out1} - V_{out2}}$ contains an IF amplitude of $\frac{\mathbf{1}}{\boldsymbol{\pi}}$*(4 V_o). Noting that the peak differential input is equal to $2V_o$, we conclude that the circuit provides a voltage conversion gain of $\frac{\mathbf{2}}{\boldsymbol{\pi}}$, equal to that of the single-balanced counterpart.



<u>OSCILLATOR:</u>

In most transmit and receive paths, one input of every mixer is driven by a periodic signal. Hence the need for oscillators. An oscillator used in an RF transceiver must satisfy two sets of requirements: (1) system specifications, e.g., the frequency of operation and the "purity" of the output, and (2) "interface" specifications, e.g., drive capability or output swing.

Oscillation frequency is given by the equation,

$$\boldsymbol{\omega_{osc}} = \frac{1}{\sqrt{\boldsymbol{L_{Tank}}\left(\boldsymbol{C_{gs}} + \mathbf{4}\boldsymbol{C_{db}} + \boldsymbol{C_{gd}} + \boldsymbol{C_{Tank}}\right)}}$$

Current Controlled Output Swing Regime is given by,

$$V_{out} = \frac{4}{\pi} I_{ss} R_p$$

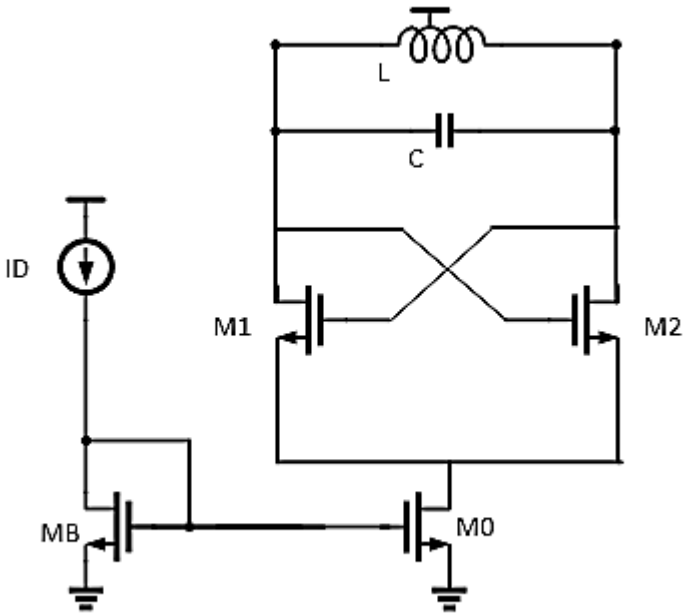
For oscillation to occur, the negative resistance must cancel the loss of the tank,

$$g_m R_p \geq 1$$

g_m can be chosen slightly greater than R_p of the tank to ensure oscillation. However, this choice leads to small voltage swings; if the swings are large, e.g., if M1 and M2 switch completely, then the gm falls below $\frac{1}{R_p}$ for part of the period, failing to sustain oscillation. (That is, with $g_m \approx \frac{1}{R_p}$, M1 and M2 must remain linear to avoid compression.) In practice, therefore, we design the circuit for nearly complete current steering between M1 and M2, inevitably choosing a g_m quite higher than $\frac{1}{R_p}$.

Andreani's Phase Noise Model:

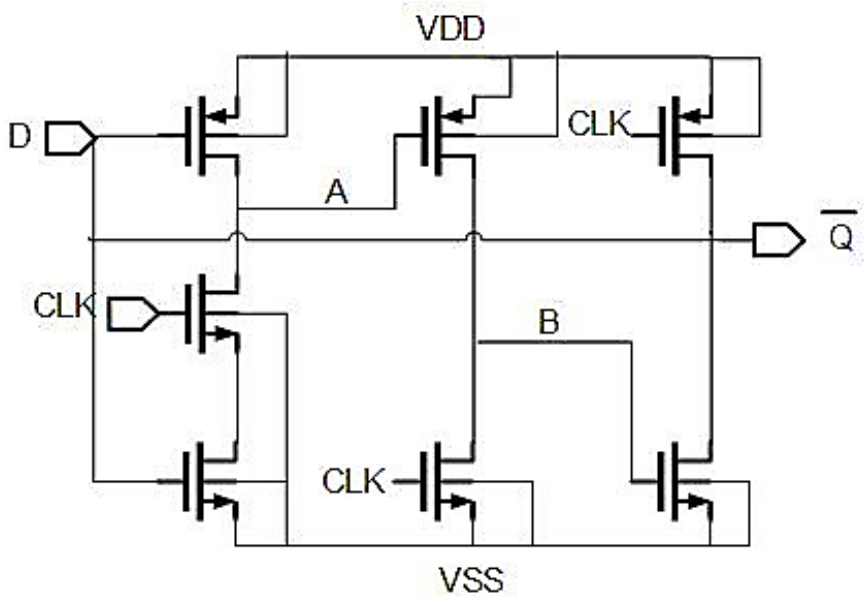
$$\mathcal{L}(\Delta\omega) = 10\, log\left(\frac{k_B T R_p (1+\gamma)}{Q^2 * Ass^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right)$$



TSPC DIVIDER:

A variant of TSPC logic that achieves higher speeds is depicted below. Here, the first stage operates as the master D latch and the last two as the slave D latch. The slave latch is designed as "ratioed" logic, i.e., both NMOS devices are strong enough to pull down B and QBar even if M4 or M6 is on. When CK is high, the first stage reduces to an inverter, the second stage forces a ZERO at B, and the third stage is in the store mode. When CK goes down, B remains low if A is high, or it rises if A is low, with QBar tracking B because M7 and M6 act as a ratioed inverter.

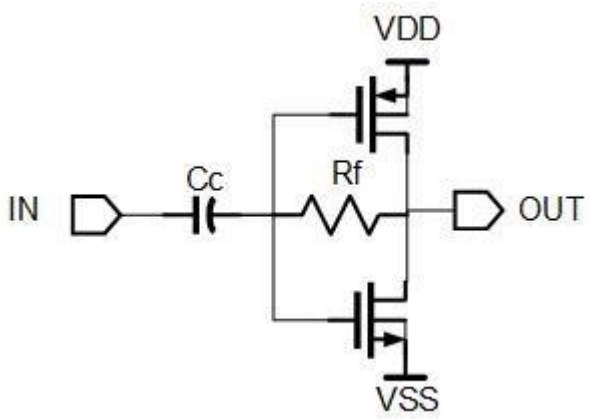
The second and third stages consume static power when their clocked transistor fights the input device. At high speeds, however, the dynamic power dominates, making this drawback less objectionable. In a typical design (with PMOS mobility about half of NMOS mobility), all transistors in the circuit can have equal dimensions, except for W5, which must be two to three times the other transistor widths to maximize the speed. This technique allows ÷2 speeds around 10 GHz and ÷3 speeds around 6 GHz in 65-nm CMOS technology.



VOLTAGE BUFFER:

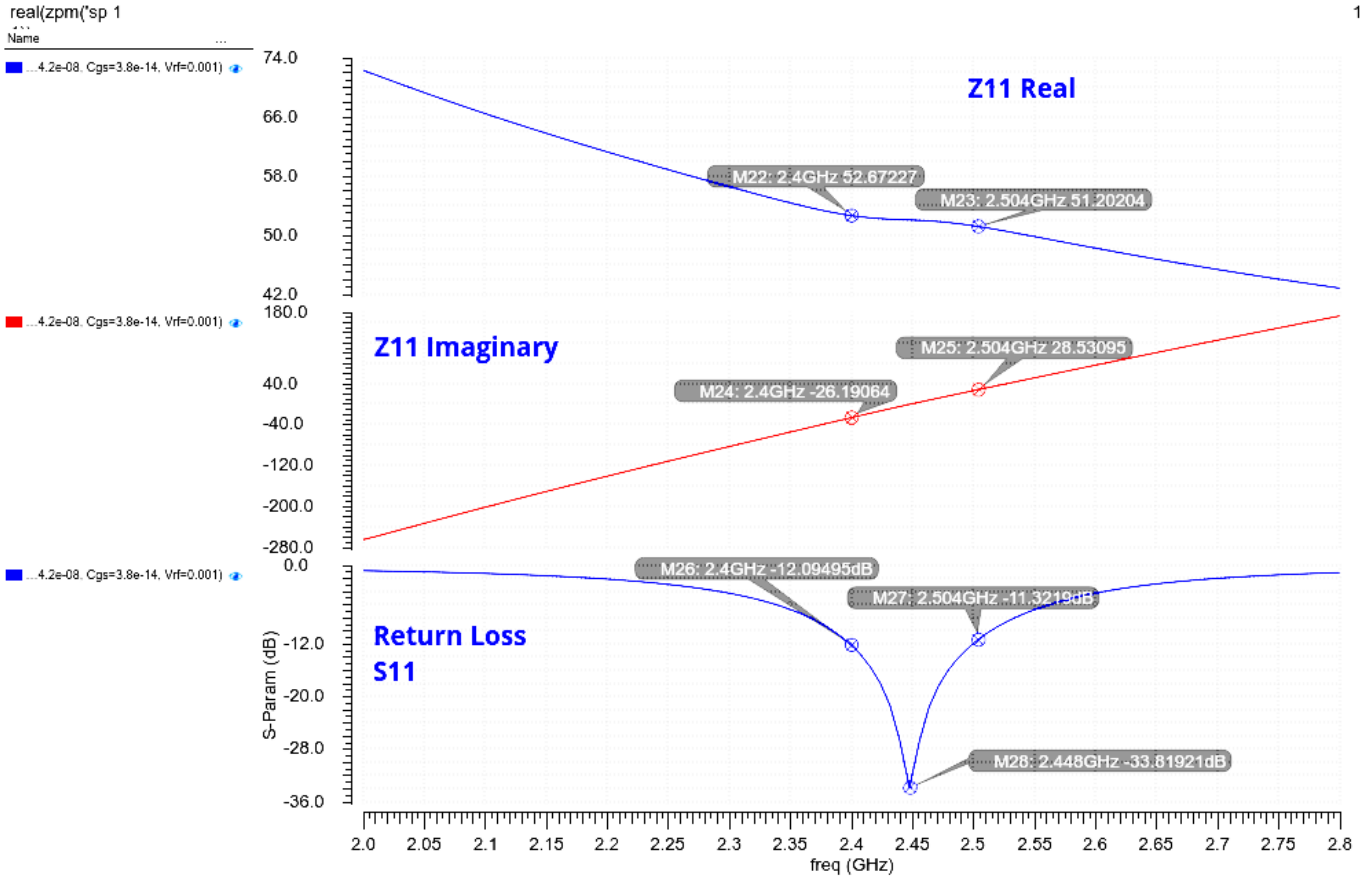
The 3dB BW is 50MHz which is (1/100) th of the lowest frequency of operation for Cc = 1pF and Gain = 20.

$$\frac{OUT}{IN} = (1 - 2g_m R_p)\frac{s}{s + \frac{2g_m}{Cc}}$$

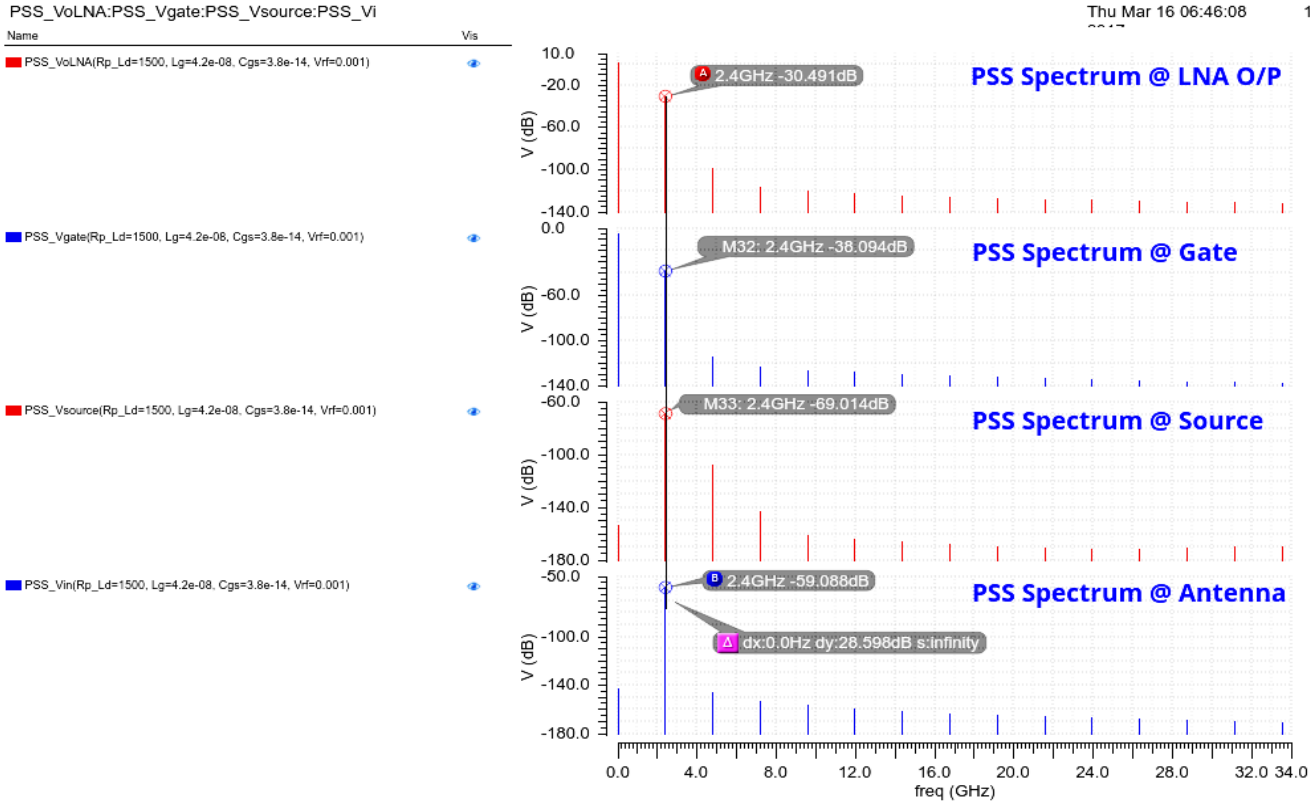


SIMULATION RESULTS for LNA:

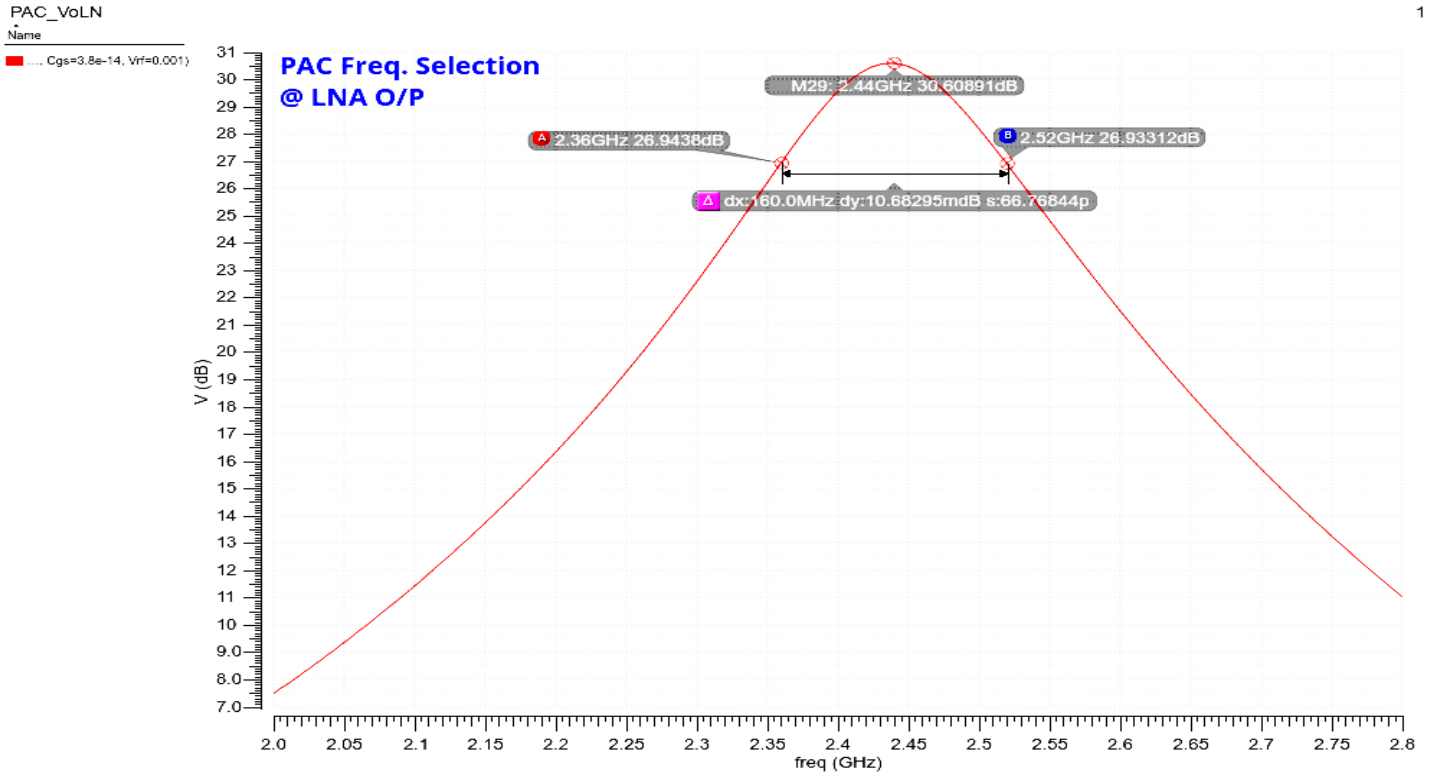
<u>Z11 and S11 of LNA</u>:



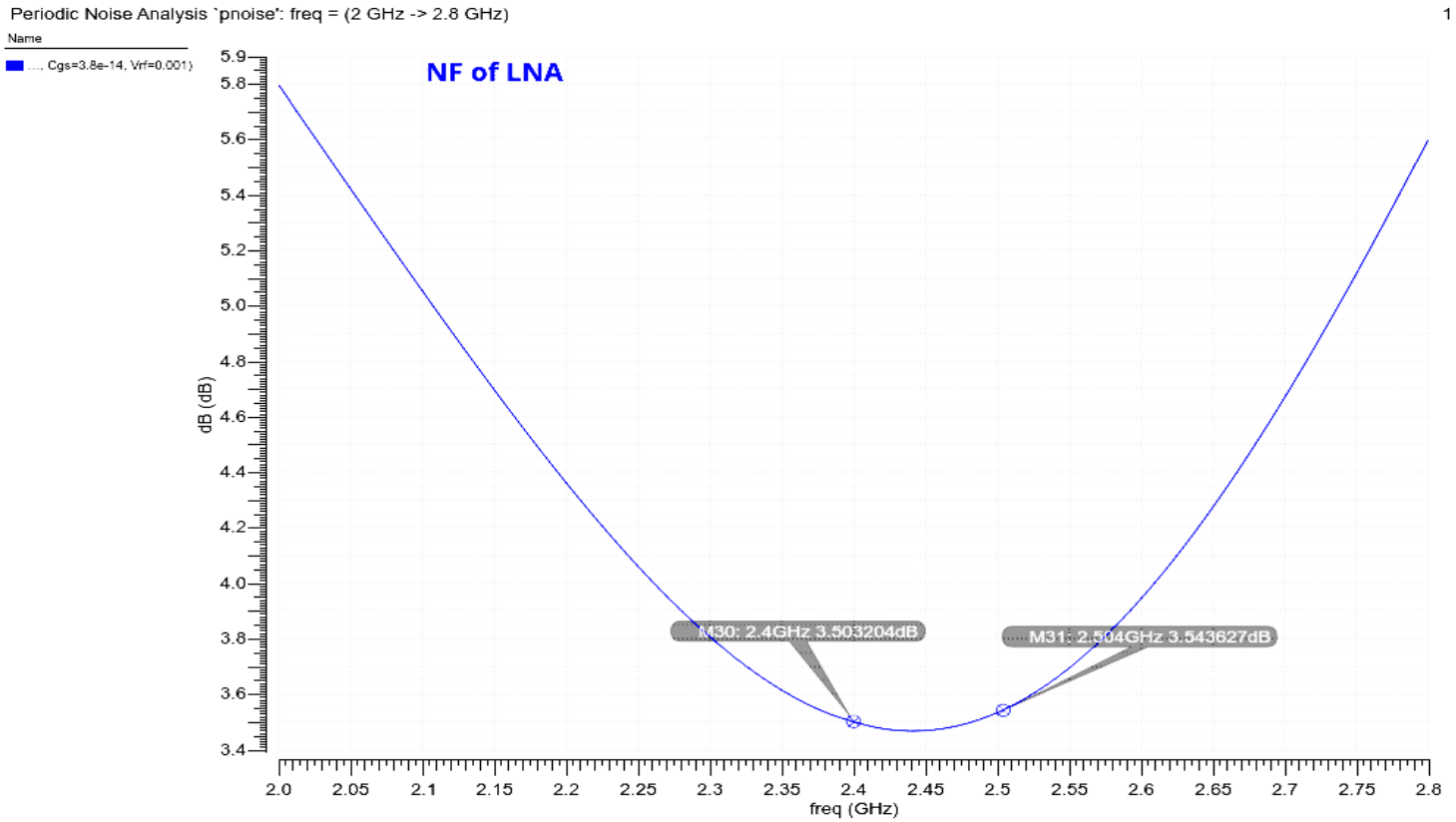
RF LNA SPRECTRUM:



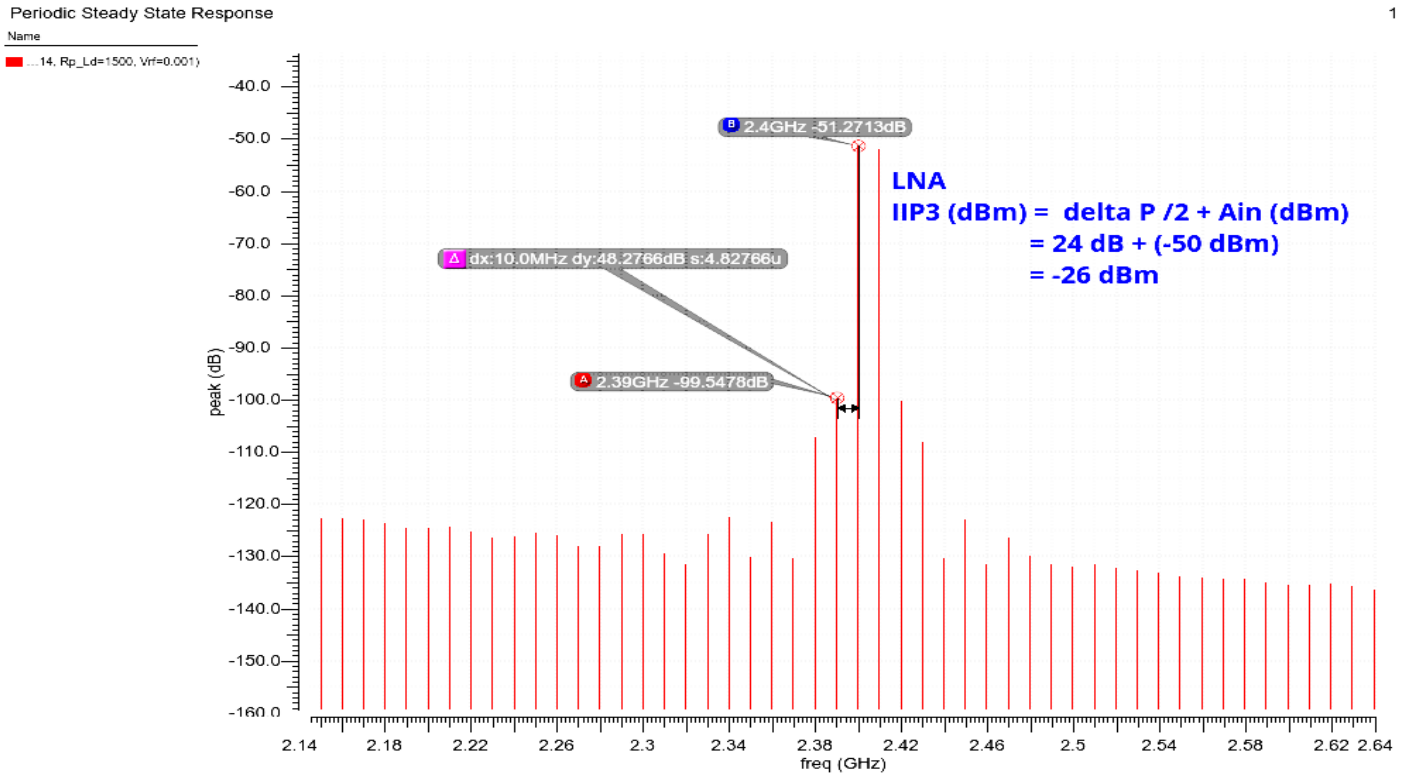
PAC O/P SPECTRUM:



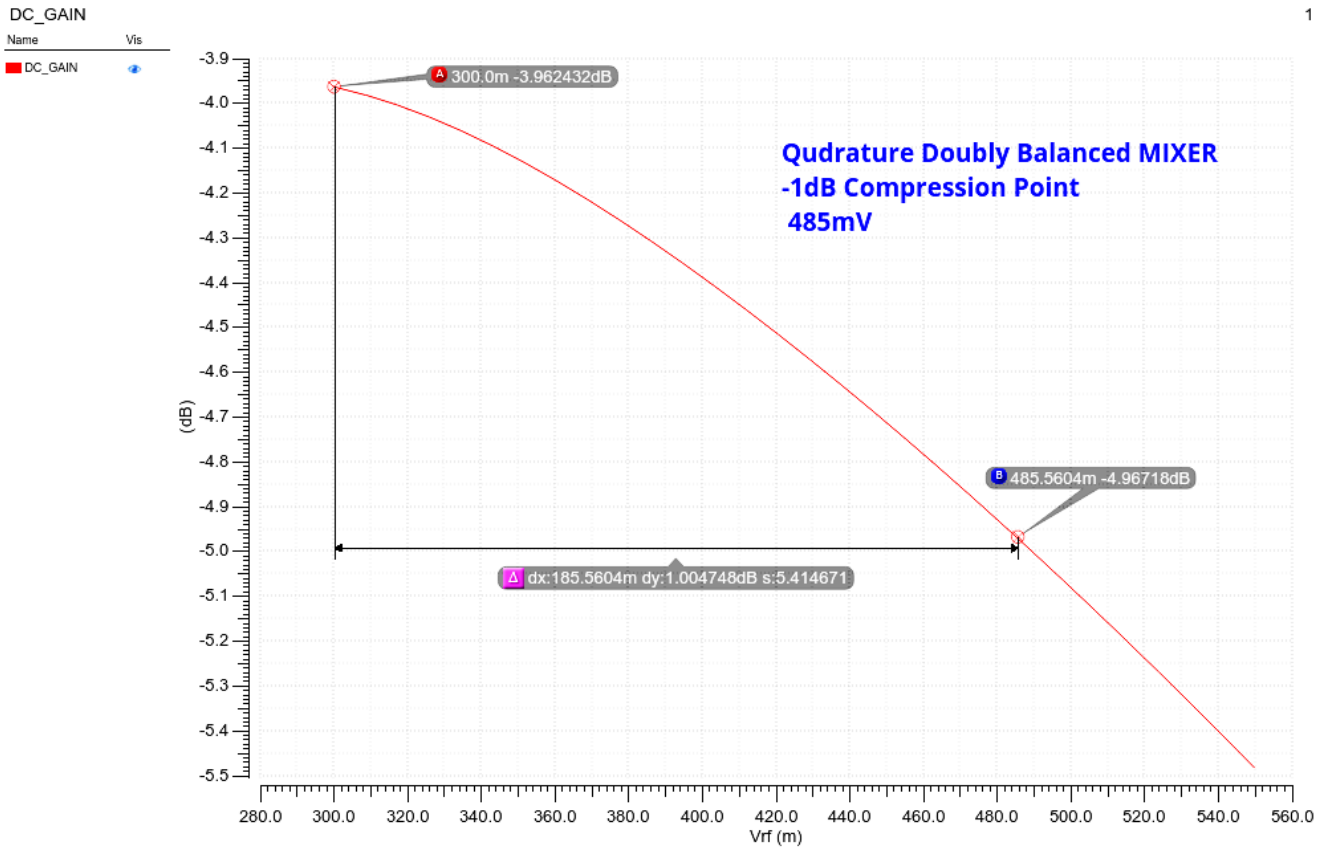
NF of LNA:



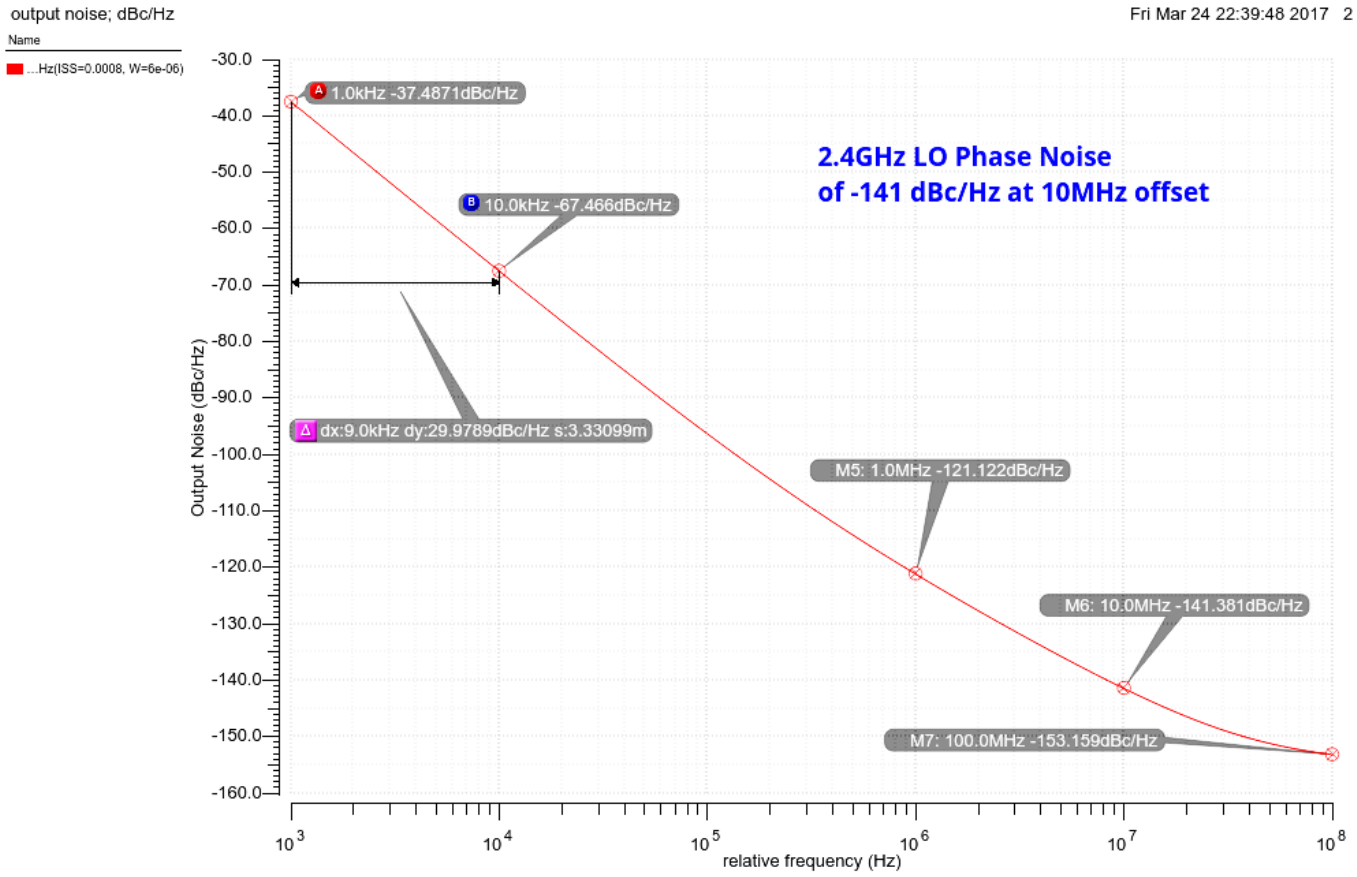
IIP3 of LNA:

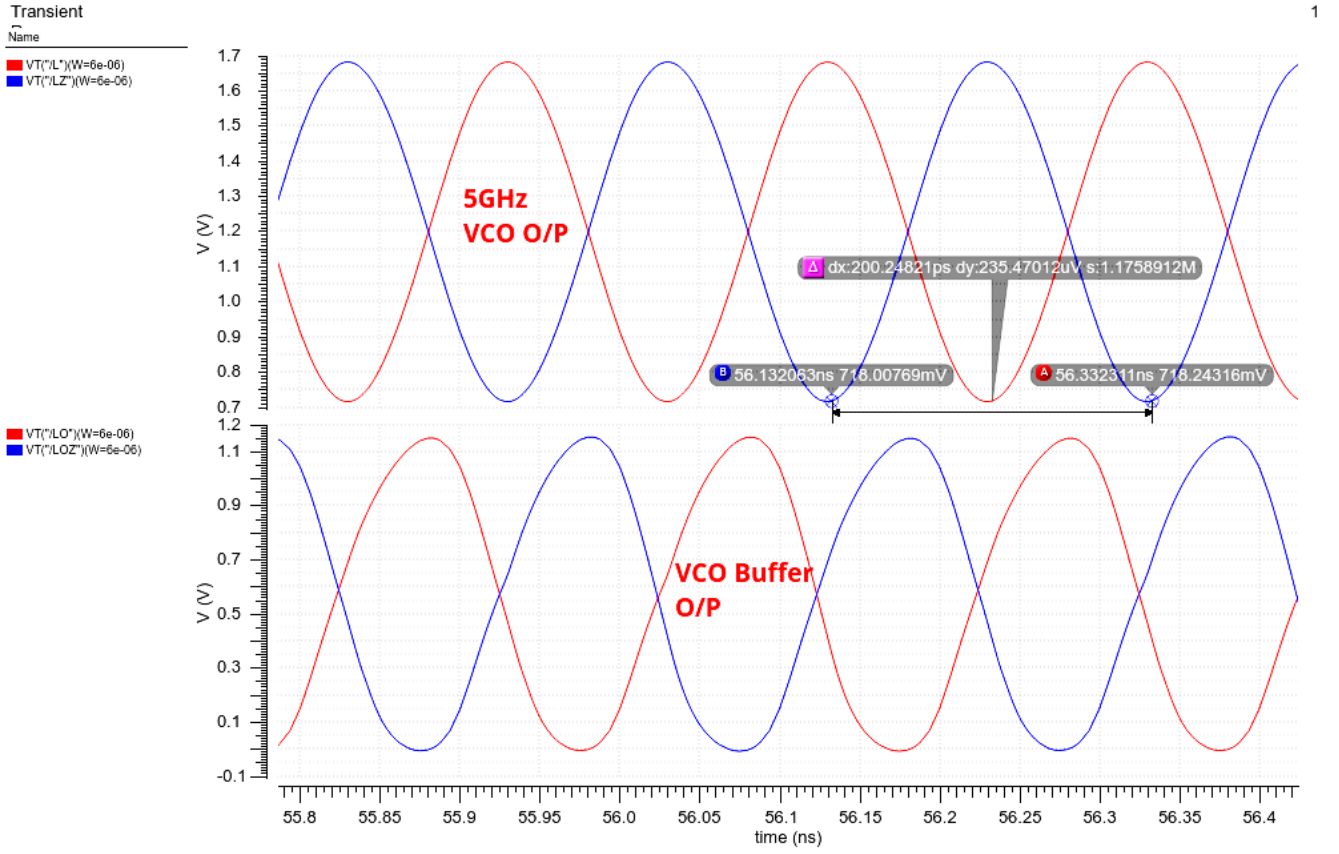


SIMULATION RESULTS for MIXER:



SIMULATION RESULTS for VCO:





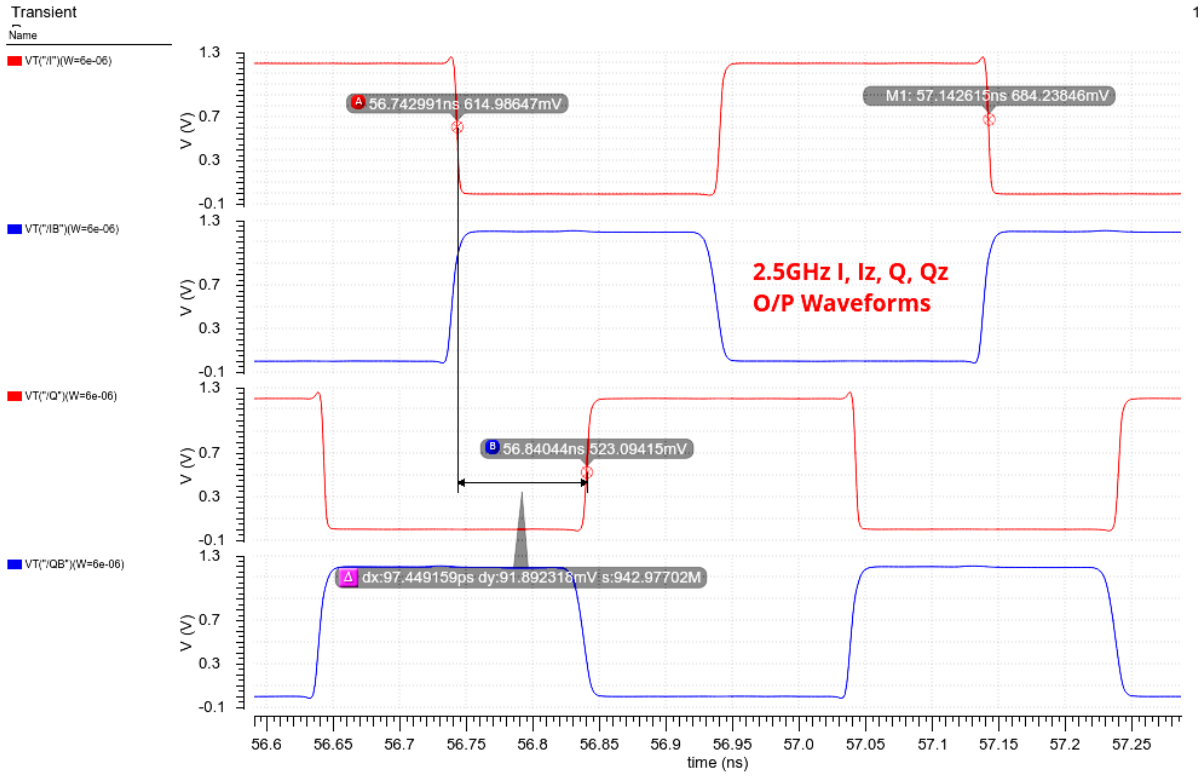
RX Front End SCM:

Parameter	Specs	SCM
Input Supply	1.2 V	
Max Current	2.1 mA	
RF Freq.	2.4 GHz	
LO Freq.	2.4 GHz	Homodyne RX
VCO Freq.	4.8GHz	
VCO PN @ 10MHz	-124 dBc/Hz	
LO Freq.	2.4 GHz	
LO PN @ 10MHz	-130 dBc/Hz	-141 dBc/Hz
RF BW	80MHz	
IF BW	40 MHz	
RX Chain Gain	10 dB	12 dB
RX Chain NF	6 dB	4 dB
-1 dB Compression Point		-24 dBm
IIP3 @ 5MHz Offset	-30 dBm	-28 dBm
S11	<-10 dB	< -12 dB

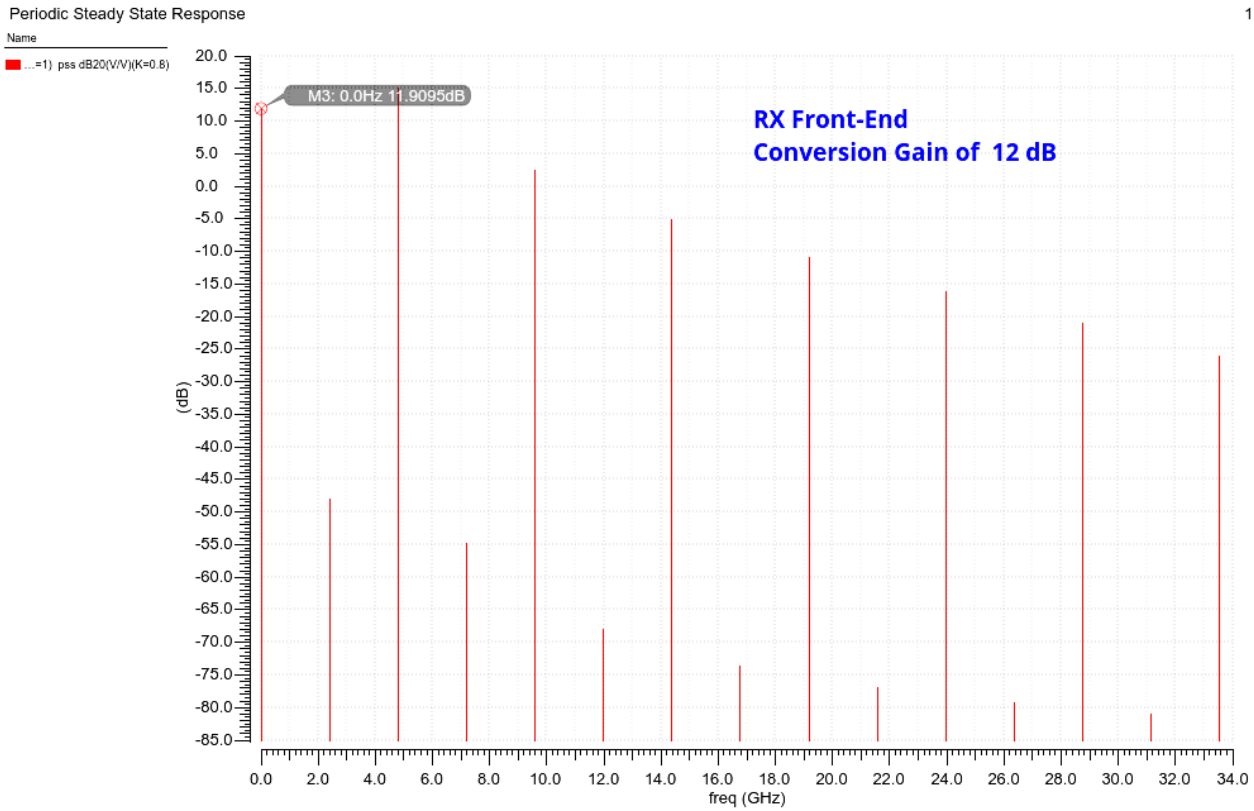
RX Front End Power consumption:

	Current (uA)	Total (uA)
LNA	330	330
VCO	600	600
VCO Buffer X2	65 X2	130
TSPC Div2 X2	477 X2	954
LO Driver X2	25 X2	50
Passive Mixer	0	0
Total		2064

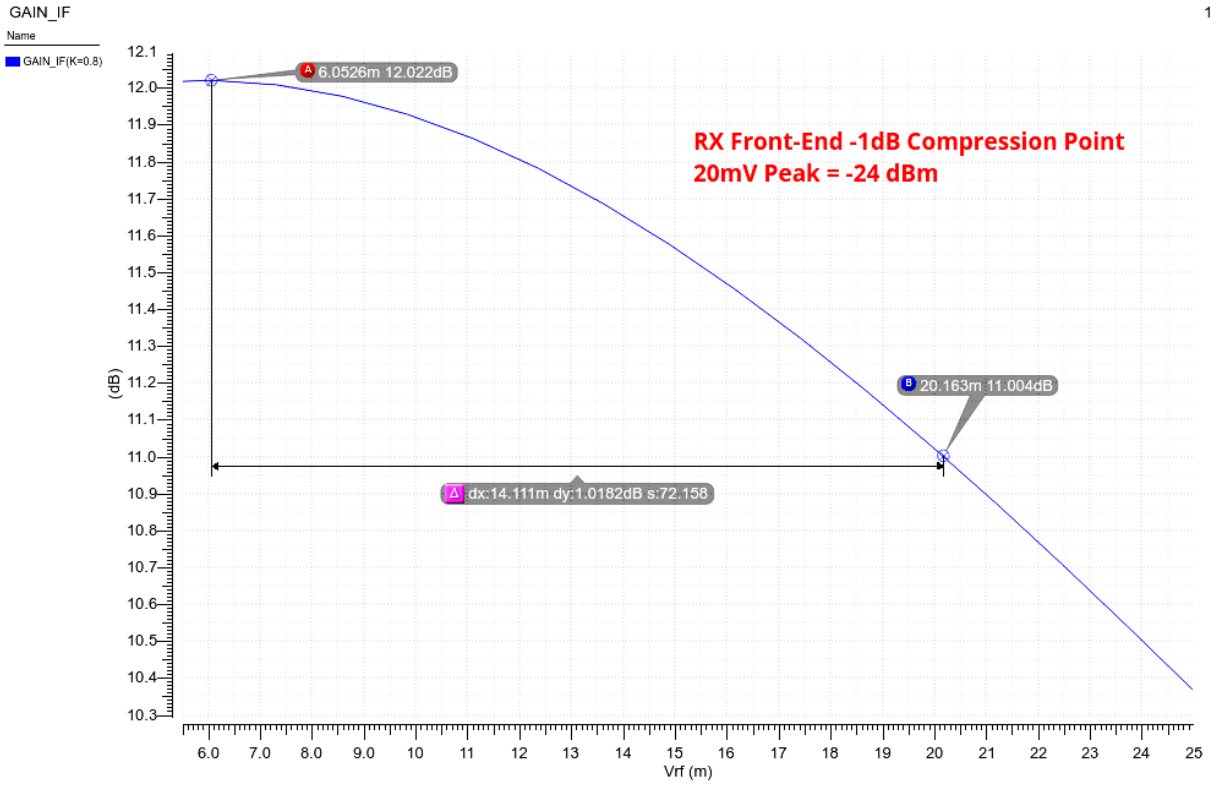
RX Front End I, Q LO Mixer Gate Waveforms



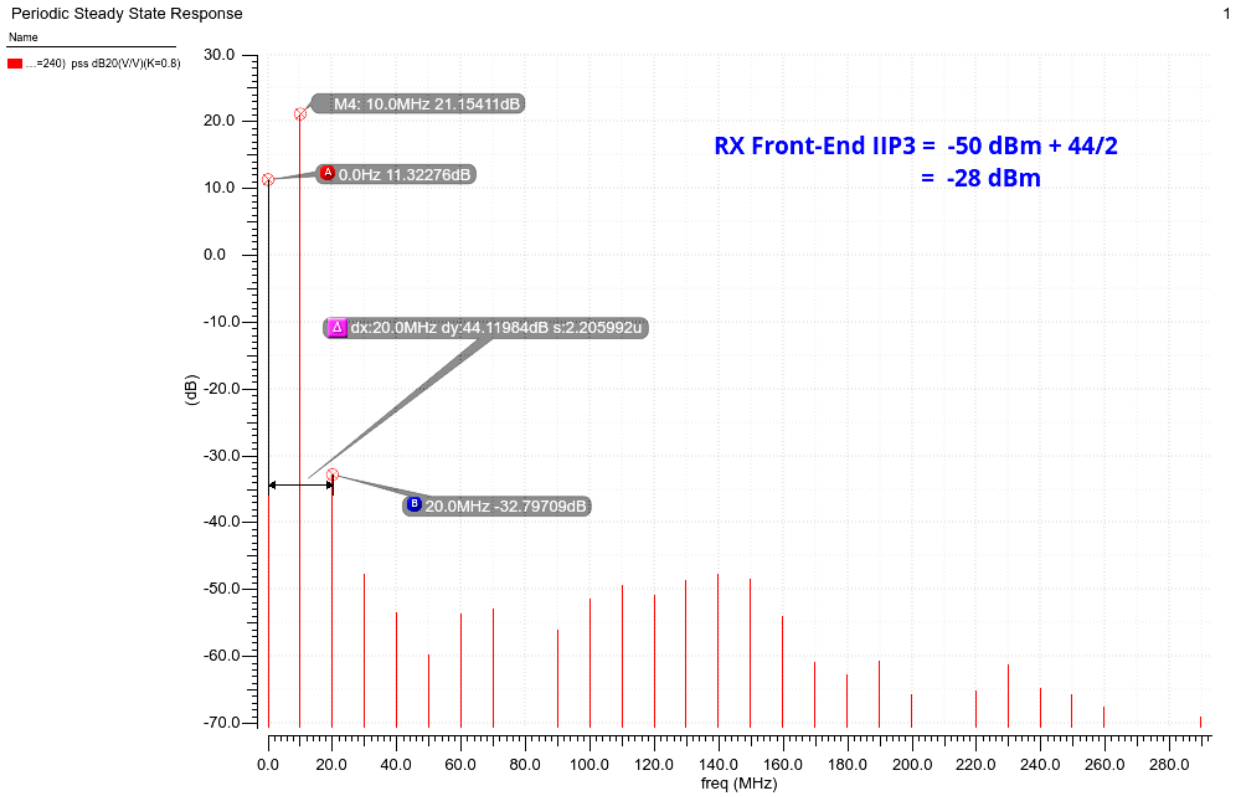
RX Front End PSS Gain



RX Front End 1dB Compression Point :



RX Front End IIP3 :



RX Front End NF Across 40MHz Base-Bandwidth :