# Ganesh Vhatkar

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Objective: To learn, work & contribute in the field of circuit design with a skilled team of engineers that is determined to create marvelous technological advancement for a better future

## EDUCATION

**OREGON STATE UNIVERSITY**
MEng in Electrical & Computer Engineering
Analog/mixed-signal/serdes/rf circuits design & layout
Expected June 2018 | Corvallis, OR
Cum. GPA: 3.5

**UNIVERSITY OF MUMBAI**
BE in Electronics & Telecommunications
May 2016 | Mumbai, India
Cum. GPA: 7.15

## COURSEWORK

### GRADUATE

- CMOS Integrated Circuits I & II
- Phase Lock Loop
- RF Circuit Design
- Energy Efficient VLSI Design
- VLSI System Design
- High-Performance Computer Architecture
- Inter-Connection Networks

## SKILLS

### TECHNICAL SKILLS

- Cadence
- Virtuoso
- Spectre
- Mentor Calibre
- HSPICE
- CosmoScope
- System Verilog
- Matlab
- Digital Oscilloscope

### SOFT SKILLS

- Persistent
- Punctual
- Self-Motivated
- Team-Player
- Creative
- Focused
- Strategic

## EXPERIENCE

**ON SEMICONDUCTOR** |Device Development & Circuit Design Intern |June 2017 to December 2017 |

- Collaborated with the team of design & process engineers from OR, AZ, ID & CZ on projects aimed to develop Non-Volatile Memories.
- Worked on a memory tester Moving Bit-Arrays (MOBA) & Demonstrator (64Kb NVM).
- Design of Level Shifters for Low Voltage (3.3V) & High Voltage(11V). Design & Layout of Schmitt Trigger & Digital Logic gates (NAND, NOR, Inverters x16) with Floating Supply Rails.
- Layout of the Colum Driver & Layout of the Row-Driver Circuit.
- DRC, LVS, & post layout simulation for PEX & Antenna Diodes.

### UNIVERSITY PROJECTS

Charge Pumped Phase Locked Loop | TSMC 65nm CMOS |

- Designed a PMOS Supply regulated 8-Stage Invertor based RO-VCO for KVCO of 3 GHz/V & -107 dBc/Hz Phase Noise with 1.2V supply.
- Designed Ratioed Logic TSPC Divide by 8 across 500 MHz to 5 GHz Clk.
- CP PLL was designed for a 60° PM for Constant UGB of 6 MHz.
- NTFs analyzed in MATLAB optimizing PLL for integrated jitter of 932 fs.

RFIC LNA & LC VCO | TSMC 65nm CMOS |

- Designed 2.4GHz Source Degenerated LNA for 80MHz RF BW, S11<-12 dB,Gain of 10 dB, NF of 3 dB,IIP3 > -30 dBm within 1.2 V Supply & 1nH Bond-Wire Inductor.
- Designed 4.8GHz NMOS Cross-Coupled LC VCO for Phase Noise 125 dBc/Hz at 1 MHz offset within 1.2 V Supply. & LC Tank Quality Factor of 21, $L_{TANK}$ = 1.9 nH & $C_{TANK}$ = 450fF.

Operational Amplifiers | TSMC 180nm & 250nm CMOS |

- Designed an NMOS Gm-Boosted Folded Cascode OTA for Open Loop DC Gain of 70dB, UGB of 80MHz and 60° PM at 2.5V .
- Designed PMOS based low-power CMFB Amplifier for a 60° Phase Margin with a CM Reference of 1.25V .
- Design & Layout of ±1 V Dual Supply Miller Compensated 2 Stage Op-Amp for UGB of 200 MHz, Open-Loop DC Gain of 70 dB, 60°PM.

Personal Projects | TSMC 180nm CMOS |

- Designed a 4-stage charge multiplier Diode connected NMOS Dickson Charge Pump with parallel NMOS operated in the linear region. DC-DC boost of 4.58V with 1.5V input DC supply.
- Designed a Serializer Circuit for High-Speed SERDES consisting of TSPC Latch & a high-speed Current-Mode logic 2:1 Multiplexer. Testbench analysed in HSPICE & CosmoScope.