2-STAGE GM-BOOSTED TELESCOPIC CASCODE OP-AMP DESIGN

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ABSTRACT:

A 2-Stage Telescopic Cascode followed by Common Source (CS) Op-Amp with Gm-Booster is designed for an Open-Loop DC Gain of 94 dB for a relative gain error of 0.01% with Open-Loop -3dB BW of 5.862 KHz and Open-Loop-UGB of 293.15MHz for a settling time of 25ns (5 ns margin from 30 ns). 54 degree PM is achieved by Miller Compensation with Cm=0.7pF and Rm=2.2Kohm The Closed-Loop system consists of 1pF and 0.2pF Capacitor feedback network for a β of 0.2. The Closed-Loop gain of 5 V/V, -3dB BW of 58.63MHz and HD3 of ≤ -50 dB is achieved with a single-ended load capacitor of 2pF in IBM 120nm LV CMOS Process.

DESIGN INTRODUCTION:

OPERATIONAL AMPLIFIER:

Operational amplifiers (op amps) are an integral part of many analog and mixed-signal systems. Op amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering. The design of op amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. We loosely define an op amp as a "high-gain differential amplifier." By "high," we mean a value that is adequate for the application, typically in the range of 10 to 10,000. Since op amps are usually employed to implement a feedback system, their open-loop gain is chosen according to the precision required of the closed-loop circuit.

Up to three decades ago, most op amps were designed to serve as "general-purpose" building blocks, satisfying the requirements of many different applications. Such efforts sought to create an "ideal" op amp, e.g., with a very high voltage gain (several hundred thousand), high input impedance, and low output impedance, but at the cost of many other aspects of the performance, e.g., speed, output voltage swings, and power dissipation.

By contrast, today's op amp design proceeds with the recognition that the trade-offs between the parameters eventually require a multi-dimensional compromise in the overall implementation, making it necessary to know the adequate value that must be achieved for each parameter. For example, if the speed is critical while the gain error is not, a topology is chosen that favours the former, possibly sacrificing the latter.

GAIN

The open-loop gain of an op amp determines the precision of the feedback system employing the op amp. As mentioned before, the required gain may vary by four orders of magnitude according to the application. Trading with such parameters as speed and output voltage swings, the

minimum required gain must therefore be known. Sometimes, a high open-loop gain may also be necessary to suppress nonlinearity.

$$A_{CL} = \frac{1}{\beta}\left\{1 - \frac{1}{A\beta}\right\}$$

For $\frac{1}{\beta} = 5$, the relative gain error is $\frac{1}{A\beta} = \frac{0.01}{100} = 10^{-4}$ Therefore $A = 5 * 10^4 =$ 94 dB and Loop Gain of $A\beta = 10^4 = 80$dB

SMALL-SIGNAL BANDWIDTH

The high-frequency behavior of op amps plays a critical role in many applications. For example, as the frequency of operation increases, the open-loop gain begins to drop, creating larger errors in the feedback system. The small-signal bandwidth is usually defined as the "unitygain" frequency, *fu*, which can reach several gigahertz in today's CMOS op amps. The 3-dB frequency, *f*3-dB, may also be specified to allow easier prediction of the closed-loop frequency response.

$$A_{CL} = \frac{\frac{A_0}{1 + A_0\beta}}{1 + \frac{s}{(1 + A_0\beta) * P_1}}$$

For settling time of 25ns (5 ns margin from 30 ns), The Unit Step Response gives

$$Open\ Loop - 3dB\ BW\ P_{1,CL} = (1 + A_0\beta) * P_1 = \frac{\ln(10^4)}{25nS} = 58.63\ MHz$$

$$Open\ Loop - 3dB\ BW\ P_1 = 5.863\ KHz$$

$$Open\ Loop\ UGB = A_0P_1 = 293.14\ MHz$$

LINEARITY

Open-loop op amps suffer from substantial nonlinearity. The input pair M1–M2 exhibits a nonlinear relationship between its differential drain current and its input voltage. The issue of nonlinearity is tackled by two approaches: using fully differential implementations to suppress even-order harmonics and allowing sufficient open-loop gain for the closed-loop feedback system to achieve adequate linearity. It is interesting to note that in many feedback circuits, the linearity requirement, rather than the gain error requirement, governs the choice of the open-loop gain.

GM-BOOSTING AUXILLARY AMPLIFIER

The limited gain of the one-stage op amps and the difficulties in using two-stage op-amps at high speeds have motivated extensive work on new topologies. In one-stage op amps, such as telescopic and folded-cascode topologies, the objective is to maximize the output impedance so as to attain a high voltage gain. The idea behind gain boosting is to further increase the output impedance without adding more cascode devices. We neglect body effect for simplicity, but it can be readily included at the end.

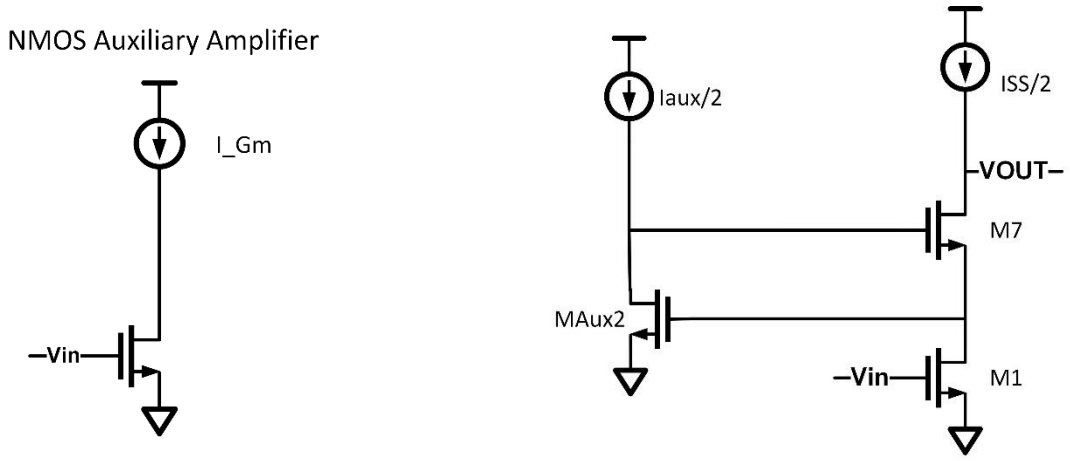


Fig.1a

We deal with the implementation of the auxiliary amplifier in the regulated cascode and extend the gain-boosting technique to op amps. The simplest realization of A1 is a common-source stage, as shown in Fig.1a. If I1 is ideal, then |A1| = gm3rO3, yielding |Vout/Vin|≈gm1rO1gm2rO2(gm3rO3+1), as in a triple cascode. However, this topology limits the output voltage swing because the minimum voltage at node P is dictated by VGS3 rather than the overdrive of M1. We note that Vout must remain above VGS3 + (VGS2 − VT H2) here

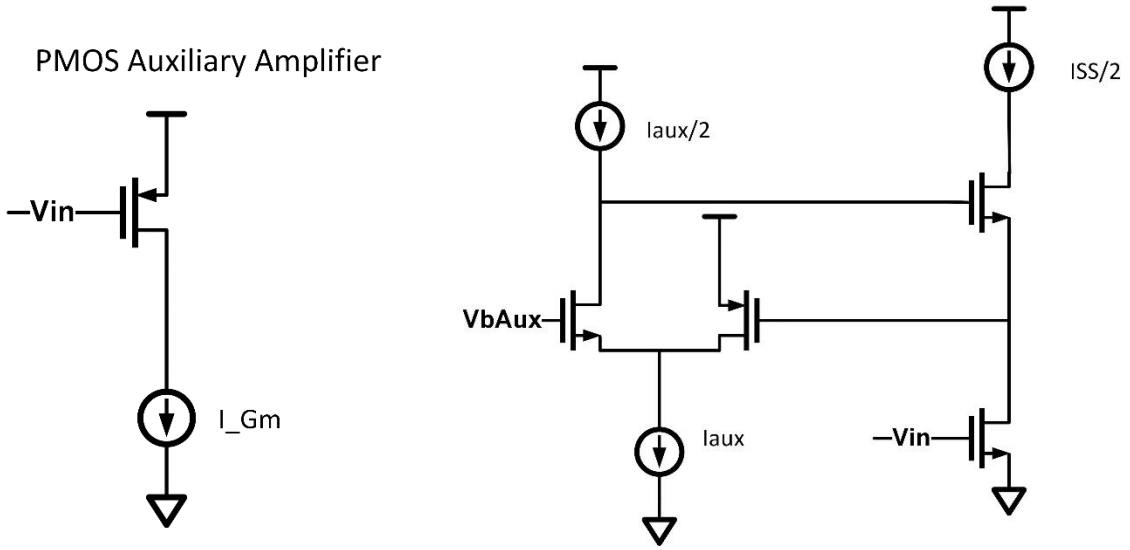


Fig. 1b.

To avoid this headroom limitation, we consider a PMOS common-source stage for A1. The analysis implies that we must insert one more stage in the feedback loop so as to reach compatible bias levels between consecutive stages. Let us interpose an NMOS common-gate stage between M3 and the gate of M2. The reader recognizes the resulting A1 topology as a folded cascode, but we also observe that M4 provides an upward level shift from its source to its drain, allowing VG to be higher than the drain voltage of M3.

TELESCOPIC CASCODE (FIRST-STAGE)

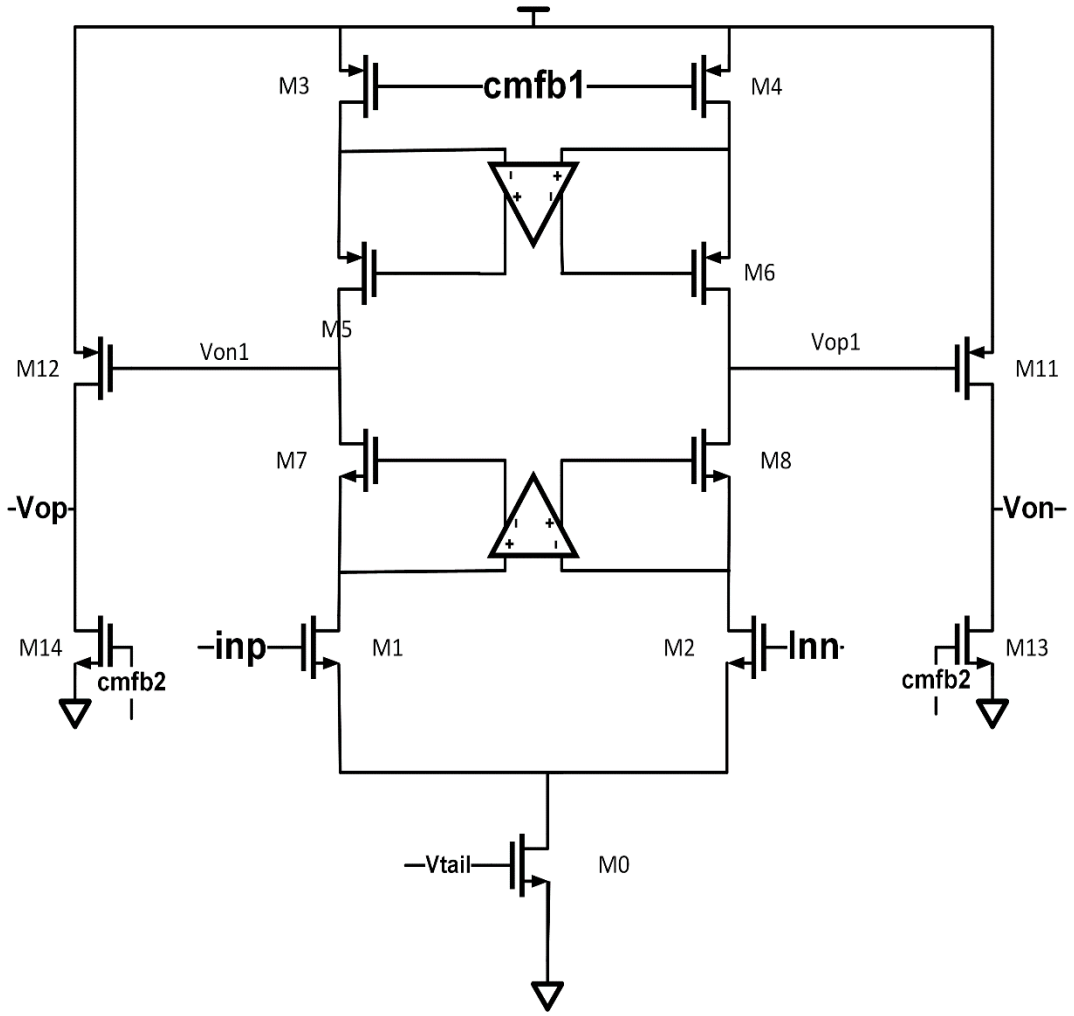


Fig. 2

Gain of Telescopic cascode amplifier is given as;

$$\frac{gm1}{\frac{gds1 * gds7}{gm7} + \frac{gds5 * gds3}{gm5}}$$

Output swing Limitations;

$$V_{Dsat8} + V_{Dsat2} + V_{Tail} \leq V_{out} \leq V_{DD} - V_{Dsat4} - V_{Dsat6}$$

Input CM swing limitations;

$$V_{GS1} + V_{Tail} \leq V_{CM} \leq V_{G7} - V_{GS7} - V_{th1}$$

TWO STAGE OPAMP

The op amps studied thus far exhibit a "one-stage" nature in that they allow the small-signal current produced by the input pair to flow directly through the output impedance, i.e., they perform voltage-to-current conversion only once. The gain of these topologies is therefore limited to the product of the input pair transconductance and the output impedance. We have also observed that cascoding in such circuits increases the gain while limiting the output swings.

In some applications, the gain and/or the output swings provided by cascode op amps are not adequate. For example, a modern op amp must operate with supply voltages as low as 0.9 V while delivering single ended output swings as large as 0.8 V. In such cases, we resort to "two-stage" op amps, with the first stage providing a high gain and the second, large swings. In contrast to cascode op amps, a two-stage configuration isolates the gain and swing requirements.

Each stage can incorporate various amplifier topologies studied in previous sections. To obtain a higher gain, the first stage can incorporate cascode devices, but the second stage is typically configured as a simple common-source stage so as, to allow maximum output swings.

The overall voltage gains of Fig.2 can be expressed as,

$$\frac{gm1}{\frac{gds1*gds7}{gm7}+\frac{gds5*gds3}{gm5}} * \frac{\boldsymbol{gm11,12}}{\boldsymbol{gds11,12+gds13,14}}$$

COMMON-MODE FEEDBACK AMPLIFIER

In high-gain amplifiers, the output CM level is sensitive to device properties and mismatches and it cannot be stabilized by means of *differential* feedback. Thus, a common-mode feedback network must be added to sense the CM level of the two outputs and adjust one of the bias currents in the amplifier. Here, we divide the task of CMFB into three operations: sensing the output CM level, comparison with a reference, and returning the error to the amplifier's bias network. Figure 3 conceptually illustrates the idea.

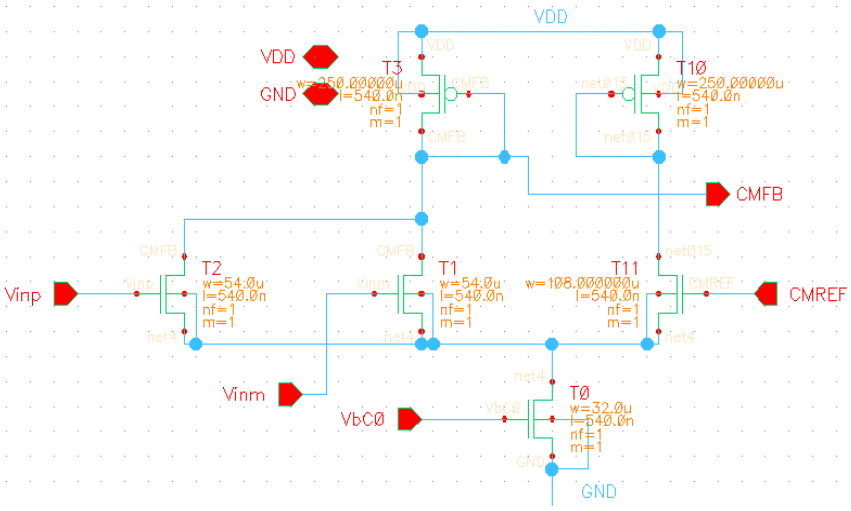


Fig. 3

CMFB LOOP CURRENT GAIN

$$gmc1\left[\frac{\boldsymbol{Vop+Vom}}{\mathbf{2}} - vocm\right] = \frac{gmc1}{2}[Vop - vocm] + \frac{gmc1}{2}[Von - vocm]$$

COMMON-MODE SENSING

In order to sense the output CM level, we recall that *Vout, CM = (Vout*1+*Vout*2*)/*2, where *Vout*1 and *Vout*2 are the single-ended outputs. It therefore seems plausible to employ a resistive divider as shown in figure 4 below, generating *Vout, CM = (R*1*Vout*2 + *R*2*Vout*1*)/(R*1 + *R*2*)*, which reduces to *(Vout*1 + *Vout*2*)/*2 if *R*1 = *R*2. The difficulty, however, is that *R*1 and *R*2 must be much greater than the output impedance of the op-amp so as to avoid lowering the open-loop gain.

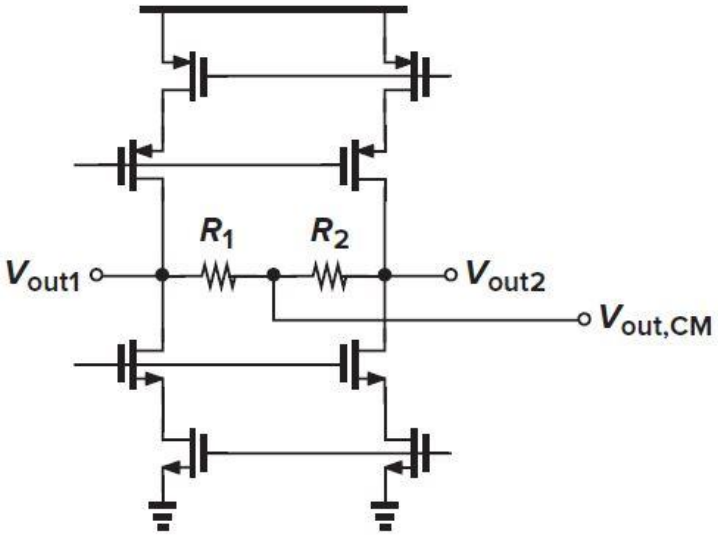


Fig.4

To eliminate the resistive loading, we can interpose source followers between each output and its corresponding resistor. This technique shown in figure below, produces a CM level that is in fact lower than the output CM level by *VGS*7,8, but this shift can be taken into account in the comparison operation. Note that *R*1 and *R*2 or *I*1 and *I*2 must be large enough to ensure that *M*7 or *M*8 is not "starved" when a large differential swing appears at the output. As conceptually depicted in Fig. 5, if, say, *Vout*2 is quite higher than *Vout*1, then *I*1 must sink both *IX* ≈ *(Vout*2 – *Vout*1*)/(R*1 + *R*2*)* and *ID*7. Consequently, if *R*1 + *R*2 or *I*1 is not sufficiently large, *ID*7 drops to zero and *Vout, CM* no longer represents the true output CM level.

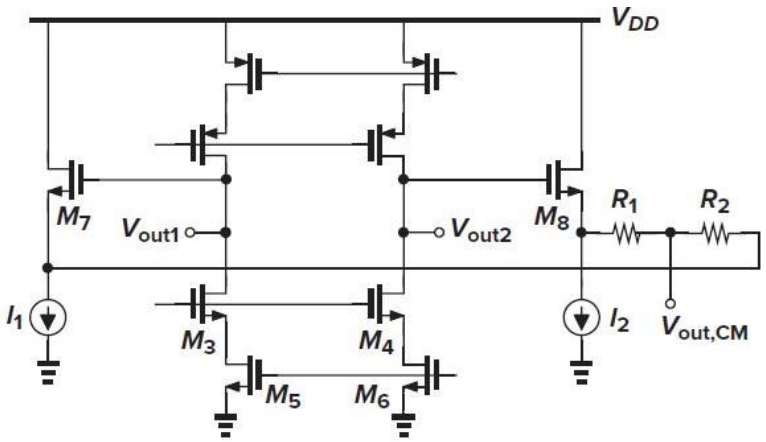


Fig. 5

CM FEEDBACK TECHNIQUES

We employ a simple amplifier to detect the difference between *Vout, CM* and a reference voltage, *VREF*, applying the result to the NMOS current sources with negative feedback. If both *Vout*1 and *Vout*2 rise, so does *VE*, thereby increasing the drain currents of *M*3–*M*4 and lowering the output CM level. In other words, if the loop gain is large, the feedback network forces the CM level of *Vout*1 and *Vout*2 to approach *VREF*. Note that the feedback can be applied to the PMOS current sources as well. Also, the feedback may control only a fraction of the current to allow optimization of the settling behavior. For example, each of *M*3 and *M*4 can be decomposed into two parallel devices, one biased at a constant current and the other driven by the error amplifier.

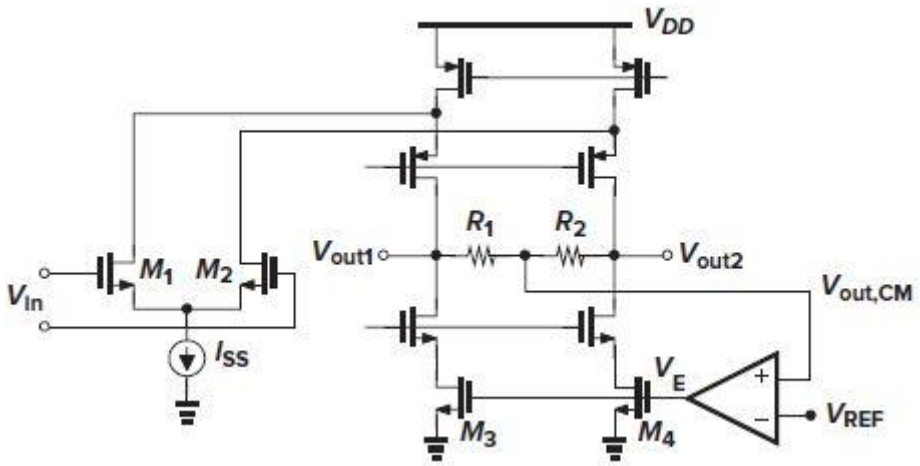


Fig.6

CMFB IN TWO-STAGE OP AMPS

Offering nearly rail-to-rail output swings, two-stage op amps find wider application than other topologies in today's designs. However, such op amps require more complex common-mode feedback. To understand the issues, we consider three different CMFB methods in the context of the simple circuit shown below.

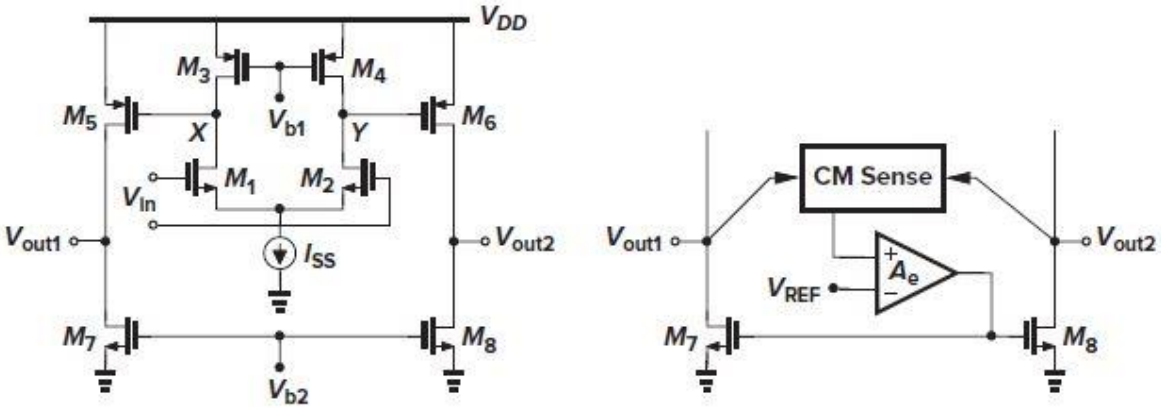


Fig.7

First, suppose the CM level of *Vout*1 and *Vout*2 is sensed and the result is used to control only *Vb*2; i.e., the second stage incorporates CMFB, but not the first stage. In this case, no mechanism exists that controls the CM level at *X* and *Y*. For example, if *ISS* happens to be less than the sum of the currents that *M*3 and *M*4 wish to draw, then *VX* and *VY* rise, driving these transistors into the triode region so that *ID*3 + *ID*4 eventually becomes equal to *ISS*. This effect also reduces |*VGS*5,6|,

establishing in*M*5–*M*8 a current that maybe well below the nominal value. This CMFB method is therefore not desired.

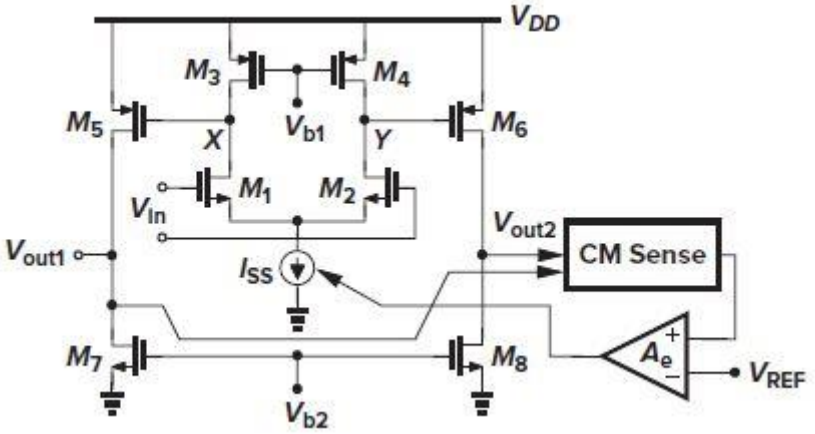


Fig.8

Second, we still sense the CM level *Vout*1 and *Vout*2 but return the result to the first stage, e.g., to *ISS.* Suppose, for example, that *Vout*1 and *Vout*2 begin too high. Then, the error amplifier, *Ae*, reduces *ISS*, allowing *VX* and *VY* to rise, |*ID*5| and |*ID*6| to fall, and *Vout*1 and *Vout*2 to go down. It is interesting to note that here *M*5 and *M*6 in fact sense the CM level at *X* and *Y*, helping the global loop control both stages' CM level. (If *M*3 and *M*4 had a tail current, as in a regular differential pair, this property would vanish and the CMFB loop would fail.)

If the first stage incorporates a telescopic cascode to achieve a high gain, then the CMFB loops can be realized as shown in Fig. 9. While not precise, the CM sensing of *X* and *Y* avoids loading the high impedances at these nodes, thereby maintaining a high voltage gain.

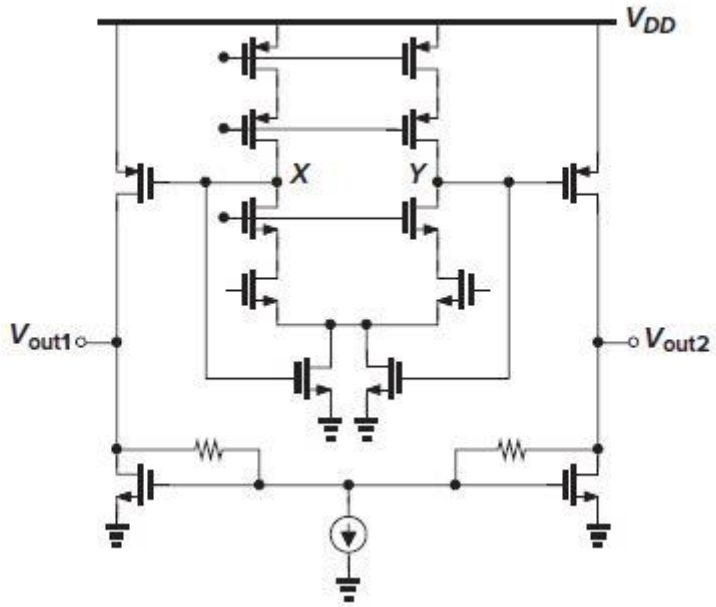
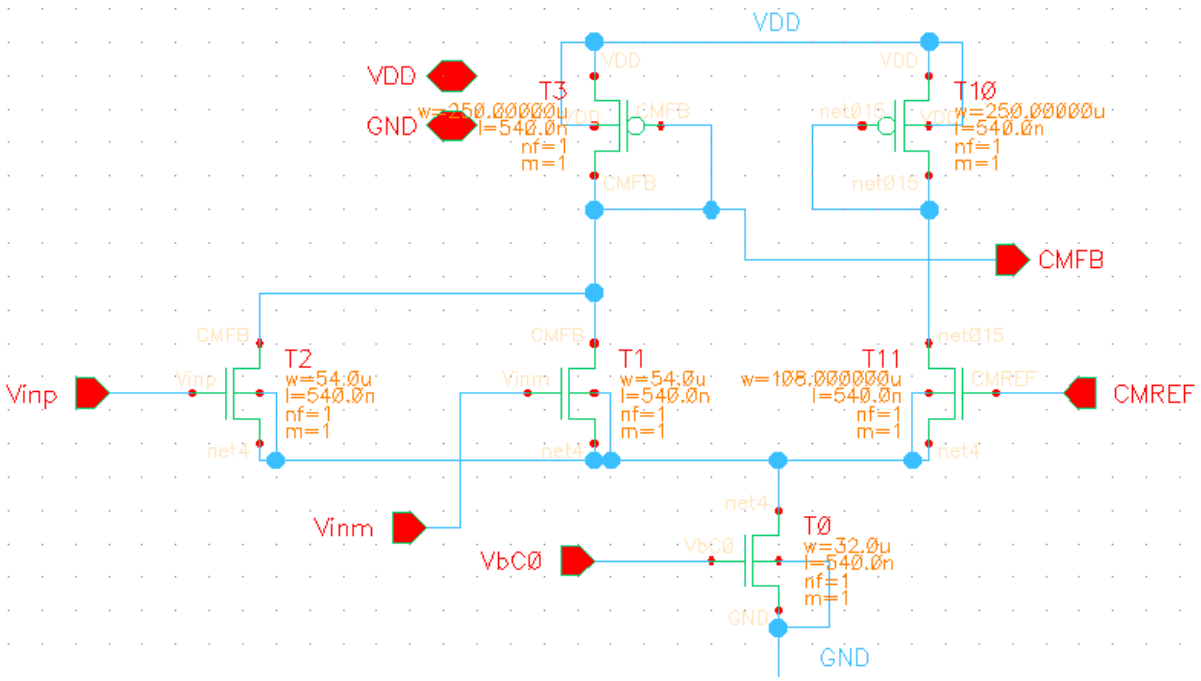


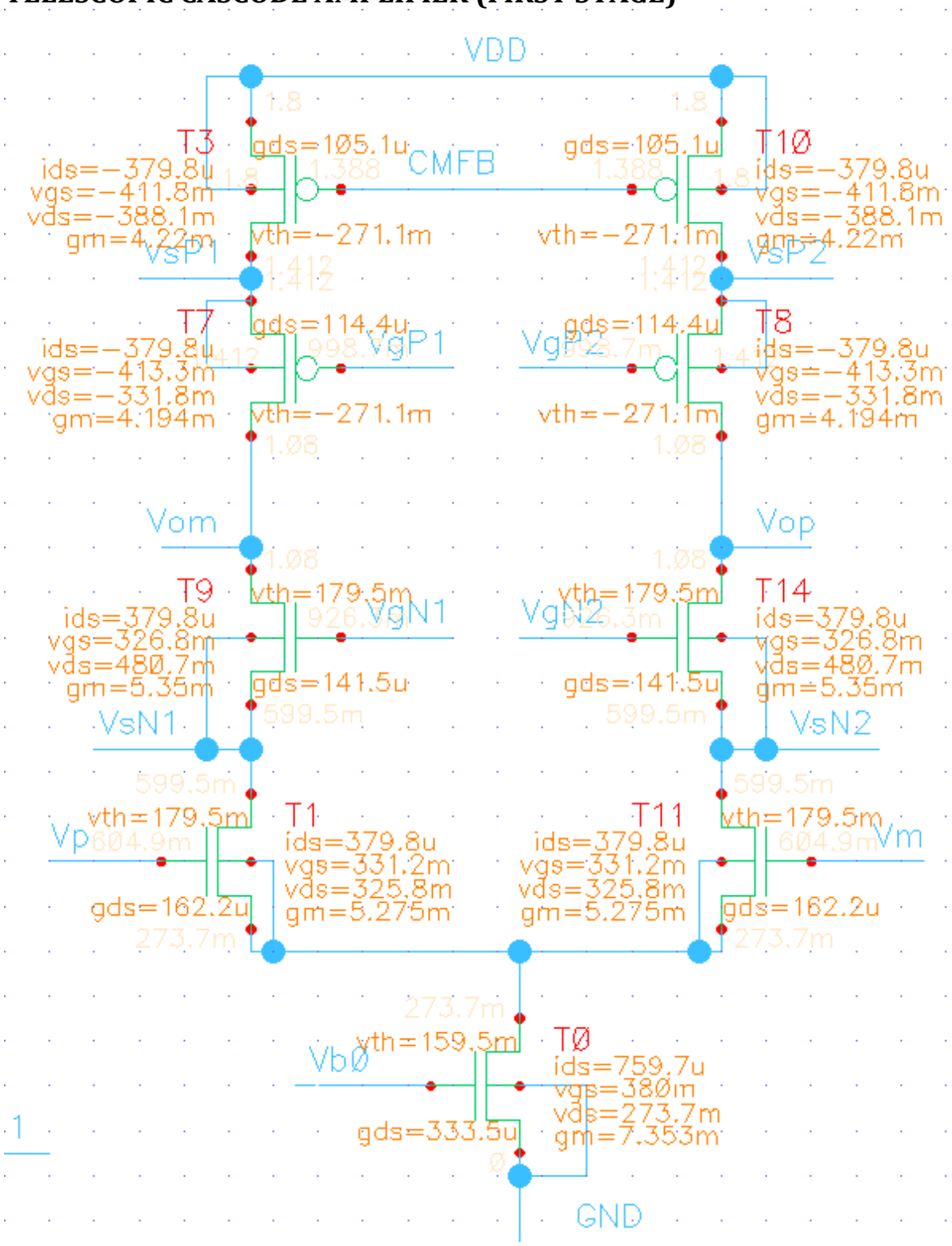
Fig.9



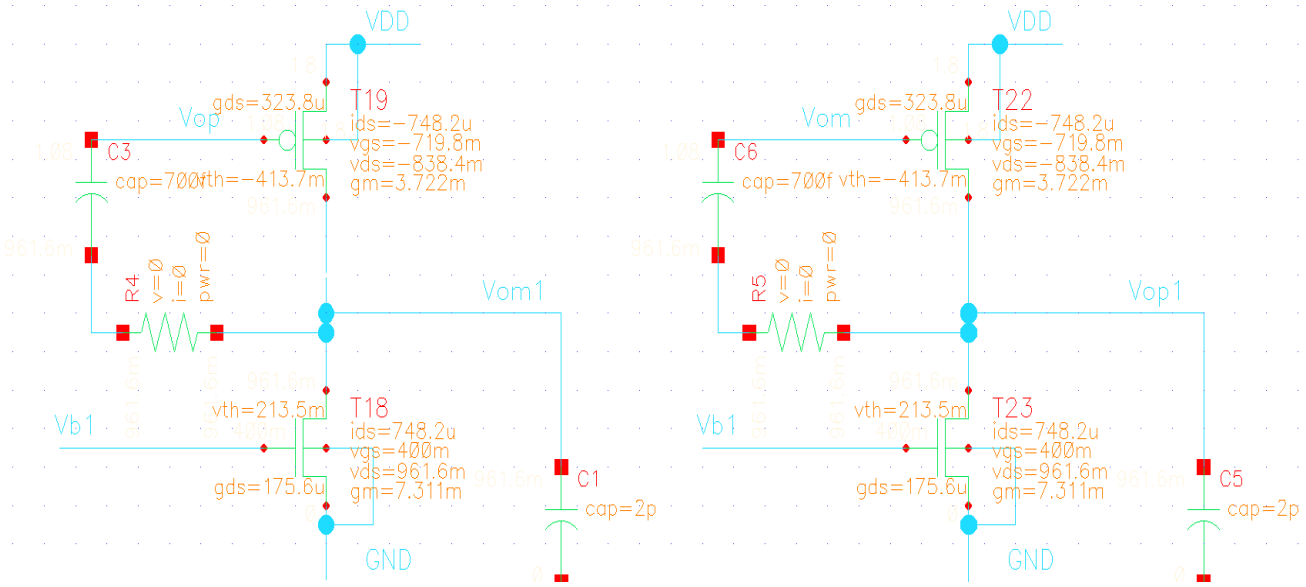
Parameter	Specs	SCM
Input Supply	1.8 V	1.8 V
Max Current	Min	
Closed Loop Gain	5	5
β	1/5=0.2	0.2 (with Cpara, **β=0.133**)
Open Loop A0	50,000=94 dB	100 dB
Loop Gain A0β	6,665=76.5 dB	79.2 dB
Relative Gain Error	0.01 %	0.01%
Settling Time	30 nS	26.6 nS
HD3	≤ -50 dB	-56 dB
Closed Loop -3dB BW	58.63 MHz	
Open Loop A -3dB BW	5.863 KHz	
Open Loop A UGB	293.15 MHz	674 MHz
CMRR @ DC		310 dB
Loop Gain A0β PM		54 degree
Loop Gain A0β GM		---

SCHEMATICS WITH ANNOTATED DC VOLTAGES

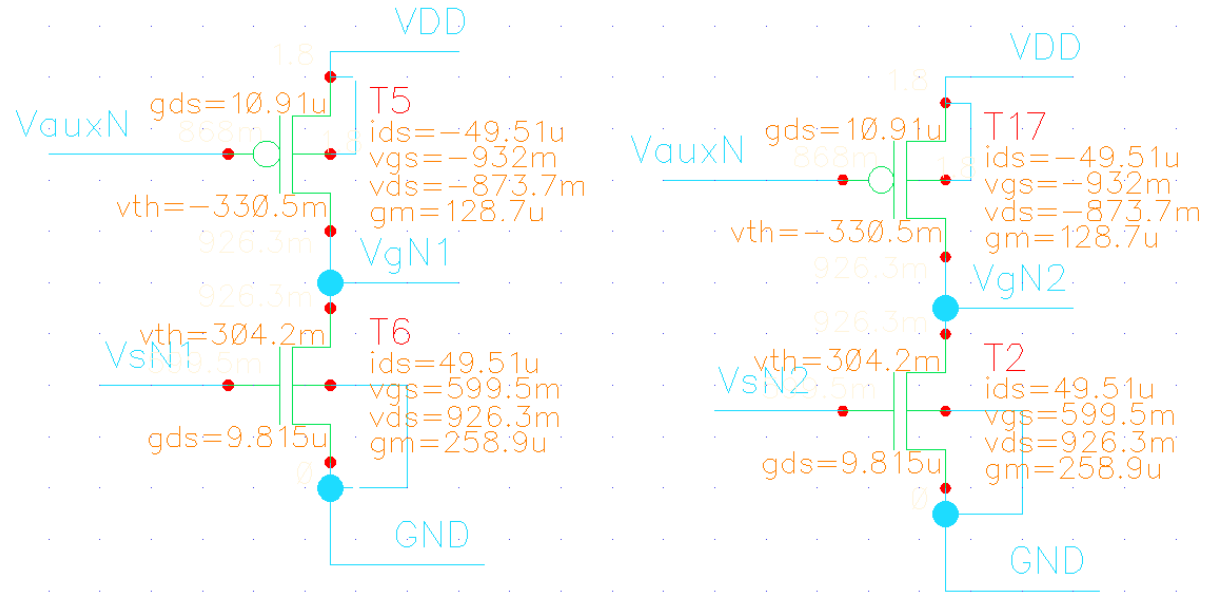
TELESCOPIC CASCODE AMPLIFIER (FIRST STAGE)



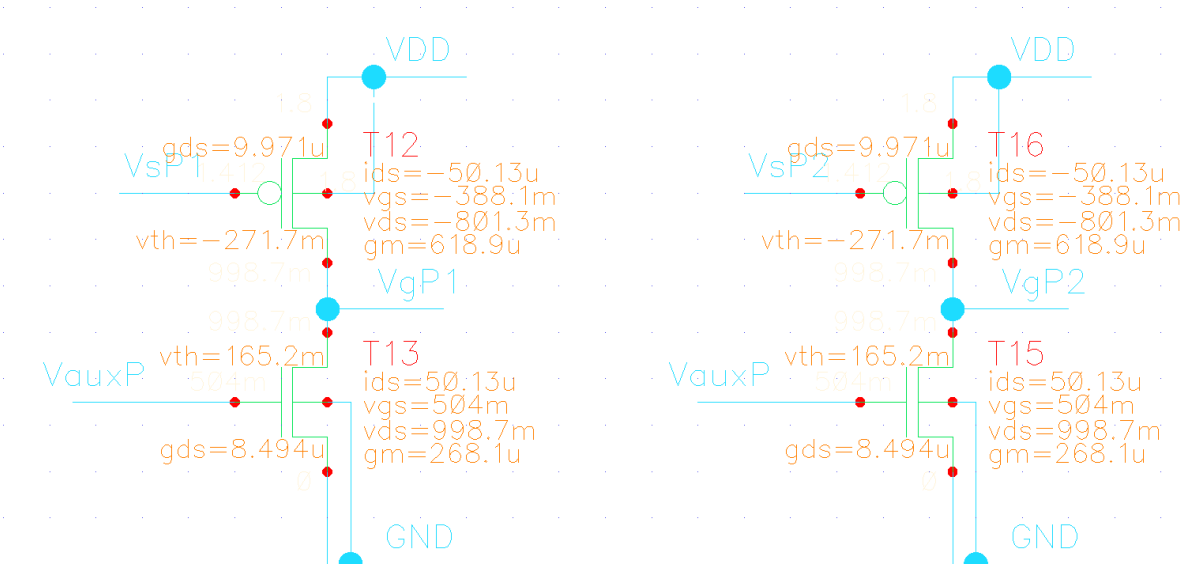
SECOND STAGE AMPLIFIER with Cm=0.7pF and Rm=2.2Kohm Miller Compensation



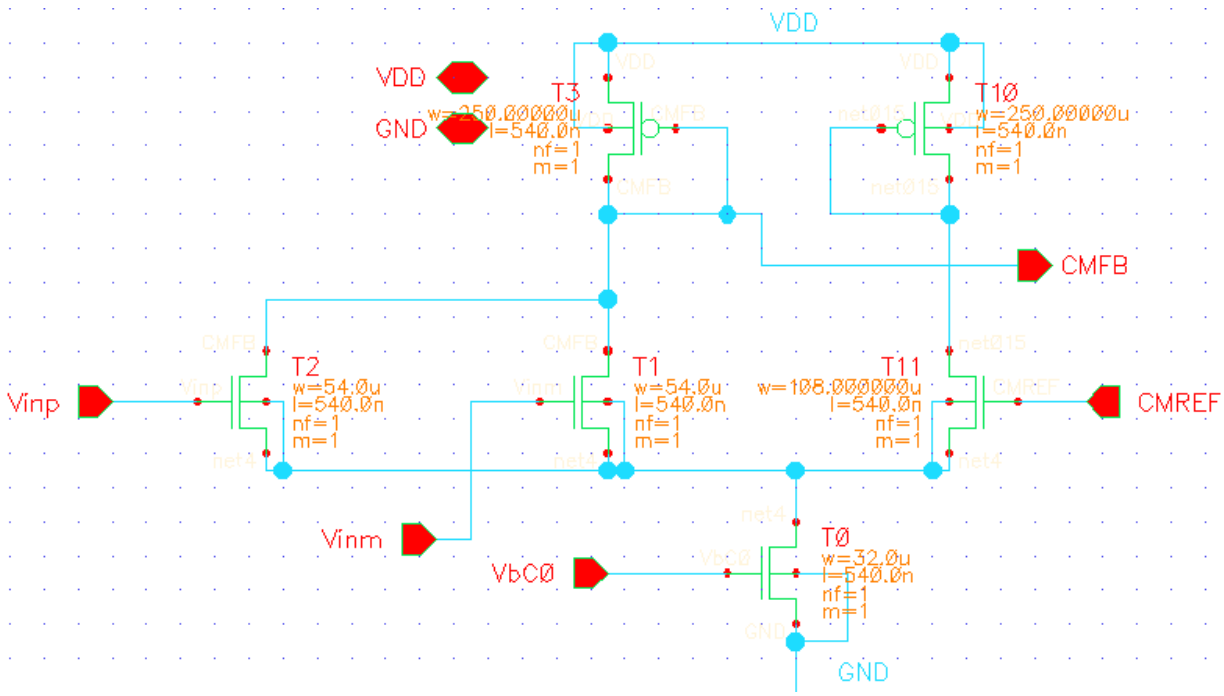
NMOS Gm-BOOSTING AMPLIFIER



PMOS Gm-BOOSTING AMPLIFIER

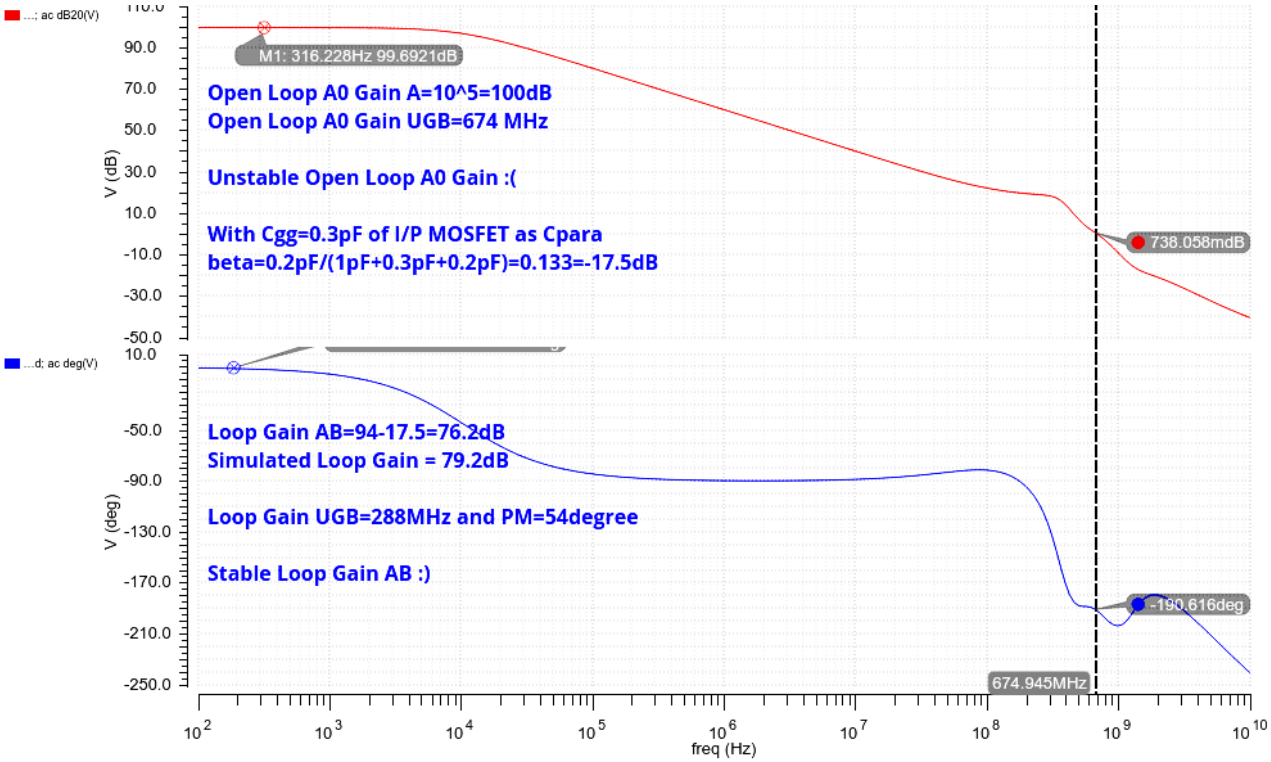


COMMON-MODE FEEDBACK AMPLIFIER

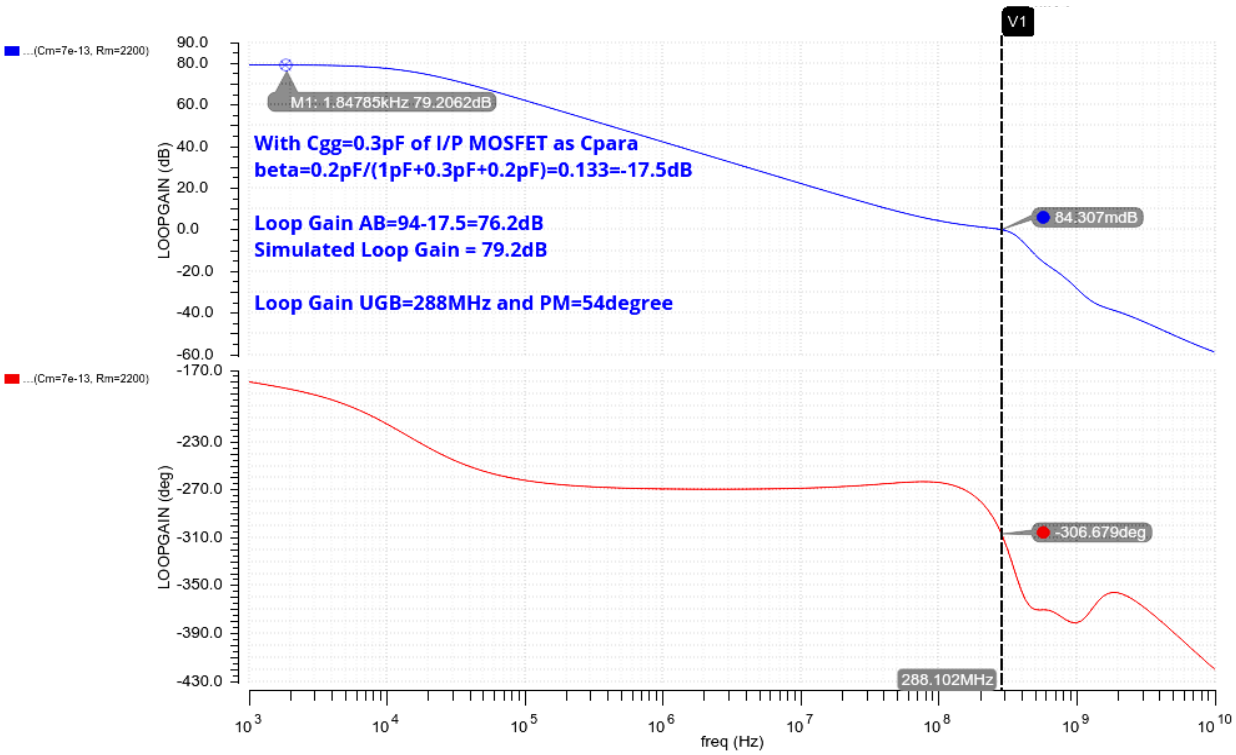


SIMULATION RESULTS

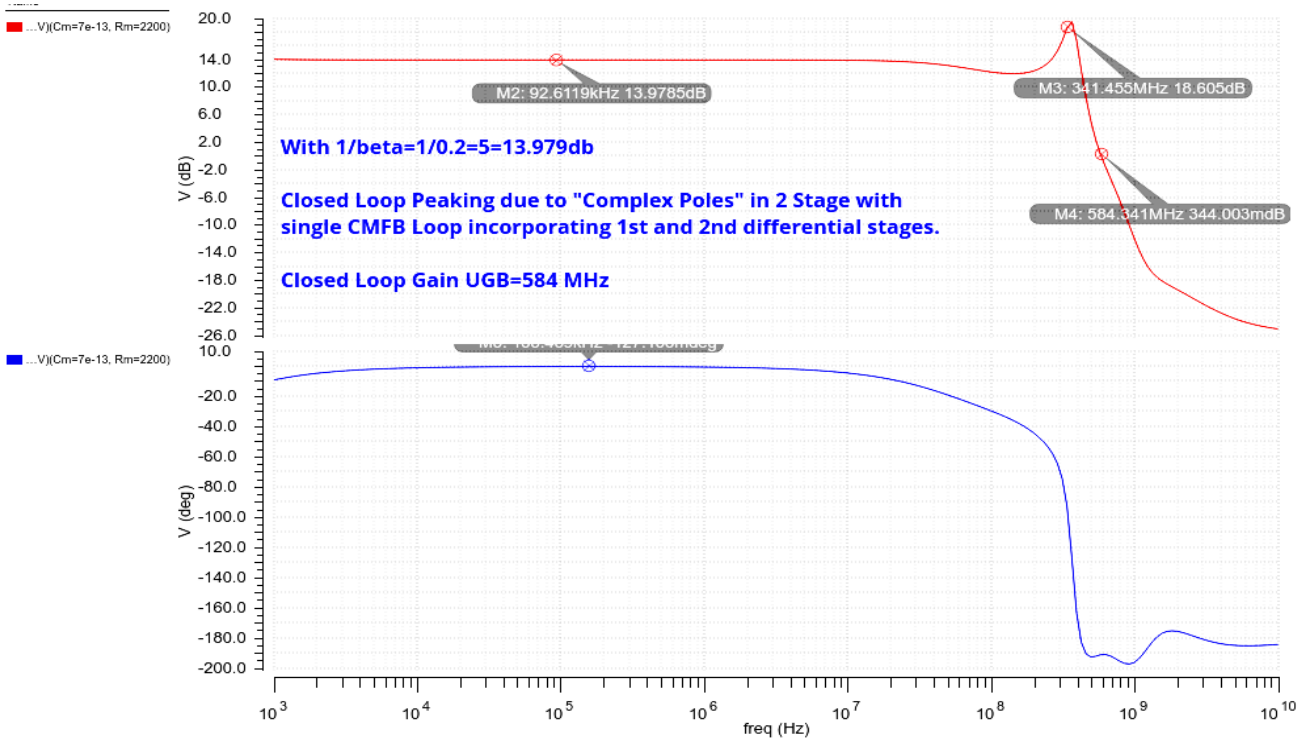
OPEN-LOOP GAIN



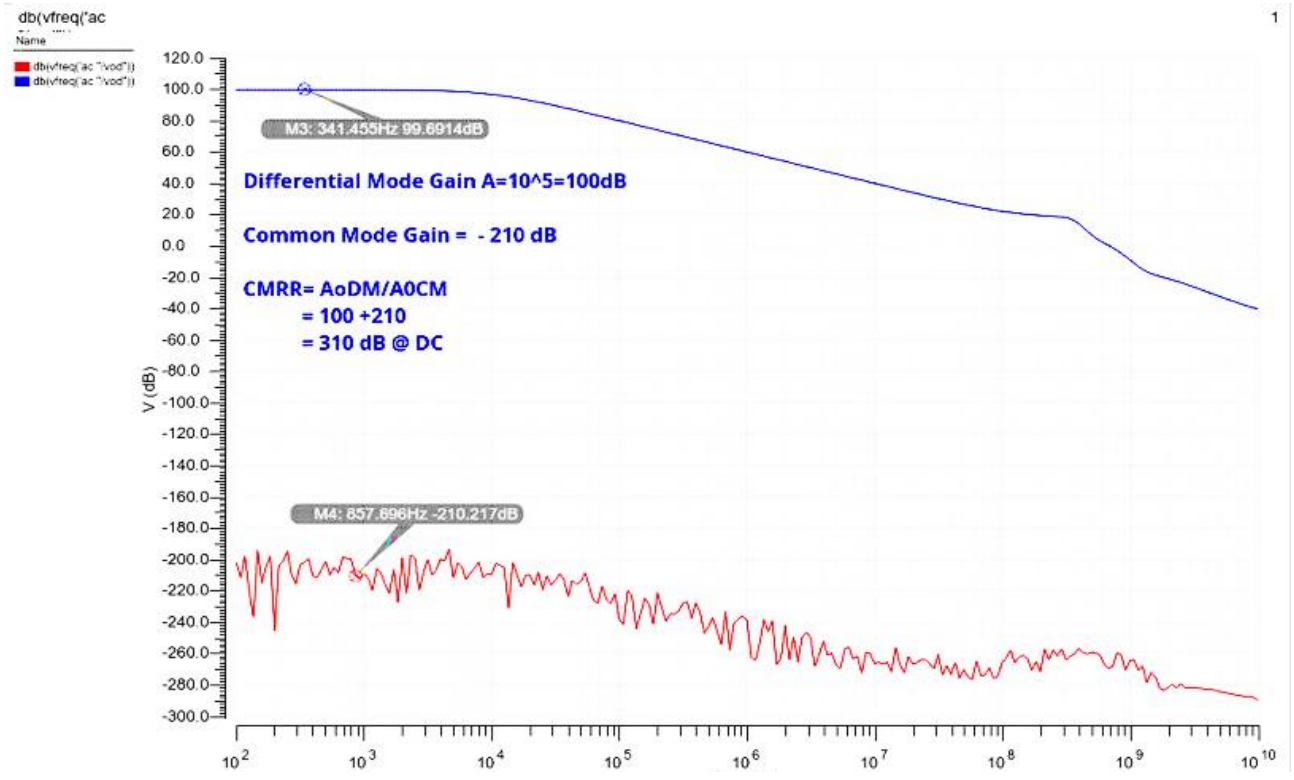
LOOP-GAIN



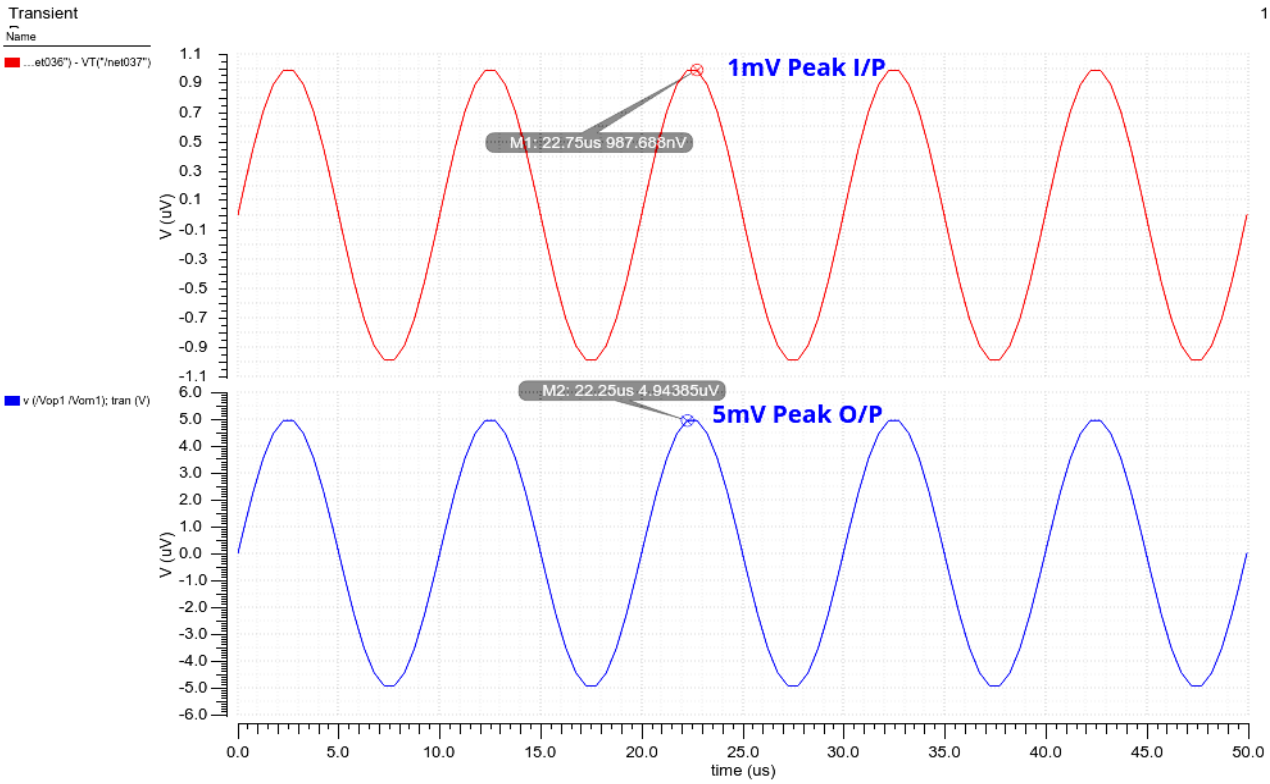
CLOSED-LOOP GAIN



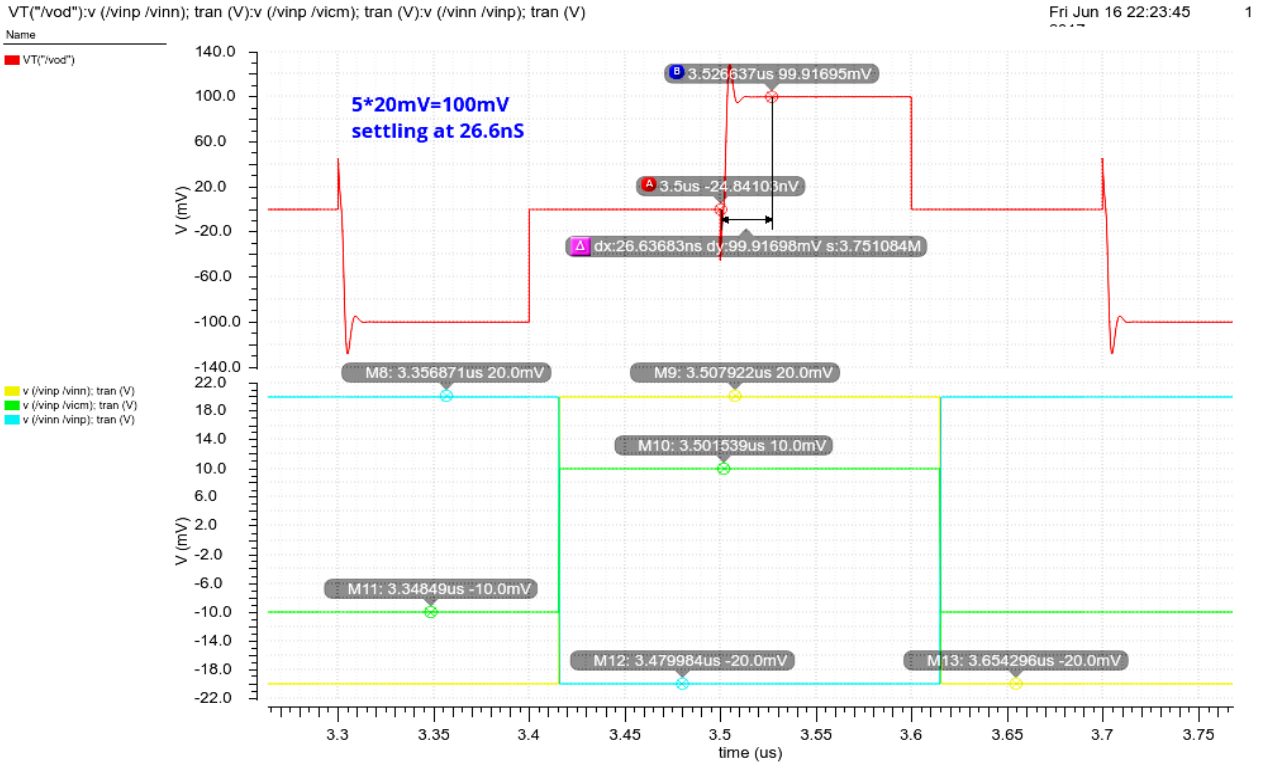
COMMON-MODE to DIFFERENTIAL-MODE REJECTION RATIO



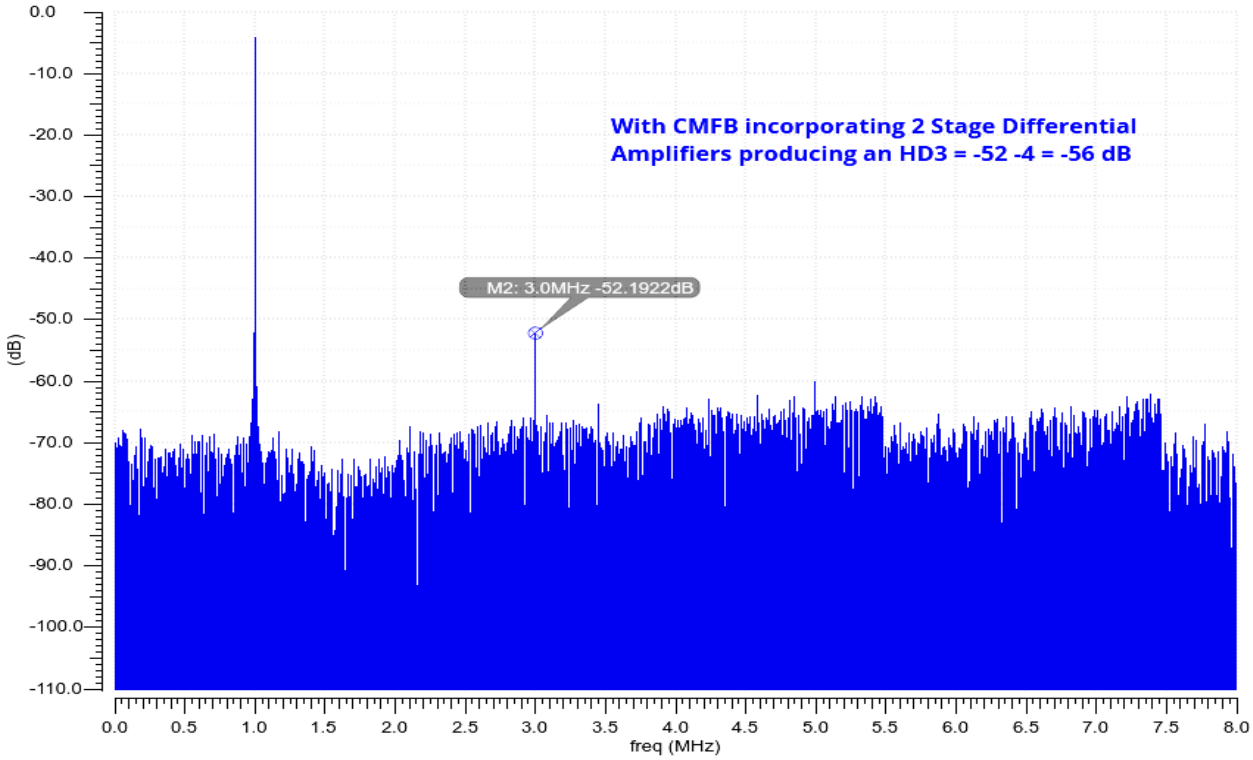
TRANSIENT SIMULATION



SETTLING TIME



HARMONIC DISTORTION



REFERENCE

1. MOSFET Sizing : Q3 of Assignment5 from IITM
   http://www.ee.iitm.ac.in/vlsi/_media/courses/ee5320_2015/assignment05.pdf
2. AIC Design from IITM
   http://nptel.ac.in/courses/117106030/
3. AIC Design from IITM
   http://www.ee.iitm.ac.in/videolectures/doku.php?id=ee5320_2015:start
4. Analysis and Design of Analog Integrated Circuits, by Paul R. Gray (Author), Paul J. Hurst (Author), Stephen H. Lewis (Author), Robert G. Meyer (Author)
5. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill