ON SEMICONDUCTOR

INTERNSHIP PROJECT REPORT

DEMONSTRATOR

GANESH VHATKAR
12/01/2017

DESCRIPTION OF THR PROJECT WORKED ON DURING THE FALL INTERNSHIP AT ON SEMICONDUCTOR, GRESHAM,OR

DEMONSTRATOR

Demonstrator is meant for I4T LogicEE M2-Phase 2. It is a fully functional memory array. It fills the gap between MoBA and IP. Memory size of 64 Kbits + parity bits. Demonstrator memory aims at improvement in reliability and area of the memory array.

BITCELL:

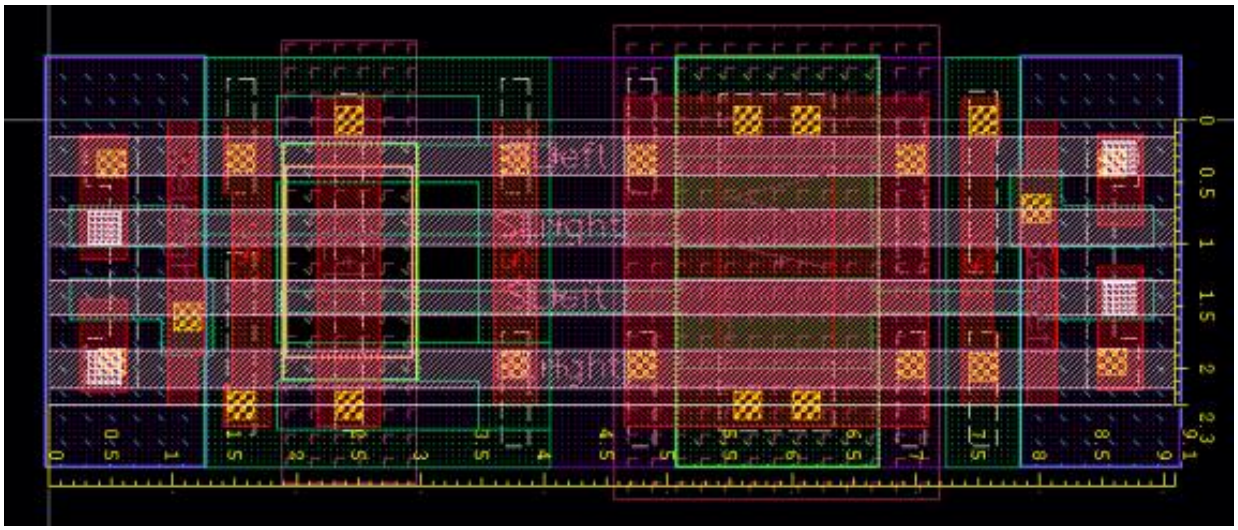


Fig.1

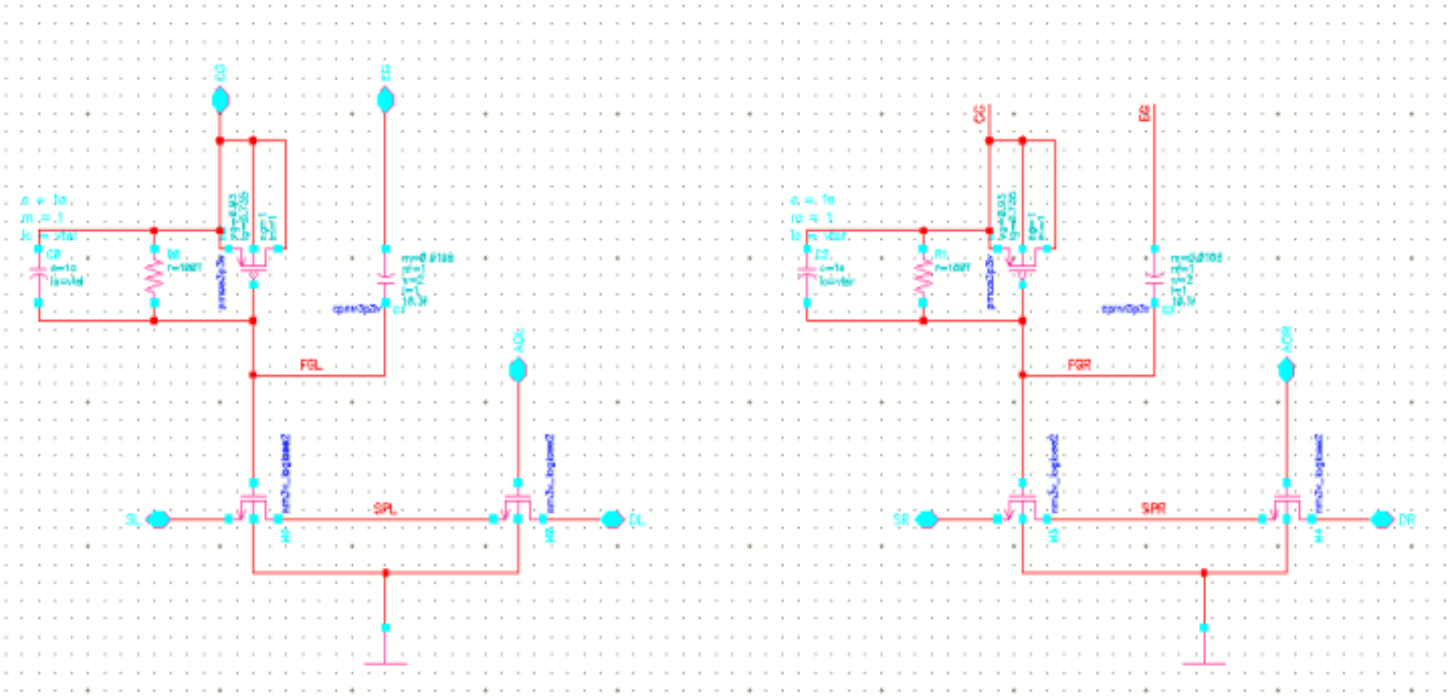


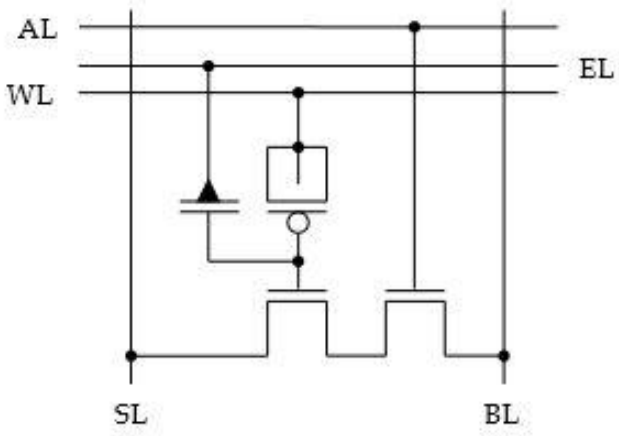
Fig.2

MEMORY CELL DESCRIPTION:

The LogicEE memory cell is made of 1) two standard NMOS, the state & the select transistors placed in series, 2) one standard PMOS, and 3) a none-linear MOS capacitor. The none-linear capacitor is a n+ implanted polysilicon gate on NWELL. The gate of the state transistor, being the floating-gate where the charges are stored, is connected to the one of the none-linear MOS capacitor and the one of the PMOS. The drain of the state transistor and the source of the select transistor are connected. The drain of the select transistor forms the drain of the memory cell. The source of the state transistor forms the source of the memory cell. The drain, source & bulk of the PMOS are tied together to form the control-gate. The NWELL of the none-linear MOS capacitor forms the erase-gate. The gate of the select transistor forms the select-gate

The onc18 LogicEE memory cell has:

- 1 NMOS state transistor,
- 1 NMOS access transistor,
- 1 PMOS-like transistor used as capacitor, and
- 1 MOS structure.
-



The terminals are:

- Bit line [BL] (drain of the access transistor),
- Source line [SL] (source of the state transistor),
- Access line [AL] (gate of the access transistor),
- Erase line [EL] (active electrode of the MOS structure),
- Word line [WL] (active electrode of the PMOS-capacitor)

The main tasks were:

- Layout of the Bit-cell
- Design and Layout of the Digital Logic Gates
- Design & Layout of Schmitt Trigger
- Design & Layout of the Low Voltage Level Shifter
- Design & Layout of the High Voltage Level Shifter
- Running rigorous simulation to verify device performance under PVT.

Digital Logic Gates:

NAND Gate with Floating Power Rails:

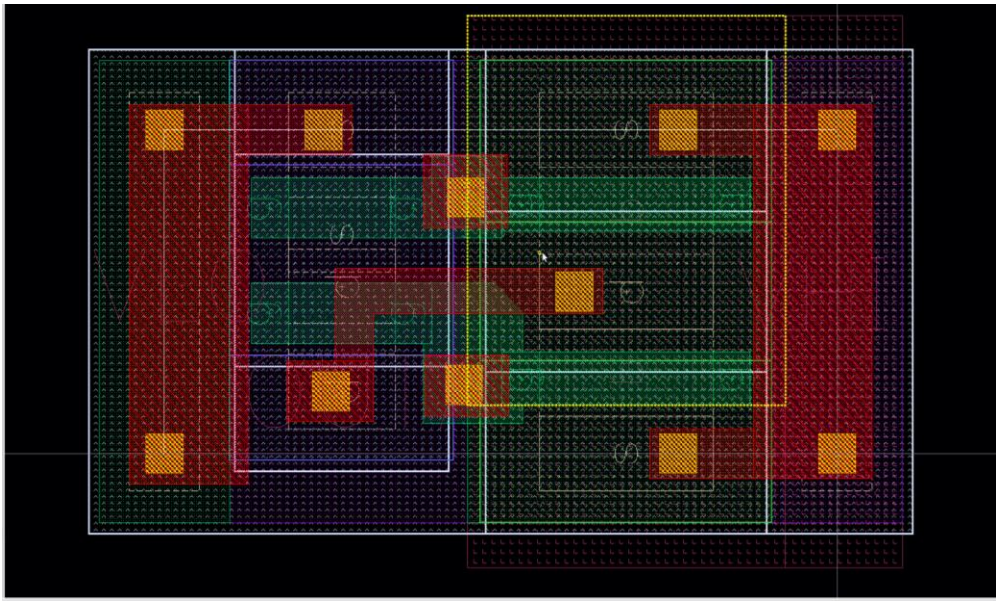


Fig. 3

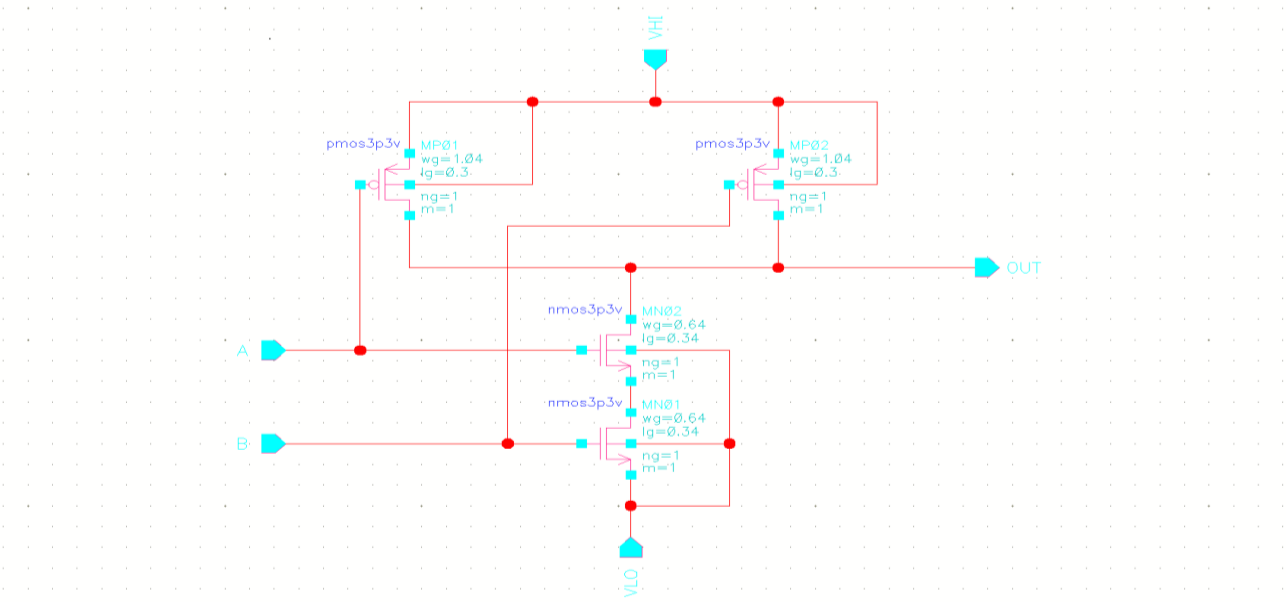


Fig.4

NOR Gate with Floating Power Rails:

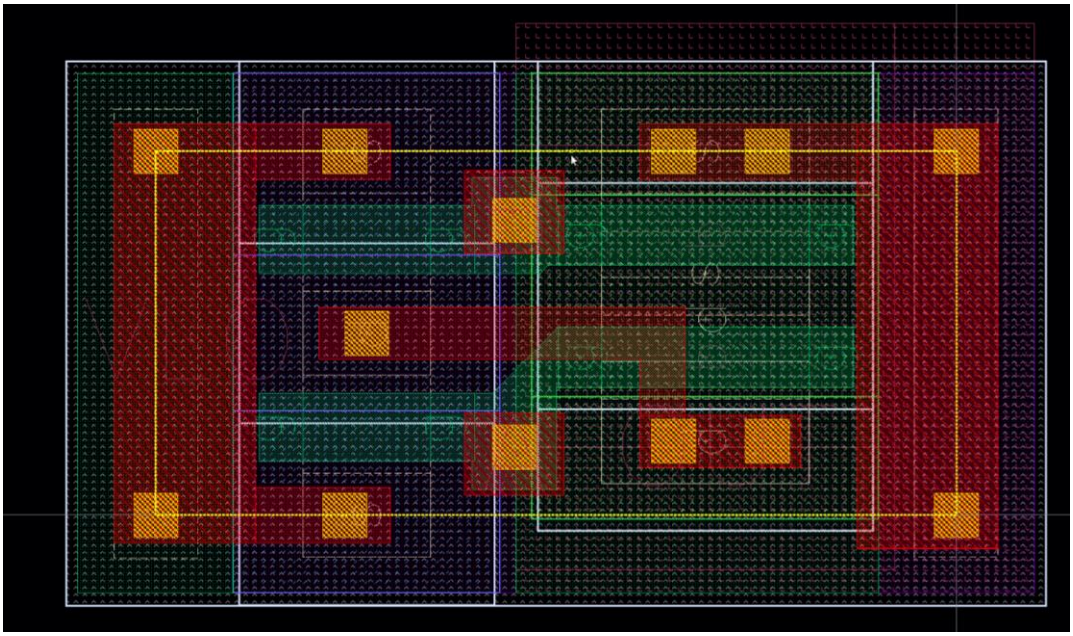


Fig.5

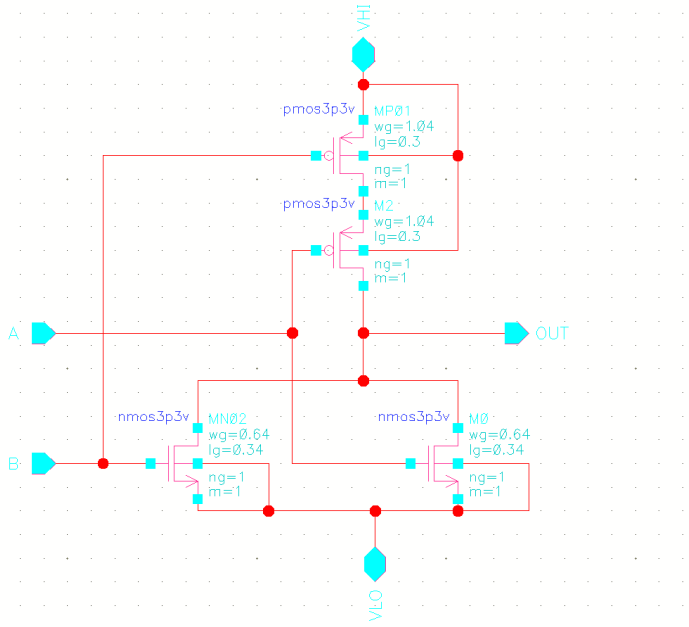


Fig.6

SCHMITT TRIGGER with Floating Power Rails:

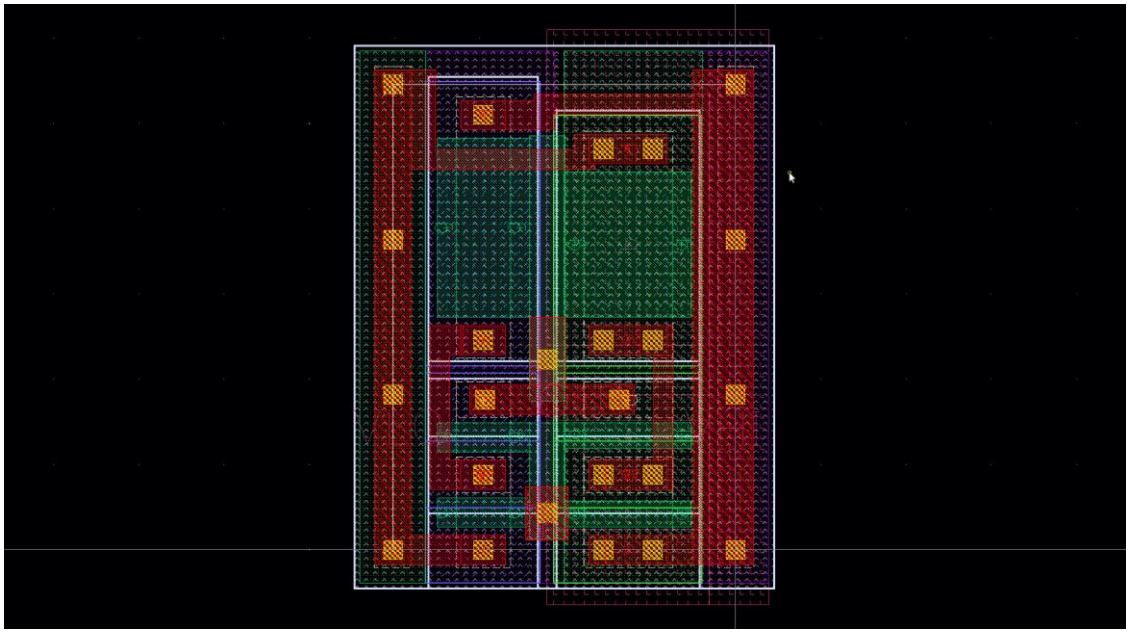


Fig.7

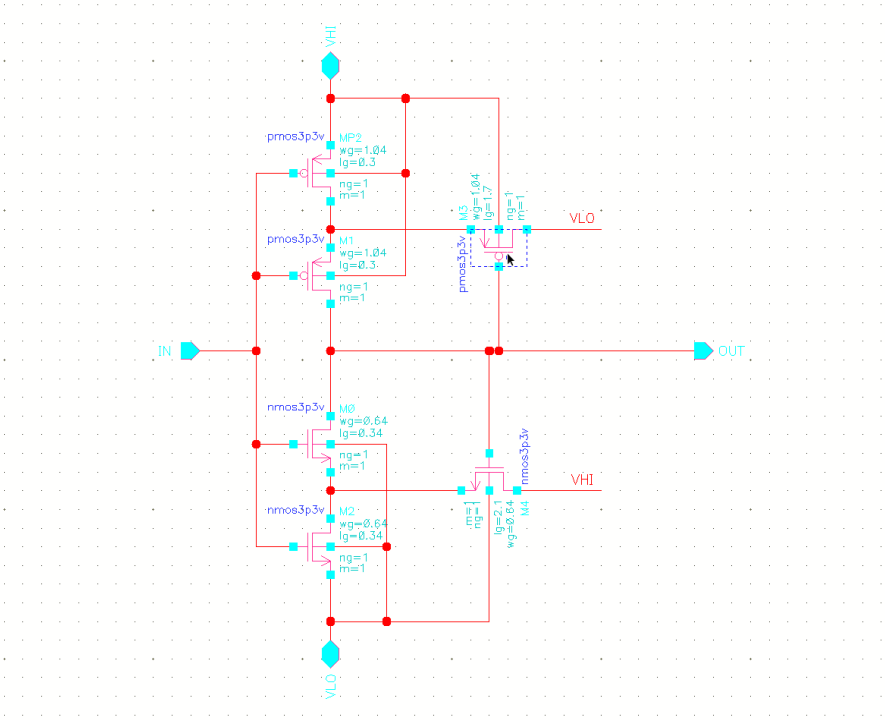


Fig.8

Level Shifter:

Low Voltage: 3.3 Volts

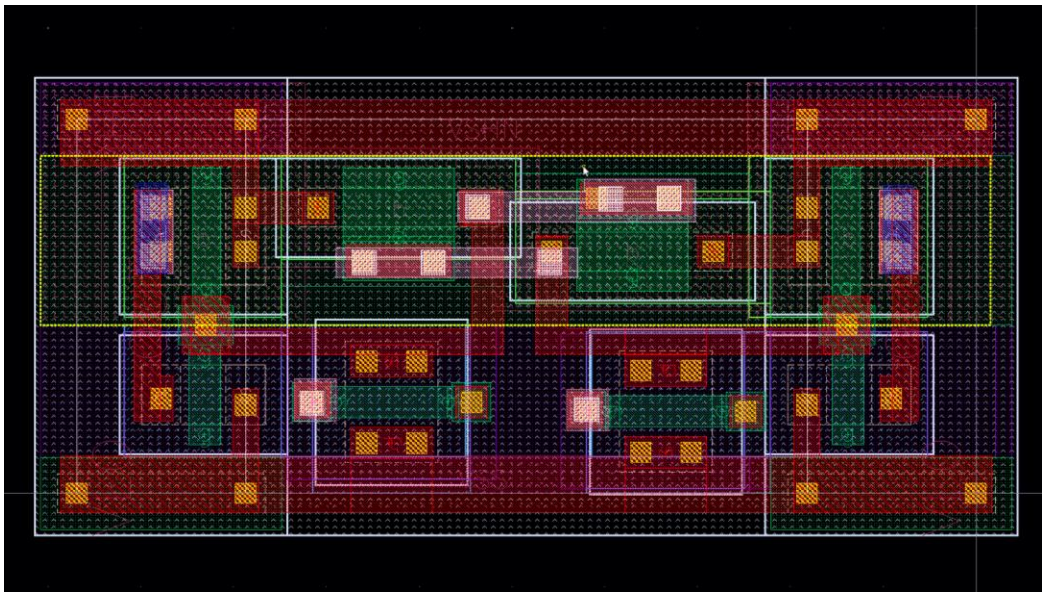


Fig.9

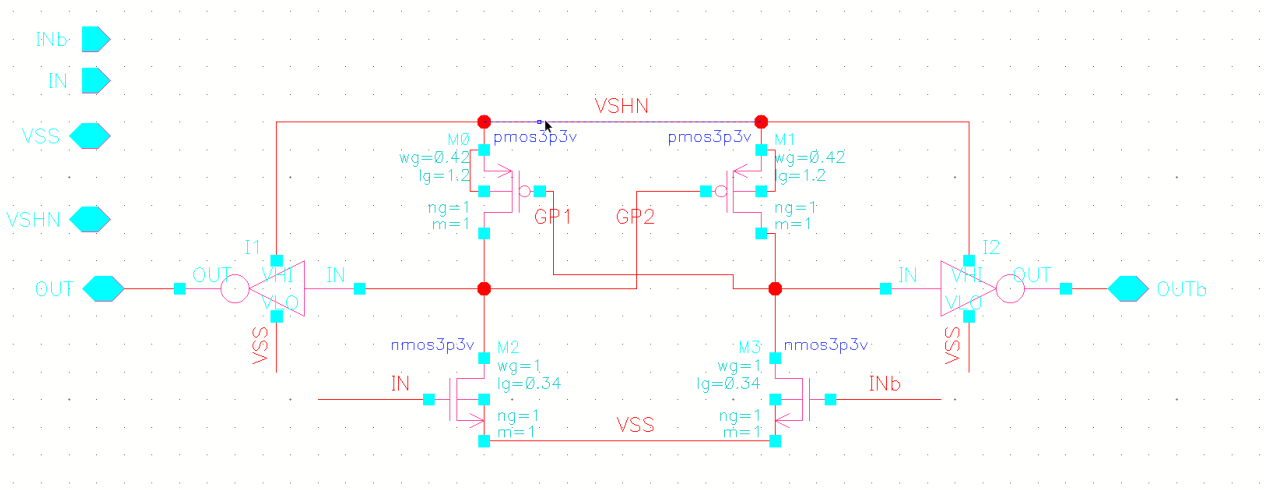


Fig.10

High Voltage: 11 Volts

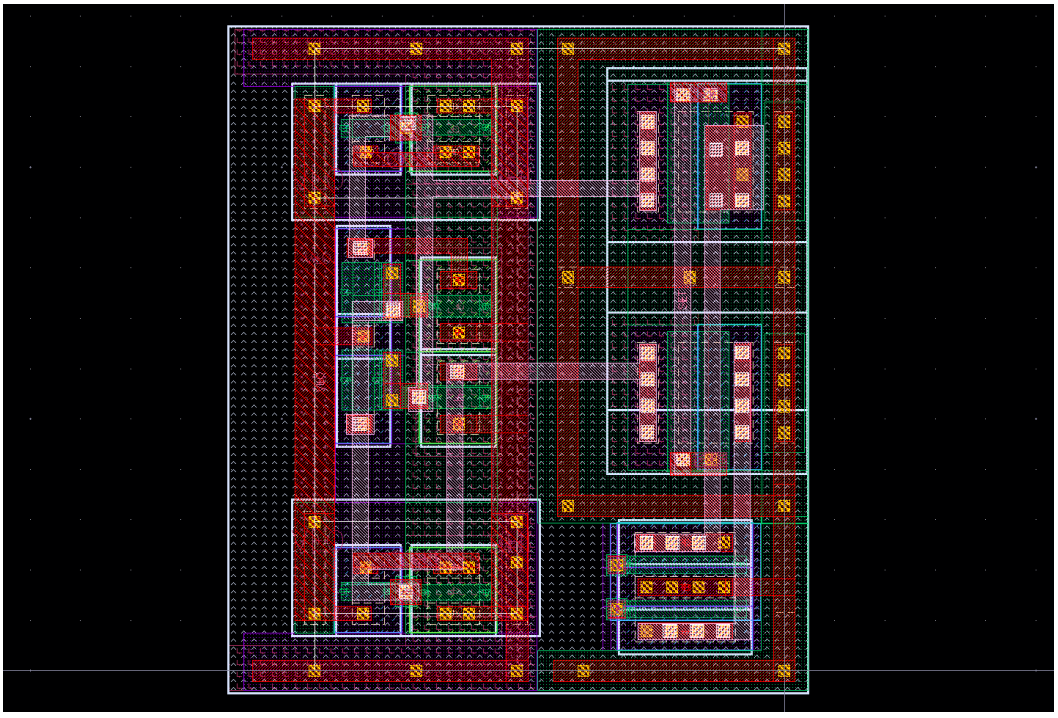


Fig.11

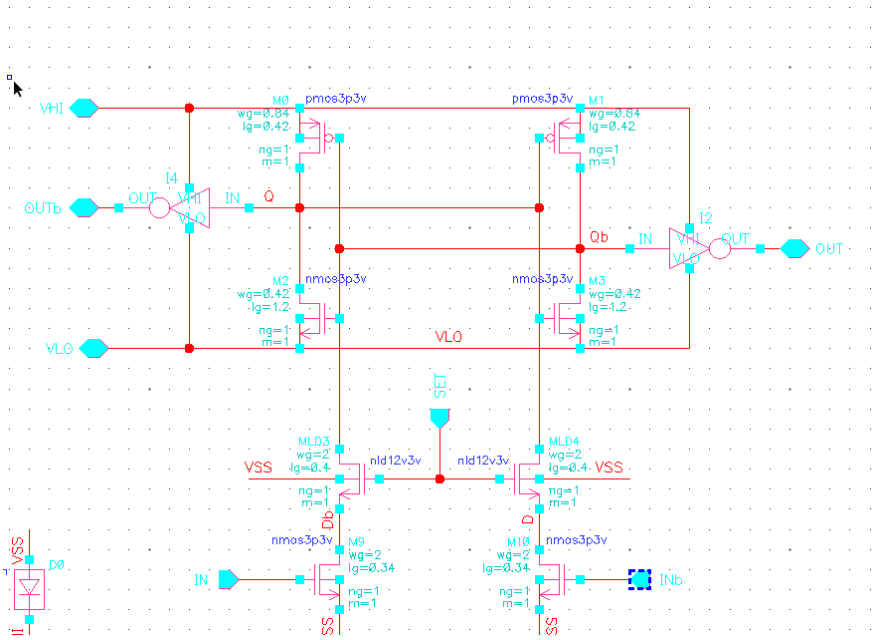

VHI
OUTb
VLO
M0
pmos3p3v
wg=0.84
lg=0.42
ng=1
m=1
M1
pmos3p3v
wg=0.84
lg=0.42
ng=1
m=1
I4
OUT
VHI
VLO
IN
Q
Qb
I2
OUT
OUT
M2
nmos3p3v
wg=0.42
lg=1.2
ng=1
m=1
M3
nmos3p3v
wg=0.42
lg=1.2
ng=1
m=1
VLO
SET
MLD3
wg=2
lg=0.4
VSS
nld12v3v
nld12v3v
MLD4
wg=2
lg=0.4
VSS
ng=1
m=1
ng=1
m=1
Db
D
nmos3p3v
M9
wg=2
lg=0.34
ng=1
m=1
nmos3p3v
M10
wg=2
lg=0.34
ng=1
m=1
IN
INb
VSS
D0
SS
SS

Fig.12

Internship take away:

- Worked on digital circuit blocks with analog circuit design skills.
- Regressive building of layout for all the circuits with proper rules set for all the metal layers and contacts.
- Design of complex circuits like row driver, column driver, Schmitt trigger and digital blocks such as logic gates, x16 inverters.
- Designing circuits for non-volatile 16kb and 64kb memories (NVM).
- Used advanced new tools like Calibre rev that helps in observing the layout and rectifying errors as well as compare two layouts by XOR operation.
- Approach while designing any circuit and thinking process involved.
- Co-ordinating with team on-site as well as in Czech Republic and Idaho.
- Scheduling meetings and discussion over a problem faced during designing.

Tools used:

- Cadence virtuoso
- Spectre
- Calibre rev

Environment:

- Linux