ON SEMICONDUCTOR

INTERNSHIP PROJECT REPORT

MOVING BIT ARRAYS

GANESH VHATKAR

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DESCRIPTION OF THE PROJECT WORKED ON DURING THE SUMMER INTERNSHIP AT ON SEMICONDUCTOR, GRESHAM, OR.

MOVING BIT ARRAYS (MOBA)

Moving bit arrays (mobas) are test structures designed for gathering statistics on large memory cell arrays in order to observe extrinsic behaviors. Moba is entirely part of the development and qualification strategy of embedded eeproms.
The current document describes the 16kbits moba.

By definition, a moba is an array of cell that can be tested on a standard engineering test bench which can all be programmed, erased and stressed in parallel using external pulses, and read sequentially thanks to a clock-based addressing system. The moba is relatively simple: there is no high voltage generation and switching on-chip, only 8 pins are needed, and the patterns that can be written in the array are "all 1" and "all 0".

The moba has 8 terminals including:

- 2 power supplies (vdd & vss),
- 2 programming terminals (cwl & cel),
- 2 sensing terminals (csl & blout), and
- 2 commands (rd & clk).

Terminal	Description
Vdd	Logic power supply high
Vss	Logic power supply low
Cwl	Common word line
Cel	Common erase line
Csl	Common source line
Blout	Bit line output
Rd	Read command
Clk	Clock

Table 1

Memory cell description:

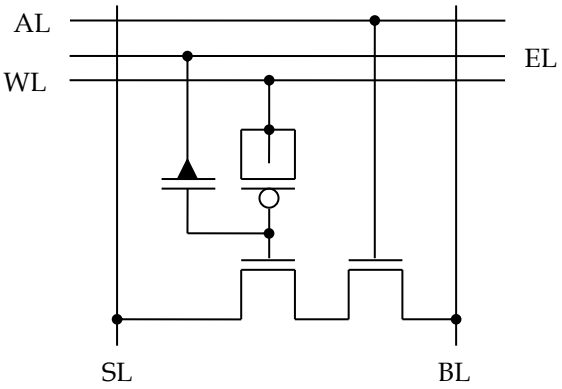
The logicee memory cell is made of 1) two standard nmos, the state & the select transistors placed in series, 2) one standard pmos, and 3) a none-linear mos capacitor. The none-linear capacitor is a n+ implanted polysilicon gate on nwell. The gate of the state transistor, being the floating-gate where the charges are stored, is connected to the one of the none-linear mos capacitor and the one of the pmos. The drain of the state transistor and the source of the select transistor are connected. The drain of the select transistor forms the drain of the memory cell. The source of the state transistor forms the source of the memory cell. The drain, source & bulk of the pmos are tied together to form the control-gate. The nwell of the none-linear mos capacitor forms the erase-gate. The gate of the select transistor forms the select-gate

The onc18 logicee memory cell has:

- 1 nmos state transistor,
- 1 nmos access transistor,
- 1 pmos-like transistor used as capacitor, and
- 1 mos structure.

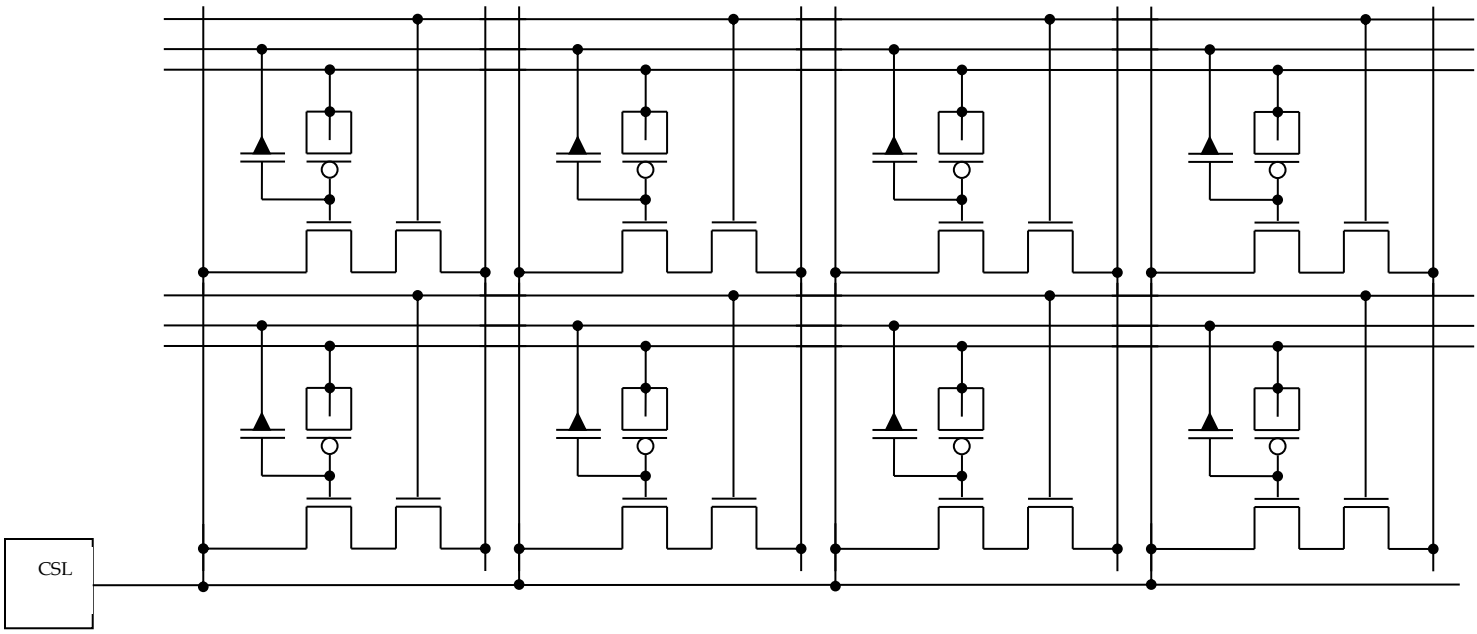
The terminals are:

- Bit line [bl] (drain of the access transistor),
- Source line [sl] (source of the state transistor),
- Access line [al] (gate of the access transistor),
- Erase line [el] (active electrode of the mos structure),
- Word line [wl] (active electrode of the pmos-capacitor)



The moba has:

- Cel connects all els in the array,
- Cwl connects all wls in the array, and
- Csl connects all sls in the array.



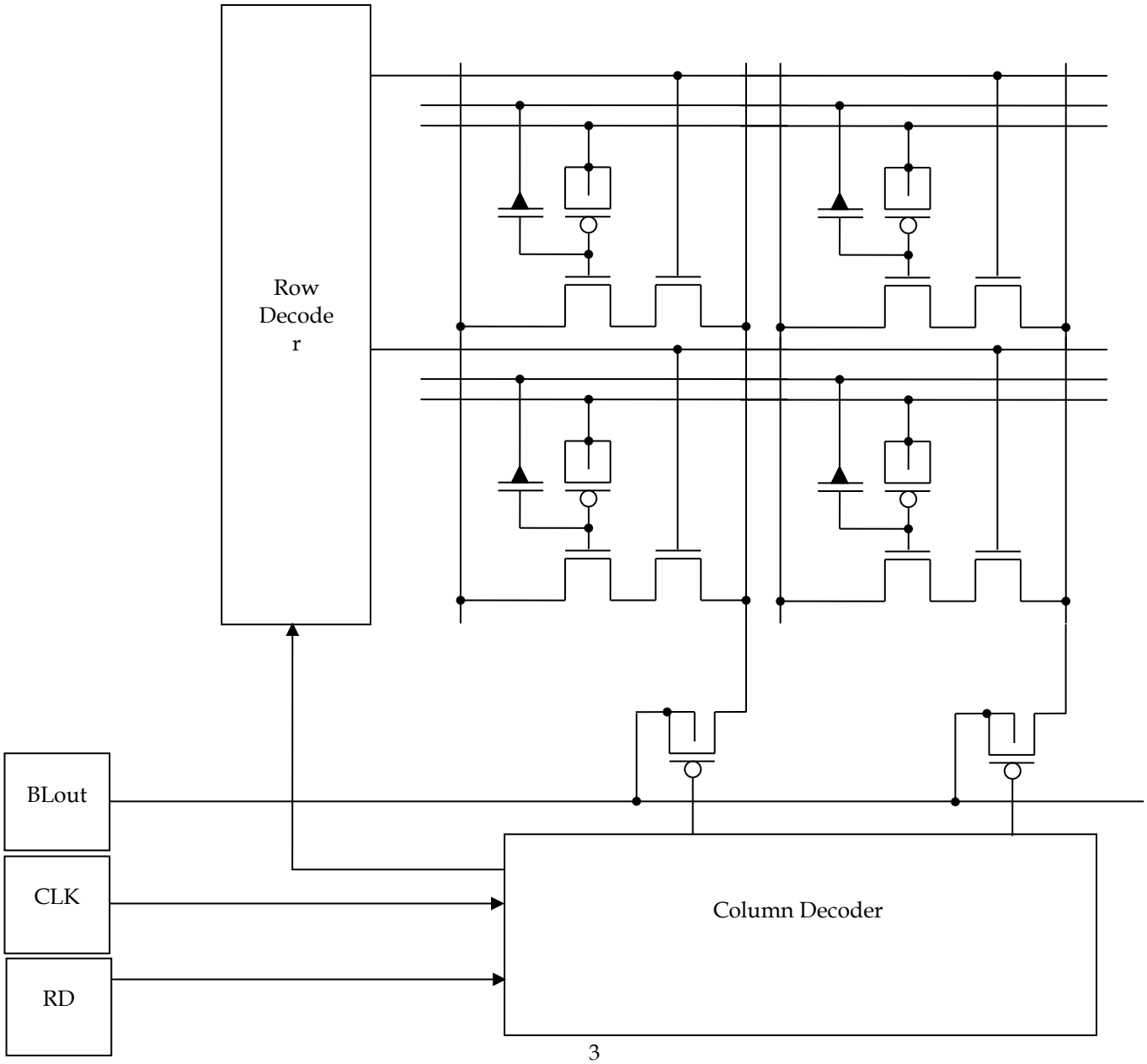
Decoded terminals:

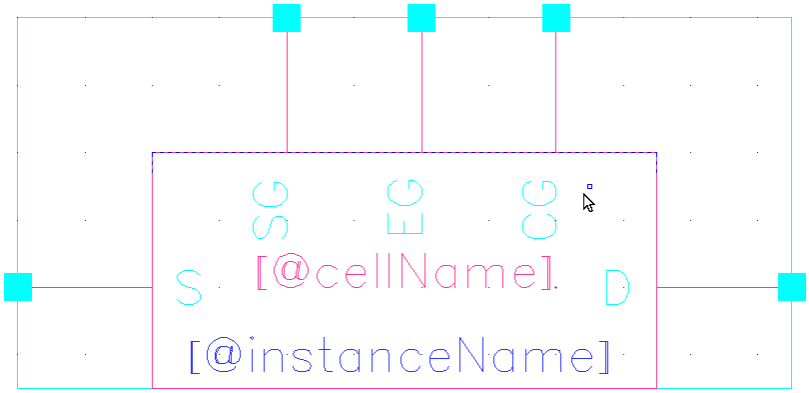
The cell's terminals that are specific to the reading operation are decoded. These terminals are bl and al. Decoding consists in selecting one bit-cell for measuring its i-v characteristic. A selected bit-cell has its access gate forced to vdd and its bl tied to blout through a pmos.

No bit-cell is selected when rd is at 0. It means that all als are grounded and all bls are disconnected from blout.

Read mode starts when rd is set to 1 and the selected bit-cell is #16383 (the last one). This means that al<127> is set to vdd and bl<127> is tied to blout.

Once in read mode, the clock signal clk can be used to address a bit-cell. At the first front edge of clk, the selected bitcell moves to #0 (al<0> & bl<0>). At the second front edge of clk, bit-cell #1 is selected. Bit-cell #n-1 is selected at the nth front edge of clk. So, after 16384 clk front edges, the selection goes back to the last bit (#16383).





Pin description

Pin-name	Input/output	Definition
D	I/o	Drain
Sg	Input	Select-gate
Eg	Input	Erase-gate
Cg	Input	Control-gate
S	I/o	Source
Psub	I/o	Global p-substrate

Table 2

The following table describes the various operating conditions and voltages applied to the ee cell.

OPERATION	ROW	COLUMN	EG	CG	SG	D	S
READ	selected	selected	VGread | GND	VGread	VDD	VDread	GND
	selected	unselected	VGread | GND	VGread	VDD	GND	GND
	unselected	selected	GND	GND	GND	VDread	GND
	unselected	unselected	GND	GND	GND	GND	GND
ERASE	selected	NA	VPP	GND	GND	GND	GND
	unselected	NA	GND	GND	GND	GND	GND
PROGRAM	selected	selected	VPP	VPP	GND	GND | VDD	GND
	selected	unselected	VPP	VPP	GND	GND | VDD	Vinh
	unselected	selected	GND	GND	GND	GND | VDD	GND
	unselected	unselected	GND	GND	GND	GND | VDD	Vinh

Table 3

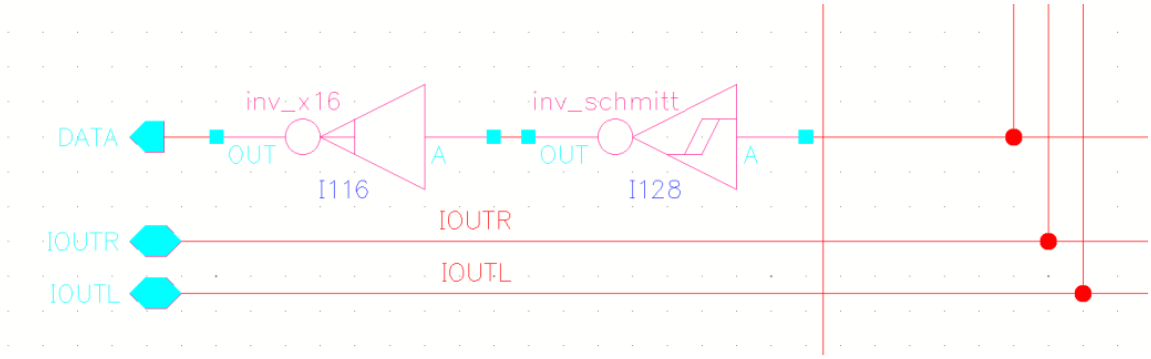
The above-mentioned theory is the concept and working of the bit-cell and moba. Most of the design work of the circuit was done and the modifications to that circuitry was carried by me.

The main tasks were:

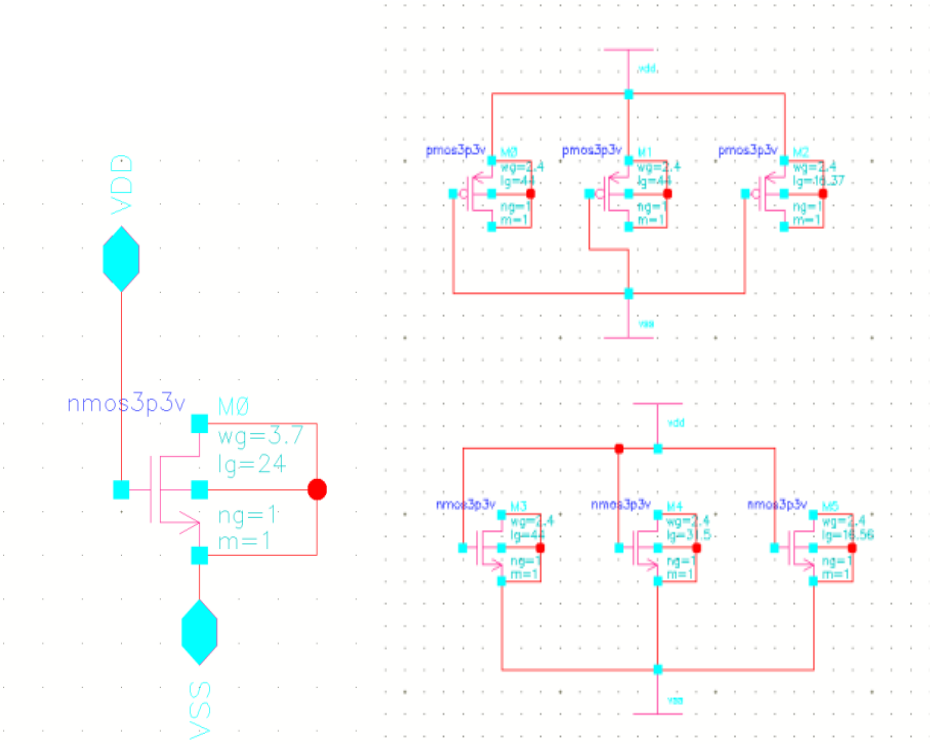
- Boost data-out signal with x16 inverter
- Add decoupling caps on power rails
- Replace 2v/3v i/o cells with 3v only.
- Un-swap the two command signals that have been swapped
- Reducing the **t_rd_set** delay.

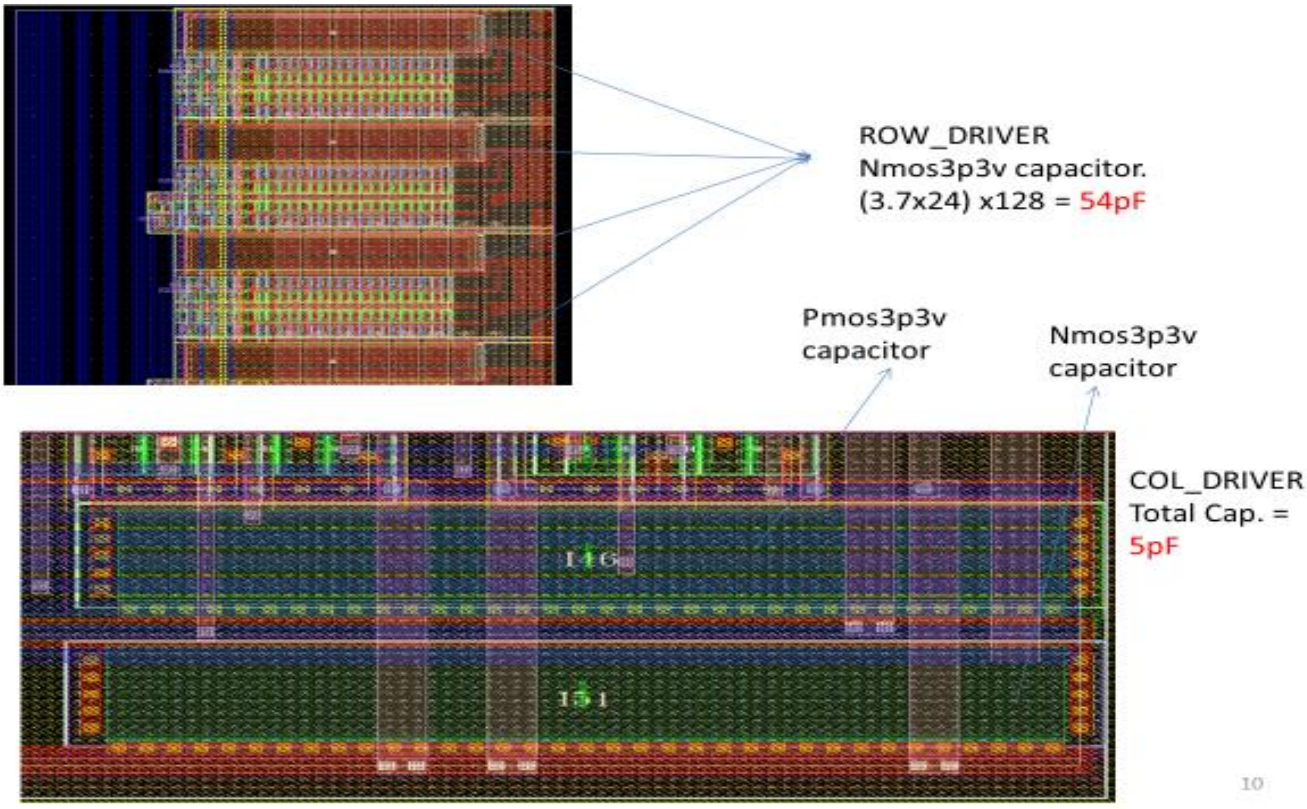
Details:

- Boost data-out signal with x16 inverter.
  Data-out signal boosted by using inverter schmitt trigger followed by x16 inverter. Challenge of making the changes at the schematic as well as layout level was overcome. Layout vs schematic (lvs) succeeded.

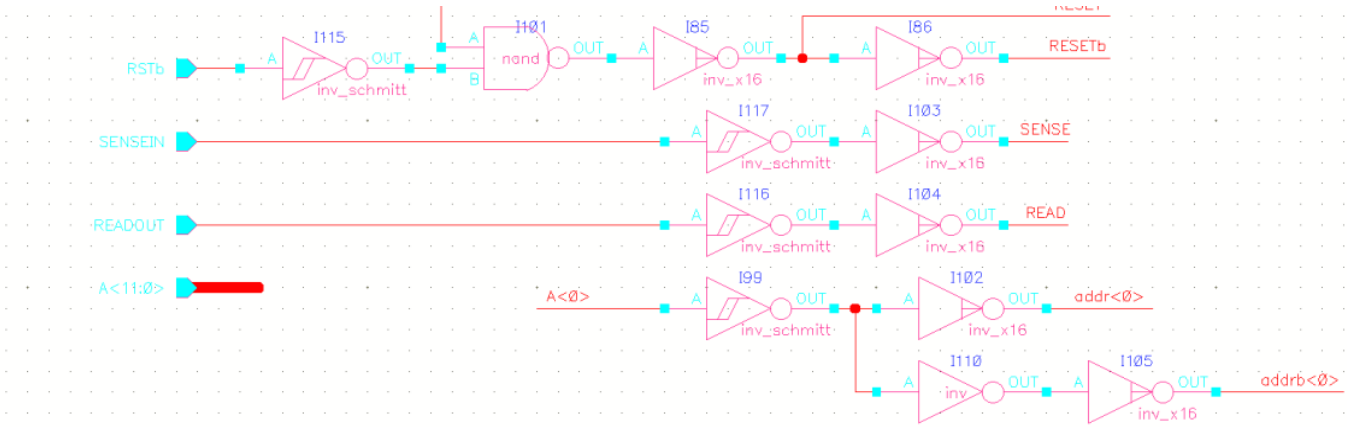


- Add decoupling caps on power rails.
  54pf capacitance added on row divider circuitry and 5pf cap. Added on column divider circuitry between the vdd and vss. Lvs succeeded. Capacitance were added at the transistor level circuitry and layout was made for row and column divider. Again, lvs was succeeded.

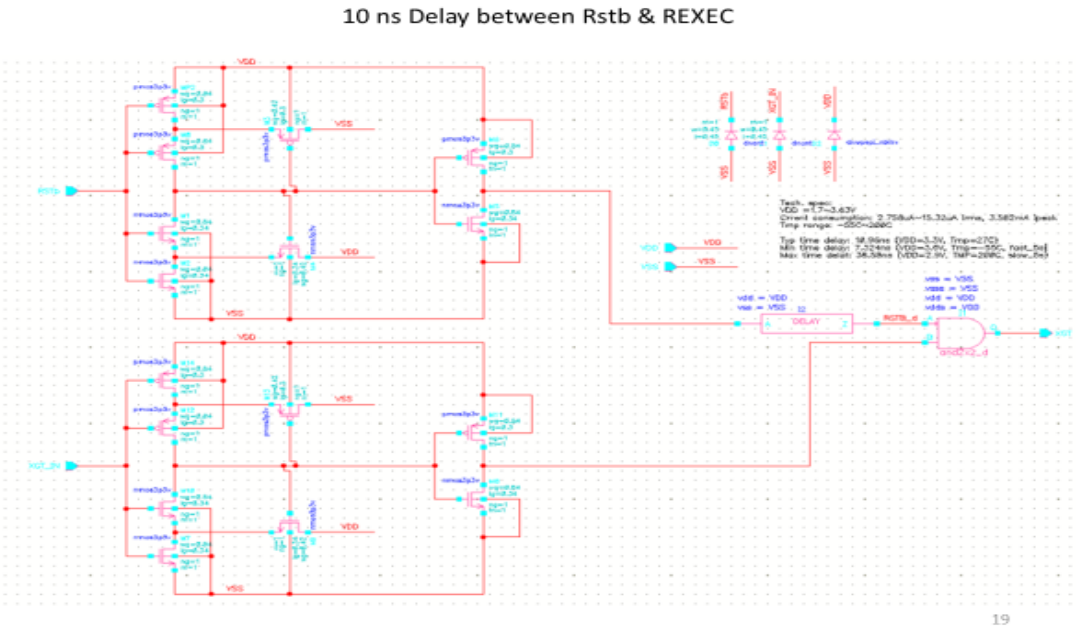

vDD
nmos3p3v
M0
wg=3.7
lg=24
ng=1
m=1
VSS
pmos3p3v
M0
M1
M2
nmos3p3v
M3
M4
M5
vdd
vss


ROW_DRIVER
Nmos3p3v capacitor.
(3.7x24) x128 = 54pF
Pmos3p3v
capacitor
Nmos3p3v
capacitor
COL_DRIVER
Total Cap. =
5pF
10

- Un-swap the two command signals that have been swapped.
  Mistake was made by swapping the read and sense signal in the circuitry. After debugging the bug was removed and the read and sense signal were connected correctly. These changes were made at the schematic and the layout level. Lvs succeeded.



- Reducing the **t_rd_set** delay.
  Delay between the signals rstb and rexec was shortened to 10 ns with designing new circuitry of inverters.



Internship take away:

- Design of complex circuits like row driver, column driver, schmitt trigger and digital blocks such as logic gates, x16 inverters.
- Designing circuits for non-volatile 16kb and 64kb memories (nvm).
- Working on io cells of a pad-ring and understanding the function and structure of each cell.
- Regressive building of layout for all the circuits with proper rules set for all the metal layers and contacts.
- Worked on digital circuit blocks with analog circuit design skills.
- Used advanced new tools like calibre rev that helps in observing the layout and rectifying errors as well as compare two layouts by xor operation.
- Approach while designing any circuit and thinking process involved.
- Co-ordinating with team on-site as well as in czech republic and idaho.
- Scheduling meetings and discussion over a problem faced during designing.

Tools used:

- Cadence virtuoso
- Calibre rev

Environment:

- Linux