GANESH VHATKAR

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Objective: Learn and contribute significantly to the design of high linearity and low power analog and mixed signal circuits and system design. To work in an ambitious & skilled team of engineers that is determined to create marvelous technological advancement for a better future

Educational Qualifications:

Degree	University	CGPA	Year
Master of Science Analog/Mixed-Signal/SERDES/RF Circuit Design	Oregon State University Corvallis, Oregon	3.45/4	Sept 2016- June 2018
Bachelor of Engineering, Electronics and Tele Communication	University of Mumbai, Mumbai, India	7.15/10	2012 2016

Skillset & Coursework:

Tools	Cadence, Virtuoso, Spectre, Mentor Calibre, HSPICE, CosmoScope MATLAB, System Verilog, Python, Dig Oscilloscope
Relevant Courses	CMOS Integrated Circuits I & II, Energy Efficient VLSI Design, VLSI System Design, Phase Lock Loop RF Circuit Design, High Performance Computer Architecture, Interconnection Networks.

Device Development & Circuit Design Intern: *ON Semiconductor* | **June'17-Dec'17**

- Collaborated with the team of design engineers from OR, AZ, ID & CZ on projects developing Non-Volatile Memories
- Worked on a memory tester Moving Bit-Arrays(MOBA)& Demonstrator(64KbNVM) and their tape-in
- Design/Layout of Level Shifters for Low Voltage(3.3V) & High Voltage(11V)
- Design/Layout of Schmitt Trigger & Digital Logic gates (NAND, NOR, Invertersx16) with Floating Supply Rails
- Layout of the Colum Driver & Layout of the Row Driver Circuit. De-bugging of schematic & layout
- DRC, LVS, & post layout simulation for PEX & Antenna Diodes

Projects:

PLL: **1 GHz – 500 MHz Low Power Quadrature Type II, 3rd Order CP PLL Design |*TSMC 65RF, 65 nm CMOS*|**

- Designed a PMOS Supply regulated/controlled Differential I, Q **8-Stage Invertor** based **Ring Oscillator VCO** for a KVCO of 3 GHz/V and -107 dBc/Hz Phase Noise at 1MHz offset with AC Coupled Buffer within 1.5mA, 1.2 V Supply
- Designed **Ratioed Logic TSPC** Divide by 8 designed across 500 MHz to 5 GHz I/P Clock within worst case 1.5 mA at Max. Clock. CP PLL was designed for a 60^0phase margin for UGB of 6 MHz for REF Frequency from 62.5 MHz to 125 MHz
- All **NTFs** were analyzed in MATLAB and PLL was optimized for an integrated jitter of 932 fs at 1 GHz O/P Clock

SERDES: **Serializer Circuit for High-Speed SERDES |TSMC 180 nm CMOS|**

- Designed a **Serializer Circuit for High-Speed SERDES** consisting of **TSPC** Latch to hold parallel data inputs.
- Designed high-speed **Current-Mode logic 2:1 Multiplexer**. Testbench analyzed in HSPICE & CosmoScope
- Understanding of IO protocols like PCIe, SATA, USB, & Ethernet for high-speed interface.
- Designed a **4-stage** charge multiplier **Diode connected NMOS Dickson Charge Pump** in parallel with NMOS operated in the linear region. DC-DC boost of 4.58V from 1.5V input DC supply **|*TSMC 180 nm CMOS*|**

RFIC: **Worked with a team involved in the design of a Receiver front-end design. |*TSMC 65RF, 65 nm CMOS*|**

- Designed a **2.4 GHz, 80 MHz RF BW Low-Noise Amplifier(LNA) with source degeneration** with 50 fF C_{PAD}, 40 nH L_G for an S_{11} < -12 dB, Gain of 10 dB, NF of 3 dB across RF BW, 1nH Bond-Wire Inductor at 1.2 V Supply
- Design of a **4.8 GHz LC VCO. NMOS Cross-Coupled LC VCO** and AC Coupled Buffers are designed for a Phase Noise of -125 dBc/Hz at 1 MHz offset in Current-Limited regime for an f_c of 4.8 GHz within 1.2 mA, 1.2 V Supply. LC Tank Quality Factor of 21 at 4.8 GHz with L_{TANK} = 1.9 nH and C_{TANK} = 450fF

OP-AMP: **Design and Layout of G_m-Boosted Fully Differential Operational Amplifier |*TSMC 250 nm CMOS*|**

- Designed an NMOS based G_m-Boosted **Folded Cascode OTA** design for an Open Loop DC Gain of 70 dB, UGB of 80 MHz and 60^0 Phase Margin for a 1 V_{P-P} swing within 3 mA, 2.5 V (±10 %) Supply across TT, FF, SS corners
- Worked on design of PMOS based low-power **CMFB Amplifier** for a 60^0 Phase Margin with a CM Reference of 1.25 V
- NMOS & PMOS based **G_m-Boosting Amplifiers** was designed for PMOS and NMOS Cascode FETs for 40 dB DC Gain

Design/Layout of ±1 V Dual Supply Miller Compensated 2 Stage Op-Amplifier

- Design/Layout of a PMOS based **5 Transistor OTA** followed by High Swing NMOS CS Amplifier for an UGB of 200 MHz for a C_{LOAD} of 2 pF. Achieved an Open-Loop DC Gain of 70 dB, 60^0 Phase Margin with Miller Compensation for a swing of 1.6 V_{P-P} within 2 mA for a Dual Supply of ±1 V.

Ring Oscillator & Full Adder | *TSMC 180NM CMOS* |

- Design/Layout of 3-stage CMOS Invertor based Ring Oscillator for an Oscillation of 600MHz
- Achieved a Phase Noise of -103dBc/Hz at 1MHz offset at 1.2V supply. DRC and LVS checks conducted
- Design/Layout of Full-Adder using 3-stage mirror adder operating at 1.8V supply
- DRC checks and LVS conducted for matched designed. PEX simulation to include the stray capacitances

SURVEY: **Processing-In Memory (PIM)**

- Study on implementations of PIM architectures as FlexRAM, DIVA, Hybrid Memory Cube (HMC), & 3D Die Stacked PIM to reduce the data access latency, improve energy efficiency and increase the processing speed of traditional separate CPU and Memory architectures.
- Examining applications of PIM for Artificial Neural Networks (ANN) for improving performance of each node in ANN
- Proposed future application of PIM for Solid State Drives (SSD/NAND FLASH). Improving the current architecture of the SSDs for fast and efficient data storage and access

Hardware Implementations of Artificial Neural Networks

- Study on various types of hardware implementations of ANN like Feed-Forward Networks & Recurrent Networks.
- Topologies implemented using FPGAs as nodes consisting of Input Layer, hidden Layer & Output Layer
- Hardware implementation using digital & analog CMOS circuitry using synaptic weights made of latches, ADCs and their trade-offs. Study on ANN topologies implemented using Memristor and Processing in Memory