ganeshprabhu2005 / **ENCODER8TO3DATAFLOW** Public

forked from naavaneetha/ENCODER8TO3DATAFLOW

GPL-3.0 license

0 stars **331** forks Branches Tags Activity

Star Notifications

Code Pull requests Actions Projects Security Insights

main 1 Branch 0 Tags Go to file Go to file Code

This branch is 1 commit ahead of naavaneetha/ENCODER8TO3DATAFLOW:main .

ganeshprabhu2005 Update README.md 2 weeks ago

db	EXP5	3 months ago
incremental_db	EXP5	3 months ago
output_files	EXP5	3 months ago
simulation/modelsim	EXP5	3 months ago
ENCODER8TO3.qpf	EXP5	3 months ago
ENCODER8TO3.qsf	EXP5	3 months ago
ENCODER8TO3.qws	EXP5	3 months ago
ENCODER8TO3.v	EXP5	3 months ago
ENCODER8TO3.v.bak	EXP5	3 months ago
LICENSE	Initial commit	3 months ago
README.md	Update README.md	2 weeks ago
Waveform.vwf	EXP5	3 months ago

README License

ENCODER 8TO3 DATAFLOW Modelling

AIM:

To implement Encoder 8 To 3 in Dataflow Modelling using verilog and validating their functionality using their functional tables

SOFTWARE REQUIRED: Quartus prime

THEORY

Encoder 8 To 3

The 8 to 3 line Encoder is also known as Octal to Binary Encoder. In 8 to 3 line encoder, there is a

total of eight inputs, i.e., D0, D1, D2, D3, D4, D5, D6, and D7 and three outputs, i.e., A0, A1, and A2. In 8-input lines, one input-line is set to true at a time to get the respective binary code in the output side. Below are the block diagram and the truth table of the 8 to 3 line encoder.

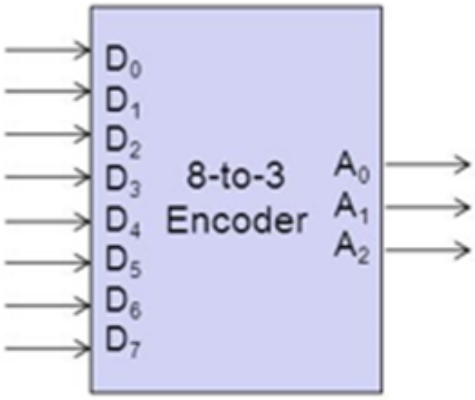


Figure 01 Block Diagram of Encoder 8 * 3

Truth Table

inputs								outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

The logical expression of the term A0, A1, and A2 are as follows:

A0 = D1 + D3 + D5 + D7

A1 = D2 + D3 + D6 + D7

A2 = D4 + D5 + D6 + D7

Logical circuit of the above expressions is given below:

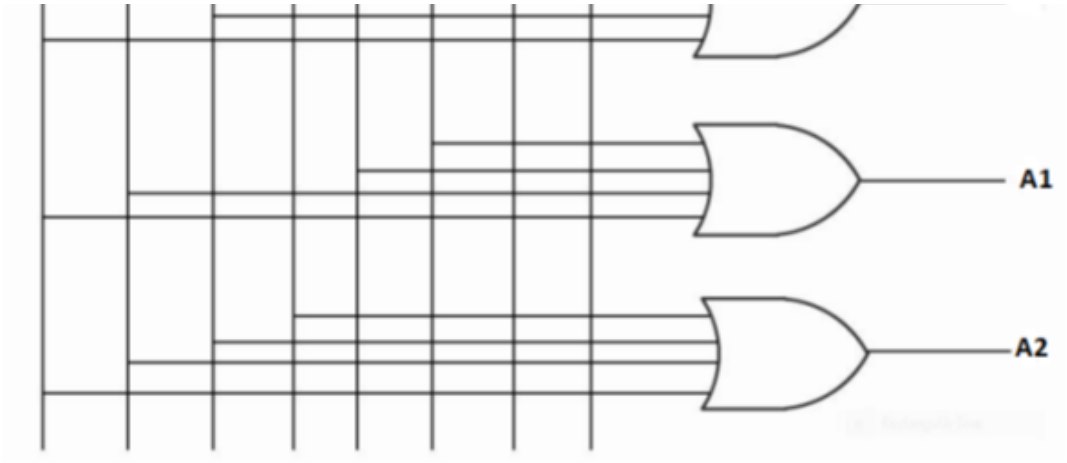


Figure 02 Encoder 8 * 3

Procedure

```
1.Type the program in Quartus software.
2.Compile and run the program.
3.Generate the RTL schematic and save the logic diagram.
4.Create nodes for inputs and outputs to generate the timing diagram.
5.For different input combinations generate the timing diagram.
```

/* write all the steps invloved */

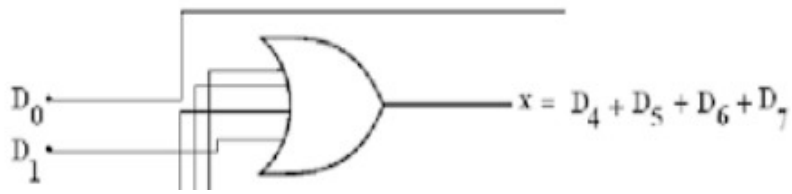
PROGRAM

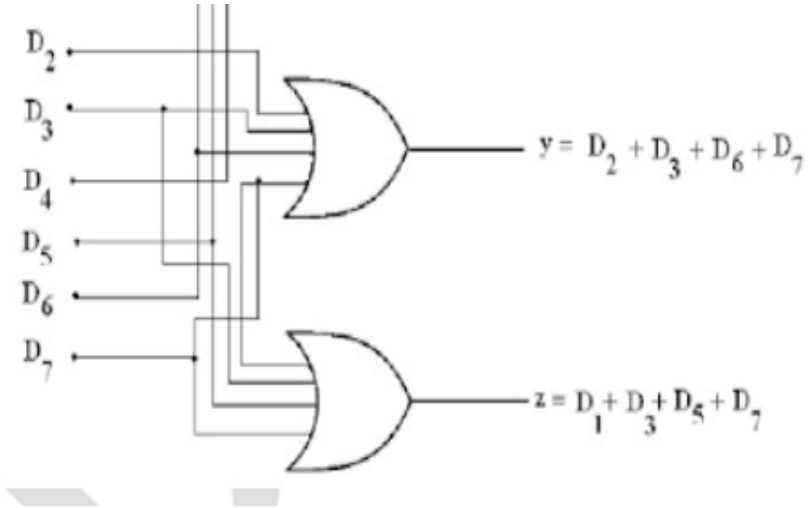
/* Program for Encoder 8 To 3 in Dataflow Modelling and verify its truth table in quartus using Verilog programming.

Developed by: GANESH PRABHU J RegisterNumber: 212223220023

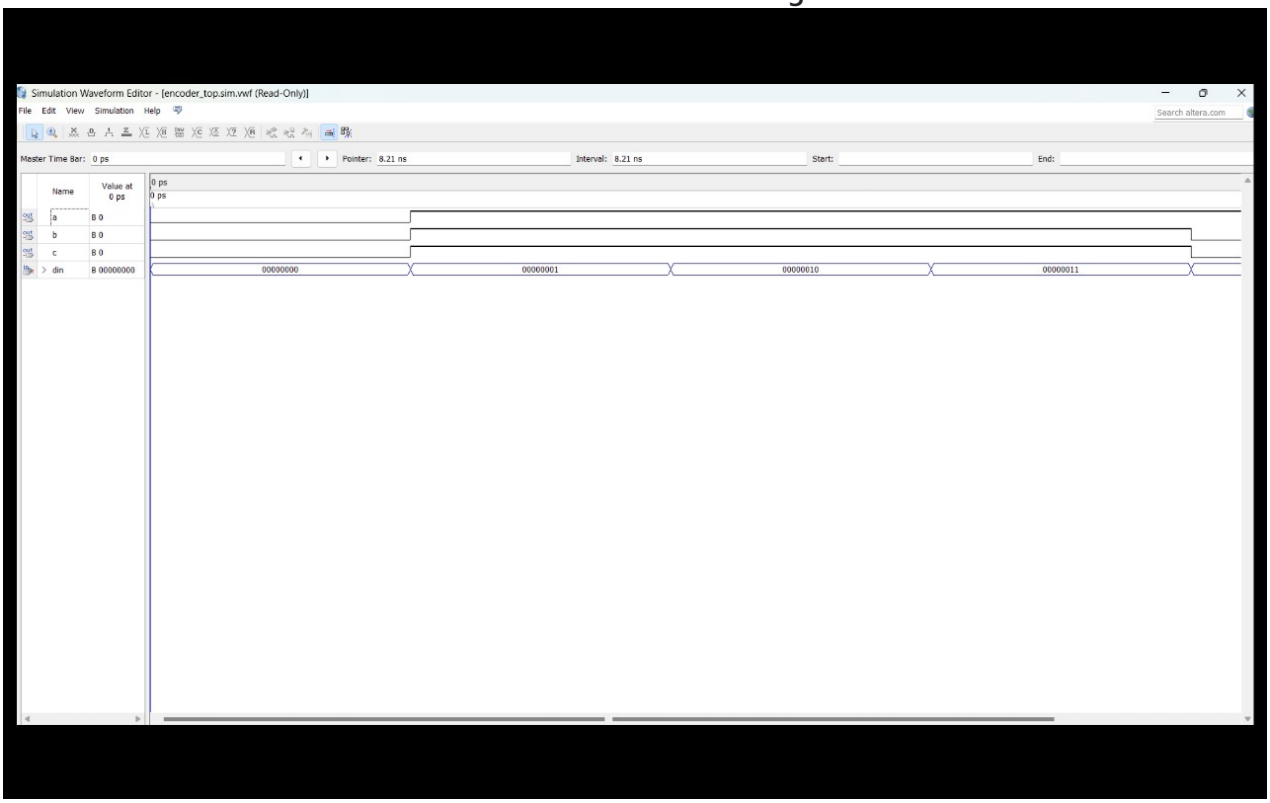
```
/* Program for Encoder 8 To 3 in Dataflow Modelling and verify its truth table in
quartus using Verilog programming.
module encoder_top(din, a, b, c);
input [0:7] din;
output a,b,c;
assign a=din[4] | din[5] | din[6] | din[7];
assign b=din[2] | din[3] | din[6] | din[7];
assign c=din[2] | din[4] | din[6] | din[7];
endmodule
```

RTL LOGIC FOR Encoder 8 To 3 in Dataflow Modelling





TIMING DIGRAMS FOR Encoder 8 To 3 in Dataflow Modelling



RESULTS

Releases

No releases published

Packages

No packages published

Languages