Lab Assignment-1

01-09-2018

Note:

- The assignment to be done in batches as indicated
- Maximum marks: 03
- Deadline: 10 to 15-09-2018 (hard deadline).
- Marking scheme: partial marks may be awarded.

Parking lot occupancy counter

Consider a parking lot with a single entry and exit gate. Two pairs of photo sensors are used to monitor the activity of cars, as shown in Figure.

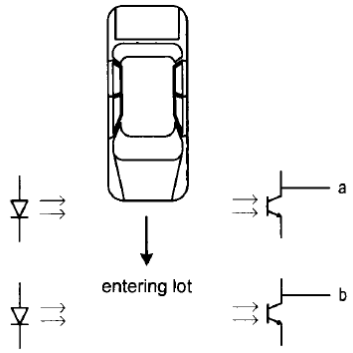

Figure: conceptual diagram of gate sensors

When an object is between the photo transmitter and the photo receiver, the light is blocked and the corresponding output is asserted to 1. By monitoring the events of two sensors, we can determine whether a car is entering or exiting or a pedestrian is passing through. For example, the following sequence indicates that a car enters the lot:

- Initially, both sensors are unblocked (i.e., the a and b signals are "00").
- Sensor a is blocked (i.e., the a and b signals are " 10").
- Both sensors are blocked (i.e., the a and b signals are "1 1 ").
- Sensor a is unblocked (i.e., the a and b signals are "01 ").
- Both sensors becomes unblocked (i.e., the a and b signals are "00").
- Design a parking lot occupancy counter as follows:

1. Design an FSM with two input signals, a and b, and two output signals, *e n t e r* and *e x i t* . The *e n t e r* and *e x i t* signals assert one clock cycle when a car enters and one clock cycle when a car exits the lot, respectively.

2. Derive the HDL code for the FSM.

3. Design a counter with two control signals, *i n c* and *d e c*, which increment and decrement the counter when asserted. Derive the HDL code.

4. Implement this in FPGA, use any two push switches for a, b inputs and the LEDs on the board to show the number of occupied slots (Binary). Assuming the maximum slots allowed is 64; indicate the non availability of slot by blinking all the 8 LEDs (one second for ON and OFF)) on the ZedBoard.