

A  
PROJECT REPORT  
ON  
**POWER QUALITY IMPROVEMENT IN THE DISTRIBUTION GRID  
BY USING 15 LEVEL MMC BASED DSTATCOM**  
Submitted in partial fulfillment of the requirements  
for the award of the degree of  
**BACHELOR OF TECHNOLOGY**  
in  
**ELECTRICAL AND ELECTRONICS ENGINEERING**

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## ABSTRACT

In this project, a new single-phase wind energy inverter (WEI) with flexible AC transmission system (FACTS) capability is presented. The proposed inverter is placed between the wind turbine and the grid, same as a regular WEI, and is able to regulate active and reactive power transferred to the grid. This inverter is equipped with distribution static synchronous compensators option in order to control the power factor (PF) of the local feeder lines. Using the proposed inverter for small-to medium-size wind applications will eliminate the use of capacitor banks as well as FACTS devices to control the PF of the distribution lines. The goal of this paper is to introduce new ways to increase the penetration of renewable energy systems into the distribution systems. This will encourage the utilities and customers to act not only as a consumer, but also as a supplier of energy.

Moreover, using the new types of converters with FACTS capabilities will significantly reduce the total cost of the renewable energy application. In this paper, modular multilevel converter is used as the desired topology to meet all the requirements of a single-phase system such as compatibility with IEEE standards, total harmonic distortion (THD), efficiency, and total cost of the system. The proposed control strategy regulates the active and reactive power using power angle and modulation index, respectively. The function of the proposed inverter is to transfer active power to the grid as well as keeping the PF of the local power lines constant at a target PF regardless of the incoming active power from the wind turbine. The simulations for an 15-level inverter have been done in MATLAB/Simulink.

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## LIST OF ABBREVIATIONS

FACTS	--	Flexible AC Transmission System
WEI	--	Wind Energy Inverter
PF	--	Power factor
THD	--	Total Harmonic Distortion
PM	--	Permanent Magnet
MPPT	--	Maximum Power Point Tracker
D-STATCOM	--	Distributed Static Compensation
STATCOM	--	Static Compensator
MMC	--	Modular Multilevel Converter
PMM	--	Pulse Width Modulation
HVDC	--	High Voltage DC
SVC	--	Static Var Compensator
TCSC	--	Thyristor Controlled Series Compensator
SSSC	--	Static Synchronous Series Compensator
DFC	--	Dynamic Flow Controller
UPFC	--	Unified Power Flow Controller
IPFC	--	Interline Power Flow Controller
IGCT	--	Insulated Gate Commutated Thyristor
IGBT	--	Insulated Gate Bipolar Transistor
TSC	--	Thyristor Switched Capacitors
TCR	--	Thyristor Switched or Controlled Reactor
FC	--	Fixed Capacitor
CPWM	--	Carrier Based Pulse Width Modulation
CMI	--	Cascaded Multilevel Inverter

# **CHAPTER-1**

## **INTRODUCTION**

The role of power electronics in distribution systems has greatly increased recently. The power electronic devices are usually used to convert the nonconventional forms of energy to the suitable energy for power grids, in terms of voltage and frequency. In permanent magnet (PM) wind applications, a back-to-back converter is normally utilized to connect the generator to the grid. A rectifier equipped with a maximum power point tracker (MPPT), converts the output power of the wind turbine to a dc power. The dc power is then converted to the desired ac power for power lines using an inverter and a transformer. With recent developments in wind energy, utilizing smarter wind energy inverters (WEIs) has become an important issue. There are a lot of single-phase lines in the United States, which power small farms or remote houses. Such customers have the potential to produce their required energy using a small-to-medium-size wind turbine. Increasing the number of small-to-medium wind turbines will make several troubles for local utilities such as harmonics or power factor (PF) issues.

A high PF is generally desirable in a power system to decrease power losses and improve voltage regulation at the load. It is often desirable to adjust the PF of a system to near 1.0. When reactive elements supply or absorb reactive power near the load, the apparent power is reduced. In other words, the current drawn by the load is reduced, which decreases the power losses. Therefore, the voltage regulation is improved if the reactive power compensation is performed near large loads. Traditionally, utilities have to use capacitor banks to compensate the PF issues, which will increase the total cost of the system. The modern ways of controlling the PF of these power lines is to use small distribution static synchronous compensators (D-STATCOMs). The D-STATCOMs are normally placed in parallel with the distributed generation systems as well as the power systems to operate as a source or sink of reactive power to increase the power quality issues of the power lines. Using regular STATCOMs for small-to-mediumsize single-phase wind applications does not make economic sense and increase the cost of the system significantly. This is where the idea of using smarter WEIs with FACTS capabilities shows itself as a new idea to meet the targets of being cost-effective as well as compatible with IEEE standards. The proposed inverter in this project is

equipped with a D-STATCOM option to regulate the reactive power of the local distribution lines and can be placed between the wind turbine and the grid, same as a regular WEI without any additional cost. The function of the proposed inverter is not only to convert dc power coming from dc link to a suitable ac power for the main grid, but also to fix the PF of the local grid at a target PF by injecting enough reactive power to the grid. In the proposed control strategy, the concepts of the inverter and the D-STATCOM have been combined to make a new inverter, which possesses FACTS capability with no additional cost. The proposed control strategy allows the inverter to act as an inverter with D-STATCOM option when there is enough wind to produce active power, and to act as a D-STATCOM when there is no wind. The active power is controlled by adjusting the power angle  $\delta$ , which is the angle between the voltages of the inverter and the grid, and reactive power is regulated by the modulation index  $m$ .

There are a large number of publications on integration of renewable energy systems into power systems. A list of complete publications on FACTS applications for grid integration of wind and solar energy was presented in [3]. In [4], new commercial wind energy converters with FACTS capabilities are introduced without any detailed information regarding the efficiency or the topology used for the converters. In [5], a complete list of the most important multilevel inverters was reviewed. Also, different modulation methods such as sinusoidal pulse width modulation (PWM), selective harmonic elimination, optimized harmonic stepped waveform technique, and space vector modulation were discussed and compared.

Among all multilevel topologies, the cascaded H-bridge multilevel converter is very well known for STATCOM applications for several reasons [10]–[12]. The main reason is that it is simple to obtain a high number of levels, which can help to connect STATCOM directly to medium voltage grids. The modular multilevel converter (MMC) was introduced in the early 2000s. Reference [15] describes a MMC converter for high voltage DC (HVDC) applications. This project mostly looks at the main circuit components. Also, it compares two different types of MMC, including H-bridge and full-bridge submodules.

In [9] and [16], a new single-phase inverter using hybrid clamped topology for renewable energy systems is presented. The proposed inverter is placed between the renewable energy source and the main grid. The main drawback of the proposed

inverter is that the output current has significant fluctuations that are not compatible with IEEE standards. The authors believe that the problem is related to the snubber circuit design.

Several other applications of custom power electronics in renewable energy systems exist, including [17] an application of a custom power interface where two modes of operation, including an active power filter and a renewable energy STATCOM. Another application [18] looks at the current source inverter, which controls reactive power and regulates voltage at the point of common coupling (PCC). Varma *et al.* [19], [20] propose an application of photovoltaic (PV) solar inverter as STATCOM in order to regulate voltage on three phase power systems, for improving transient stability and power transfer limit in transmission systems. The authors called their proposed system PV-STATCOM. Similar to wind farms (when there is no wind), solar farms are idle during nights. We proposed a control strategy that makes the solar farms to act as STATCOMs during night when they are not able to produce active power. The main purpose of the PV-STATCOM system is to improve the voltage control and the PF correction on three-phase transmission systems.

In this project, the proposed WEI utilizes MMC topology, which has been introduced recently for HVDC applications. Replacing conventional inverters with this inverter will eliminate the need to use a separate capacitor bank or a STATCOM device to fix the PF of the local distribution grids. Obviously, depending on the size of the power system, multiple inverters might be used in order to reach the desired PF. The unique work in this project is the use of MMC topology for a single phase voltage-source inverter, which meets the IEEE standard 519 requirements, and is able to control the PF of the grid regardless of the wind speed Fig. 1 shows the complete grid-connected mode configuration of the proposed inverter. The dc link of the inverter is connected to the wind turbine through a rectifier using MPPT and its output terminal is connected to the utility grid through a series-connected second-order filter and a distribution transformer.

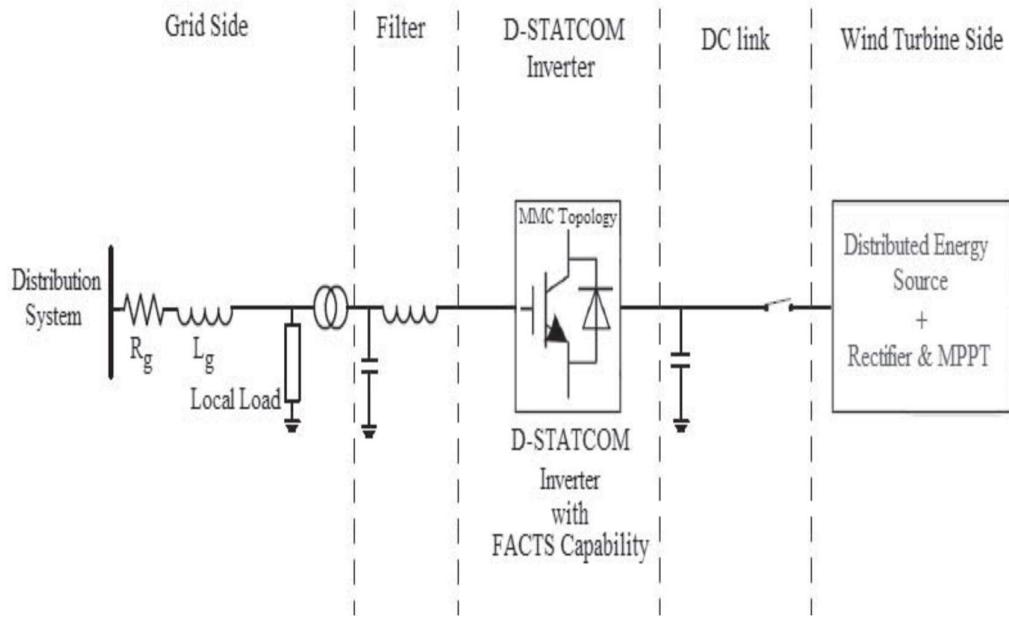


Fig. 1.1 Complete configuration of the proposed inverter with FACTS capability

# **CHAPTER-2**

## **FACTS**

### **2.1 FACTS Devices**

Flexible AC Transmission Systems, called FACTS, got in the recent years a well-known term for higher controllability in power systems by means of power electronic devices. Several FACTS-devices have been introduced for various applications worldwide. A number of new types of devices are in the stage of being introduced in practice.

In most of the applications the controllability is used to avoid cost intensive or landscape requiring extensions of power systems, for instance like upgrades or additions of substations and power lines. FACTS-devices provide a better adaptation to varying operational conditions and improve the usage of existing installations. The basic applications of FACTS-devices are:

- Power flow control,
- Increase of transmission capability,
- Voltage control,
- Reactive power compensation,
- Stability improvement,
- Power quality improvement,
- Power conditioning,
- Flicker mitigation,
- Interconnection of renewable and distributed generation and storages.

Figure 2.1 shows the basic idea of FACTS for transmission systems. The usage of lines for active power transmission should be ideally up to the thermal limits. Voltage and stability limits shall be shifted with the means of the several different FACTS devices. It can be seen that with growing line length, the opportunity for FACTS devices gets more and more important.

The influence of FACTS-devices is achieved through switched or controlled shunt compensation, series compensation or phase shift control. The devices work

electrically as fast as current, voltage or impedance controllers. The power electronic component allows very short reaction times down to far below one second.

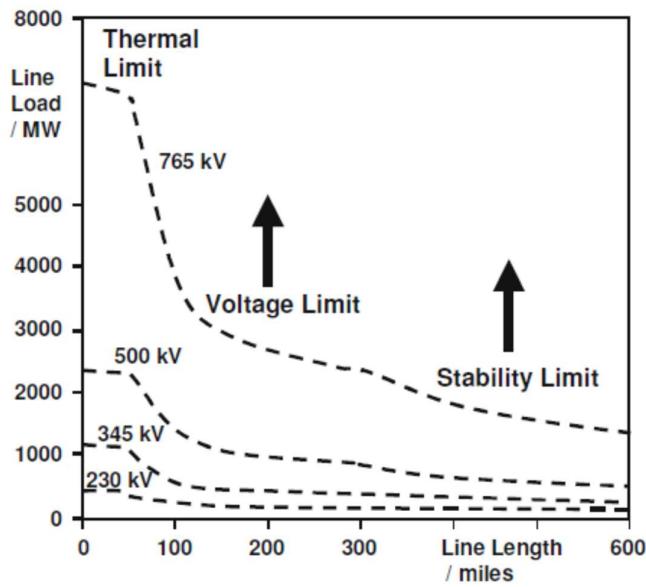


Fig 2.1 Operational limits of transmission lines for different voltage levels

The development of FACTS-devices has started with the growing capabilities of power electronic components. Devices for high power levels have been made available in converters for high and even highest voltage levels. The overall starting points are network elements influencing the reactive power or the impedance of a part of the power system. Figure 2.2 shows a number of basic devices separated into the conventional ones and the FACTS-devices.

For the FACTS side the taxonomy in terms of 'dynamic' and 'static' needs some explanation. The term 'dynamic' is used to express the fast controllability of FACTS-devices provided by the power electronics. This is one of the main differentiation factors from the conventional devices. The term 'static' means that the devices have no moving parts like mechanical switches to perform the dynamic controllability. Therefore most of the FACTS-devices can equally be static and dynamic.

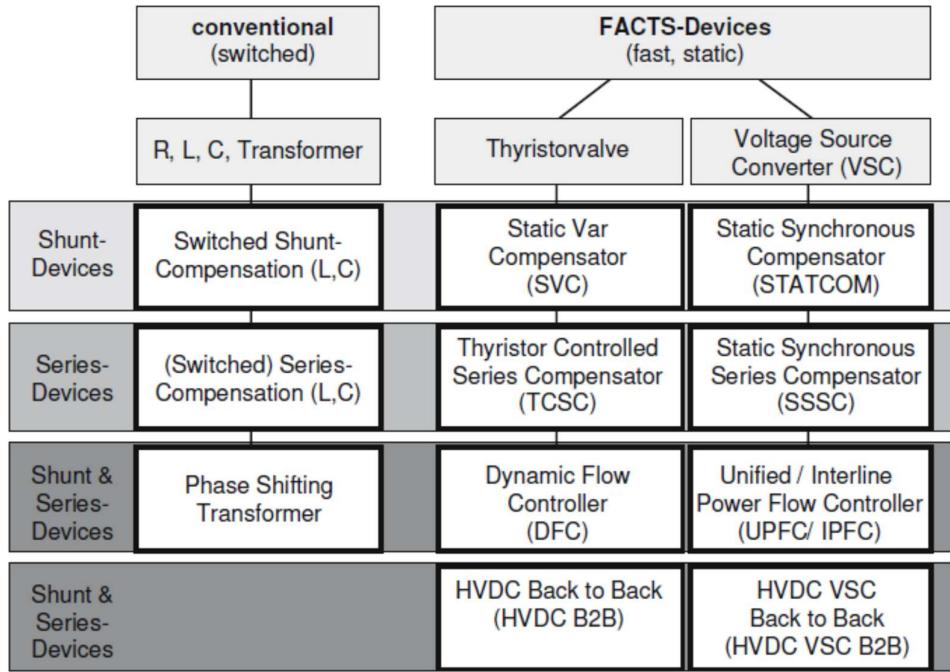


Fig 2.2 Overview of major FACTS-Devices

## 2.2 Overview of Major FACTS-Devices:

The left column in Figure 2.2 contains the conventional devices build out of fixed or mechanically switchable components like resistance, inductance or capacitance together with transformers. The FACTS-devices contain these elements as well but use additional power electronic valves or converters to switch the elements in smaller steps or with switching patterns within a cycle of the alternating current. The left column of FACTS-devices uses Thyristor valves or converters. These valves or converters are well known since several years. They have low losses because of their low switching frequency of once a cycle in the converters or the usage of the Thyristors to simply bridge impedances in the valves.

The right column of FACTS-devices contains more advanced technology of voltage source converters based today mainly on Insulated Gate Bipolar Transistors (IGBT) or Insulated Gate Co006DUMutated Thyristors (IGCT). Voltage Source Converters provide a free controllable voltage in magnitude and phase due to a pulse width modulation of the IGBTs or IGCTs. High modulation frequencies allow to get low harmonics in the output signal and even to compensate disturbances coming from the network. The disadvantage is that with an increasing switching frequency, the losses are increasing as well. Therefore special designs of the converters are required to compensate this.

## **2.3 Configurations of FACTS-Devices**

### **2.3.1 Shunt Devices:**

The most used FACTS-device is the SVC or the version with Voltage Source Converter called STATCOM. These shunt devices are operating as reactive power compensators. The main applications in transmission, distribution and industrial networks are:

- Reduction of unwanted reactive power flows and therefore reduced network losses.
- Keeping of contractual power exchanges with balanced reactive power.
- Compensation of consumers and improvement of power quality especially with huge demand fluctuations like industrial machines, metal melting plants, railway or underground train systems.
- Compensation of Thyristor converters e.g. in conventional HVDC lines.
- Improvement of static or transient stability.

Almost half of the SVC and more than half of the STATCOMs are used for industrial applications. Industry as well as commercial and domestic groups of users require power quality. Flickering lamps are no longer accepted, nor are interruptions of industrial processes due to insufficient power quality. Railway or underground systems with huge load variations require SVCs or STATCOMs.

### **2.3.2 Static Var Compensator (SVC):**

Electrical loads both generate and absorb reactive power. Since the transmitted load varies considerably from one hour to another, the reactive power balance in a grid varies as well. The result can be unacceptable voltage amplitude variations or even a voltage depression, at the extreme a voltage collapse.

A rapidly operating Static Var Compensator (SVC) can continuously provide the reactive power required to control dynamic voltage oscillations under various system conditions and thereby improve the power system transmission and distribution stability.

### **2.3.3 Applications of the SVC systems in transmission systems**

- a. To increase active power transfer capacity and transient stability margin
- b. To damp power oscillations
- c. To achieve effective voltage control

## **1. in transmission systems**

- To reduce temporary over voltages
- To damp sub synchronous resonances
- To damp power oscillations in interconnected power system

## **2. in traction systems**

- To balance loads
- To improve power factor
- To improve voltage regulation

## **3. In HVDC systems**

- To provide reactive power to ac–dc converters

## **4. In arc furnaces**

- To reduce voltage variations and associated light flicker

Installing an SVC at one or more suitable points in the network can increase transfer capability and reduce losses while maintaining a smooth voltage profile under different network conditions. In addition an SVC can mitigate active power oscillations through voltage amplitude modulation.

SVC installations consist of a number of building blocks. The most important is the Thyristor valve, i.e. stack assemblies of series connected anti-parallel Thyristors to provide controllability. Air core reactors and high voltage AC capacitors are the reactive power elements used together with the Thyristor valves. The step up connection of this equipment to the transmission voltage is achieved through a power transformer.

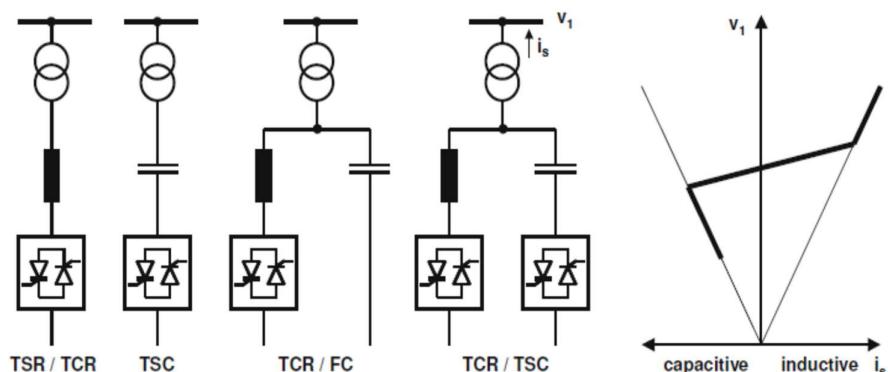


Fig 2.3 SVC building blocks and voltage / current characteristic

In principle the SVC consists of Thyristor Switched Capacitors (TSC) and Thyristor Switched or Controlled Reactors (TSR / TCR). The coordinated control of a combination of these branches varies the reactive power as shown in Figure 2.4. The first commercial SVC was installed in 1972 for an electric arc furnace. On transmission level the first SVC was used in 1979. Since then it is widely used and the most accepted FACTS-device.

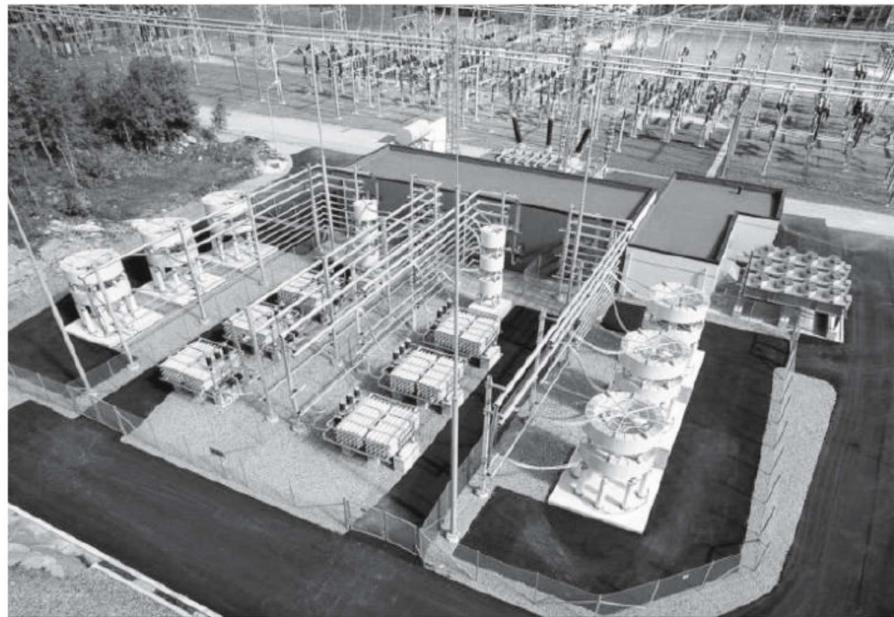


Fig 2.4 Static var compensator reactive power

#### 2.4 SVC USING A TCR AND AN FC:

In this arrangement, two or more FC (fixed capacitor) banks are connected to a TCR (thyristor controlled reactor) through a step-down transformer. The rating of the reactor is chosen larger than the rating of the capacitor by an amount to provide the maximum lagging vars that have to be absorbed from the system. By changing the firing angle of the thyristor controlling the reactor from  $90^\circ$  to  $180^\circ$ , the reactive power can be varied over the entire range from maximum lagging vars to leading vars that can be absorbed from the system by this compensator.

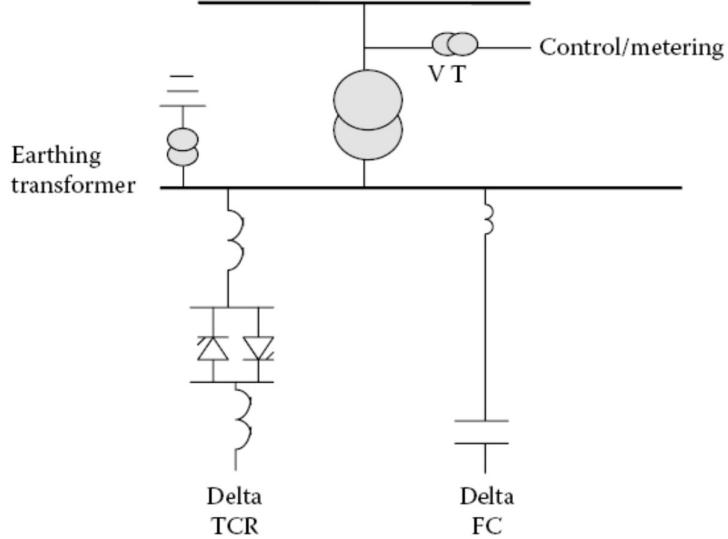


Fig 2.5 SVC using a TCR and an FC

#### 2.4.1 SVC of the FC/TCR type:

The main disadvantage of this configuration is the significant harmonics that will be generated because of the partial conduction of the large reactor under normal sinusoidal steady-state operating condition when the SVC is absorbing zero MVar. These harmonics are filtered in the following manner. Triplex harmonics are canceled by arranging the TCR and the secondary windings of the step-down transformer in delta connection. The capacitor banks with the help of series reactors are tuned to filter fifth, seventh, and other higher-order harmonics as a high-pass filter. Further losses are high due to the circulating current between the reactor and capacitor banks.

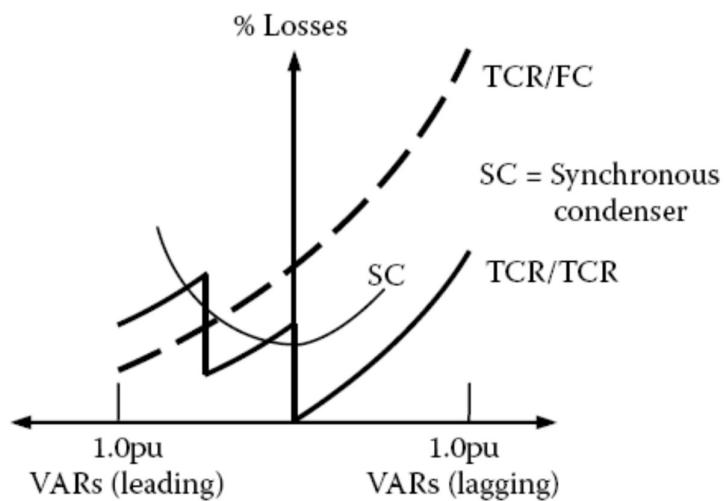


Fig 2.6 Loss characteristics

Comparison of the loss characteristics of TSC–TCR, TCR–FC compensators and synchronous condenser

These SVCs do not have a short-time overload capability because the reactors are usually of the air-core type. In applications requiring overload capability, TCR must be designed for short-time overloading, or separate thyristor-switched overload reactors must be employed.

#### 2.4.2 SVC USING A TCR AND TSC:

This compensator overcomes two major shortcomings of the earlier compensators by reducing losses under operating conditions and better performance under large system disturbances. In view of the smaller rating of each capacitor bank, the rating of the reactor bank will be  $1/n$  times the maximum output of the SVC, thus reducing the harmonics generated by the reactor. In those situations where harmonics have to be reduced further, a small amount of FCs tuned as filters may be connected in parallel with the TCR.

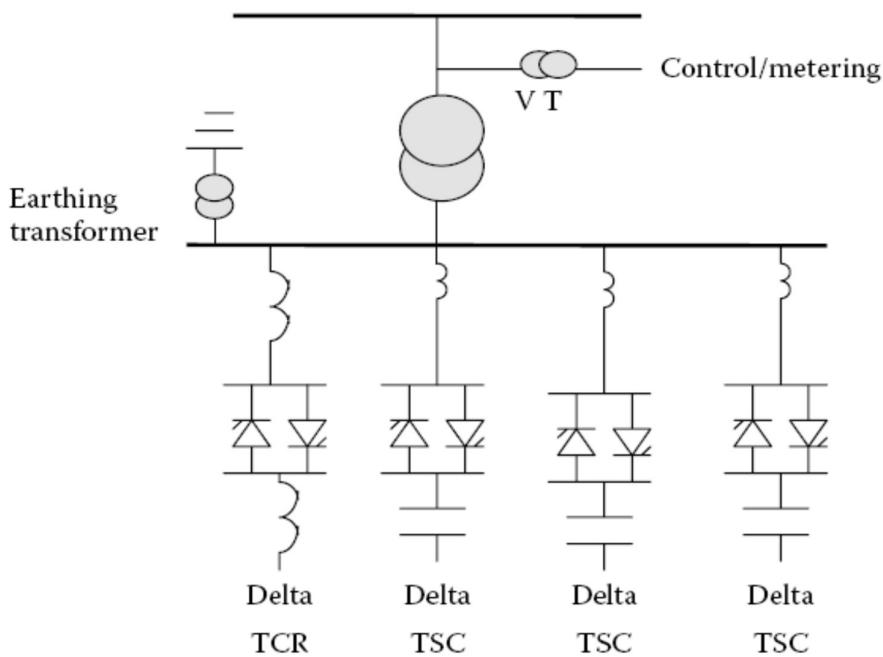


Fig 2.7 SVC using a TCR and TSC

#### 2.4.3 SVC of combined TSC and TCR type

When large disturbances occur in a power system due to load rejection, there is a possibility for large voltage transients because of oscillatory interaction between system and the SVC capacitor bank or the parallel. The LC circuit of the SVC in the

FC compensator. In the TSC–TCR scheme, due to the flexibility of rapid switching of capacitor banks without appreciable disturbance to the power system, oscillations can be avoided, and hence the transients in the system can also be avoided. The capital cost of this SVC is higher than that of the earlier one due to the increased number of capacitor switches and increased control complexity.

## 2.5 STATCOM:

In 1999 the first SVC with Voltage Source Converter called STATCOM (Static Compensator) went into operation. The STATCOM has a characteristic similar to the synchronous condenser, but as an electronic device it has no inertia and is superior to the synchronous condenser in several ways, such as better dynamics, a lower investment cost and lower operating and maintenance costs. A STATCOM is built with Thyristors with turn-off capability like GTO or today IGBT or with more and more IGBTs. The static line between the current limitations has a certain steepness determining the control characteristic for the voltage.

The advantage of a STATCOM is that the reactive power provision is independent from the actual voltage on the connection point. This can be seen in the diagram for the maximum currents being independent of the voltage in comparison to the SVC. This means, that even during most severe contingencies, the STATCOM keeps its full capability.

In the distributed energy sector the usage of Voltage Source Converters for grid interconnection is common practice today. The next step in STATCOM development is the combination with energy storages on the DC-side. The performance for power quality and balanced network operation can be improved much more with the combination of active and reactive power.

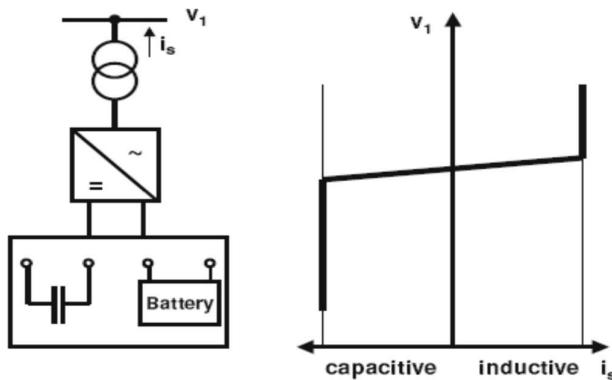


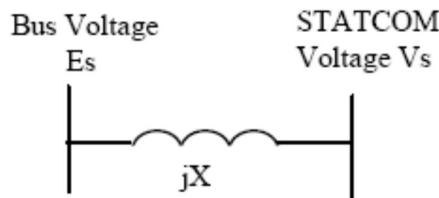
Fig 2.8 STATCOM structure and voltage / current characteristic

STATCOMs are based on Voltage Sourced Converter (VSC) topology and utilize either Gate-Turn-off Thyristors (GTO) or Isolated Gate Bipolar Transistors (IGBT) devices. The STATCOM is a very fast acting, electronic equivalent of a synchronous condenser. If the STATCOM voltage,  $V_s$ , (which is proportional to the dc bus voltage  $V_c$ ) is larger than bus voltage,  $E_s$ , then leading or capacitive VARS are produced. If  $V_s$  is smaller than  $E_s$  then lagging or inductive VARS are produced.

### 2.5.1 Six Pulses STATCOM

The three phases STATCOM makes use of the fact that on a three phase, fundamental frequency, steady state basis, and the instantaneous power entering a purely reactive device must be zero. The reactive power in each phase is supplied by circulating the instantaneous real power between the phases. This is achieved by firing the GTO/diode switches in a manner that maintains the phase difference between the ac bus voltage  $E_s$  and the STATCOM generated voltage  $V_s$ . Ideally it is possible to construct a device based on circulating instantaneous power which has no energy storage device (ie no dc capacitor).

A practical STATCOM requires some amount of energy storage to accommodate harmonic power and ac system unbalances, when the instantaneous real power is non-zero. The maximum energy storage required for the STATCOM is much less than for a TCR/TSC type of SVC compensator of comparable rating.



$$I = (E_s - V_s) / jX$$

Fig 2.9 STATCOM Equivalent Circuit

Several different control techniques can be used for the firing control of the STATCOM. Fundamental switching of the GTO/diode once per cycle can be used. This approach will minimize switching losses, but will generally utilize more complex transformer topologies. As an alternative, Pulse Width Modulated (PWM) techniques, which turn on and off the GTO or IGBT switch more than once per cycle, can be used.

This approach allows for simpler transformer topologies at the expense of higher switching losses.

The 6 Pulse STATCOM using fundamental switching will of course produce the 6 N1 harmonics. There are a variety of methods to decrease the harmonics. These methods include the basic 12 pulse configuration with parallel star / delta transformer connections, a complete elimination of 5th and 7th harmonic current using series connection of star/star and star/delta transformers and a quasi-12 pulse method with a single star-star transformer, and two secondary windings, using control of firing angle to produce a 30 phase shift between the two 6 pulse bridges. This method can be extended to produce a 24 pulse and a 48 pulse STATCOM, thus eliminating harmonics even further. Another possible approach for harmonic cancellation is a multi-level configuration which allows for more than one switching element per level and therefore more than one switching in each bridge arm. The ac voltage derived has a staircase effect, dependent on the number of levels. This staircase voltage can be controlled to eliminate harmonics.

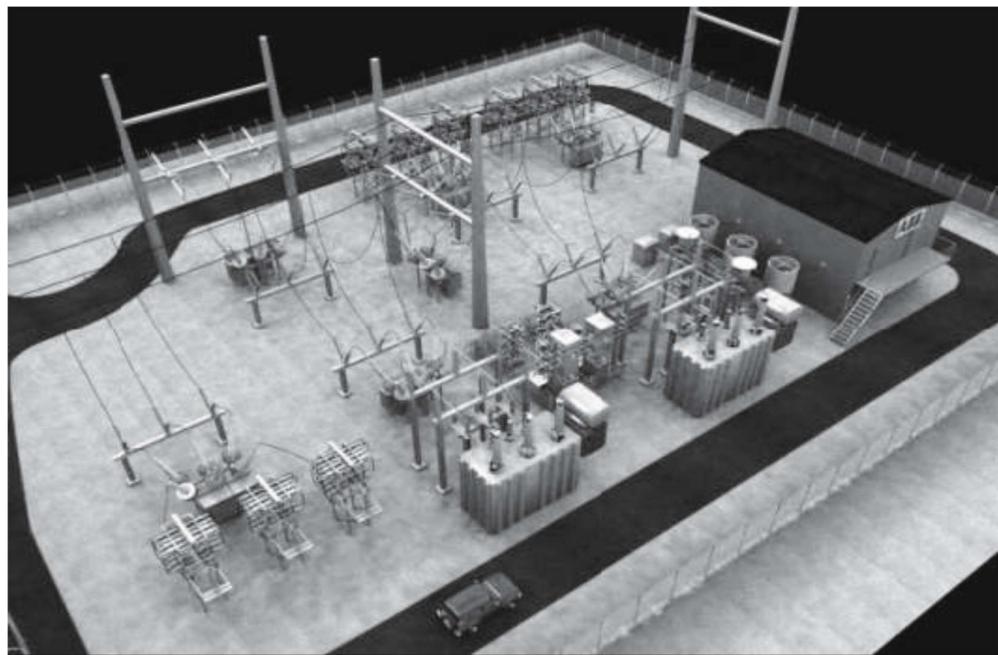


Fig 2.10 Substation with a STATCOM

### 2.5.2 Series Devices:

Series devices have been further developed from fixed or mechanically switched compensations to the Thyristor Controlled Series Compensation (TCSC) or even Voltage Source Converter based devices.

The main applications are:

- Reduction of series voltage decline in magnitude and angle over a power line,
- Reduction of voltage fluctuations within defined limits during changing power transmissions,
- Improvement of system damping resp. damping of oscillations,
- Limitation of short circuit currents in networks or substations,
- Avoidance of loop flows resp. power flow adjustments.

## 2.6 TCSC:

Thyristor Controlled Series Capacitors (TCSC) addresses specific dynamical problems in transmission systems. Firstly, it increases damping when large electrical systems are interconnected. Secondly it can overcome the problem of Sub Synchronous Resonance (SSR), a phenomenon that involves an interaction between large thermal generating units and series compensated transmission systems.

The TCSC's high speed switching capability provides a mechanism for controlling line power flow, which permits increased loading of existing transmission lines, and allows for rapid readjustment of line power flow in response to various contingencies. The TCSC also can regulate steady-state power flow within its rating limits.

From a principal technology point of view, the TCSC resembles the conventional series capacitor. All the power equipment is located on an isolated steel platform, including the Thyristor valve that is used to control the behavior of the main capacitor bank. Likewise the control and protection is located on ground potential together with other auxiliary systems. Figure shows the principle setup of a TCSC and its operational diagram. The firing angle and the thermal limits of the Thyristors determine the boundaries of the operational diagram.

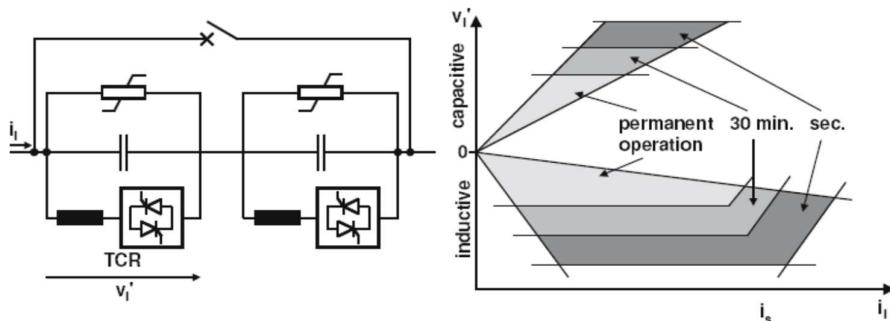


Fig 2.11 Thyristor Controlled Series Capacitors (TCSC)

## **Advantages**

- Continuous control of desired compensation level
- Direct smooth control of power flow within the network
- Improved capacitor bank protection
- Local mitigation of sub synchronous resonance (SSR). This permits higher levels of compensation in networks where interactions with turbine-generator torsional vibrations or with other control or measuring systems are of concern.
- Damping of electromechanical (0.5-2 Hz) power oscillations which often arise between areas in a large interconnected power network. These oscillations are due to the dynamics of inter area power transfer and often exhibit poor damping when the aggregate power transfer over a corridor is high relative to the transmission strength.

### **2.6.1 Shunt and Series Devices**

#### **Dynamic Power Flow Controller**

A new device in the area of power flow control is the Dynamic Power Flow Controller (DFC). The DFC is a hybrid device between a Phase Shifting Transformer (PST) and switched series compensation. The Dynamic Flow Controller consists of the following components:

- A standard phase shifting transformer with tap-changer (PST)
- Series-connected Thyristor Switched Capacitors and Reactors (TSC / TSR)
- A mechanically switched shunt capacitor (MSC). (This is optional depending on the system reactive power requirements)

Based on the system requirements, a DFC might consist of a number of series TSC or TSR. The mechanically switched shunt capacitor (MSC) will provide voltage support in case of overload and other conditions. Normally the reactance of reactors and the capacitors are selected based on a binary basis to result in a desired stepped reactance variation. If a higher power flow resolution is needed, a reactance equivalent to the half of the smallest one can be added.

The switching of series reactors occurs at zero current to avoid any harmonics. However, in general, the principle of phase-angle control used in TCSC can be applied for a continuous control as well. The operation of a DFC is based on the following rules:

- TSC / TSR are switched when a fast response is required.
- The relieve of overload and work in stressed situations is handled by the TSR

- The switching of the PST tap-changer should be minimized particularly for the currents higher than normal loading.
- The total reactive power consumption of the device can be optimized by the operation of the MSC, tap changer and the switched capacities and reactors.

In order to visualize the steady state operating range of the DFC, we assume an inductance in parallel representing parallel transmission paths. The overall control objective in steady state would be to control the distribution of power flow between the branch with the DFC and the parallel path. This control is accomplished by control of the injected series voltage.

The PST (assuming a quadrature booster) will inject a voltage in quadrature with the node voltage. The controllable reactance will inject a voltage in quadrature with the throughput current. Assuming that the power flow has a load factor close to one, the two parts of the series voltage will be close to collinear. However, in terms of speed of control, influence on reactive power balance and effectiveness at high/low loading the two parts of the series voltage has quite different characteristics. The steady state control range for loadings up to rated current is illustrated in Figure 2.12, where the x-axis corresponds to the throughput current and the y-axis corresponds to the injected series voltage.

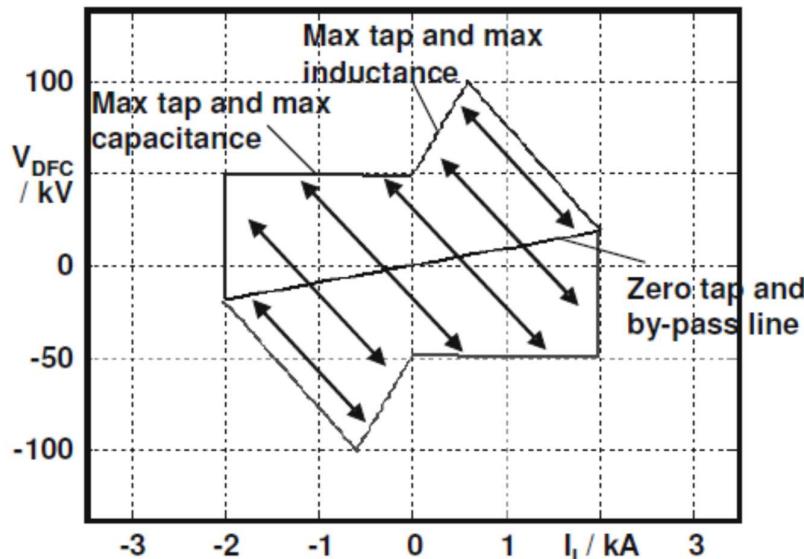


Fig 2.12 Operational diagram of a DFC

Operation in the first and third quadrants corresponds to reduction of power through the DFC, whereas operation in the second and fourth quadrants corresponds to increasing the power flow through the DFC. The slope of the line passing through the origin (at which the tap is at zero and TSC / TSR are bypassed) depends on the short circuit reactance of the PST.

Starting at rated current (2 kA) the short circuit reactance by itself provides an injected voltage (approximately 20 kV in this case). If more inductance is switched in and/or the tap is increased, the series voltage increases and the current through the DFC decreases (and the flow on parallel branches increases). The operating point moves along lines parallel to the arrows in the figure. The slope of these arrows depends on the size of the parallel reactance. The maximum series voltage in the first quadrant is obtained when all inductive steps are switched in and the tap is at its maximum.

Now, assuming maximum tap and inductance, if the throughput current decreases (due e.g. to changing loading of the system) the series voltage will decrease. At zero current, it will not matter whether the TSC / TSR steps are in or out, they will not contribute to the series voltage. Consequently, the series voltage at zero current corresponds to rated PST series voltage. Next, moving into the second quadrant, the operating range will be limited by the line corresponding to maximum tap and the capacitive step being switched in (and the inductive steps by-passed). In this case, the capacitive step is approximately as large as the short circuit reactance of the PST, giving an almost constant maximum voltage in the second quadrant.

## 2.7 Unified Power Flow Controller:

The UPFC is a combination of a static compensator and static series compensation. It acts as a shunt compensating and a phase shifting device simultaneously.

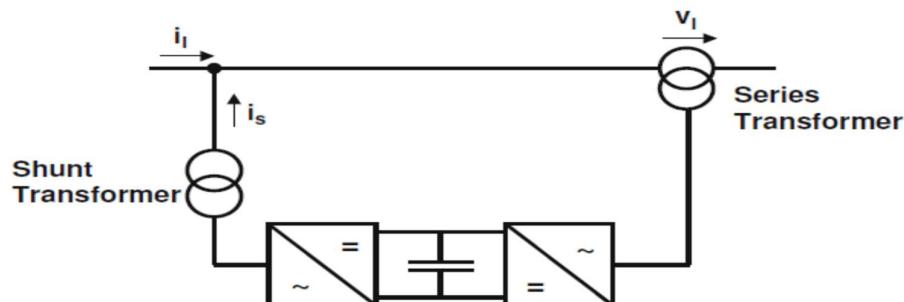


Fig 2.13 Principle configuration of an UPFC

The UPFC consists of a shunt and a series transformer, which are connected via two voltage source converters with a common DC-capacitor. The DC-circuit allows the active power exchange between shunt and series converter to control the phase shift of the series voltage. This setup, as shown in Figure 2.7, provides the full controllability for voltage and power flow. The series converter needs to be protected with a Thyristor bridge. Due to the high efforts for the Voltage Source Converters and the protection, an UPFC is getting quite expensive, which limits the practical applications where the voltage and power flow control is required simultaneously.

### 2.7.1 OPERATING PRINCIPLE OF UPFC

The basic components of the UPFC are two voltage source inverters (VSIs) sharing a common dc storage capacitor, and connected to the power system through coupling transformers. One VSI is connected to in shunt to the transmission system via a shunt transformer, while the other one is connected in series through a series transformer. A basic UPFC functional scheme is shown in fig 2.14

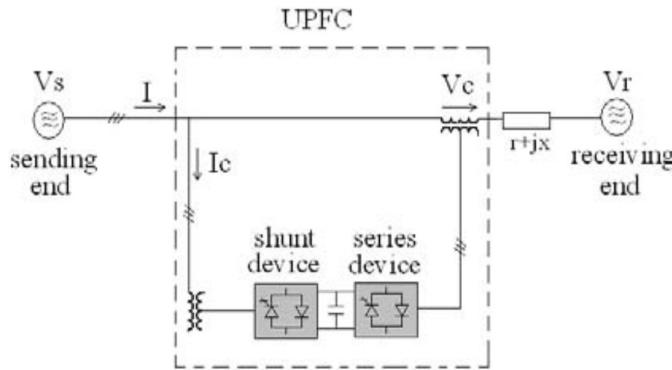


Fig 2.14 Functional scheme of UPSC

The series inverter is controlled to inject a symmetrical three phase voltage system ( $V_{se}$ ), of controllable magnitude and phase angle in series with the line to control active and reactive power flows on the transmission line. So, this inverter will exchange active and reactive power with the line. The reactive power is electronically provided by the series inverter, and the active power is transmitted to the dc terminals. The shunt inverter is operated in such a way as to demand this dc terminal power (positive or negative) from the line keeping the voltage across the storage capacitor  $V_{dc}$  constant. So, the net real power absorbed from the line by the UPFC is equal only to the losses of the inverters and their transformers. The remaining capacity of the shunt inverter can be used to exchange reactive power with the line so to provide a voltage regulation at the connection point.

The two VSI's can work independently of each other by separating the dc side. So in that case, the shunt inverter is operating as a STATCOM that generates or absorbs reactive power to regulate the voltage magnitude at the connection point. Instead, the series inverter is operating as SSSC that generates or absorbs reactive power to regulate the current flow, and hence the power low on the transmission line.

The UPFC has many possible operating modes. In particular, the shunt inverter is operating in such a way to inject a controllable current, is into the transmission line. The shunt inverter can be controlled in two different modes:

**VAR Control Mode:** The reference input is an inductive or capacitive VAR request. The shunt inverter control translates the var reference into a corresponding shunt current request and adjusts gating of the inverter to establish the desired current. For this mode of control a feedback signal representing the dc bus voltage,  $V_{dc}$ , is also required.

**Automatic Voltage Control Mode:** The shunt inverter reactive current is automatically regulated to maintain the transmission line voltage at the point of connection to a reference value. For this mode of control, voltage feedback signals are obtained from the sending end bus feeding the shunt coupling transformer.

The series inverter controls the magnitude and angle of the voltage injected in series with the line to influence the power flow on the line. The actual value of the injected voltage can be obtained in several ways.

- Direct Voltage Injection Mode:** The reference inputs are directly the magnitude and phase angle of the series voltage.
- Phase Angle Shifter Emulation mode:** The reference input is phase displacement between the sending end voltage and the receiving end voltage.
- Line Impedance Emulation mode:** The reference input is an impedance value to insert in series with the line impedance
- Automatic Power Flow Control Mode:** The reference inputs are values of P and Q to maintain on the transmission line despite system changes.

# CHAPTER-3

## MULTILEVEL INVERTERS

### 3.1 Introduction

Inverters have been developed over the last three decades for the purpose of meeting the drive high voltage rating and low dv/dt value requirements that could not be met by the classical two-level inverter. Until recently, power transistors were slow, and their long turn-on and off times resulted in excessive switching losses that constrained the switching frequency to several kHz values. Also the voltage blocking capability of power transistors was below a kilovolt that implied such switches could not be utilized in two-level inverters at high voltage levels and could not be operated at switching frequencies in the tens of kilohertz range.

#### 3.1.1 Introduction GTO

In the early 1980's utilizing darlington power transistors and Gate Turn Off Thyristors (GTOs), the three-level NPC inverter could provide effectively quadrupled switching frequency and could provide high inverter voltage ratings (twice that of the two-level inverter). As a result, power and voltage levels above that of two-level inverter could be reached and the three-level NPC inverter has found immediate application in traction drives and industrial drives.

#### 3.1.2 Introduction IGBT

In the 1990's, the IGBT was introduced as a fast turn-on, fast turn-off device that provided significant switching loss reduction and also the secondary breakdown of the Bipolar Junction Transistor (BJT) was absent. As a result, IGBTs with higher switching frequencies and blocking voltages have extended the two-level inverter ratings to the kilovolt level and some of the three-level NPC inverter applications could be replaced with the two-level inverter. However, in particular in the 400 V and above voltage levels, the two-level inverter turned out to be problematic in terms of the dv/dt stresses during the fast switching of IGBTs. As a result, the NPC inverter has been favored again due to its reduced dv/dt rating compared to the two-level inverter. As a result at 400 V and above, when fast IGBTs are utilized it is presently favorable to utilize the three-level NPC inverter.

At the present time, as the power converter rating increases above a megawatt, which also implies a voltage rating above 400 V, the practical power converter topology is a multilevel inverter topology. In the lower megawatt range the three levels NPC inverter and at the higher range the cascaded H-bridge topology have been in use in industry for longer than a decade.

Utility power electronics applications such as Static Compensator (STATCOM), Unified Power Flow Controller (UPFC), and Flexible AC Transmission System (FACTS) applications involve higher level inverters such as four, five or higher level NPC inverters and recently the flying capacitor topology has also been considered.

In the utility power electronics applications, multilevel inverters are required because the voltage levels involved are very high (kV range) and the required level can only be reached by either series connection of large number of power semiconductor or by means of multilevel inverter topologies involving large number of levels. At the 400 V distribution system level, generally the three-level inverter topology suffices.

### 3.2 Types of Multilevel inverters

In general, multilevel inverter topologies synthesize variable frequency variable voltage that is nearly sinusoidal output waveform with low dv/dt, reduced common mode voltage, and low harmonics yielding a motor friendly performance. Although the topology types are various, in all multilevel inverter topologies the basic idea is to utilize low voltage rating power transistors in series connection along with multistage DC capacitor voltage levels such that higher output voltage levels with small incremental steps could be obtained.

With high voltage waveform quality, the multilevel inverters result in negligible bearing current and decrease the effect of winding insulation breakdown in motor drives. Due to the reduced stresses and EMI, they provide better interface between DC voltage sources/loads and the AC utility grid when operated as PWM rectifiers and power conditioners.

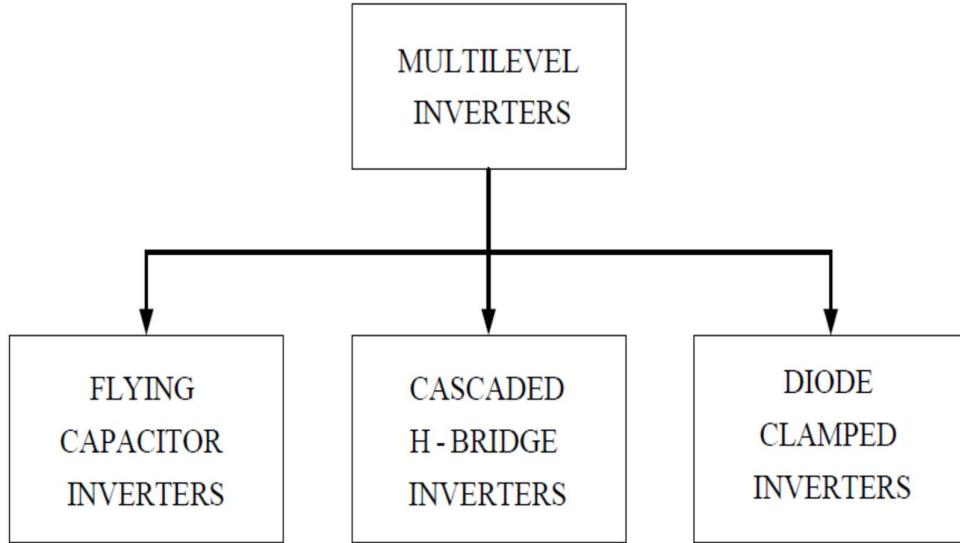


Fig: 3.1 multilevel inverter topologies.

In multilevel inverters, to increase the number of output voltage levels, the number of semiconductor devices and capacitor voltage sources should be increased. As a result, the power and control circuit of the multilevel inverter becomes more complex, large and costly. In addition, significant voltage imbalance problems arise. Therefore, with the three-level inverter being the most common, mainly up to five-level inverters has been reported. The topology option is more constrained than the number of levels. As illustrated in Figure 3.2, multilevel inverter technology involves three different topological structures.

### 3.2.1 Flying Capacitor Multilevel Inverter Topology

The flying capacitor multilevel inverter topology was proposed in 1992. The flying capacitor topology is also called as “capacitor clamped multilevel inverter.” Fig 3.2.10(a) shows one phase leg of the three-level version of this topology and Fig 3.2.10(b) shows corresponding output voltage waveform when switching at the fundamental frequency. The five-level flying capacitor inverter circuit topology and its output voltage waveform are shown in Fig 3.1 and Fig 3.2, respectively. With all capacitor voltages being equal, in the three-level flying capacitor inverter, the output voltage  $V_{U0}$  has three different voltage levels  $-V_{dc}/2$ , 0, and  $+V_{dc}/2$ . For the voltage level  $+V_{dc}/2$  the semiconductor switches SU1 and SU2 have to be turned ON. For the 0 level, semiconductor switches SU1 and SU3 or SU2 and SU4 need to be turned ON.

For  $-V_{dc}/2$ , semiconductor switches SU3 and SU4 need to be turned ON. For the five-level case the same strategy can be used to obtain five-level output voltage waveform.

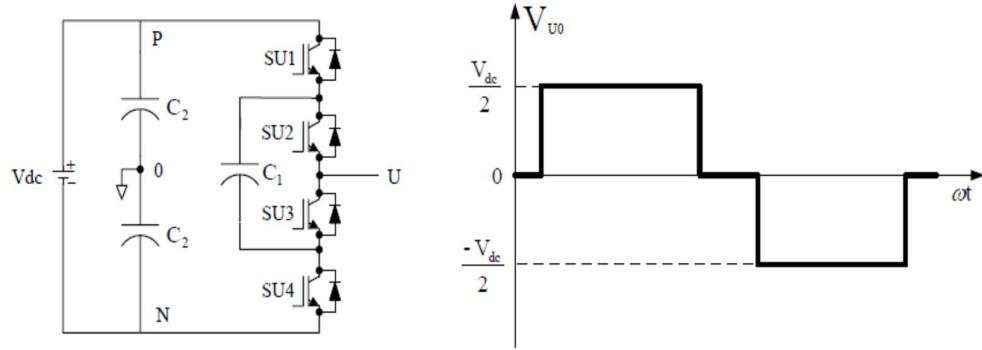


Fig: 3.2 Three-level flying capacitor inverter phase leg structure (a) and output voltage waveform (b).

The capacitor charge control method of the flying capacitor inverter topology is complex and the required control algorithm to maintain capacitor voltages within a specified range is involved. The flying capacitor topology requires larger capacitors (the flying capacitors) than the diode-clamped multilevel inverter DC bus capacitors. Therefore, the flying capacitor topology is not feasible for ASD systems and has mainly been considered for utility power electronics applications.

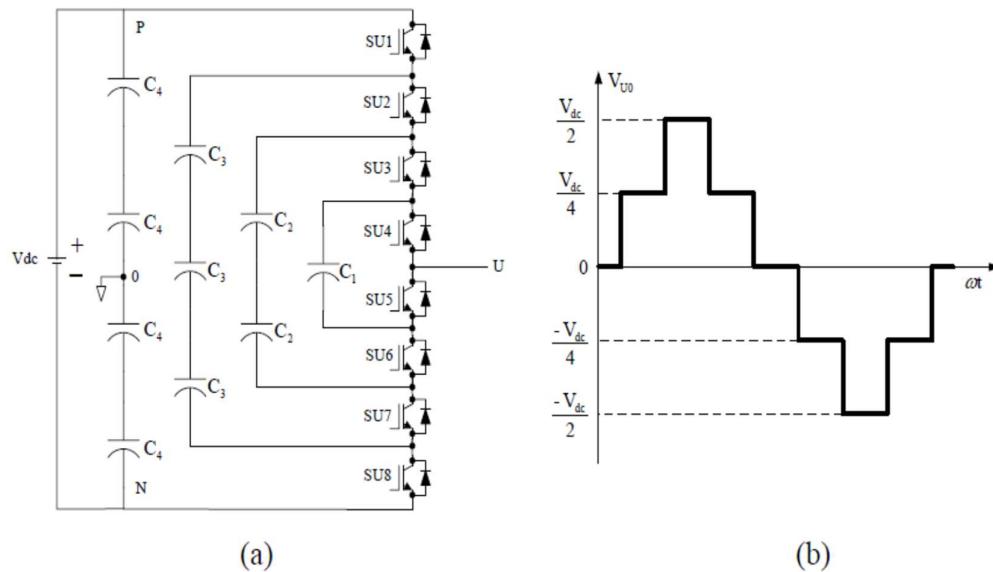


Fig: 3.3 Five-level flying capacitor inverter phase leg structure (a) and output voltage waveform (b).

### 3.2.2 Cascaded H-Bridge Multilevel Inverter Topology

In the cascaded H-bridge inverter topology, single phase H-bridge inverters with isolated (separate) DC sources are connected in series. Each such unit is called a cell. Figure 3.2.2 (a) shows one phase of the five-level cascaded H-bridge inverter topology and Figure 3.2.2 (b) shows the output voltage waveform. This topology has been utilized in industry for medium voltage motor drive applications. Each single-phase H-bridge inverter generates three voltage levels at the output:  $-V_{dc}$ , 0, and  $+V_{dc}$ . This is made possible by connecting the capacitors sequentially to the AC side via semiconductor switches. In the five-level cascaded inverter, two cells per-phase are connected in series as shown in Figure 3.2.2 (a). Of the two cells of a phase, in each cell, the DC bus voltage can be different provided that in each phase the same level cell has the same voltage. Then various voltage step waveforms could be obtained. In the case that the voltage levels of all cells are the same, the analysis and synthesis becomes simple. In this case, depending on the output voltage of each cell, the phase output voltage can be one of the following discrete levels;  $2V_{dc}$ ,  $-V_{dc}$ , 0,  $+V_{dc}$ ,  $+2V_{dc}$ .

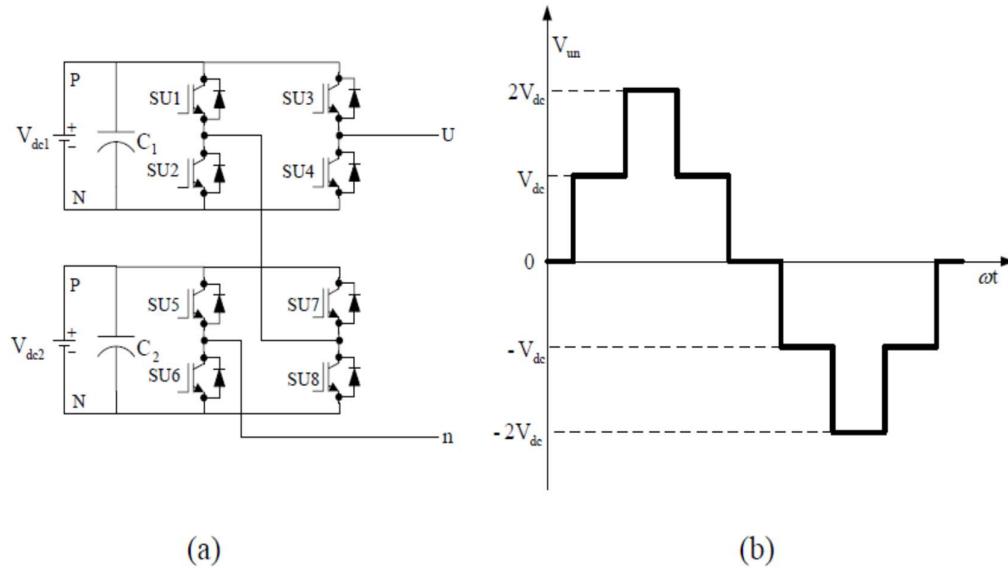


Fig: 3.4 The structure of one phase leg of the five-level cascaded multilevel inverter (a) and its output voltage waveform (b).

The cascaded H-bridge multilevel inverter topology has low harmonic content at the motor terminal voltages and low  $dv/dt$  rating. By selecting various DC bus voltage levels for various cells and also by selecting a sufficiently large cell count, it is possible to obtain high output voltage waveform quality even at very high voltage and power levels. The cascaded H-bridge inverter topology is fault tolerant. A fault in a single-

phase inverter does not necessitate complete shutdown of the ASD system. This structure has modularity, and for this reason maintenance is easy. Isolated DC voltages could be provided via multi winding transformers and with appropriate rectifier and transformer design the drive AC input current waveform could be made of high quality yielding a utility line friendly performance. However, the cascaded H-bridge inverter topology involves a relatively large number of isolated H-bridge modules, a fairly large and complex input transformer, and moreover complex control circuitry. As a result, the topology is utilized in megawatt power rating motor drives. At power ratings below megawatt, the topology is prohibitive in terms of cost and complexity.

### 3.2.3 Diode Clamped Multilevel Inverters

As the first practical multilevel inverter topology, the three-level neutral point clamped (NPC) voltage source inverter was invented by Nabae, et al, in 1980 . Figure 3.2.3 (a) shows one phase leg of this topology and Figure 3.2.3 (b) shows its output voltage waveform. The NPC inverter is also called as the “Three-Level Diode Clamped” NPC inverter. In the topology, the DC bus voltage must be split in two via series connected capacitor banks. In the three-level inverter, the output voltage  $V_{U0}$  has three levels;  $-V_{dc}/2$ , 0, and  $+V_{dc}/2$ . For  $+V_{dc}/2$  semiconductor switches  $S_{U1}$  and  $S_{U2}$  are turned ON. For 0 output voltage, semiconductor switches  $S_{U2}$  and  $S_{U3}$  are turned ON. And for  $-V_{dc}/2$  semiconductor switches  $S_{U3}$  and  $S_{U4}$  are turned ON. The semiconductor switches ( $S_{U1}, S_{U3}$ ) and ( $S_{U2}, S_{U4}$ ) are turned ON and OFF in complementary logic. The clamping diodes  $D_{U1}$  and  $D_{U2}$  clamp the semiconductor switch voltage to half of the DC bus voltage.

In three-phase inverter, the NPC inverter phase output voltage levels and the line-to-line output voltage levels are related with the  $2n-1$  relation. The number of voltage levels of the line to line output voltage waveform is  $2n-1$ , where  $n$  is the number of the phase voltage output levels. Therefore, for the three<sup>17</sup> level NPC inverter case line-to-line output voltage consists of five different voltage levels. The three-level NPC inverter structure was originally developed for the purpose of increasing the power ratings of power converters (to megawatt levels) without paralleling or in series connecting converter modules or semiconductor devices. Since its invention the NPC inverter has found place in significant number of applications involving high voltage and/or power ratings

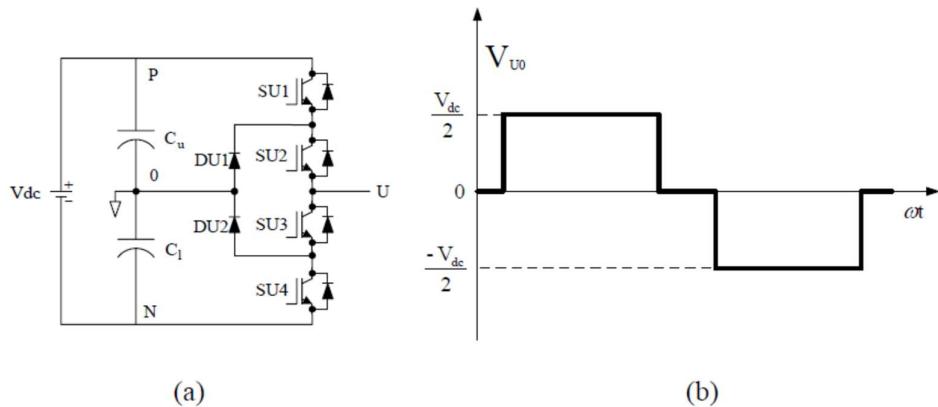


Fig: 3.5 The three-level diode clamped inverter phase leg structure (a) and output voltage waveform (b).

Although the early applications involved niche areas such as railway drives, presently the utilization has spread to the general purpose ASD area. The three-level diode clamped inverter (NPC) inverter has been utilized in 400 V and above voltage ratings in the power range from a few kilowatts to megawatt. This wide range places the three-level NPC inverter in a special place among all the multilevel inverter topologies. Similar to the flying capacitor topology, the three-level NPC inverter topology also has the drawback of capacitor voltage variation. In the three-level NPC inverter the neutral point (connection point of the two DC bus capacitors) potential may drift or vary and countermeasures must be taken when employing this topology.

### 3.3 Cascaded Multilevel Inverters

The smallest number of voltage levels for a multilevel inverter using cascaded inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Fig. 3.6. The inverter circuit consists of four main switches and four freewheeling diodes.

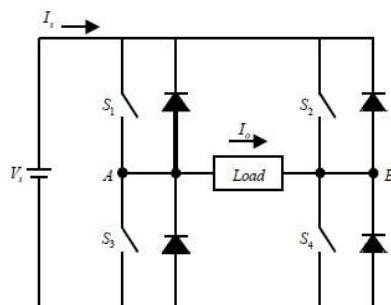


Fig: 3.6 An H-bridge cell.

### 3.3.1 Gate Signal and Inverter Operation

According to four-switch combination, three output voltage levels, +V, -V, and 0, can be synthesized for the voltage across A and B. During inverter operation shown in Fig. 3.6, switch of S1 and S4 are closed at the same time to provide  $V_{AB}$  a positive value and a current path for  $I_o$ . Switch S2 and S3 are turned on to provide  $V_{AB}$  a negative value with a path for  $I_o$ . Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes. When all switches are turned off, the current will flow through the freewheeling diodes.

In case of zero level, there are two possible switching patterns to synthesize zero level, for example, 1) S1 and S2 on, S3 and S4 off, and 2) S1 and S2 off and S3 and S4 on. A simple gate signal, repeated zero-level patterns, is shown in Fig. 3.3.1 All zero levels are generated by turning on S1 and S2.

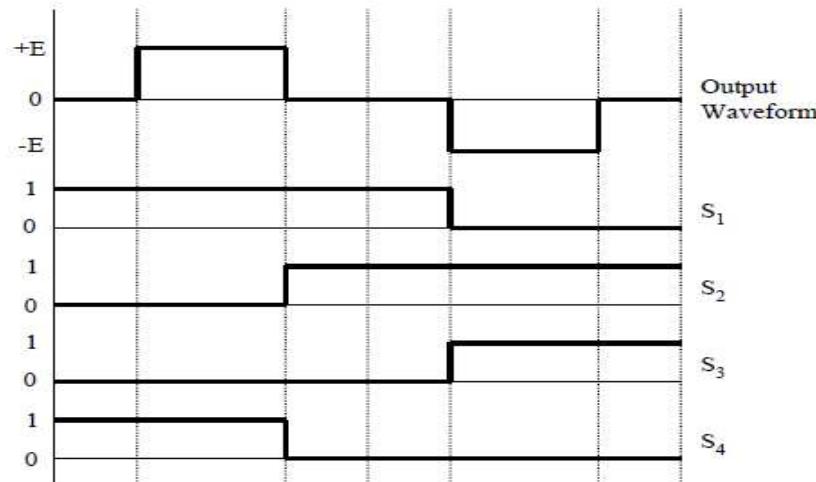


Figure 3.7 (a) Repeated zero-level switching pattern

Note that level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. In Fig. 3.7, S1 and S2 are turned on longer than S3 and S4 do in each cycle because the same zero level switching pattern is used. As a result, S1 and S2 are consuming more power and getting higher temperature than the other two switches. To avoid such a problem, a different switching pattern for zero level is applied. In the first zero stage, S1 and S2 are turned on; then, in the second zero stage, S3 and S4 are turned on instead of S1 and S2. By applying this method, turn-on time for each switch turns out to be equal, as shown in Fig. 3.8. This switching pattern will be used for experimental verification in this thesis.

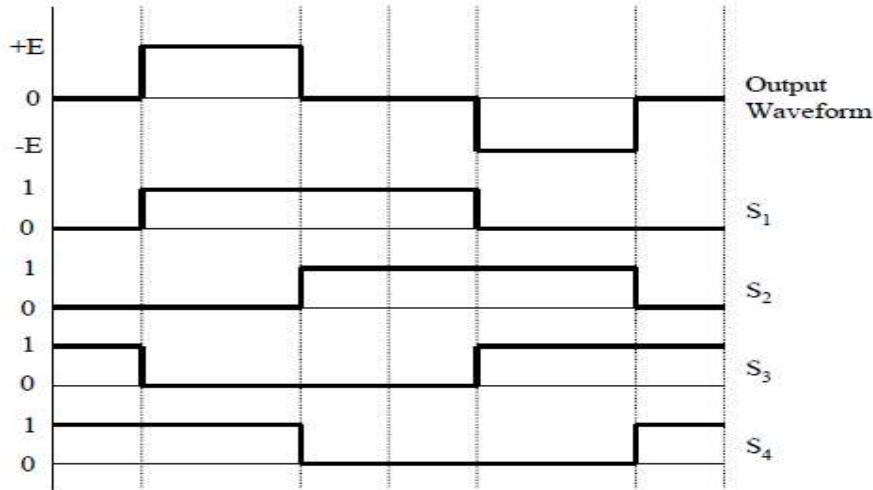


Figure: 3.8 Swapped zero-level switching pattern

### 3.3.2 Blanking Time

Another issue that has to be concerned is providing blanking time for gate signal. In the switches were assumed to be ideal, which allowed the state of the two switches in an inverter leg to change simultaneously from on to off and vice versa. In practice, switching devices are not ideal. To completely turn-off the devices, a short period, which depends on the type of the device, is needed. Usually, because of the finite turn-off and turn-on times associated with any types of switch, a switch is turned off at the switching time instant. However, the turn-on of the other switching in that inverter leg is delayed by a blanking time,  $t_D$ , which is conservatively chosen to avoid cross conduction current through the leg. A blanking time concept is illustrated in Fig 3.9 The leg of S1 and S3 are used as an example.

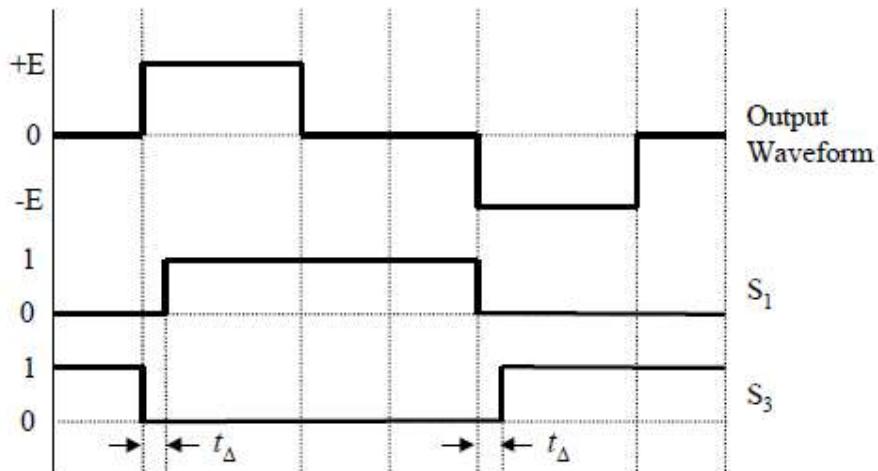


Figure: 3.9 Apply blanking time to the gate signal.

### 3.4 Cascade Inverter Configuration

#### 3.4.1 Single-Phase Structure

To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

$$m = 2s + 1 \text{ where } s \text{ is the number of dc sources} \quad \dots (3.1)$$

For example, a nine-level output phase voltage waveform can be obtained with four-separated dc sources and four H-bridge cells. Fig 3.4.1 (a) shows a general single-phase  $m$ -level cascaded inverter.

From Fig. 3.10, the phase voltage is the sum of each H-bridge outputs and is given as

$$V_{AN} = V_{dc1} + V_{dc2} + \dots + V_{dc(s-1)} + V_{dcS} \quad \dots (3.2)$$

Because zero voltage is common for all inverter outputs, the total level of output voltage waveform becomes  $2s+1$ . An example phase voltage waveform for a nine-level cascaded inverter and all H-bridge cell output waveforms are shown in Fig. 3.10. In this thesis, all dc voltage is assumed to be equal, i.e.,  $V_{dc1} = V_{dc2} = \dots = V_{dc(s-1)} = V_{dcS}$

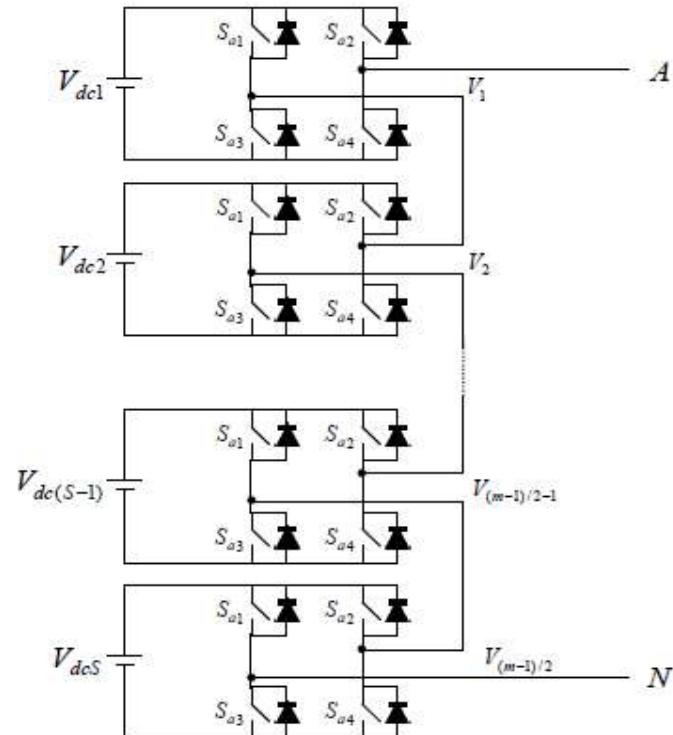


Figure 3.10 Single-phase configuration of an  $m$ -level cascaded inverter.

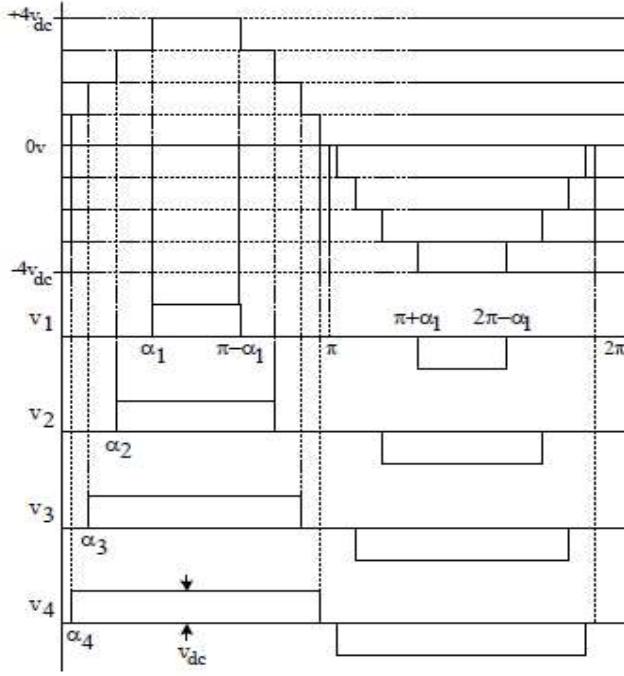


Figure 3.11 Waveform showing a nine-level output phase voltage and each H-bridge output voltage.

According to sinusoidal-like waveform, each H-bridge output waveform must be quarter-symmetric as illustrated by V1 waveform in Fig. 3.11. Obviously, no even harmonic components are available in such a waveform. To minimize THD, all switching angles will be numerically calculated, which will be proposed.

### 3.4.2 Three-Phase Structure

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration. Fig 3.12 illustrates the schematic diagram of wye-connected seven-level inverter using three H-bridge cells and three SDCSs per phase, which will be used to verify the concept of the optimized harmonic stepped-waveform technique.

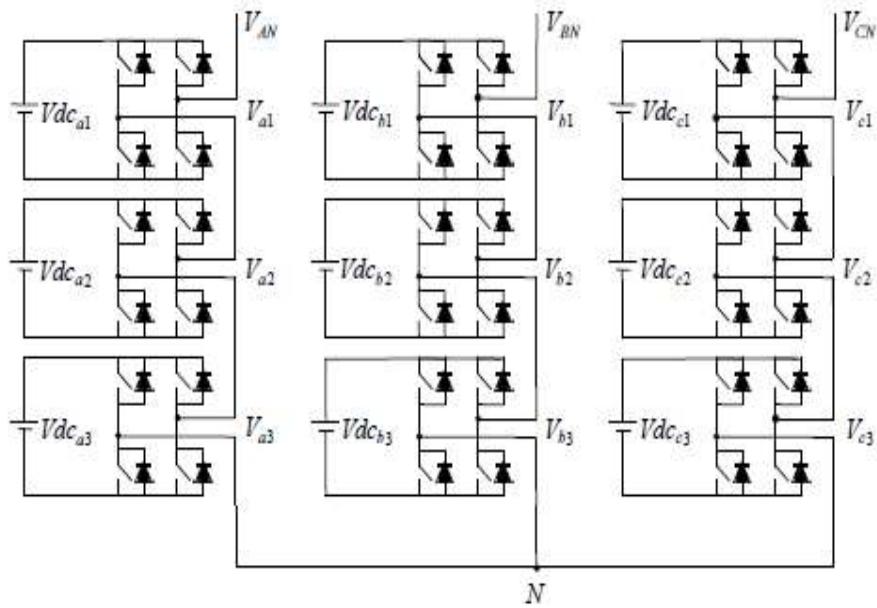


Fig: 3.12 Three-phase seven-level inverter using cascaded-inverters with SDCSs.

From Fig 3.4.2 (a),  $V_{AN}$  is voltage of phase A, which is the sum of  $V_{a1}$ ,  $V_{a2}$ , and  $V_{a3}$ . The same idea is applied to phase B and phase C. To synthesize seven-level phase voltage, three firing angles are required. The same three switching angles can be used in all three phase with delaying 0, 120, and 240 electrical degree for phase A, B, and C, respectively.

According to three-phase theory, line voltage can be expressed in term of two phase voltages. For example, the potential between phase A and B is so-called  $V_{AB}$ , which can be written as follows:

$$V_{AB} = V_{AN} - V_{BN} \quad \dots\dots(3.3)$$

Where

$V_{AB}$  is line voltage

$V_{AN}$  is voltage of phase A with respect to point N

$V_{BN}$  is voltage of phase B with respect to point N

Theoretically, the maximum number of line voltage levels is  $2m-1$ , where  $m$  is the number of phase voltage levels. The number of line voltage level depends on the modulation index and the given harmonics to be eliminated. The seven-level cascaded inverter, for example, can synthesize up to thirteen-level line voltage.

The advantage of three-phase system is that all triplen harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. Therefore,

only non-triplet harmonic components need to be eliminated from phase voltage. In single phase nine-level waveform, for example, the 3<sup>rd</sup>, 5<sup>th</sup>, and 7<sup>th</sup> harmonics will be eliminated from output phase voltage. Compared to single-phase inverter, in three-phase nine-level inverter, the 5<sup>th</sup>, 7<sup>th</sup>, and 11<sup>th</sup> harmonics will be eliminated from output phase voltage. Thus, the 9<sup>th</sup> harmonic is the lowest harmonic component in phase voltage in single phase system, while the 13<sup>th</sup> harmonic is the lowest harmonic component appearing in line voltage of three-phase system.

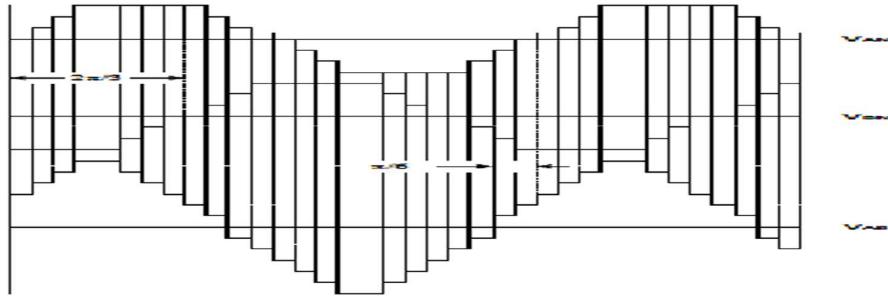


Figure 3.13 Two phase and line voltages of three-phase seven-level cascaded inverter

Fig 3.13 shows output voltage of phase A,  $V_{AN}$ , and output voltage of phase B,  $V_{BN}$ , line voltage waveform,  $V_{AB}$  of seven-level cascaded inverter in Fig 3.13. From Fig. 3.13, assuming the positive sequence three-phase system, output voltage of phase B lags output voltage of phase A by 120 electrical degree. The line voltage,  $V_{AB}$ , therefore, leads voltage of phase A by 30 electrical degree, which is according to the three-phase theory.

### 3.4.3 Separated DC Sources (SDCSs)

To avoid short circuit of dc sources, the separated dc source configuration is applied to the multilevel inverter using cascaded-inverter. This section will discuss about why cascaded inverter have to employ the separated dc sources (SDCSs). To explain this, two possible dc sources connections are assumed. In the first case, all H-bridge cells in the same leg share the same dc source. Another connection is that the same dc source is shared in the same level of each phase. Fig. 3.13 illustrate the first connection and the second connection of five-level cascaded inverter, respectively.

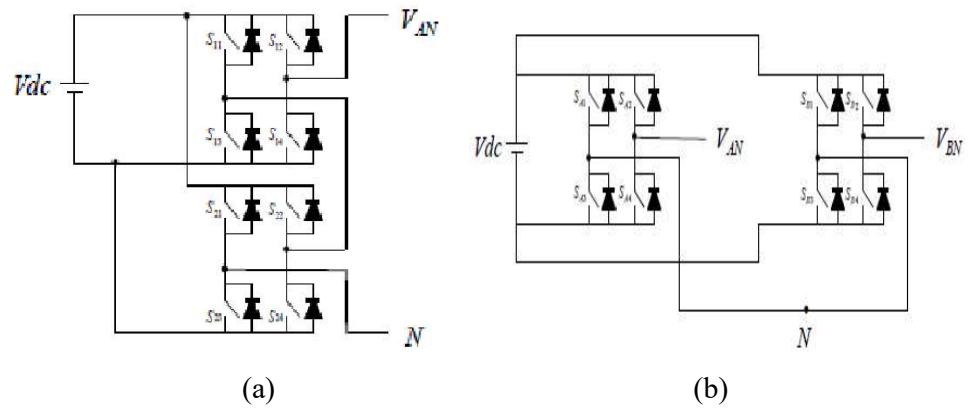


Figure 3.14 Shows two possible dc source connections

To avoid confusing, both cases will be assumed that no self shoot-through described in 1.2 is possible. However, there are many combinations, which make short circuit happen. Therefore, one possibility of each case will be presented. In the first case, short circuit across the dc source exists when switches  $S_{11}$  and  $S_{24}$  are turned on simultaneously, which is illustrated in Fig. 3.14. Likewise, in the second connection, when switch  $S_{A1}$  and  $S_{B3}$  are on at the same time, which is shown in Fig. 3.14 short circuit will be happened.

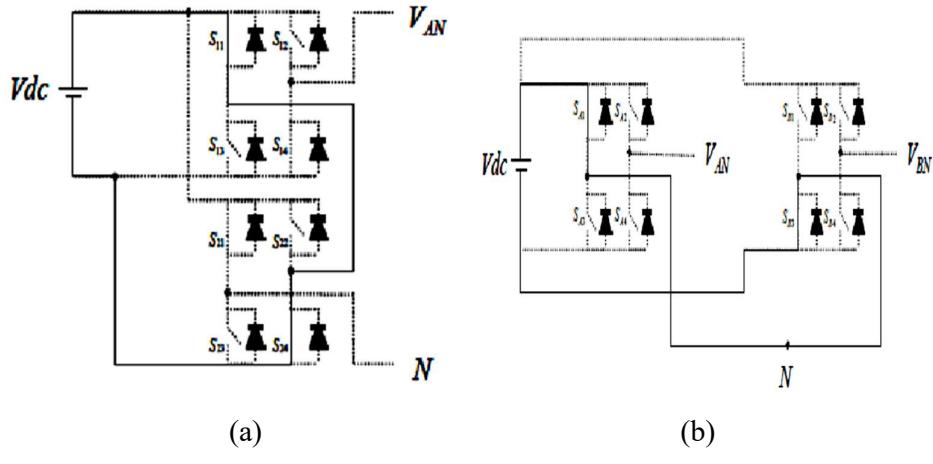


Figure 3.15 Shows a short circuit possibility of each case.

## CHAPTER-4

# MODULAR MULTILEVEL CONVERTER

MMC has gained increasing attention recently. A number of projects were published on the structure, control, and application of this topology, but none has suggested the use of that for inverter + D-STATCOM application. This topology consists of several half-bridge (HB) submodules (SMs) per each phase, which are connected in series. An  $n$ -level single phase MMC consists of a series connection of  $2(n - 1)$  basic SMs and two buffer inductors. Each SM possesses two semiconductor switches, which operate in complementary mode, and one capacitor. The exclusive structure of MMC becomes it an ideal candidate for medium-to-high-voltage applications such as wind energy applications. Moreover, this topology needs only one dc source, which is a key point for wind applications. MMC requires large capacitors which may increase the cost of the systems; however, this problem is offset by the lack of need for any snubber circuit.

The main benefits of the MMC topology are: modular design based on identical converter cells, simple voltage scaling by a series connection of cells, simple realization of redundancy, and possibility of a common dc bus. Fig. 4 shows the circuit configuration of a single-phase MMC and the structure of its SMs consisting of two power switches and a floating capacitor. The output voltage of each SM ( $v_o$ ) is either equal to its capacitor voltage ( $v_c$ ) or zero, depending on the switching states. The buffer inductors must provide current control in each phase arm and limit the fault currents. To describe the operation of MMC, each SM can be considered as a two-pole switch. If  $S_{ui}$ , which is defined as the status of the  $i$ th sub-module in the upper arm, is equal to unity, then the output of the  $i$ th SM is equal to the corresponding capacitor voltage; otherwise it is zero. Likewise, if  $S_{li}$  which is defined as the status of the  $i$ th sub-module in the lower arm, is equal to unity, then the output of the  $i$ th lower SM is equal to the corresponding capacitor voltage; otherwise it is zero.

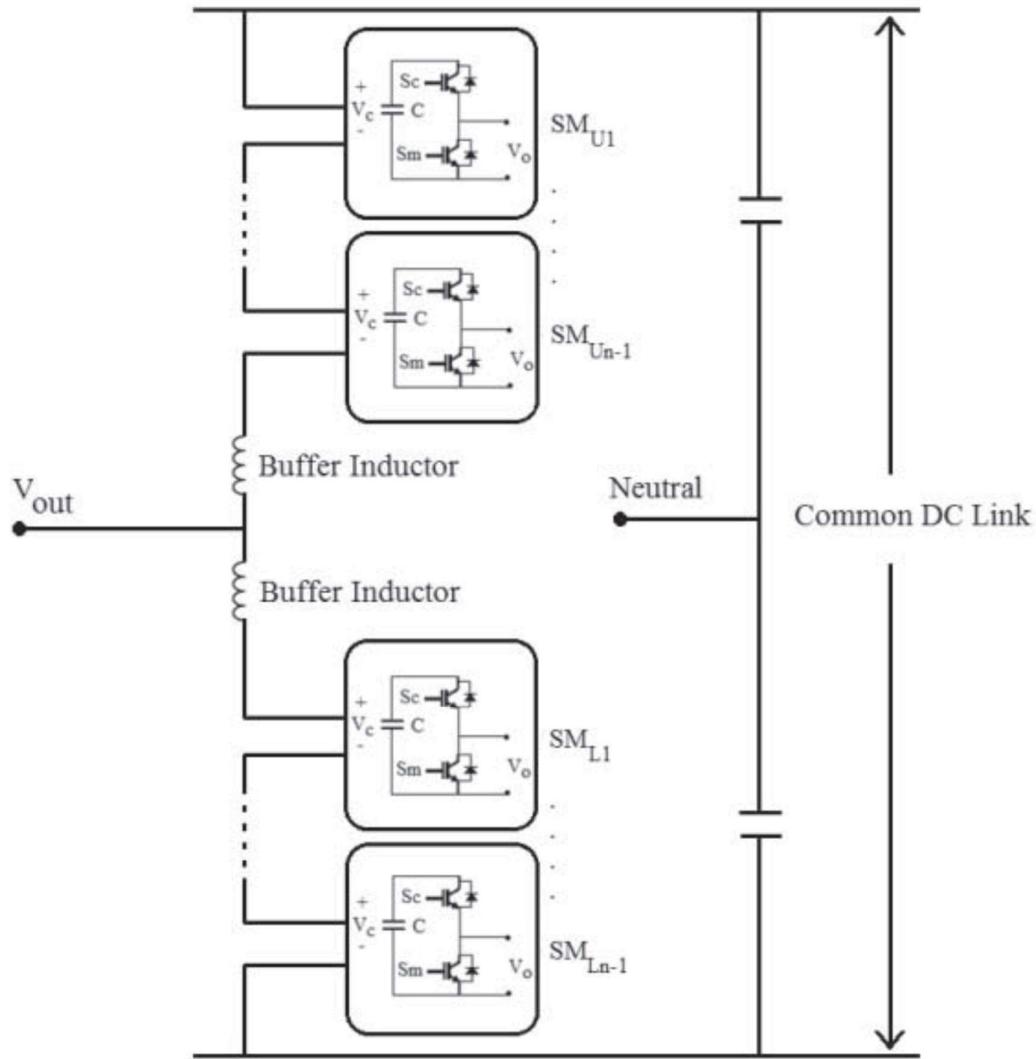


Fig. 4.1 Structure of a single-phase MMC inverter structure

Generally, when  $S_{ui}$  or  $S_{li}$  is equal to unity, the  $i$ th upper or lower SM is ON; otherwise, it is OFF. Therefore, the upper and lower arm voltages of the MMC are as follows:

$$v_{\text{upperArm}} = \sum_{i=1}^{n-1} (S_{ui} v_{ci}) + v_{11} \quad (1)$$

$$v_{\text{lowerArm}} = \sum_{i=1}^{n-1} (S_{li} v_{ci}) + v_{12} \quad (2)$$

Where  $v_{11}$  and  $v_{12}$  are the voltages of the upper and lower buffer inductors,  $n$  is the number of voltage levels, and  $v_{ci}$  is the voltage of the  $i$ th SMs capacitor in upper arm or lower arm. A single-phase 11-levelMMC inverter consists of 20 SMs which

translates to 40 power switches, 20 capacitors, and 2 buffer inductors. The dc and ac voltages of the 11-level MMC are described by

$$v_{DC} = v_{upperArm} + v_{lowerArm} \\ = \sum_{i=1}^{10} (S_{ui} v_{ci}) + \sum_{i=1}^{10} (S_{ui} v_{ci}) + (v_{11} + v_{12}) \quad (3)$$

$$v_{out} = \frac{v_{DC}}{2} - v_{upperArm} = -\frac{v_{DC}}{2} + v_{lowerArm}. \quad (4)$$

## 4.1 Control Strategy

The proposed controller consists of three major functions. The first function is to control the active and reactive power transferred to the power lines, the second function is to keep the voltages of the SMs' capacitors balanced, and the third function is to generate desired PWM signals. Fig. 4.1 (a) shows the complete proposed controller system.

The aim of the designed inverter is to transfer active power coming from the wind turbine as well as to provide utilities with distributive control of volt-ampere reactive (VAR) compensation and PF correction of feeder lines. The application of the proposed inverter requires active and reactive power to be controlled fully independent, so that if wind is blowing, the device should be working as a normal inverter plus being able to fix the PF of the local grid at a target PF (D-STATCOM option), and if there is no wind, the device should be only operating as a D-STATCOM (or capacitor bank) to regulate PF of the local grid. This translates to two modes of operation: 1) when wind is blowing and active power is coming from the wind turbine: the inverter plus D-STATCOM mode. In this mode, the device is working as a regular inverter to transfer active power from the renewable energy source to the grid as well as working as a normal D-STATCOM to regulate the reactive power of the grid in order to control the PF of the grid and 2) when wind speed is zero or too low to generate active power: the D-STATCOM mode. In this case, the inverter is acting only as a source of reactive power to control the PF of the grid, as a D-STATCOM. This option eliminates the use of additional capacitor banks or external STATCOMs to regulate the PF of the distribution feeder lines. Obviously, the device is capable of outputting up to its rated maximum real power and/or reactive power, and will always output all real power

generated by the wind turbine to the grid. The amount of reactive power, up to the design maximum, is dependent only on what the utility asks the device to produce.

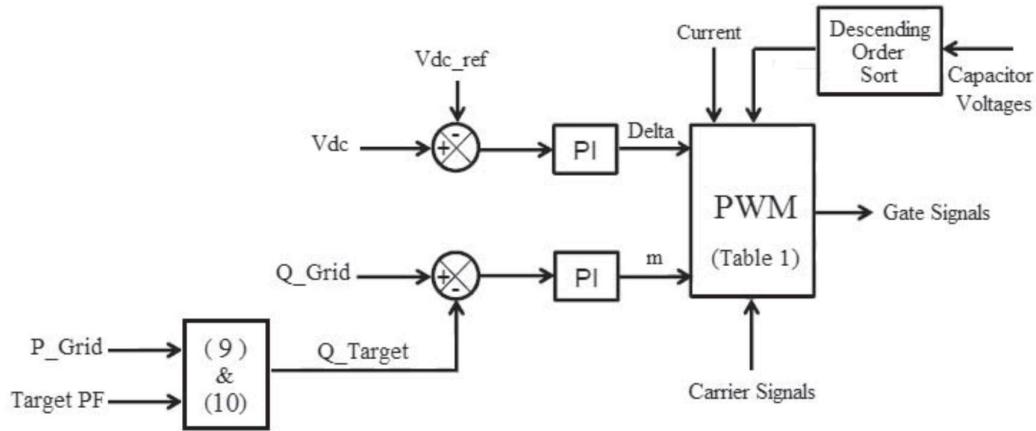


Fig. 4.2 Schematic of the proposed controller system

Generally, (5) and (6) dictate the power flow between a STATCOM device and power lines

$$P_S = -\frac{E_S E_L}{X} \sin \delta \quad (5)$$

$$Q_S = -\frac{E_S E_L \cos \delta - E_L^2}{X} \quad (6)$$

Where  $X$  is the inductance between the STATCOM (here as inverter) and the grid which is normally considered as output filter inductance added to the transmission line inductance. The root mean square (RMS) voltage of the STATCOM (= inverter) is given as  $E_S$  and is considered to be out of phase by an angle of  $\delta$  to the RMS line voltage  $E_1$ .

In the proposed control strategy, active and reactive power transferred between the inverter and the distribution grid is controlled by selecting both the voltage level of the inverter and the angle  $\delta$  between the voltages of inverter and grid, respectively. The amplitude of the inverter voltage is regulated by changing the modulation index  $m$  and the angle  $\delta$  by adding a delay to the firing signals which concludes

$$P_S = -\frac{m E_S E_L}{X} \sin \delta \quad (7)$$

$$Q_S = -\frac{m E_S E_L \cos \delta - E_L^2}{X}. \quad (8)$$

In this project,  $m$  is the key factor to control the reactive power compensation and its main task is to make the PF of the grid equal to the target PF.  $\delta$  is the control parameter to adjust the active power control between the inverter and the grid.

Several assumptions should be considered for the proposed controller which is as: 1) the load on the feeder line should be considered fixed for a small window of time and there is no change in the load during a cycle of the grid frequency; 2) the feeder line can be accurately modeled as a constant  $P, Q$  load. This means that the power produced by a wind turbine will displace other power on the feeder line and not add to it; and 3) although making a change in  $m$  or  $\delta$  has effect on both (7) and (8), it is assumed that a change in the modulation index will predominantly affect  $Q$ , while a change in delta will predominantly affect  $P$ . Any effect on  $Q$  from a small change in delta is thus ignored. This results in controlling  $P$  and  $Q$  independently. Equation (9) shows the relation between the target reactive power and the target PF

$$P_G = \left( \sqrt{P_G^2 + Q_T^2} \right) \times \text{PF}_T \quad (9)$$

Where  $P_G$  is the amount of active power on the grid,  $Q_T$  is the target amount of reactive power, and  $\text{PFT}$  is the target PF desired by the utility. So,  $Q_T$  can be calculated as

$$Q_T = \sqrt{\left( \frac{P_G}{\text{PF}_T} \right)^2 - P_G^2}. \quad (10)$$

Using (9) and (10), the target reactive power for the grid is determined and is compared with the actual value of the reactive power of the grid. Using a PI compensator will determine the desired value for the modulation index. The power angle is also determined by comparing the actual dc voltage of the inverter with a reference value. A PI compensator determines the desired value for the power angle.

The second function of the controller systems is to keep the capacitors' voltages balanced. In order to do this, a carrier based pulse width modulation (CPWM) method is used. The top graph in Fig:4.1(b) shows the reference signal and the carrier waveforms for an 11-level MMC inverter using CPWM technique. The bottom graph of Fig: 4.1(b) shows the output voltage levels generated based on Table I.

In an 11-level CPWM technique, ten carrier signals are compared with a reference sinusoidal signal. In Fig 4.1(b), based on the phase of the reference signal ( $v_r$ ), there are 11 operating regions where each region defines a voltage level in the output

$$n_{\text{upperArm}} + n_{\text{lowerArm}} = 10 \quad (11)$$

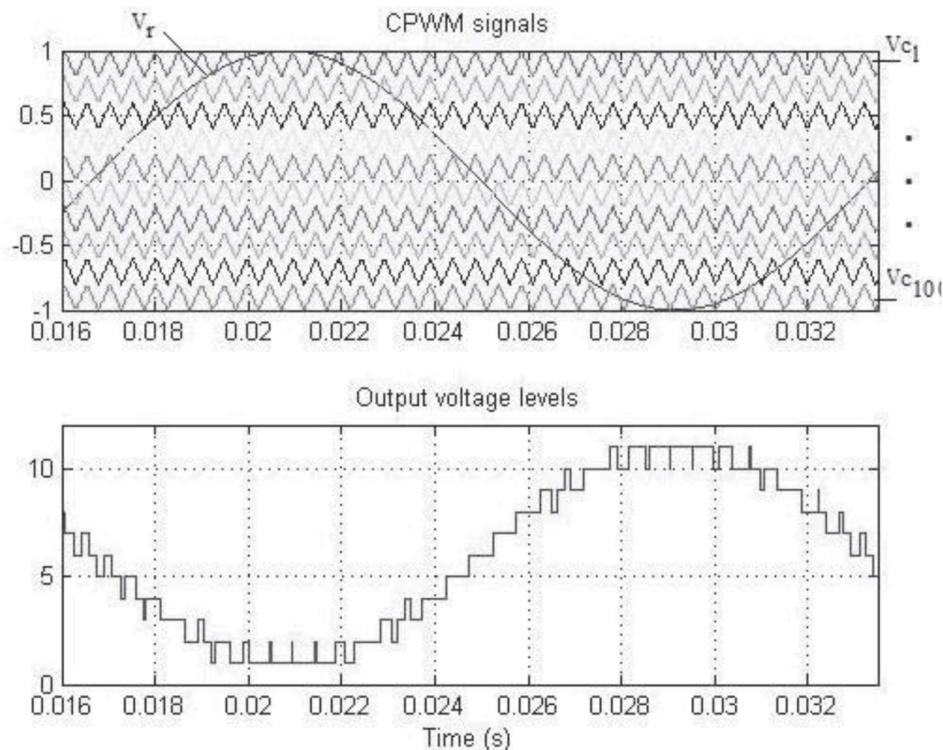


Fig. 4.3 CPWM waveforms for an 11-level MMC inverter, and the generated output voltage levels

Where  $n_{\text{upper Arm}}$  and  $n_{\text{lower Arm}}$  are the numbers of SMs which are ON ( $S_c$  is ON and  $S_m$  is OFF in Fig. 1) in the upper arm or lower arm, respectively.

In an 11-level MMC inverter, there are ten upper and ten lower SMs where each SM has a capacitor. For instance, in voltage level 1 of Table I, all the upper SMs should be OFF and all the lower SMs should be ON, which translates to the fact that the main switches  $S_m$  of all upper SMs and the auxiliary switches ( $S_c$ ) of all lower SMs have to be ON and all the other switches have to be OFF. In this case, the input dc voltage is applied only to the ten lower capacitors, so that the output voltage is  $v_{DC}/2$ . Fig:4.1 (c) illustrates the selection of capacitors for different voltage levels shown in Table I.

**TABLE I**  
**Operating Regions For An 11-Level Mmc Inverter**

Voltage level	Status	n <sub>UpperArm</sub>	n <sub>LowerArm</sub>	V <sub>out</sub>
1	$v_r \geq v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	0	10	$5v_{dc}/10$
2	$v_r < v_{c1}$ $v_r \geq v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	1	9	$4v_{dc}/10$
3	$v_r < v_{c1}, v_{c2}$ $v_r \geq v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	2	8	$3v_{dc}/10$
4	$v_r < v_{c1}, v_{c2}, v_{c3}$ $v_r \geq v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	3	7	$2v_{dc}/10$
5	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}$ $v_r \geq v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	4	6	$v_{dc}/10$
6	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}$ $v_r \geq v_{c7}, v_{c8}, v_{c9}, v_{c10}$	5	5	0
7	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}$ $v_r \geq v_{c7}, v_{c8}, v_{c9}, v_{c10}$	6	4	$-v_{dc}/10$
8	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}$ $v_r \geq v_{c8}, v_{c9}, v_{c10}$	7	3	$-2v_{dc}/10$
9	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}$ $v_r \geq v_{c9}, v_{c10}$	8	2	$-3v_{dc}/10$
10	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}$ $v_r \geq v_{c10}$	9	1	$-4v_{dc}/10$
11	$v_r < v_{c1}, v_{c2}, v_{c3}, v_{c4}, v_{c5}, v_{c6}, v_{c7}, v_{c8}, v_{c9}, v_{c10}$	10	0	$-5v_{dc}/10$

The most critical issue to control MMC is to maintain the voltage balance across all the capacitors. Therefore, the SMs' voltages are measured and sorted in descending order during each cycle. If the current flowing through the switches is positive, so that capacitors are being charged, nupper Arm and nupper Arm and of the SMs in upper

arm and lower arm with the lowest voltages are selected, respectively. As a result, ten capacitors with lowest voltages are chosen to be charged.

Likewise, if the current flowing through the switches is negative, so that capacitors are being discharged, *n*upper Arm and *n*upper Arm of the SMs in upper arm and lower arm with highest voltages are selected, respectively. As a result, ten capacitors with highest voltages are chosen to be discharged. Consequently, the voltages of the SMs' capacitors are balanced. Considering Table I and based on the direction of the current flowing through the switches, the proper algorithm will be selected to maintain capacitor balance.

The third function of the controller system is the PWM generation block. In this block, based on the desired modulation index, power angle, voltages of the capacitors, direction of the current flowing through the switches and using Table I, the controller generates the PWM signals in order to meet all the system requirements.

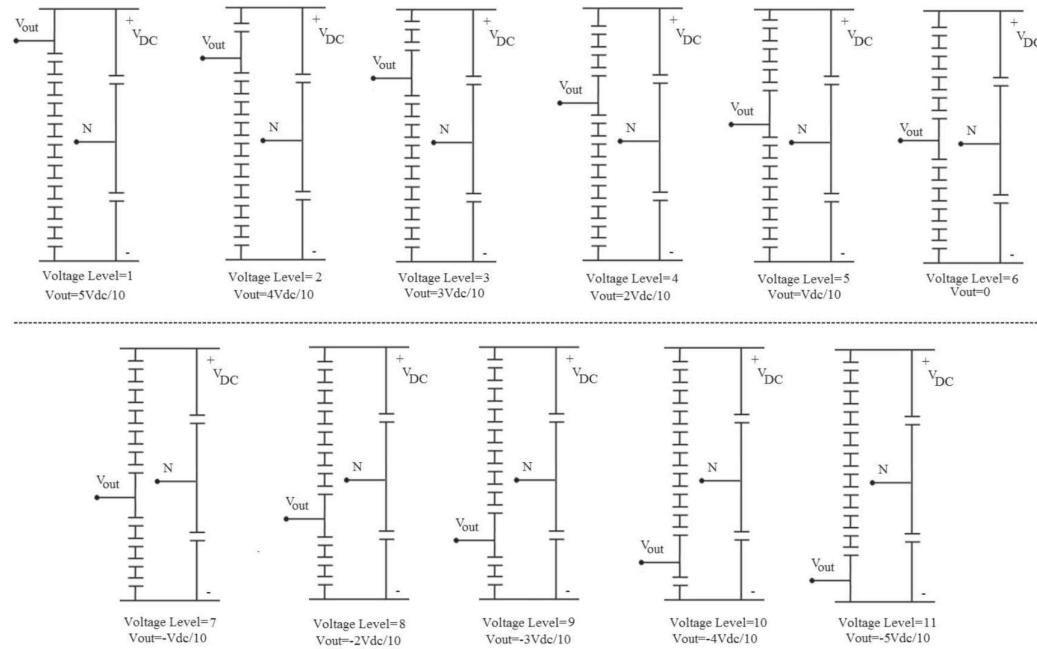


Fig. 4.4 Selection of SMs' capacitors for different voltage levels

# CHAPTER-5

## MATLAB & SIMULINK

### 5.1 MATLAB

#### 5.1.1 Introduction

MATLAB is a high-level technical computing language and interactive environment for algorithm development, data visualization, data analysis, and numeric computation. Using the MATLAB product, you can solve technical computing problems faster than with traditional programming languages, such as C, C++, and FORTRAN.

MATLAB is used in wide range of applications, including signal and image processing, communications, control design, test and measurement, financial modeling and analysis, and computational biology. Add-on toolboxes (collections of special-purpose MATLAB functions, available separately) extend the MATLAB environment to solve particular classes of problems in these application areas.

MATLAB provides a number of features for documenting and sharing your work. You can integrate your MATLAB code with other languages and applications, and distribute your MATLAB algorithms and applications.

#### 5.1.2 Key Features

- High-level language for technical computing
- Development environment for managing code, files, and data
- Interactive tools for iterative exploration, design, and problem solving
- Mathematical functions for linear algebra, statistics, Fourier analysis, filtering, optimization, and numerical integration
- 2-D and 3-D graphics functions for visualizing data
- Tools for building custom graphical user interfaces
- Functions for integrating MATLAB based algorithms with external applications and languages, such as C, C++, Fortran, Java, COM, and Microsoft Excel

## 5.2 SIMULINK

### 5.2.1 Introduction

Simulink® is an environment for multi-domain simulation and Model-Based Design for dynamic and embedded systems. It provides an interactive graphical environment and a customizable set of block libraries that let you design, simulate, implement, and test a variety of time-varying systems, including communications, controls, signal processing, video processing, and image processing.

Add-on products extend Simulink software to multiple modeling domains, as well as provide tools for design, implementation, and verification and validation tasks.

Simulink is integrated with MATLAB®, providing immediate access to an extensive range of tools that let you develop algorithms, analyze and visualize simulations, create batch processing scripts, customize the modeling environment, and define signal, parameter, and test data.

### 5.2.2 Key Features

- Extensive and expandable libraries of predefined blocks
- Interactive graphical editor for assembling and managing intuitive block diagrams
- Ability to manage complex designs by segmenting models into hierarchies of design components
- Model Explorer to navigate, create, configure, and search all signals, parameters, properties, and generated code associated with your model
- Application programming interfaces (APIs) that let you connect with other simulation programs and incorporate hand-written code
- Embedded MATLAB™ Function blocks for bringing MATLAB algorithms into Simulink and embedded system implementations
- Simulation modes (Normal, Accelerator, and Rapid Accelerator) for running simulations interpretively or at compiled C-code speeds using fixed- or variable-step solvers
- Graphical debugger and profiler to examine simulation results and then diagnose performance and unexpected behavior in your design
- Full access to MATLAB for analyzing and visualizing results, customizing the modeling environment, and defining signal, parameter, and test data

- Model analysis and diagnostics tools to ensure model consistency and identify modeling errors.

### 5.2.3 Block Diagram

A Simulink block diagram is a pictorial model of a dynamic system. It consists of a set of symbols, called blocks, interconnected by lines. Each block represents an elementary dynamic system that produces an output either continuously (a continuous block) or at specific points in time (a discrete block). The lines represent connections of block inputs to block outputs. Every block in a block diagram is an instance of a specific type of block. The type of the block determines the relationship between a block's outputs and its inputs, states, and time. A block diagram can contain any number of instances of any type of block needed to model a system. Blocks represent elementary dynamic systems that Simulink knows how to simulate. A block comprises one or more of the following:

- A set of inputs,
- A set of states, and
- A set of outputs

A block's output is a function of time and the block's inputs and states (if any). The specific function that relates a block's output to its inputs, states, and time depends on the type of block of which the block is an instance. Continuous Versus discrete Blocks Simulink's standard block set includes continuous blocks and discrete blocks. Continuous blocks respond continuously to continuously changing input. Discrete blocks, by contrast, respond to changes in input only at integral multiples of a fixed interval called the block's sample time. Discrete blocks hold their output constant between successive sample time hits. Each discrete block includes a sample time parameter that allows you to specify its sample rate. The Simulink blocks can be either continuous or discrete, depending on whether they are driven by continuous or discrete blocks. A block that can be either discrete or continuous is said to have an implicit sample rate. The implicit sample time is continuous if any of the block's inputs are continuous. The implicit sample time is equal to the shortest input sample time if all the input sample times are integral multiples of the shortest time. Otherwise, the input sample time is equal to the fundamental sample time of the inputs, where the fundamental sample time of a set of sample times is defined as the greatest integer divisor of the set of sample times.

Simulink can optionally color code a block diagram to indicate the sample times of the blocks it contains, e.g., black (continuous), magenta (constant), yellow (hybrid), red (fastest discrete), and so on. The block contains block name, icon, and block library that contain the block, the purpose of the block.

#### 5.2.4 Simulink Block Libraries

Simulink organizes its blocks into block libraries according to their behavior:

- The Sources library contains blocks that generate signals.
- The Sinks library contains blocks that display or write block output.
- The Discrete library contains blocks that describe discrete-time components.
- The Continuous library contains blocks that describe linear functions.
- The Math library contains blocks that describe general mathematics functions.
- The Functions & Tables library contains blocks that describe general functions and table look-up operations.
- The Nonlinear library contains blocks that describe nonlinear functions.
- The Signal & Systems library contains blocks that allow multiplexing and de-multiplexing, implement external input/output, pass data to other parts of the model, and perform other functions.
- The Subsystems library contains blocks for creating various types of subsystems.
- The Block sets and Toolboxes library contains the Extras block library of specialized blocks.

#### 5.2.5 Sub Systems

Simulink allows to model a complex system as a set of interconnected subsystems each of which is represented by a block diagram. We create a subsystem using Simulink's Subsystem block and the Simulink model editor. We can embed subsystems with subsystems to any depth to create hierarchical models. We can create conditionally executed subsystems that are executed only when a transition occurs on a triggering or enabling input.

### **5.2.6 Solvers**

Simulink simulates a dynamic system by computing its states at successive time step solver a specified time span, using information provided by the model. The process of computing the successive states of a system from its model is known as solving the model. No single method of solving a model suffices for all systems. Accordingly, Simulink provides a set of programs, known as solvers, that each embody a particular approach to solving a model. The Simulation Parameters dialog box allows us to choose the solver most suitable for our model.

#### **5.2.6.1 Fixed-Step Solvers**

Fixed-step solvers solve the model at regular time intervals from the beginning to the end of the simulation. The size of the interval is known as the step-size. We can specify the step size or let the solver choose the step size. Generally decreasing the step size increases the accuracy of the results while increasing the time required to simulate the system.

#### **5.2.6.2 Variable-Step Solvers**

Variable-step solvers vary the step size during the simulation, reducing the step size to increase accuracy when a model's states are changing rapidly and increasing the step size to avoid taking unnecessary steps when the model's states are changing slowly. Computing the step size adds to the computational overhead at each step but can reduce the total number of steps, and hence simulation time, required to maintain a specified level of accuracy for models with rapidly changing or piecewise continuous states.

#### **5.2.6.3 Continuous Solvers**

Continuous solvers use numerical integration to compute a model's continuous states at the current time step from the states at previous time steps and the state derivatives. Continuous solvers rely on the model's blocks to compute the values of the model's discrete states at each time step. Mathematicians have developed a wide variety of numerical integration techniques for solving the ordinary differential equations (ODEs) that represent the continuous states of dynamic systems. Simulink provides an extensive set of fixed-step and variable-step continuous solvers, each implementing a specific ODE solution method. Some continuous solvers subdivide the simulation time span into major and minor steps, where a minor time step represents a subdivision of

the major time step. The solver produces a result at each major time step. It uses results at the minor time steps to improve the accuracy of the result at the major time step.

#### 5.2.6.4 Discrete Solvers

Discrete solvers exist primarily to solve purely discrete models. They compute the next simulation time-step for a model and nothing else. They do not compute continuous states and they rely on the model's blocks to update the model's discrete states. We can use a continuous solver, but not a discrete solver, to solve a model that contains both continuous and discrete states. This is because a discrete solver does not handle continuous states. If you select a discrete solver for a continuous model, Simulink disregards your selection and uses a continuous solver instead when solving the model.

Simulink provides two discrete solvers, a fixed-step discrete solver and a variable-step discrete solver. The fixed-step solver by default chooses a step size and hence simulation rate fast enough to track state changes in the fastest block in our model. The variable-step solver adjusts the simulation step size to keep pace with the actual rate of discrete state changes in our model. This can avoid unnecessary steps and hence shorten simulation time for multirate models.

### 5.3 The Power System Block Set

Electrical power systems are combinations of electrical circuits and Electro-mechanical devices, like motors and generators. Engineers working in this discipline are frequently tasked to improve the performance of the systems. Requirements for drastically increased efficiency have forced power system designers to use power electronic devices and sophisticated control system concepts that tax traditional analysis tools and techniques. Further complicating the analyst's role is the fact that the system is often so nonlinear that the only way to understand it is through simulation. Land-based power generation from hydroelectric, steam, or other devices is not the only use of power systems. A common attribute of these systems is their use of power electronics and control systems to achieve their performance objectives. The Power System Block set was designed to provide a modern design tool that will allow scientists and engineers to rapidly and easily build models that simulate power systems. The block set uses the Simulink® environment allowing a model to be built using

simple click and drag procedures. Not only can the circuit topology be drawn rapidly, but the analysis of the circuit can include its interactions with mechanical, thermal, control, and other disciplines. This is possible because all the electrical parts of the simulation interact with Simulink's extensive modeling library. Because Simulink uses MATLAB® as the computational engine, you can use MATLAB's toolboxes as you design your simulation.

The block set can be put to work rapidly. The libraries contain models of typical power equipment, such as transformers, lines, machines, and power electronics. These models are proven ones coming from textbooks, and their validity is based on the experience of the Power Systems Testing and Simulation Laboratory of Hydro-Québec, a large North American utility located in Canada. The capabilities of the block set for modeling a typical electrical grid are illustrated in demonstration files. The block set fits well with other specialized analytical tools you use in the power system community.

## 5.4 Simulink Blocks used in the Simulation:

### 1. Three-Phase Source:



**Purpose:** Implement three-phase source with internal R-L impedance

**Description:** The Three-Phase Source block implements a balanced three-phase voltage source with internal R-L impedance. The three voltage sources are connected in Y with a neutral connection that can be internally grounded or made accessible. You can specify the source internal resistance and inductance either directly by entering R and L values or indirectly by specifying the source inductive short-circuit level and X/R ratio.

### 2. In port:



**Purpose: Provide a link to an external input and for linearization.**

**Description:** In ports are the links from the outside world into a system. Inside a subsystem block, there is an in port corresponding to each input port on the block. A signal that arrives at an input port on a subsystem block flows out of the corresponding in port within that block. The imports within a subsystem block must be numbered consecutively, starting with 1.

### 3. Out port:

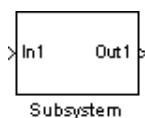


**Purpose:** provide a link to an external output and for linearization.

**Description:** The Out port block provides a mechanism for labeling a system's outputs.

In a subsystem, output ports correspond to outputs on the subsystem block.

### 4. Subsystem:



**Purpose:** Group blocks into a subsystem

**Description:** Subsystem blocks represent one system within another system. Any set of blocks and lines can be converted to a Subsystem block with the Group command on the options menu. The Group command removes all selected objects from the active window and replaces them within a Subsystem block. This new block, when opened, redisplays all of the grouped objectives.

### 5. Gain:



**Purpose:** Multiply its input by a constant.

**Description:** The Gain block implements  $Y=KU$ , where  $Y$  is the output,  $U$  is the input, and  $K$  is the specified gain. The Gain block displays scalar gain data entered as variable or a constant. The block displays the text as it appears in the dialog box.

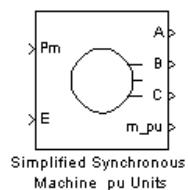
### 6. Scope:



**Purpose:** Display signals during simulation.

**Description:** While the simulation is running, the Scope block displays the output of the block driving it. Opening a scope block produces a scope window. The title of this window matches the name of the block.

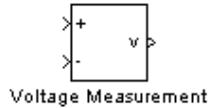
### 7. Simplified Synchronous Machine:



**Purpose:** Model the dynamics of a simplified three-phase synchronous machine

**Description:** The Simplified Synchronous Machine block models both the electrical and mechanical characteristics of a simple synchronous machine. The electrical system for each phase consists of a voltage source in series with RL impedance, which implements the internal impedance of the machine. The value of R can be zero but the value of L must be positive.

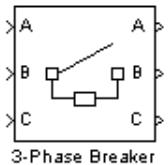
#### 8. Voltage Measurement:



**Purpose:** Measure a voltage in a circuit

**Description:** The Voltage Measurement block is used to measure the instantaneous voltage between two electric nodes. The output is a Simulink signal that can be used by other Simulink blocks.

#### 9. Breaker:



**Purpose:** Implement a circuit breaker opening at current zero crossing

**Description:** The Breaker block implements a circuit breaker that is controlled by a Simulink signal applied on its second input. The control signal must be 0 or 1, 0 for open and 1 for closed. The arc extinction process is simulated by opening the breaker when the current passes through zero (first current zero-crossing following the transition of the Simulink control input from 1 to 0). When the breaker is closed, it behaves as a series RL circuit. The R and L values can be set as small as necessary in order to be negligible compared with external components (typical values Ron=10mΩ, Lon=10μH). When the breaker is open, it has infinite impedance. If the breaker's initial state is set to 1 (closed), initializes all the states of the linear circuit and breaker initial current so that the simulation starts in steady-state.

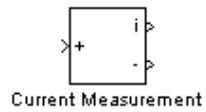
#### 10. Bus bar:



**Purpose:** Implement a labeled network node

**Description:** The Bus Bar block is used to interconnect components. It allows multiple electrical block outputs and inputs to be connected together.

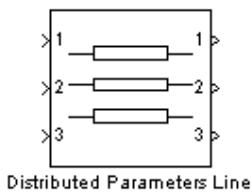
### 11. Current Measurement:



**Purpose:** Measure a current in a circuit

**Description:** The Current Measurement block is used to measure the instantaneous current flowing in any electrical block or connection line. The first output provides a Simulink signal that can be used by other Simulink blocks.

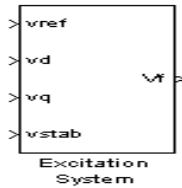
### 12. Distributed Parameter Line:



**Purpose:** Implement an N-phase distributed parameter transmission line model with lumped losses

**Description:** The Distributed Parameter Line block implements an N-phase distributed parameter line model with lumped losses.

### 13. Excitation System:

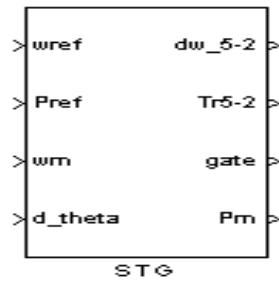


**Purpose:** Provide an excitation system for the synchronous machine and regulate its terminal voltage in generating mode

**Description:** The basic elements that form the Excitation System block are the voltage regulator and the exciter. The voltage regulator consists of a main regulator with gain  $K_a$  and time constant  $T_a$  and a lead-lag compensator with time constants  $T_b$  and  $T_c$ . A derivate feedback is also provided with gain  $K_f$  and time constant  $T_f$ . The limits  $E_{f\min}$  and  $E_{f\max}$  are imposed to the output of the voltage regulator. The upper limit can be constant and equal to  $E_{f\max}$  or variable and equal to the rectified stator terminal voltage  $V_{tf}$  times a proportional gain  $K_p$ . If  $K_p$  is set to zero, the former will apply. If  $K_p$  is set

to a positive value, the latter will apply. The stator terminal voltage transducer is represented by a first-order low-pass filter with time constant  $T_r$ .

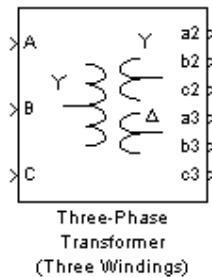
#### 14. Steam Turbine and Governor:



**Purpose:** Model a steam turbine and a PID governor system

**Description:** The Steam Turbine and Governor implement a steam turbine model, a PID governor system, and a servo-motor. The static gain of the governor is equal to the inverse of the permanent droop  $R_p$  in the feedback loop. The input to this feedback loop can be selected to be the gate position or the electrical power deviation by setting the droop reference parameter in the dialog box to one or zero, respectively.

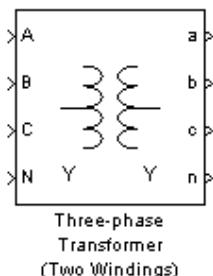
#### 15. Linear Transformer:



**Purpose:** Implement a two- or three-winding linear transformer

**Description:** The Linear Transformer block model shown below consists of three coupled windings wound on the same core.

#### 16. Saturable Transformer:



**Purpose:** Implement a two- or three-winding saturable transformer

**Description:** The Saturable Transformer block model shown below consists of three coupled windings wound on the same core.

# CHAPTER-6

## SIMULATION RESULTS

- The simulation model of a single phase MMC inverter is shown below

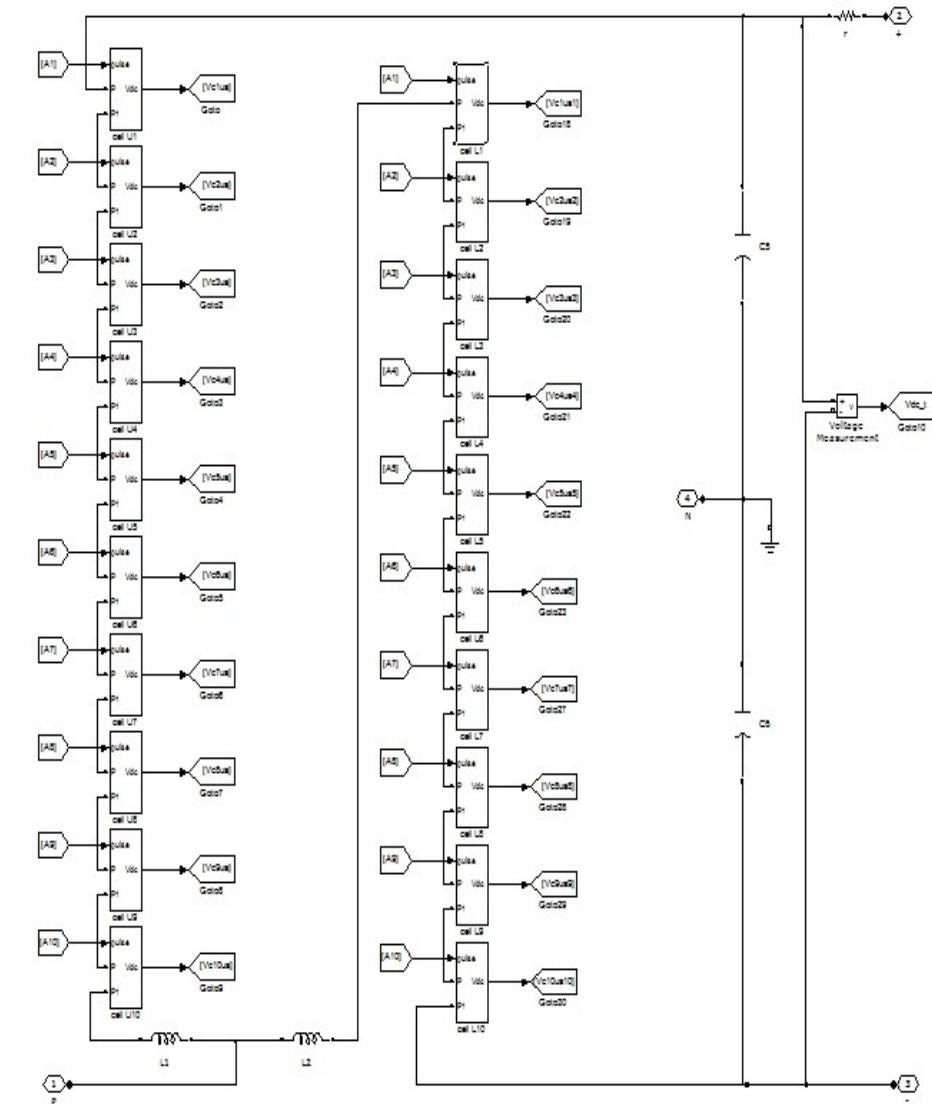


Fig: 6.1 Simulation of Structure of a single-phase MMC inverter structure

- The CPWM waveform for an 11 level MMC inverter is shown below

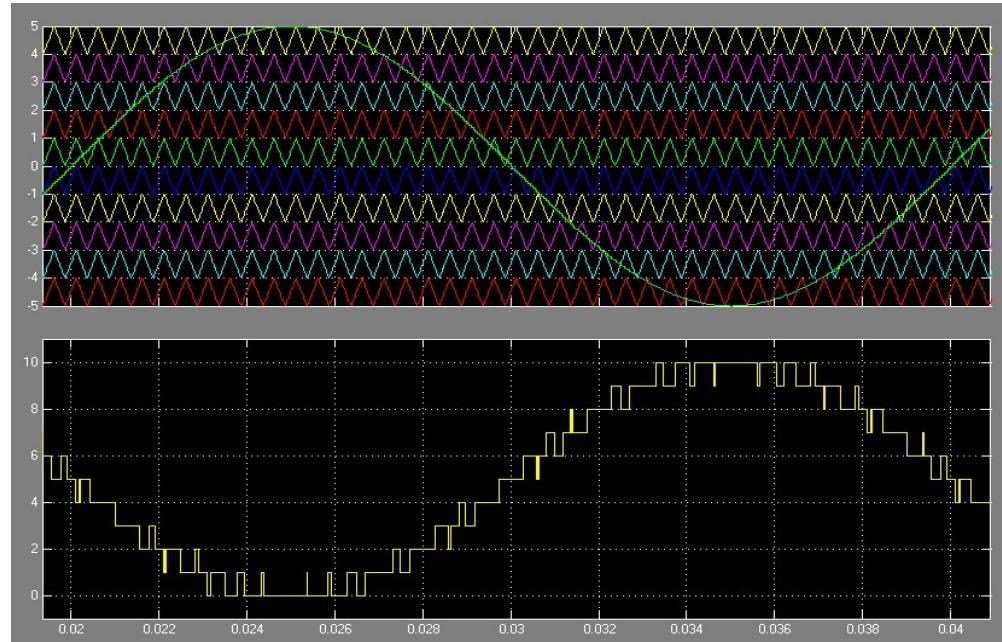


Fig: 6.2 CPWM waveforms for an 11-level MMC inverter

- The CPWM waveform for a 15-level MMC inverter is shown below

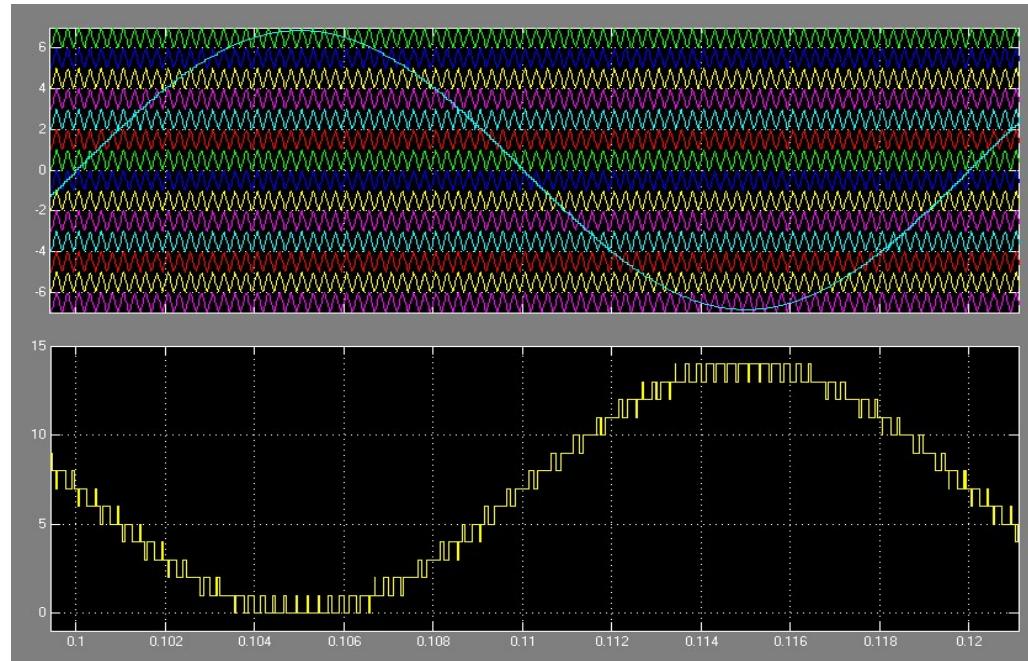


Fig:6.3 CPWM waveforms for a 15-level MMC inverter

- The simulated output voltage of a 5-level inverter is shown below

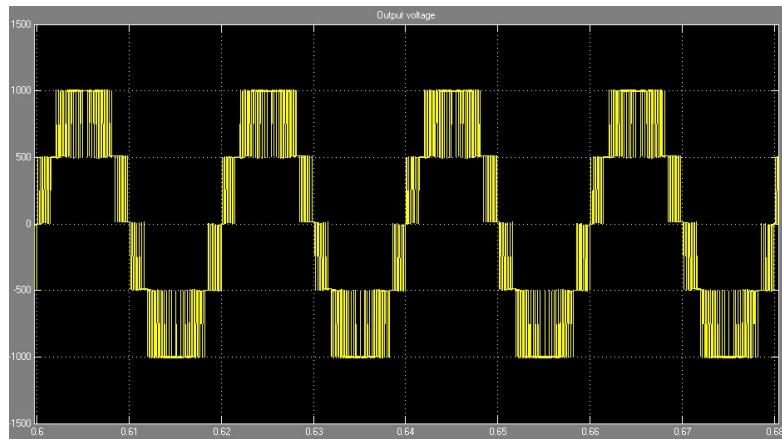


Fig:6.4 Simulated output voltage of a 5-level inverter

- The %THD of a 5-level inverter is shown below

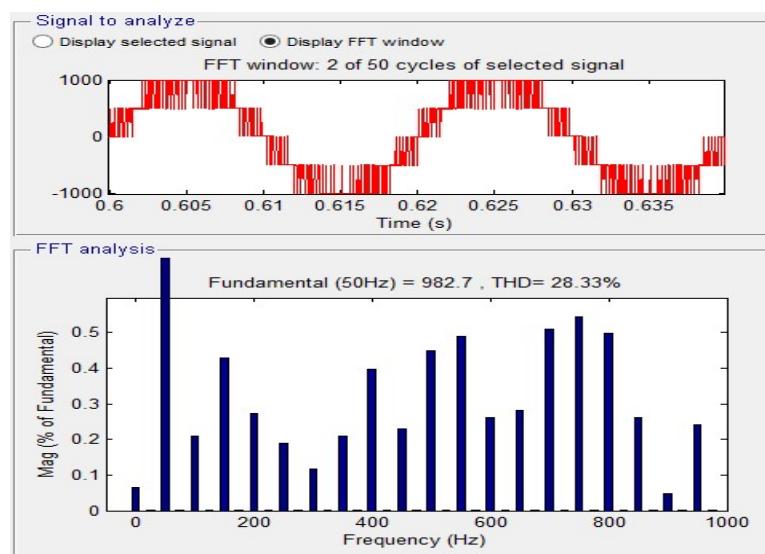


Fig:6.5 % THD of a 5-level inverter

- The simulated output voltage of a 7-level inverter is shown below

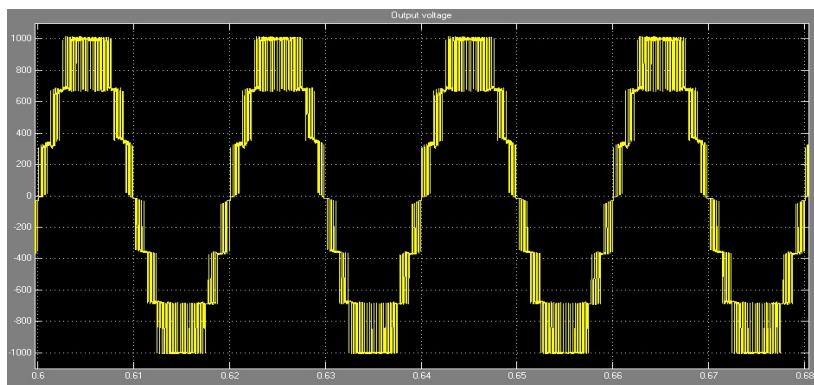


Fig:6.6 Simulated output voltage of a 7-level inverter

- The %THD of a 7-level inverter is shown below

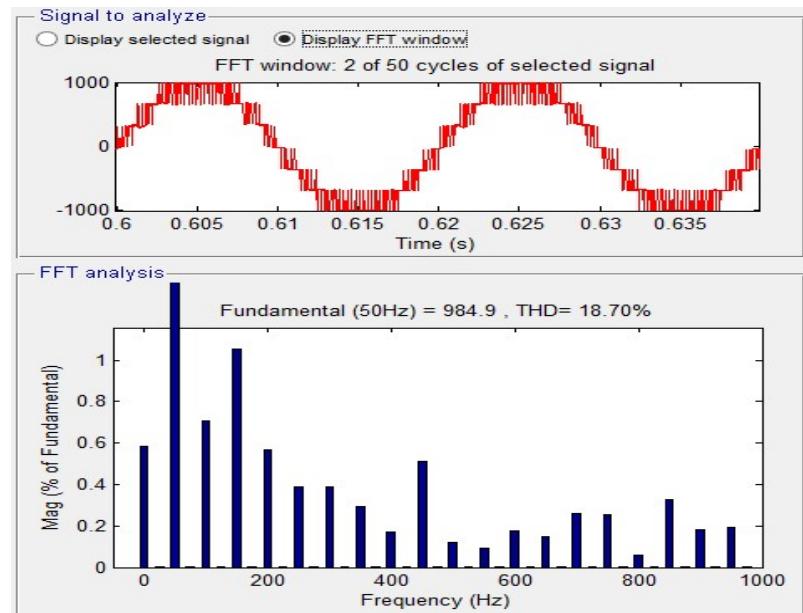


Fig: 6.7 % THD of a 7-level inverter

- The Simulated output voltage of a 9-level inverter is shown below

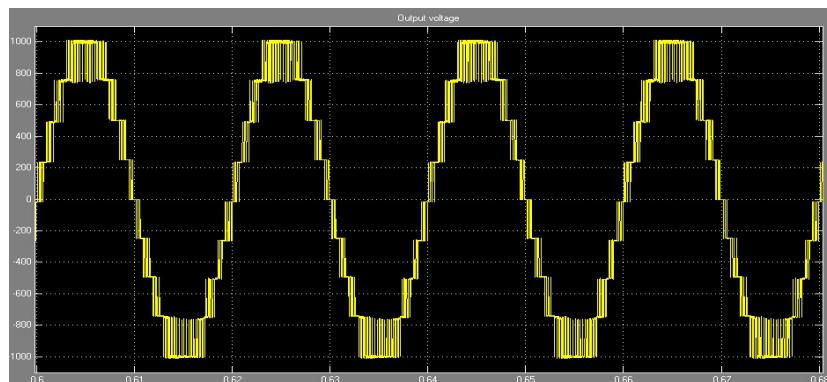


Fig: 6.8 Simulated output voltage of a 9-level inverter

- The %THD of a 9-level inverter is shown below

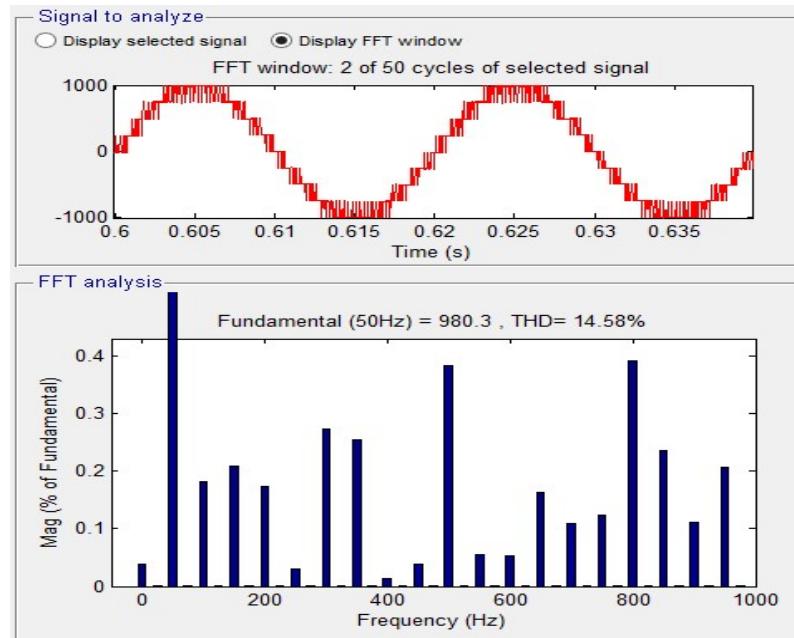


Fig:6.9 % THD of a 9-level inverter

- The simulated output voltage of a 11-level inverter is shown below

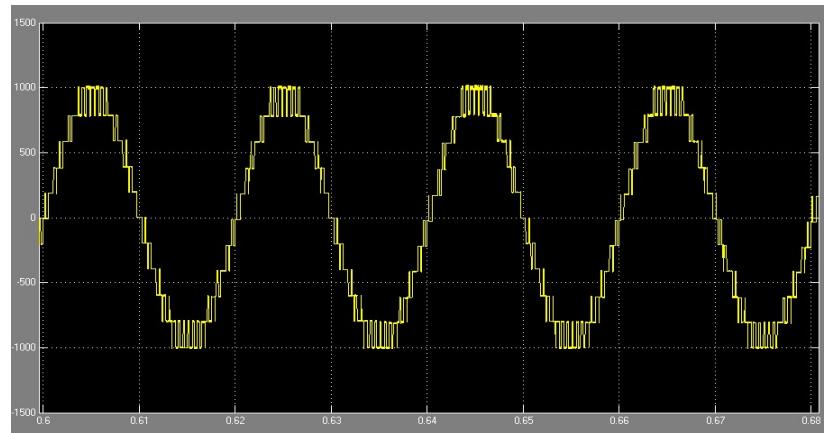


Fig:6.10 Simulated output voltage of a 11-level inverter

- The %THD of an 11-level inverter is shown below

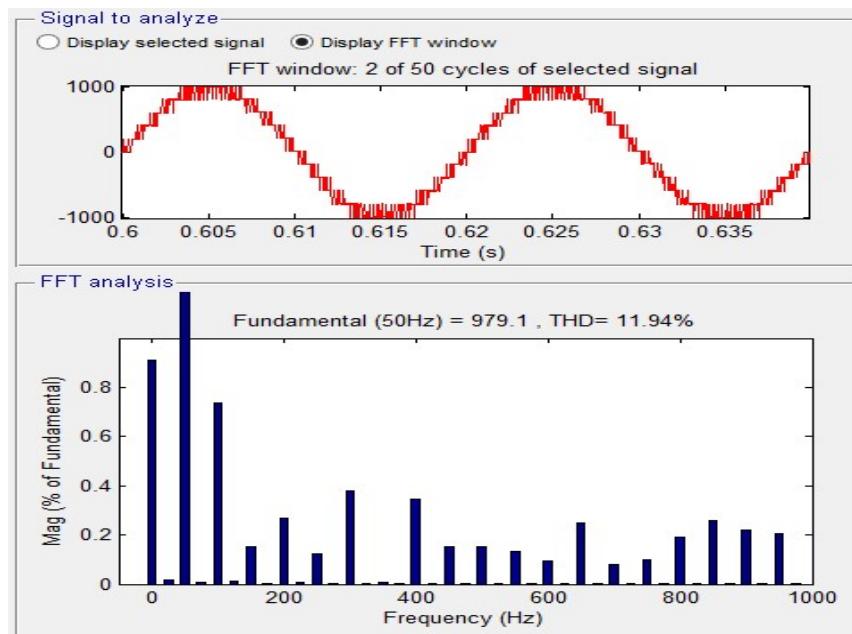


Fig: 6.11 % THD of an 11-level inverter

- The simulated output voltage of a 13-level inverter

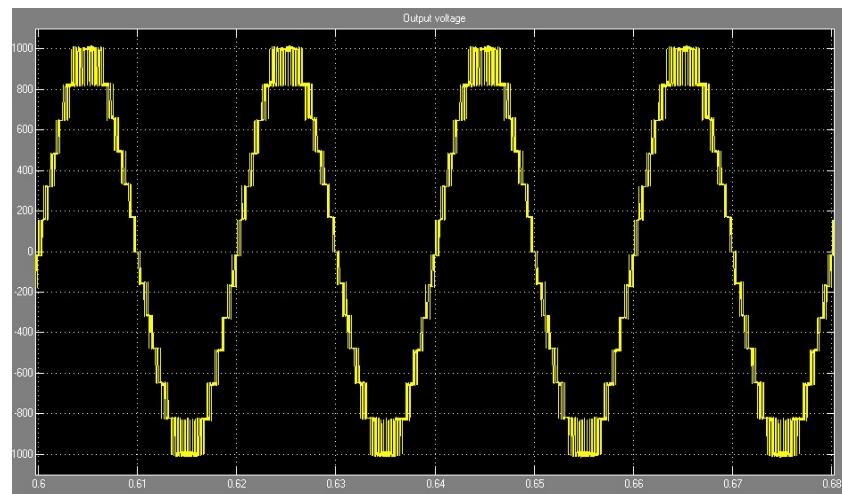


Fig:6.12 Simulated output voltage of a 13-level inverter

- The %THD of a 13-level inverter is shown below

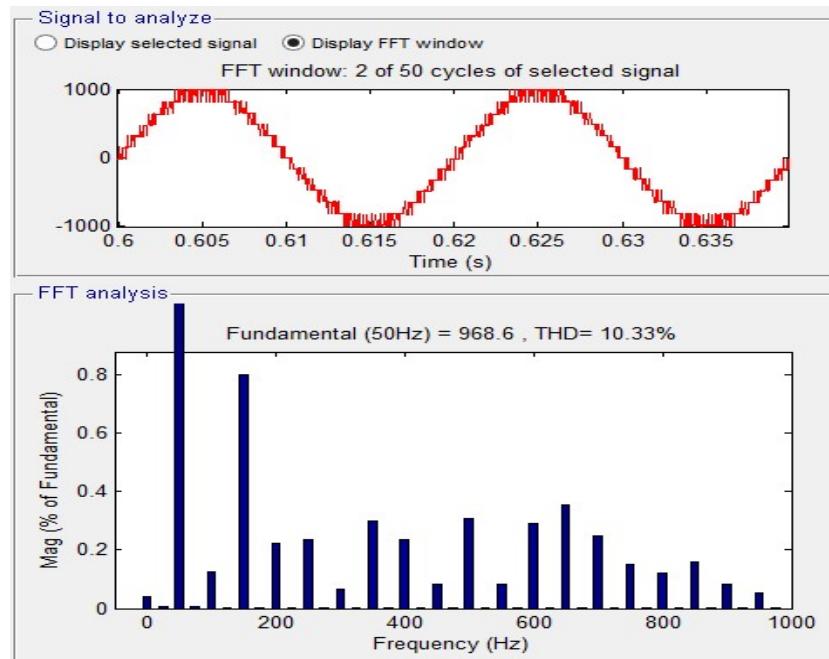


Fig: 6.13 % THD of a 13-level inverter

- The Simulated output voltage of a 15-level inverter is shown below

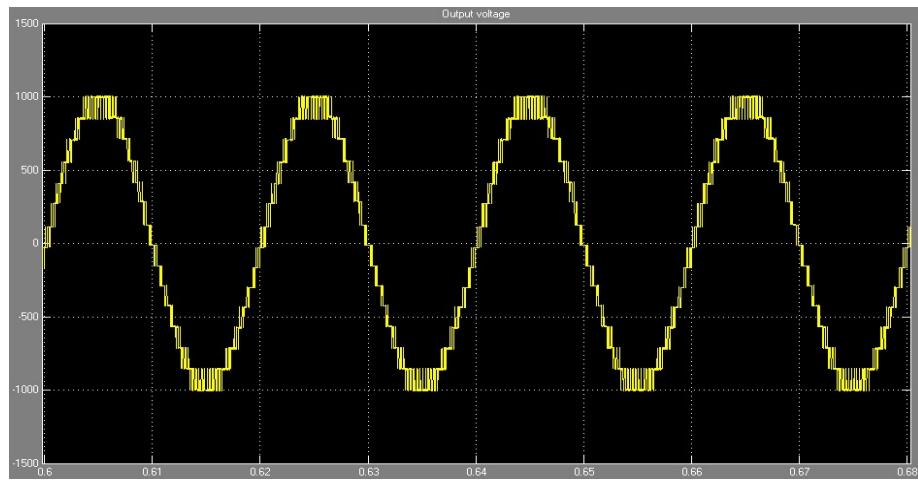


Fig:6.14 Simulated output voltage of a 15-level inverter

- The %THD of a 13-level inverter is shown below

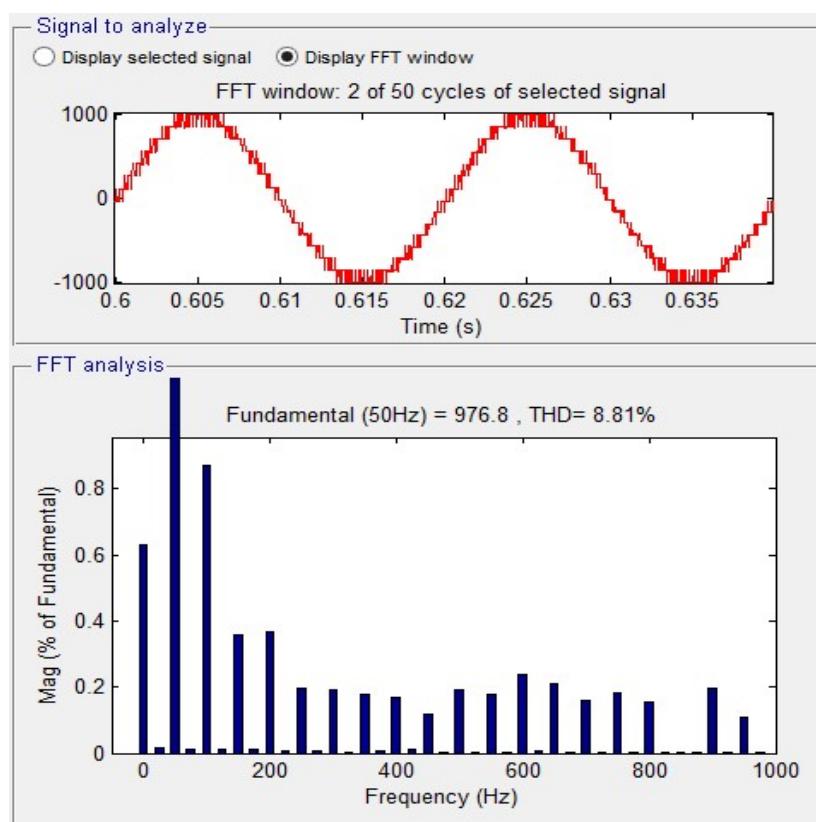


Fig: 6.15 % THD of a 13-level inverter

## **CONCLUSION**

In this project, the concept of a new multilevel inverter with FACTS capability for small-to-mid-size wind installations is presented. The proposed system demonstrates the application of a new inverter with FACTS capability in a single unit without any additional cost. Replacing the traditional renewable energy inverters with the proposed inverter will eliminate the need of any external STATCOM devices to regulate the PF of the grid.

Clearly, depending on the size of the compensation, multiple inverters may be needed to reach the desired PF. This shows a new way in which distributed renewable sources can be used to provide control and support in distribution systems. The proposed controller system adjusts the active power by changing the power angle ( $\delta$ ) and the reactive power is controllable by the modulation index  $m$ . The simulation results for an 15-level inverter are presented in MATLAB/Simulink.

## **FUTURE SCOPE**

MMC-based DSTATCOMs offer a flexible and modular solution for power quality improvement in distribution systems, and there are several control methods available to achieve the desired performance. The choice of the control method will depend on the specific application requirements and the design constraints of the MMC-based DSTATCOM.

## REFERENCES

- [1] *U.S. Solar Market Insight, 2010 Year End Review Executive Summary*, SEIA, Washington, DC, USA, 2011.
- [2] *AWEA U.S. Wind Industry Annual Market Report Year Ending 2010*, AWEA, Washington, DC, USA, 2011.
- [3] S. A. Rahman, R. K. Varma, and W. H. Litzenberger, “Bibliography of FACTS applications for grid integration of wind and PV solar power systems: 1995–2010 IEEE working group report,” in *Proc. IEEE Power Energy Soc. General Meeting*, Jul. 2011, pp. 1–17.
- [4] A. Beekmann, J. Marques, E. Quitmann, and S. Wachtel, “Wind energy converters with FACTS capabilities for optimized integration of wind power into transmission and distribution systems,” in *Proc. CIGRE/IEEE PES Joint Symp. Integr. Wide, Scale Renew. Resour. Power Del. Syst.*, Jul. 2009, pp. 1–9.
- [5] J. Rodriguez, J. S. Lai, and F. Z. Peng, “Multilevel inverters: Survey of topologies, controls, and applications,” *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [6] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, “A multilevel voltage-source inverter with separate DC sources for static VAr generation,” *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Oct. 1996.
- [7] L. M. Tolbert and F. Z. Peng, “Multilevel converters as a utility interface for renewable energy systems,” in *Proc. IEEE Power Eng. Soc. Summer Meeting*, vol. 2. Jul. 2000, pp. 1271–1274.
- [8] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, *et al.*, “Recent advances and industrial applications of multilevel converters,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [9] C. Tareila, P. Sotoodeh, and R. D. Miller, “Design and control of a single-phase D-STATCOM inverter for wind application,” in *Proc. PEMWA*, Jul. 2012, pp. 1–5.
- [10] B. Gultekin and M. Ermis, “Cascaded multilevel converter-based transmission STATCOM: System design methodology and development of a 12 kV  $\pm$ 12 MVA<sub>r</sub> power stage,” *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4930–4950, Nov. 2013.
- [11] K. Sano and M. Takasaki, “A transformerless D-STATCOM based on a multivoltage cascade converter requiring no DC sources,” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2783–2795, Jun. 2012.

- [12] X. Liang, Y. Xu, X. Chen, and C. Guo, “The simulation research of STATCOM based on cascaded multi-level converter,” in *Proc. 4th Int. Conf. Electr. Util. DRPT*, Jul. 2011, pp. 494–498.
- [13] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann, and D. Soerangr, *HVDC PLUS Basic and Principle of Operation*. Erlandgen, Germany: Siemens AG Energy Sector, 2009.
- [14] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, “Prospects of multilevel VSC technologies for power transmission,” in *Proc. IEEE Transmiss. Distrib. Conf. Exposit.*, Apr. 2008, pp. 1–16.
- [15] C. D. Barker and N. M. Kirby, “Reactive power loading of components within a modular multi-level HVDC VSC converter,” in *Proc. IEEE EPEC*, Oct. 2011, pp. 86–90.
- [16] C. P. Tareila, “A single-phase D-STATCOM Inverter for distributed energy sources,” M.S. thesis, Dept. Electr. Comput. Eng., Kansas State Univ., Manhattan, KS, USA, Aug. 2011.
- [17] Z. Yang, C. Shen, L. Zhang, M. L. Crow, and S. Atcity, “Integration of a STATCOM and battery energy storage,” *IEEE Trans. Power Syst.*, vol. 16, no. 2, pp. 254–260, May 2001.
- [18] S. Chakraborty, B. Kroposki, and W. Kramer, “Evaluation of control and voltage regulation functionalities in a single-phase utility-connected inverter for distributed energy applications,” in *Proc. IEEE ECCE*, Sep. 2009, pp. 1753–1759.
- [19] R. K. Varma, S. A. Rahman, A. C. Mahendra, R. Seethapathy, and T. Vanderheide, “Novel nighttime application of PV solar farms as STATCOM (PV-STATCOM),” in *Proc. IEEE Power Energy Soc. General Meeting*, Jul. 2012, pp. 1–8.
- [20] R. K. Varma, E. M. Siavashi, B. Das, and V. Sharma, “Real-time digital simulation of a PV solar system as STATCOM (PV-STATCOM) for voltage regulation and power factor correction,” in *Proc. EPEC*, Oct. 2012, pp. 157–163.
- [21] R. K. Varma, S. A. Rahman, V. Sharma, and T. Vanderheide, “Novel control of a PV solar system as STATCOM (PV-STATCOM) for preventing instability of induction motor load,” in *Proc. 25th IEEE CCECE*, May 2012, pp. 1–5.
- [22] R. Marquardt and A. Lesnicar, “New concept for high voltage—Modular multilevel converter,” in *Proc. PESC*, Jun. 2004, pp. 1–5.
- [23] A. Lesnicar and R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range,” in *Proc. IEEE Power Tech. Conf.*, vol. 3. Jun. 2003, pp. 1–6.

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Declaration : The above information provided by me is true and correct to the best of knowledge.

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