ey Terms

ddress bus	execute cycle	multilane distribution
ddress lines	fetch cycle	packets
rbitration	flit	PCI Express (PCIe)
alanced transmission	flow control function	peripheral component interconnect (PCI)
us	instruction cycle	phit
ontrol lines	interrupt	QuickPath Interconnect (QPI)
ata bus	interrupt handler	root complex
ata lines	interrupt service routine (ISR)	system bus
fferential signaling	lane	
sabled interrupt	memory address register (MAR)	
stributed arbitration	memory buffer register (MBR)	
ror control function		

Review Questions

3.1 Describe the three key concepts of the von Neumann architecture.

3.2 State the difference between an I/O address register and an I/O buffer register.

3.3 What are the drawbacks of disabling interrupts? Give an appropriate example.

3.4 What types of transfers must a computer's interconnection structure (e.g., bus) support?

3.5 List and briefly define the QPI protocol layers.

3.6 List and briefly define the PCIe protocol layers.

Problems

3.1 The hypothetical machine of Figure 3.4 also has two I/O instructions:

0011 = Load AC from I/O

0111 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

1. Load AC from device 5.
2. Add contents of memory location 940.
3. Store AC to device 6.

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.

3.2 The program execution of Figure 3.5 is described in the text using six steps. Expand this description to show the use of the MAR and MBR.

3.3 Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.
   a. What is the maximum directly addressable memory capacity (in bytes)?
   b. Discuss the impact on the system speed if the microprocessor bus has:
      1. 32-bit local address bus and a 16-bit local data bus, or
      2. 16-bit local address bus and a 16-bit local data bus.
   c. How many bits are needed for the program counter and the instruction register?

3.4 Consider a hypothetical microprocessor generating a 16-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus.
   a. What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?
   b. What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"?
   c. What architectural features will allow this microprocessor to access a separate "I/O space"?
   d. If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support? How many 16-bit I/O ports? Explain.

3.5 Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/sec? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make, and explain. *Hint:* Determine the number of bytes that can be transferred per bus cycle.

3.6 Consider a computer system that contains an I/O module controlling a simple keyboard/printer teletype. The following registers are contained in the processor and connected directly to the system bus:

INPR: Input Register, 8 bits
OUTR: Output Register, 8 bits
FGI: Input Flag, 1 bit
FGO: Output Flag, 1 bit
IEN: Interrupt Enable, 1 bit

Keystroke input from the teletype and printer output to the teletype are controlled by the I/O module. The teletype is able to encode an alphanumeric symbol to an 8-bit word and decode an 8-bit word into an alphanumeric symbol.
   a. Describe how the processor, using the first four registers listed in this problem, can achieve I/O with the teletype.
   b. Describe how the function can be performed more efficiently by also employing IEN.

3.7 Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.
   a. Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?
   b. Repeat assuming that half of the operands and instructions are one byte long.

3.8 Figure 3.26 indicates a distributed arbitration scheme that can be used with an obsolete bus scheme known as Multibus I. Agents are daisy-chained physically in priority order. The left-most agent in the diagram receives a constant *bus priority in* (BPRN) signal indicating that no higher-priority agent desires the bus. If the agent does not require the bus, it asserts its *bus priority out* (BPRO) line. At the beginning of a clock

3.13 A microprocessor has a memory write timing as shown in Figure 3.18. Its manufacturer specifies that the width of the Write signal can be determined by 0.75 * T, where T is the clock period in ns.

a. What width should we expect for the Write signal if the bus clocking rate is 8 MHz, and 12 MHz?

b. The data sheet for the microprocessor specifies that the data remain valid for 15 ns after the falling edge of the Write signal. What is the total duration of valid data presentation to memory?

c. How many wait states should we insert if the memory requires valid data presentation for at least 95 ns?

3.14 A microprocessor has a decrement memory direct instruction, which subtracts 1 from the value in a memory location. The instruction has five stages: fetch opcode (two bus clock cycles), fetch operand address (five cycles), fetch operand (five cycles), subtract 1 from operand (four cycles), and store operand (two cycles).

a. By what amount (in percent) will the duration of the instruction increase if we have to insert one bus wait state in each memory read and memory write operation?

b. Repeat assuming that the decrement operation takes 8 cycles instead of 4 cycles.

3.15 The Intel 8088 microprocessor has a read bus timing similar to that of Figure 3.18, but requires four processor clock cycles. The valid data is on the bus for an amount of time that extends into the fourth processor clock cycle.

a. What is the maximum data transfer rate if the processor clock rate is 20 MHz and 50 MHz?

b. Repeat part (a) but assume the need to insert one wait state per byte transferred.

3.16 The Intel 8086 is a 16-bit processor similar in many ways to the 8-bit 8088. The 8086 uses a 16-bit bus that can transfer 2 bytes at a time, provided that the lower-order byte has an even address. However, the 8086 allows both even- and odd-aligned word operands. If an odd-aligned word is referenced, two memory cycles, each consisting of four bus cycles, are required to transfer the word. Consider an instruction on the 8086 that involves four 16-bit operands. How long does it take to fetch the operands? Give the range of possible answers. Assume a clocking rate of 2 MHz and no wait states.

3.17 Consider a 64-bit microprocessor whose bus cycle is the same duration as that of a 32-bit microprocessor. Assume that, on average, 25% of the operands and instructions are 16 bits long, 25% are 64 bits long, and 50% are 32 bits long. Calculate the improvement achieved when fetching instructions and operands with the 64-bit microprocessor.

3.18 The microprocessor of Problem 3.14 initiates the fetch operand address stage of the decrement memory direct instruction at the same time that a keyboard activates an interrupt request line. After how long does the processor enter the interrupt processing cycle? Assume a bus clocking rate of 50 MHz.