Review Questions

5.1 What are the three most common functional terminals of a memory cell?

5.2 What are two interpretations of the term *random-access memory*?

5.3 What is the difference between DRAM and SRAM in terms of application?

5.4 What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, and cost?

5.5 Explain why one type of RAM is considered to be analog and the other digital.

5.6 What are some common forms of read-mostly memory?

5.7 What are the differences among EPROM, EEPROM, and flash memory?

5.8 Explain the function of each pin in Figure 5.4b.

5.9 What is hard failure in a semiconductor memory system?

5.10 How is the syndrome for the Hamming code interpreted?

5.11 How does SDRAM differ from ordinary DRAM?

5.12 What is DDR RAM?

5.13 What is the difference between NAND and NOR flash memory?

5.14 List and briefly define three newer nonvolatile solid-state memory technologies.

Problems

5.1 Why do synchronous DRAMs make use of a register, called a mode register, not used in conventional DRAMs?

5.2 Consider a dynamic RAM that must be given a refresh cycle 128 times per ms. Each refresh operation requires 200 ns; a memory cycle requires 250 ns. What percentage of the memory's total operating time must be given to refreshes?

5.3 Figure 5.20 shows a simplified timing diagram for a DRAM read operation over a bus. The access time is considered to last from t_1 to t_2. Then there is a recharge time, lasting from t_2 to t_3, during which the DRAM chips will have to recharge before the processor can access them again.

a. Assume that the access time is 151 ns and the recharge time is 49 ns. What is the memory cycle time? What is the maximum data rate this DRAM can sustain, assuming a 2-bit output, and a 4-bit output?

b. Constructing a 64-bit wide memory system using these chips yields what data transfer rate?

5.4 Figure 5.6 indicates how to construct a module of chips that can store 1 MB based on a group of four 256-Kbyte chips. Let's say this module of chips is packaged as a single 1-MB chip, where the word size is 1 byte. Give a high-level chip diagram of how to construct an 8-MB computer memory using eight 1-MB chips. Be sure to show the address lines in your diagram and what the address lines are used for.

5.10 For the Hamming code shown in Figure 5.10, show what happens when a check bit rather than a data bit is in error?

5.11 Suppose an 8-bit data word stored in memory is 00010011. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. Show how you got your answer.

5.12 For the 8-bit word 00100001, the check bits stored with it would be 1001. Suppose when the word is read from memory, the check bits are calculated to be 0101. What is the data word that was read from memory?

5.13 How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 4096-bit data word?

5.14 Develop an SEC code for a 16-bit data word. Generate the code for the data word 0101000000111001. Show that the code will correctly identify an error in data bit 5.