

chapter.5 Internal Memory

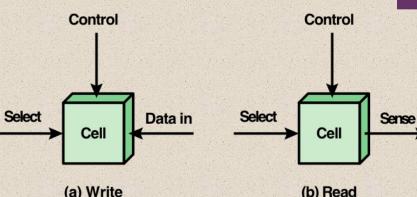


Figure 5.1 Memory Cell Operation

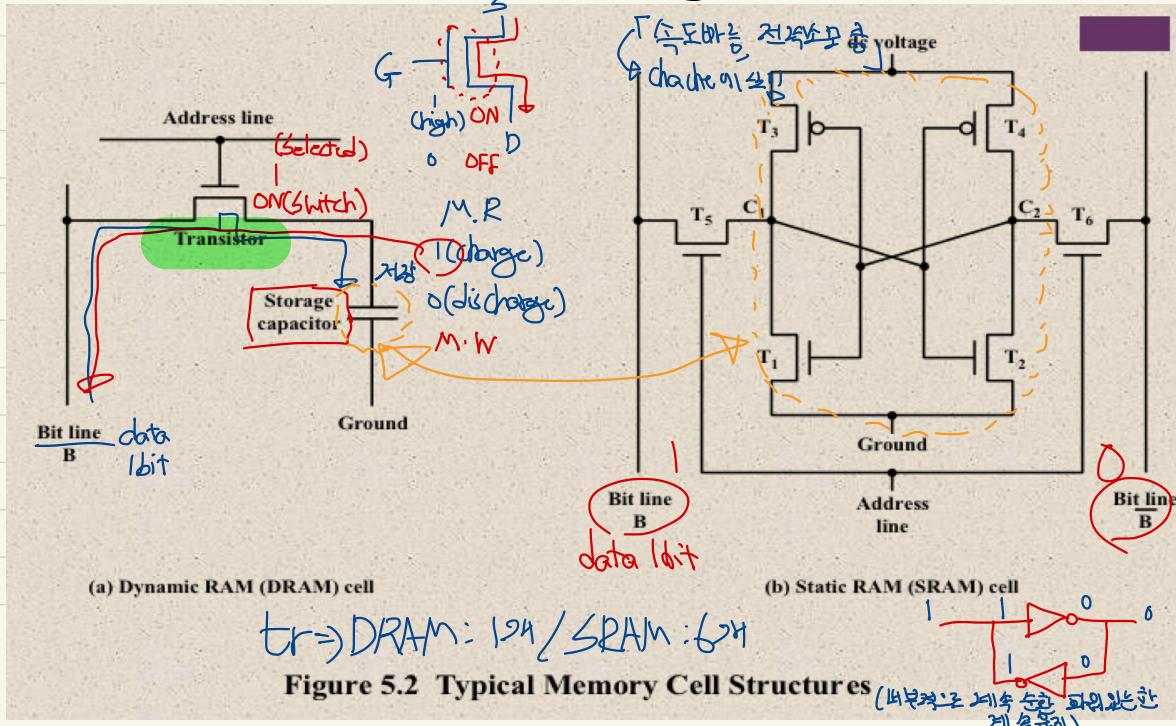
Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile (회복성)
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)				
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level	Electrically	Nonvolatile
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

→ Read, write 가능

Table 5.1
Semiconductor Memory Types

Ram Technology

- Dynamic RAM (DRAM) : Main memory (DDR4)
- Static RAM (SRAM) : Cache memory



SRAM VS DRAM

- Both Volatile (둘다 흐(발성))

- Dynamic Cell

- Simpler to build, Smaller

- More dense

- Less expensive

- Requires the supporting

- refresh circuitry

(자동방전 때문에 증기적으로
충전된다)

- Static Cell

- Faster

- Used for Cache memory

ROM (Read Only Memory)

- 한번 써놓으면 강신 X

- 값을 유지하는데 전원이 필요 X

- Bit-by-bit 교환나도 전부 바꿔야 함

⇒ Programmable ROM

Flash Memory

- Intermediate between EPROM and EEPROM in both cost and functionality

- Uses an electrical erasing technology, does not provide byte-level erasure block level로 지우침

- Microchip is organized so that a section of memory cells are erased in a single action or "flash"

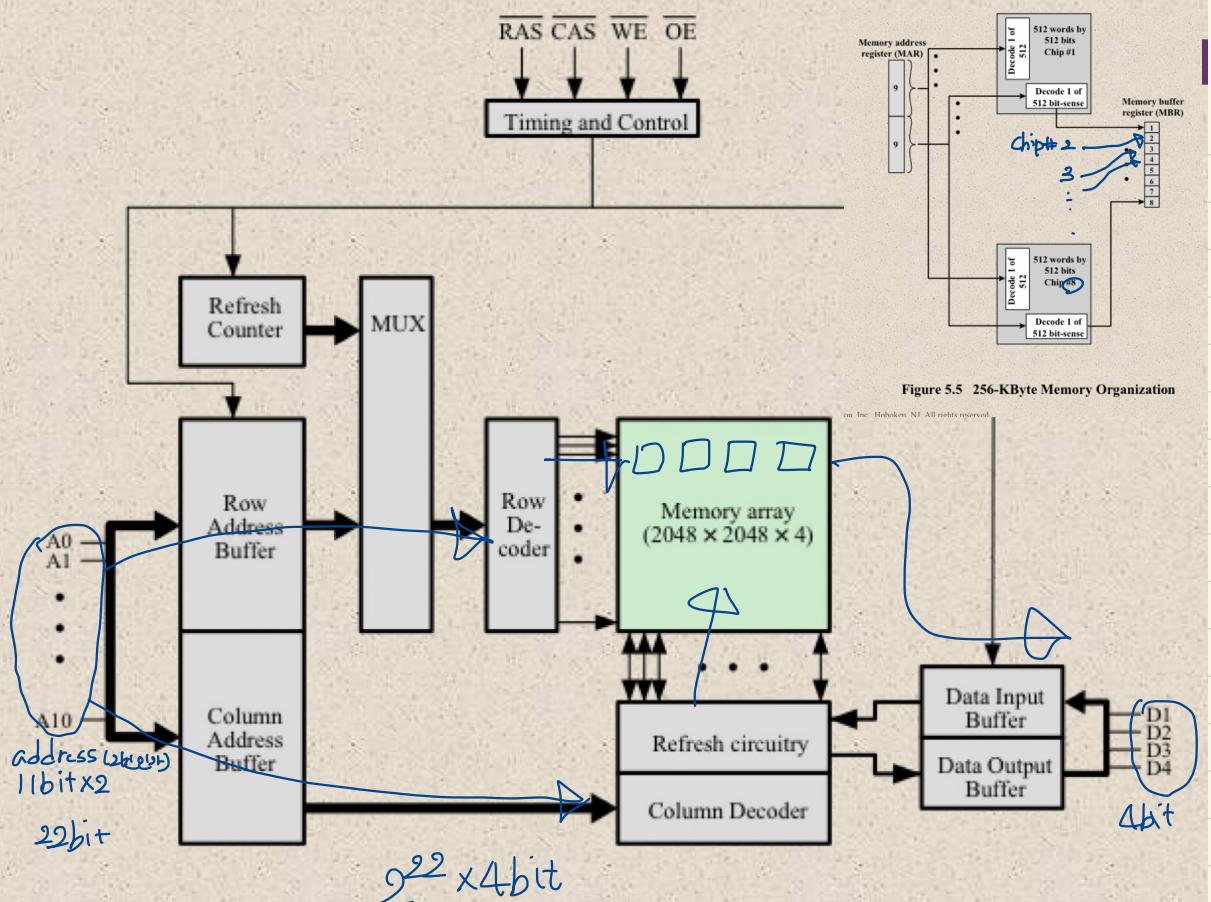
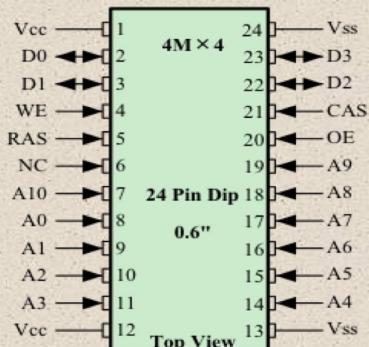
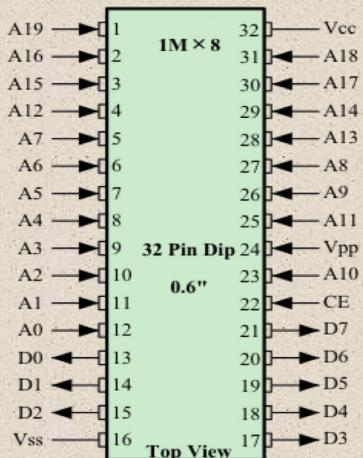


Figure 5.3 Typical 16 Megabit DRAM (4M × 4)



RAS
(Row Address Select)
CAS
(Column Address Select)

(a) 8 Mbit EPROM

$$2^3 \times 8 \text{ bit} = 8 \text{ Mbit}$$

(b) 16 Mbit DRAM D = 4 bit

$$2^{11} \times 4 \text{ bit} = 16 \text{ Mbit}$$

$$A = 11 \text{ bit}$$

Error Correction

- Hard Failure (한 번 고장나면 수2(x))

- Soft Error (영구적인 손상x)

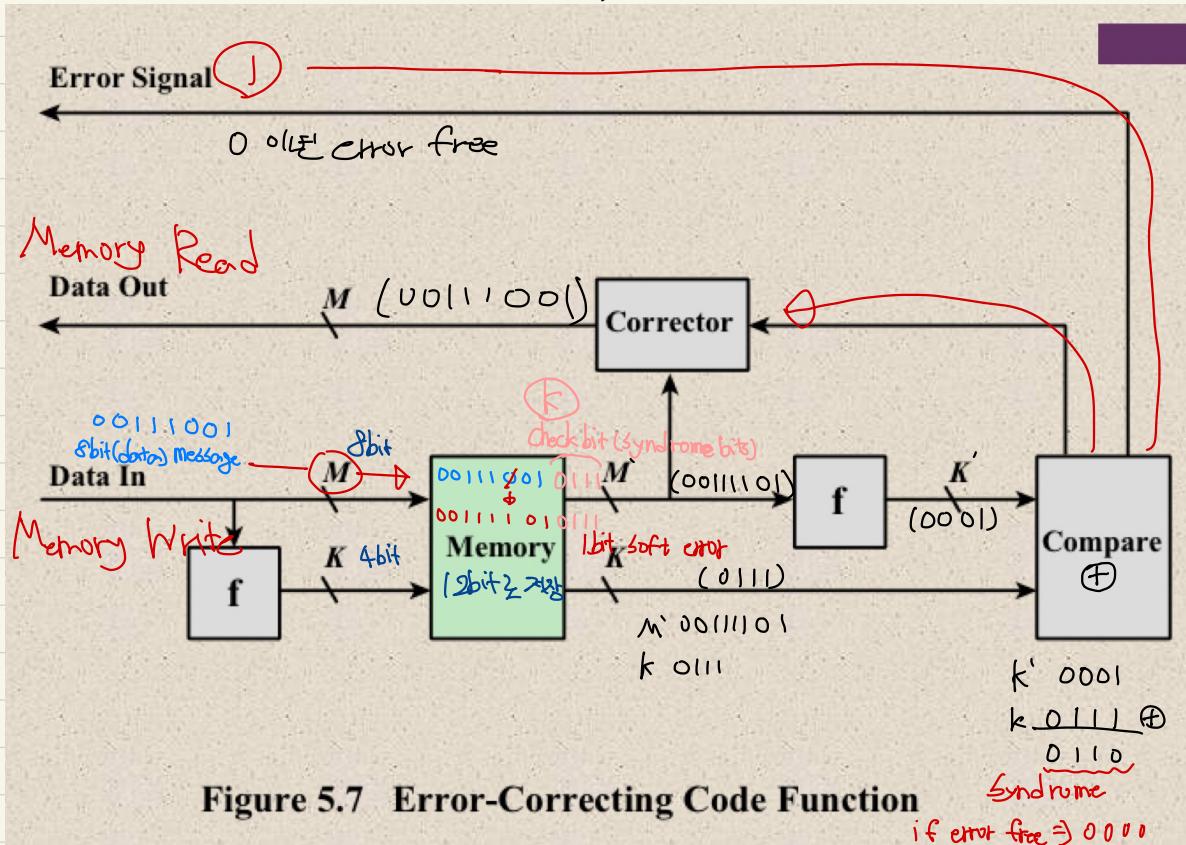
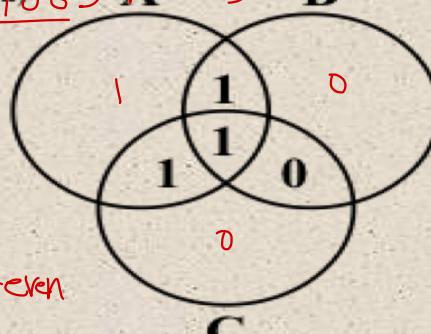
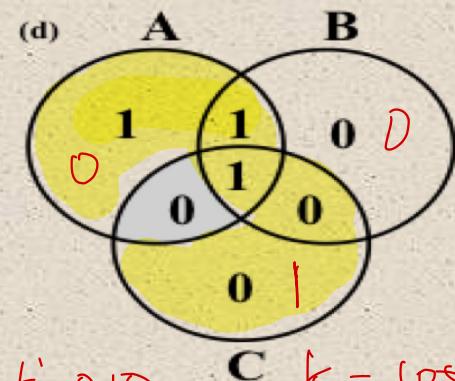
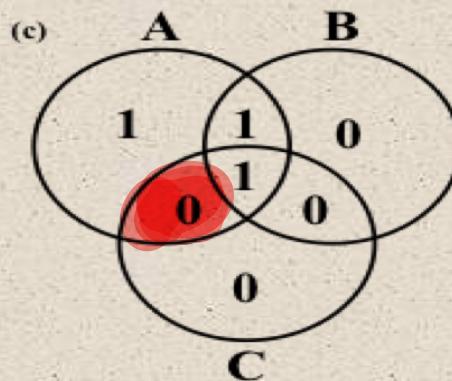
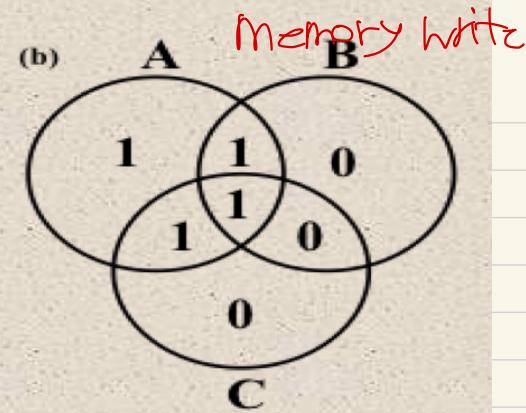


Figure 5.7 Error-Correcting Code Function

$M=4$ $k=3$
 $1110 / \underline{100} \rightarrow$ Parity Bits (f)



parity-even



$k=010$

$M=1110$

$M=\underline{1100}$

$k=100$

$\oplus k' 010$

$\boxed{1110}$

error

Figure 5.8 Hamming Error-Correcting Code

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$M=4$ $k=3$

$n+1$ (24)

error = $n+1-2$

$$2^k - 1 \geq M+k$$

$D_8 \sim D_1$ (8bit)

$C_8 C_4 C_2 C_1$ (4bit)

Bit position	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check bit					C8				C4		C2	C1

Figure 5.9 Layout of Data Bits and Check Bits

Step. 1 Check bit 먼저 배치
→ Step. 2 Data bit 배치

$$C_1 : 2^0 \text{위치가 있음} \quad \text{Data bit} = D_1 \oplus D_2 \oplus D_4 \oplus D_5 \oplus D_7$$

$$C_2 : 2^1 \text{위치가 있음} \quad = D_1 \oplus D_3 \oplus D_4 \oplus D_6 \oplus D_7$$

$$C_3 : 2^2 \text{위치가 있음} \quad = D_2 \oplus D_3 \oplus D_4 \oplus D_8$$

$$C_4 : 2^3 \text{위치가 있음} \quad = D_5 \oplus D_6 \oplus D_7 \oplus D_8$$

Bit position	12	11	10	9	8	7	6	5	4	3	2	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check bit					C8				C4		C2	C1
MW stored as	0	0	1	1	0	1	0	0	1	1	1	1
MR fetched as	0	0	1	1	0	1	1	0	1	1	1	1
Position number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Check bit					0				0	0	0	1

Figure 5.10 Check Bit Calculation

$$C_4 : 0 \oplus 0 \oplus 1 \oplus 0 = 1 \quad k=0111$$

$$C_4 : 0 \oplus 1 \oplus 1 \oplus 0 = 0 \quad \underline{k=0001 \oplus}$$

$$S = 0110$$

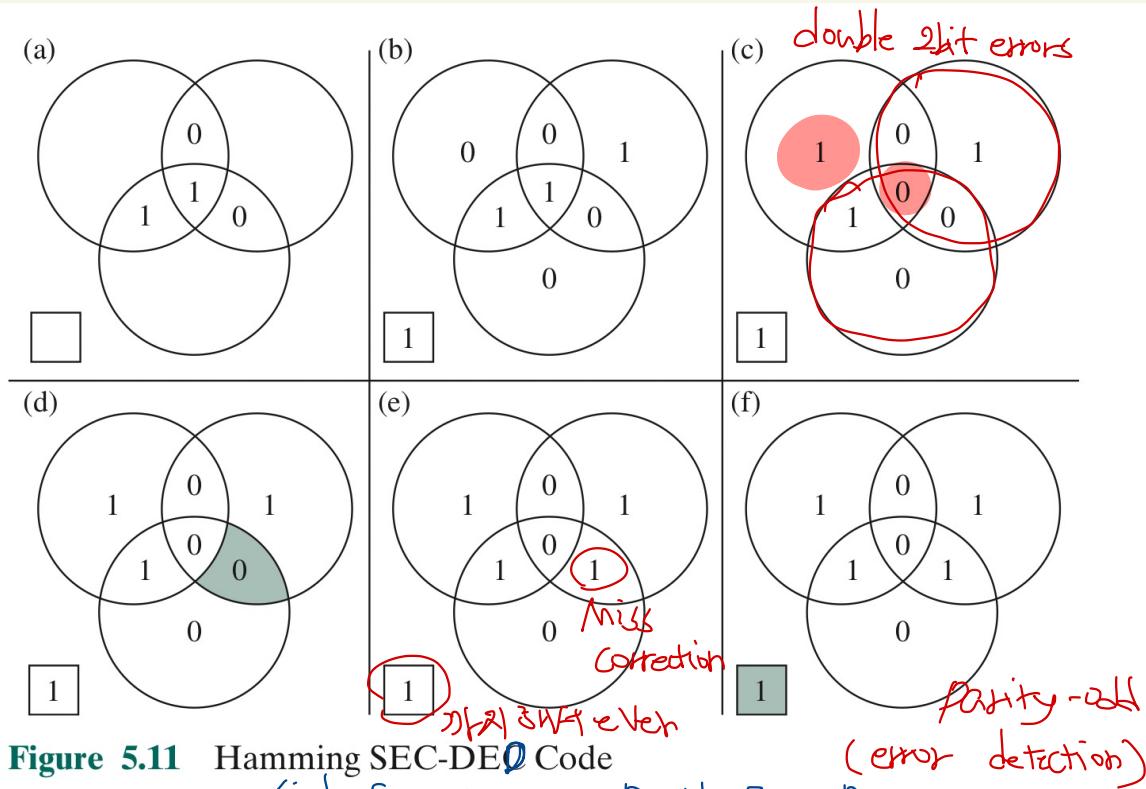


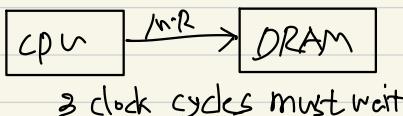
Figure 5.11 Hamming SEC-DED Code

Single Error Correcting - Double Error Detecting

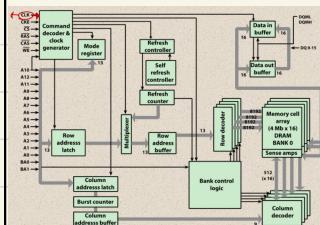
SEC DED IBM computer M:64 K=8

M=8 M=8
k=4 k=5

asynchronous (비동기) no clock

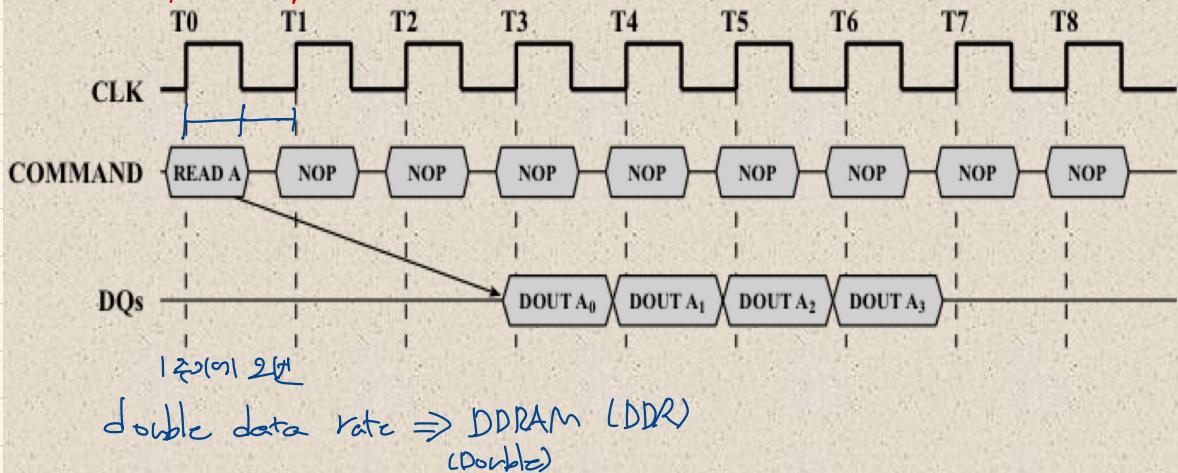


Synchronous (동기) Dynamic RAM (SDRAM)
CPU가 소는 시간이 없음



SDRAM Read Timing

120)
clock period
→



Flash Memory

- 2진수로 한 블록을 지움 (1 block erase) ← 단점
- Write : erased + write (delay)
- Read : 빠름

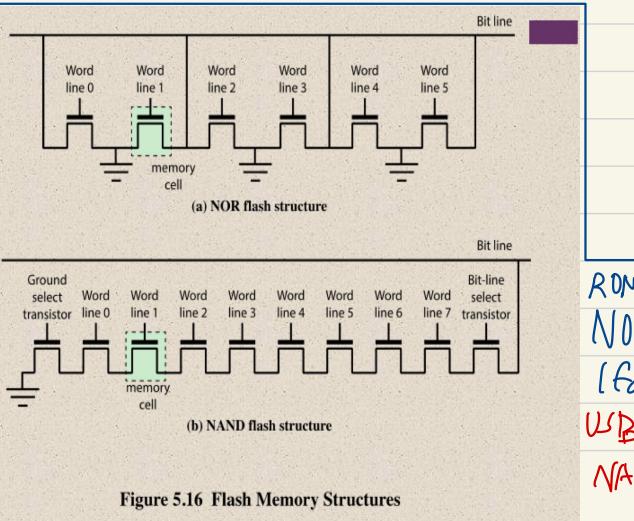
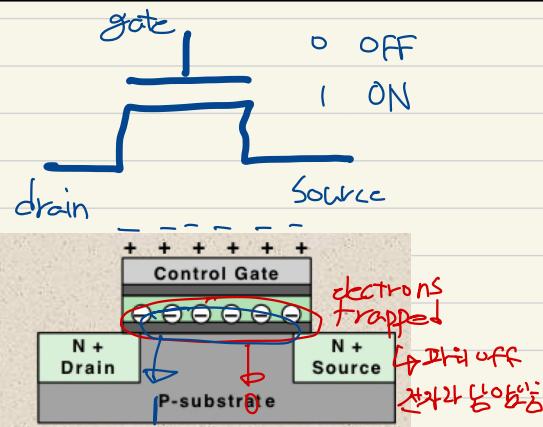


Figure 5.16 Flash Memory Structures



(c) Flash memory cell in zero state
Non volatile

ROM ← boot loader
NOR Flash : byte level Read/Write
(fast speed)

USB SSD

NAND Flash : block level (density ↑)