Problems

13.1 Given the following memory values and a one-address machine with an accumulator, what values do the following instructions load into the accumulator?

- Word 3 contains 15.
- Word 12 contains 18.
- Word 15 contains 24.
- Word 18 contains 36.

a. LOAD IMMEDIATE 3
b. LOAD DIRECT 3
c. LOAD INDIRECT 3
d. LOAD IMMEDIATE 15
e. LOAD INDIRECT 12
f. LOAD DIRECT 18

13.3 An address field in an instruction contains decimal value 96. Where is the corresponding operand located for

a. immediate addressing?
b. direct addressing?
c. indirect addressing?
d. register addressing?
e. register indirect addressing?

13.4 Consider a 16-bit processor in which the following appears in main memory, starting at location 100:

100	Load to AC	Mode
101	300	
102	Next instruction	

The first part of the first word indicates that this instruction loads a value into an accumulator. The Mode field specifies an addressing mode and, if appropriate, indicates a source register; assume that when used, the source register is R1, which has a value of 200. There is also a base register that contains the value 100. The value of 300 in location 101 may be part of the address calculation. Assume that location 199 contains the value 799, location 200 contains the value 800, and so on. Determine the effective address and the operand to be loaded for the following address modes:

a. Direct
b. Immediate
c. Indirect
d. PC Relative
e. Displacement
f. Register
g. Register indirect
h. Autoindexing with increment, using R1

Problems

14.1 **a.** If the last operation performed on a computer with an 8-bit word was an addition in which the two operands were 00100100 and 00010001, what would be the value of the following flags?

- Carry
- Zero
- Overflow
- Sign
- Even Parity
- Half-Carry

b. Repeat for the addition of −2 (twos complement) and +3.

14.2 Repeat Problem 14.1 for the operation A−B, where A contains 11001100 and B contains 00110011.

14.3 A microprocessor has a clock cycle of 0.125 ns.

a. What is the clock rate of this processor?
b. What is the duration of a particular type of machine instruction consisting of seven clock cycles?

14.7 Consider the timing diagram of Figures 14.10. Assume that there is only a two-stage pipeline (fetch, execute). Redraw the diagram to show how many time units are now needed for four instructions.

14.8 Assume a pipeline with four stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Draw a diagram similar to Figure 14.10 for a sequence of 7 instructions, in which the third instruction is a branch that is taken and in which there are no data dependencies.

14.9 A pipelined processor has a clock rate of 5 GHz and executes a program with 5 million instructions. The pipeline has four stages, and instructions are issued at a rate of two per clock cycle. Ignore penalties due to branch instructions and out-of-sequence executions.

a. What is the speedup of this processor for this program compared to a nonpipelined processor, making the same assumptions used in Section 14.4?

b. What is the throughput (in MIPS) of the pipelined processor?

14.10 A nonpipelined processor has a clock rate of 10 GHz and an average CPI (cycles per instruction) of 5. An upgrade to the processor introduces a four-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor has to be reduced to 9 GHz.

a. What is the speedup of this processor for this program compared to a nonpipelined processor, making the same assumptions used in Section 14.4?

b. What is the throughput (in MIPS) of the pipelined processor?

14.11 Consider an instruction sequence of length n that is streaming through the instruction pipeline. Let p be the probability of encountering a conditional or unconditional branch instruction, and let q be the probability that execution of a branch instruction I causes a jump to a nonconsecutive address. Assume that each such jump requires the pipeline to be cleared, destroying all ongoing instruction processing, when I emerges from the last stage. Revise Equations (14.1) and (14.2) to take these probabilities into account.