5.3 SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory.

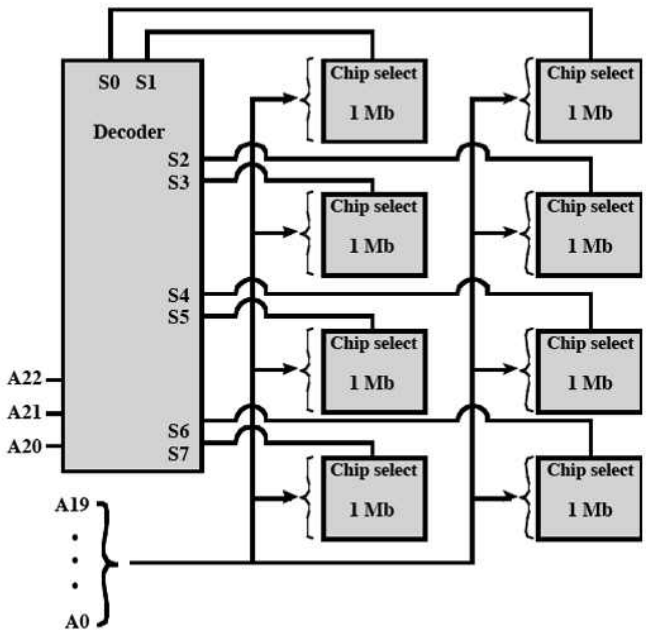
5.4 SRAMs generally have faster access times than DRAMs. DRAMS are less expensive and smaller than SRAMs.

5.11 Unlike the traditional DRAM, which is asynchronous, the SDRAM exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.

5.13 In **NOR flash memory**, the basic unit of access is a bit, referred to as a *memory cell*. Cells in NOR flash are connected in parallel to the bit lines so that each cell can be read/write/erased individually. If any memory cell of the device is turned on by the corresponding word line, the bit line goes low. This is similar in function to a NOR logic gate. **NAND flash memory** is organized in transistor arrays with 16 or 32 transistors in series. The bit line goes low only if all the transistors in the corresponding word lines are turned on. This is similar in function to a NAND logic gate.

5.2 In 1 ms, the time devoted to refresh is 128 × 200 ns = 25,600 ns. The fraction of time devoted to memory refresh is $(25.6 \times 10^{-6}\ \text{s})/10^{-3}\ \text{s} = 0.0256$, which is approximately 2.56%.

5.4



5.10 The stored word is 001101001111, as shown in Figure 5.10. Now suppose that the only error is in C8, so that the fetched word is 001111001111. Then the received block results in the following table:

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Block	0	0	1	1	1	1	0	0	1	1	1	1
Codes			1010	1001		0111				0011		

The check bit calculation after reception:

Position	Code
Hamming	1111
10	1010
9	1001
7	0111
3	0011
XOR = syndrome	1000

The nonzero result detects and error and indicates that the error is in bit position 8, which is check bit C8.

5.11

Position	12	11	10	9	8	7	6	5	4	3	2	1
Block	D8	D7	D6	D5	C4	D4	D3	D2	C4	D1	C2	C1
Bits	0	0	0	1		0	0	1		1		

The check bits are in bit numbers 8, 4, 2, and 1.
Check bit 8 calculated by values in bit numbers: 12, 11, 10 and 9
Check bit 4 calculated by values in bit numbers: 12, 7, 6, and 5
Check bit 2 calculated by values in bit numbers: 11, 10, 7, 6 and 3
Check bit 1 calculated by values in bit numbers: 11, 9, 7, 5 and 3
Thus, the check bits are: 1 1 1 1

5.12 The Hamming Word initially calculated was:

bit number:	12	11	10	9	8	7	6	5	4	3	2	1
	0	0	1	0	1	0	0	0	0	1	0	1

Doing an exclusive-OR of 1001 and 0101 yields 1100 indicating an error in bit 12 of the Hamming Word. Thus, the data word read from memory was 10100001.

5.13 Need K check bits such that $4096 + K \leq 2^K - 1$.
The minimum value of K that satisfies this condition is 13.

5.14 As Table 5.2 indicates, 5 check bits are needed for an SEC code for 16-bit data words. The layout of data bits and check bits:

Bit Position	Position Number	Check Bits	Data Bits
21	10101		M16
20	10100		M15
19	10011		M14
18	10010		M13
17	10001		M12
16	10000	C16	
15	01111		M11
14	01110		M10
13	01101		M9
12	01100		M8
11	01011		M7
10	01010		M6
9	01001		M5
8	01000	C8	
7	00111		M4
6	00110		M3
5	00101		M2
4	00100	C4	
3	00011		M1
2	00010	C2	
1	00001	C1	

The equations are calculated as before, for example,
C1= M1 ⊕ M2 ⊕M4 ⊕ M5 ⊕ M7 ⊕ M9 ⊕ M11 ⊕ M12 ⊕ M14 ⊕ M16.

For the word 0101000000111001, the code is
C16 = 1; C8 = 1; C 4 = 1; C2 = 1; C1 = 0.

If an error occurs in data bit 4:
C16 = 1 ; C8 =1; C4 = 0; C2 = 0; C1 = 1.

Comparing the two:

C16	C8	C4	C2	C1
1	1	1	1	0
1	1	0	0	1
0	0	1	1	1

The result is an error identified in bit position 7, which is data bit 4.