SH1106

Preliminary

132 X 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller

Features

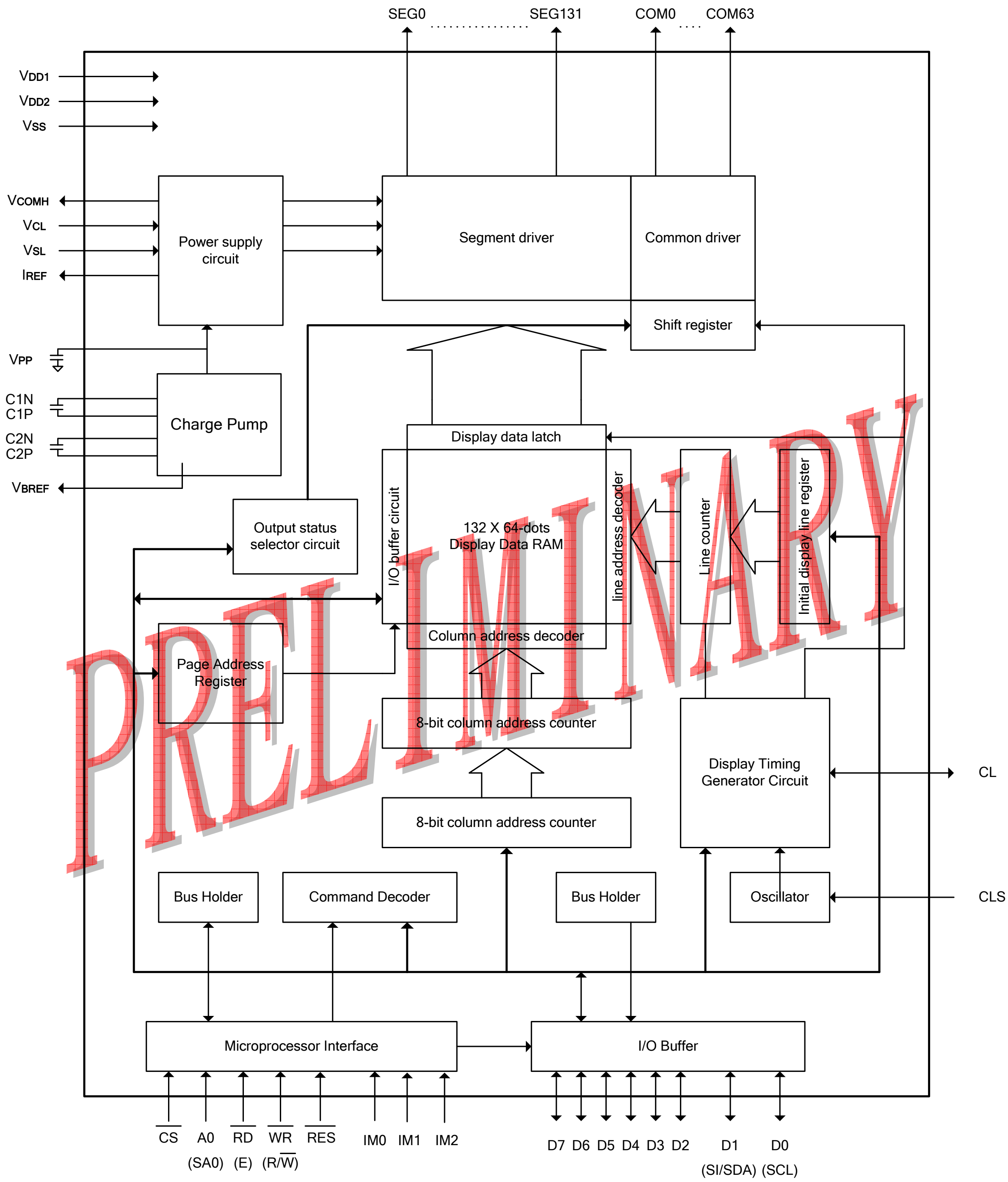
- Support maximum 132 X 64 dot matrix panel
- Embedded 132 X 64 bits SRAM
- Operating voltage:
  - Logic voltage supply: V_{DD1} = 1.65V - 3.5V
  - DC-DC voltage supply: V_{DD2} = 3.0V – 4.2V
- OLED Operating voltage supply:
  External V_{PP} supply = 6.4V - 13.0V
  Internal V_{PP} generator = 6.4V - 9.0V
- Maximum segment output current: 200µA
- Maximum common sink current: 27mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, 3-wire & 4-wire serial peripheral interface, 400KHz fast I^2C bus interface
- Programmable frame frequency and multiplexing ratio
- Row re-mapping and column re-mapping (ADC)
- Vertical scrolling
- On-chip oscillator
- Programmable Internal charge pump circuit output
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
  - Sleep mode: <5µA
  - VDD1=0V，VDD2=3.0V – 4.2V: <5µA
  - VDD1,2=0V，VPP=3.0V – 4.2V: <5µA
- Wide range of operating temperatures: -40 to +85°C
- Available in COG form, thickness: 300µm

General Description

SH1106 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1106 consists of 132 segments, 64 commons that can support a maximum display resolution of 132 X 64. It is designed for Common Cathode type OLED panel.

SH1106 embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1106 is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.

Block Diagram



Pad Description

Power Supply

Symbol	I/O	Description
V_{DD1}	Supply	Power supply input: 1.65 - 3.5V
V_{DD2}	Supply	3.0 – 4.2V power supply pad for Power supply for charge pump circuit. This pin can be disconnected or connect to V_{DD1} when V_{PP} is supplied externally
Vss	Supply	Ground.
V_{SL}	Supply	This is a segment voltage reference pad. This pad should be connected to Vss externally.
V_{CL}	Supply	This is a common voltage reference pad. This pad should be connected to Vss externally.

OLED Driver Supplies

Symbol	I/O	Description
I_{REF}	O	This is a segment current reference pad. A resistor should be connected between this pad and Vss. Set the current at 10μA.
V_{COMH}	O	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and Vss.
V_{BREF}	NC	This is an internal voltage reference pad for booster circuit. Keep floating.
V_{PP}	P	OLED panel power supply. Generated by internal charge pump. Connect to capacitor. It could be supplied externally.
C1N, C1P	P	Connect to charge pump capacitor. These pins are not used and should be disconnedted when Vpp is supplied externally.
C2P, C2N	P	Connect to charge pump capacitor. These pins are not used and should be disconnedted when Vpp is supplied externally.

System Bus Connection Pads

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>CL</td><td>I/O</td><td>This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.</td></tr>
<tr><td>CLS</td><td>I</td><td>This is the internal clock enable pad.
CLS = “H”: Internal oscillator circuit is enabled.
CLS = “L”: Internal oscillator circuit is disabled (requires external input).
When CLS = “L”, an external clock source must be connected to the CL pad for normal operation.</td></tr>
<tr><td>IM0
IM1
IM2</td><td>I</td><td>These are the MPU interface mode select pads.
<table>
<tr><th></th><th>8080</th><th>I²C</th><th>6800</th><th>4-wire SPI</th><th>3-wire SPI</th></tr>
<tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>This pad is the chip select input. When $\overline{CS}$ = “L”, then the chip select becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>This is a reset signal input pad. When $\overline{RES}$ is set to “L”, the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.</td></tr>
<tr><td>A0</td><td>I</td><td>This is the Data/Command control pad that determines whether the data bits are data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.
In I²C interface, this pad serves as SA0 to distinguish the different address of OLED driver.</td></tr>
<tr><td>$\overline{WR}$
($R/\overline{W}$)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When $R/\overline{W}$ = “H”: Read.
When $R/\overline{W}$ = “L”: Write.</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU , this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
When $\overline{RD}$ = “H”: Enable.
When $\overline{RD}$ = “L”: Disable.</td></tr>
<tr><td>D0 - D7
(SCL)
(SI/SDA)</td><td>I/O
I
I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance.
When the I²C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDAI). At this time, D2 to D7 are set to high impedance.</td></tr>
</table>

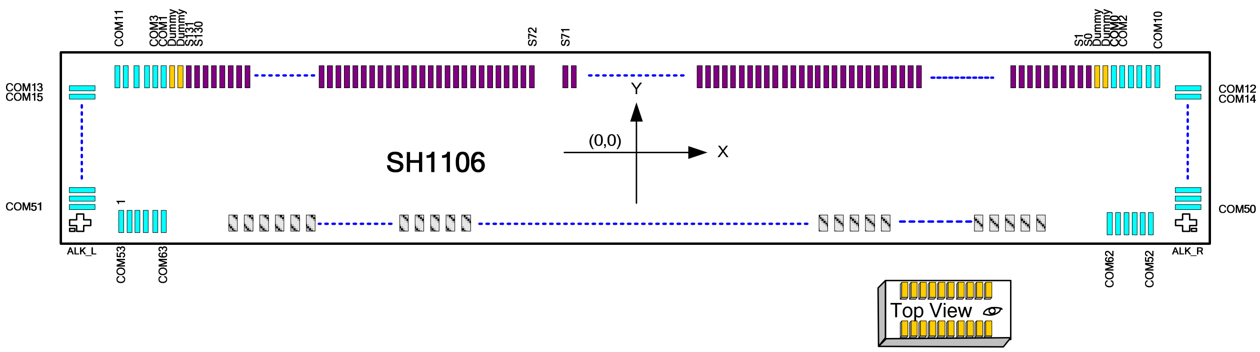
OLED Drive Pads

Symbol	I/O	Description
COM0,2, - 60, 62	O	These pads are even Common signal output for OLED display.
COM1,3 - 61,63	O	These pads are odd Common signal output for OLED display.
SEG0 - 131	O	These pads are Segment signal output for OLED display.

Test Pads

Symbol	I/O	Description
TEST1-3	I	Test pad, internal pull low, no connection for user.
Dummy	-	These pads are not used. Keep floating.

Pad Configuration



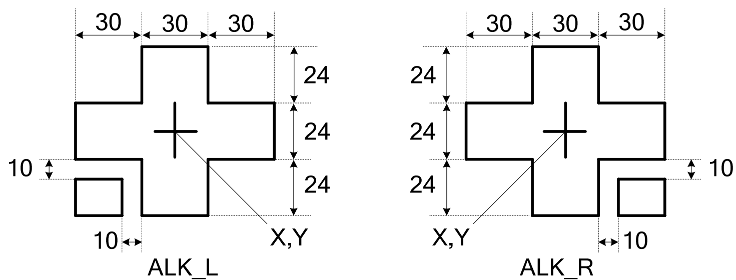
Chip Outline Dimensions

Item	Pad No.	Size (µm) X	Size (µm) Y
		X	Y
Chip boundary	-	5076	814
Chip height	All pads	300	
Bump size	I/O	40	80
	SEG	15	110
	COM	15	110
		110	15
Pad pitch	COM	30	
	SEG	30.75	
	I/O	55	
Bump height	All pads	9±2	

Alignment Mark Location

unit: µm

NO	X	Y
ALK_L	-2470	-348
ALK_R	2470	-348



Pad Location (Total: 266 pads)

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	COM53	-2287.62	-329	69	VCOMH	1721.81	-299.95	137	SEG30	1122.38	329	205	SEG98	-1030.12	329
2	COM55	-2257.62	-329	70	VCOMH	1776.81	-299.95	138	SEG31	1091.63	329	206	SEG99	-1060.87	329
3	COM57	-2227.62	-329	71	VPP	1831.81	-299.95	139	SEG32	1060.88	329	207	SEG100	-1091.62	329
4	COM59	-2197.62	-329	72	VPP	1886.81	-299.95	140	SEG33	1030.13	329	208	SEG101	-1122.37	329
5	COM61	-2167.62	-329	73	COM62	2137.62	-329	141	SEG34	999.38	329	209	SEG102	-1153.12	329
6	COM63	-2137.62	-329	74	COM60	2167.62	-329	142	SEG35	968.63	329	210	SEG103	-1183.87	329
7	C21N	-1688.19	-299.95	75	COM58	2197.62	-329	143	SEG36	937.88	329	211	SEG104	-1214.62	329
8	C21N	-1633.19	-299.95	76	COM56	2227.62	-329	144	SEG37	907.13	329	212	SEG105	-1245.37	329
9	C21N	-1578.19	-299.95	77	COM54	2257.62	-329	145	SEG38	876.38	329	213	SEG106	-1276.12	329
10	C21N	-1523.19	-299.95	78	COM52	2287.62	-329	146	SEG39	845.63	329	214	SEG107	-1306.87	329
11	C21P	-1468.19	-299.95	79	COM50	2460	-285	147	SEG40	814.88	329	215	SEG108	-1337.62	329
12	C21P	-1413.19	-299.95	80	COM48	2460	-255	148	SEG41	784.13	329	216	SEG109	-1368.37	329
13	C21P	-1358.19	-299.95	81	COM46	2460	-225	149	SEG42	753.38	329	217	SEG110	-1399.12	329
14	C21P	-1303.19	-299.95	82	COM44	2460	-195	150	SEG43	722.63	329	218	SEG111	-1429.87	329
15	C22P	-1248.19	-299.95	83	COM42	2460	-165	151	SEG44	691.88	329	219	SEG112	-1460.62	329
16	C22P	-1193.19	-299.95	84	COM40	2460	-135	152	SEG45	661.13	329	220	SEG113	-1491.37	329
17	C22P	-1138.19	-299.95	85	COM38	2460	-105	153	SEG46	630.38	329	221	SEG114	-1522.12	329
18	C22P	-1083.19	-299.95	86	COM36	2460	-75	154	SEG47	599.63	329	222	SEG115	-1552.87	329
19	C22N	-1028.19	-299.95	87	COM34	2460	-45	155	SEG48	568.88	329	223	SEG116	-1583.62	329
20	C22N	-973.19	-299.95	88	COM32	2460	-15	156	SEG49	538.13	329	224	SEG117	-1614.37	329
21	C22N	-918.19	-299.95	89	COM30	2460	15	157	SEG50	507.38	329	225	SEG118	-1645.12	329
22	C22N	-863.19	-299.95	90	COM28	2460	45	158	SEG51	476.63	329	226	SEG119	-1675.87	329
23	VDD2	-808.19	-299.95	91	COM26	2460	75	159	SEG52	445.88	329	227	SEG120	-1706.62	329
24	VDD2	-753.19	-299.95	92	COM24	2460	105	160	SEG53	415.13	329	228	SEG121	-1737.37	329
25	VDD2	-698.19	-299.95	93	COM22	2460	135	161	SEG54	384.38	329	229	SEG122	-1768.12	329
26	VDD2	-643.19	-299.95	94	COM20	2460	165	162	SEG55	353.63	329	230	SEG123	-1798.87	329
27	VBREF	-588.19	-299.95	95	COM18	2460	195	163	SEG56	322.88	329	231	SEG124	-1829.62	329
28	VPP	-533.19	-299.95	96	COM16	2460	225	164	SEG57	292.13	329	232	SEG125	-1860.37	329
29	VPP	-478.19	-299.95	97	COM14	2460	255	165	SEG58	261.38	329	233	SEG126	-1891.12	329
30	VCOMH	-423.19	-299.95	98	COM12	2460	285	166	SEG59	230.63	329	234	SEG127	-1921.87	329
31	VCOMH	-368.19	-299.95	99	COM10	2287.62	329	167	SEG60	199.88	329	235	SEG128	-1952.62	329
32	VSS(REF)	-313.19	-299.95	100	COM8	2257.62	329	168	SEG61	169.13	329	236	SEG129	-1983.37	329
33	VSS	-258.19	-299.95	101	COM6	2227.62	329	169	SEG62	138.38	329	237	SEG130	-2014.12	329
34	VSS	-203.19	-299.95	102	COM4	2197.62	329	170	SEG63	107.63	329	238	SEG131	-2044.87	329
35	VSS	-148.19	-299.95	103	COM2	2167.62	329	171	SEG64	76.88	329	239	DUMMY	-2075.62	329
36	VCL	-93.19	-299.95	104	COM0	2137.62	329	172	SEG65	46.13	329	240	DUMMY	-2105.62	329
37	VCL	-38.19	-299.95	105	DUMMY	2105.63	329	173	SEG66	15.38	329	241	COM1	-2137.62	329
38	VSL	16.81	-299.95	106	DUMMY	2075.63	329	174	SEG67	-15.37	329	242	COM3	-2167.62	329
39	VSL	71.81	-299.95	107	SEG0	2044.88	329	175	SEG68	-46.12	329	243	COM5	-2197.62	329
40	TEST1	126.81	-299.95	108	SEG1	2014.13	329	176	SEG69	-76.87	329	244	COM7	-2227.62	329
41	TEST2	181.81	-299.95	109	SEG2	1983.38	329	177	SEG70	-107.62	329	245	COM9	-2257.62	329
42	TEST3	236.81	-299.95	110	SEG3	1952.63	329	178	SEG71	-138.37	329	246	COM11	-2287.62	329
43	CL	291.81	-299.95	111	SEG4	1921.88	329	179	SEG72	-230.62	329	247	COM13	-2460	285
44	CLS	346.81	-299.95	112	SEG5	1891.13	329	180	SEG73	-261.37	329	248	COM15	-2460	255
45	VDD1	401.81	-299.95	113	SEG6	1860.38	329	181	SEG74	-292.12	329	249	COM17	-2460	225
46	VDD1	456.81	-299.95	114	SEG7	1829.63	329	182	SEG75	-322.87	329	250	COM19	-2460	195
47	IM1	511.81	-299.95	115	SEG8	1798.88	329	183	SEG76	-353.62	329	251	COM21	-2460	165
48	VSS	566.81	-299.95	116	SEG9	1768.13	329	184	SEG77	-384.37	329	252	COM23	-2460	135
49	IM2	621.81	-299.95	117	SEG10	1737.38	329	185	SEG78	-415.12	329	253	COM25	-2460	105
50	VDD1	676.81	-299.95	118	SEG11	1706.63	329	186	SEG79	-445.87	329	254	COM27	-2460	75
51	IM0	731.81	-299.95	119	SEG12	1675.88	329	187	SEG80	-476.62	329	255	COM29	-2460	45
52	VSS	786.81	-299.95	120	SEG13	1645.13	329	188	SEG81	-507.37	329	256	COM31	-2460	15
53	CSB	841.81	-299.95	121	SEG14	1614.38	329	189	SEG82	-538.12	329	257	COM33	-2460	-15
54	RESB	896.81	-299.95	122	SEG15	1583.63	329	190	SEG83	-568.87	329	258	COM35	-2460	-45
55	A0	951.81	-299.95	123	SEG16	1552.88	329	191	SEG84	-599.62	329	259	COM37	-2460	-75
56	VSS	1006.81	-299.95	124	SEG17	1522.13	329	192	SEG85	-630.37	329	260	COM39	-2460	-105
57	WRB	1061.81	-299.95	125	SEG18	1491.38	329	193	SEG86	-661.12	329	261	COM41	-2460	-135
58	RDB	1116.81	-299.95	126	SEG19	1460.63	329	194	SEG87	-691.87	329	262	COM43	-2460	-165
59	D0	1171.81	-299.95	127	SEG20	1429.88	329	195	SEG88	-722.62	329	263	COM45	-2460	-195
60	D1	1226.81	-299.95	128	SEG21	1399.13	329	196	SEG89	-753.37	329	264	COM47	-2460	-225
61	D2	1281.81	-299.95	129	SEG22	1368.38	329	197	SEG90	-784.12	329	265	COM49	-2460	-255
62	D3	1336.81	-299.95	130	SEG23	1337.63	329	198	SEG91	-814.87	329	266	COM51	-2460	-285
63	D4	1391.81	-299.95	131	SEG24	1306.88	329	199	SEG92	-845.62	329				
64	D5	1446.81	-299.95	132	SEG25	1276.13	329	200	SEG93	-876.37	329				
65	D6	1501.81	-299.95	133	SEG26	1245.38	329	201	SEG94	-907.12	329				
66	D7	1556.81	-299.95	134	SEG27	1214.63	329	202	SEG95	-937.87	329				
67	VSS	1611.81	-299.95	135	SEG28	1183.88	329	203	SEG96	-968.62	329				
68	IREF	1666.81	-299.95	136	SEG29	1153.13	329	204	SEG97	-999.37	329				

Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) or I^2C Interface can be selected by different selections of IM0~2 as shown in Table 1.

Table. 1

Interface	Config			Data signal								Control signal				
	IM0	IM1	IM2	D7	D6	D5	D4	D3	D2	D1	D0	E/$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
6800	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	E	R/$\overline{W}$	$\overline{CS}$	A0	$\overline{RES}$
8080	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
4-Wire SPI	0	0	0	Pull Low						SI	SCL	Pull Low			A0	$\overline{RES}$
3-Wire SPI	1	0	0	Pull Low						SI	SCL	Pull Low				$\overline{RES}$
I^2C	0	1	0	Pull Low						SDA	SCL	Pull Low			SA0	$\overline{RES}$

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. When $\overline{WR}$ (R/$\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ (R/$\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table. 2.

Table. 2

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	0	1	6800 microprocessor bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D0 to D7

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 1 below.

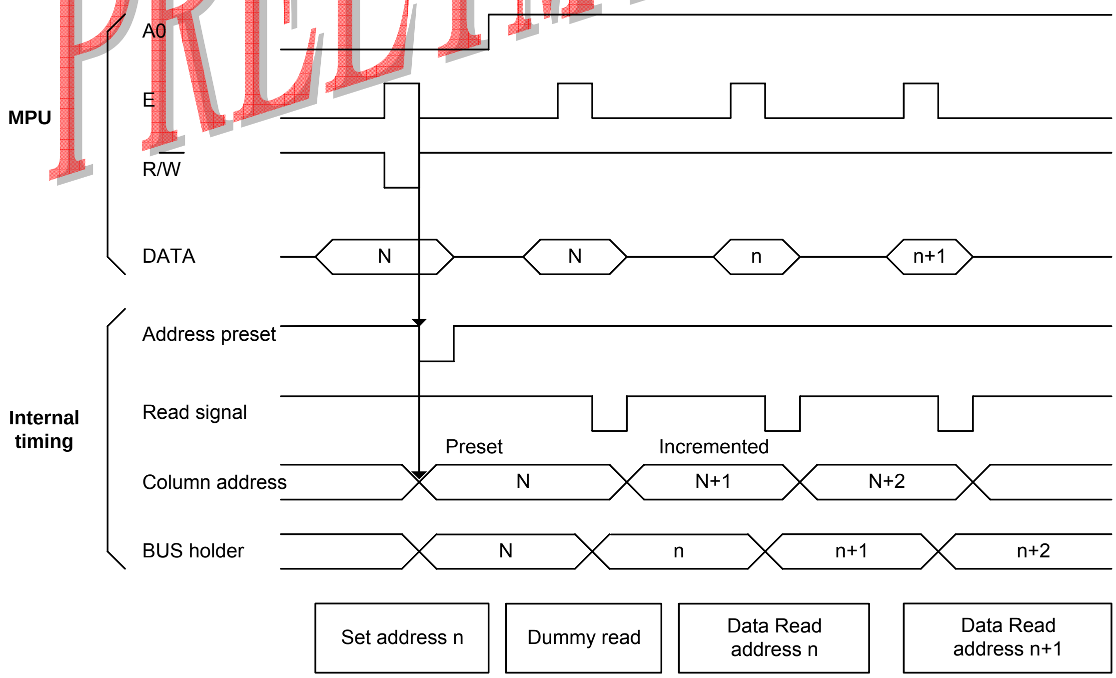


Figure. 1

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ ($R/\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by A0 signal. The $\overline{WR}$ ($R/\overline{W}$) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table. 3.

Table. 3

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	1	1	8080 microprocessor bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1106 identifies the data bus signal according to A0, $\overline{RD}$ (E) and $\overline{WR}$ ($R/\overline{W}$) signals.

Table. 4

Common	6800 processor	8080 processor		Function
A0	($R/\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM (A0=1) or command register (A0=0) in the same clock. See Figure. 2.

Table. 5

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	0	0	4-wire SPI	Pull Low	A0	-	-	SCL	SI	(HZ)

Note: "-" and Hz pin Must always be HIGH or LOW.

$\overline{CS}$ signal could always pull low in SPI-bus application.

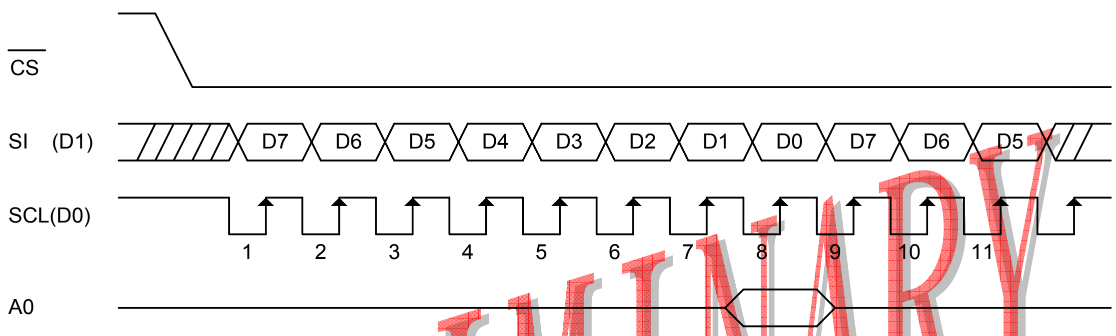


Figure. 2 4-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into an 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6, … and D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$=1) or command register ($D/\overline{C}$=0).

Table. 6

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
1	0	0	3-wire SPI	Pull Low	Pull Low	-	-	SCL	SI	(HZ)

Note: "-" and Hz pin Must always be HIGH or LOW.

$\overline{CS}$ signal could always pull low in SPI-bus application.

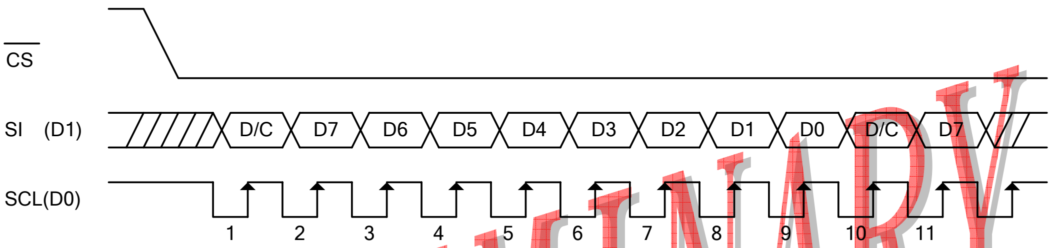


Figure. 2A -wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

I^2C-bus Interface

The SH1106 can transfer data via a standard I^2C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	1	0	I^2C Interface	Pull Low	SA0	-	-	SCL	SDA	(HZ)

Note: "-" and Hz pin Must always be HIGH or LOW.

$\overline{CS}$ signal could always pull low in I^2C-bus application.

Characteristics of the I^2C-bus

The I^2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of V_{DD1}.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

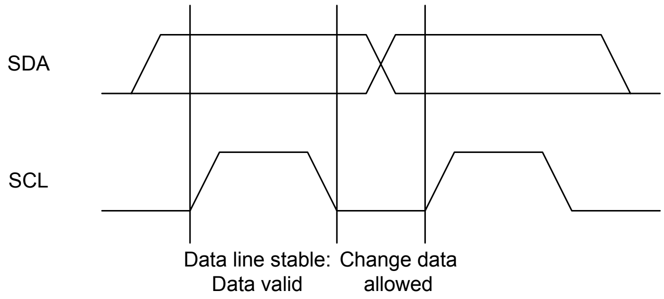


Figure. 3 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

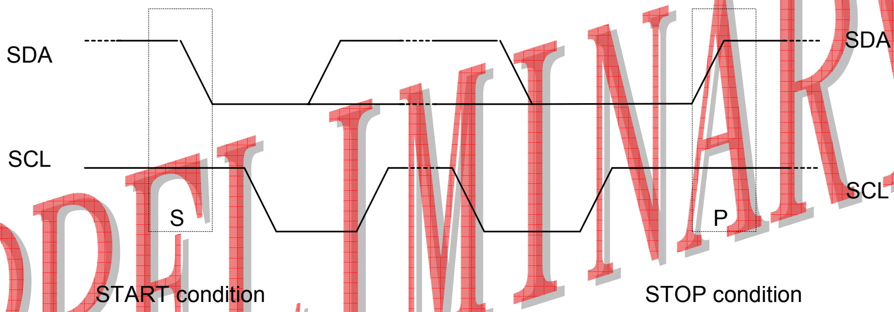


Figure. 4 Start and Stop conditions

System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

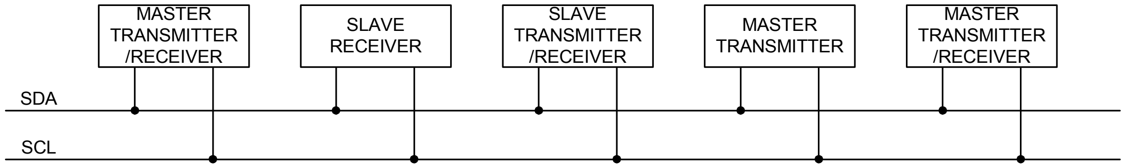


Figure. 5 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

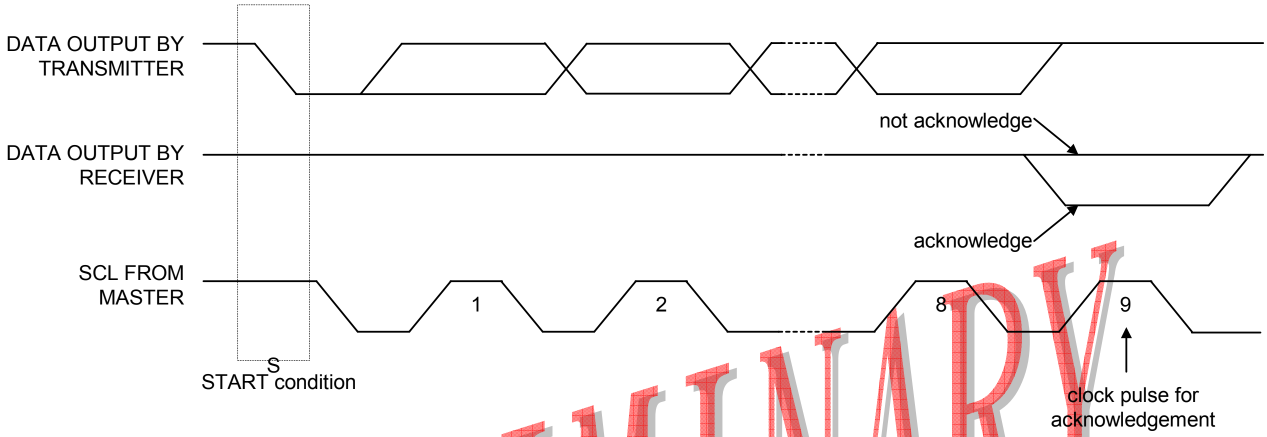


Figure 6 Acknowledge

Protocol

The SH1106 supports both read and write access. The R/$\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I^{2}C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SH1106. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1 (VDD1). The I^{2}C-bus protocol is illustrated in Fig.7. The sequence is initiated with a START condition (S) from the I^{2}C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^{2}C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$ (note1), plus a data byte (see Fig.7). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the D/$\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the D/$\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the D/$\overline{C}$ bit was set to ‘1’, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SH1106 device. If the D/$\overline{C}$ bit of the last control byte was set to ‘0’, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I^{2}C-bus master issues a stop condition (P). If the R/$\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the D/$\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

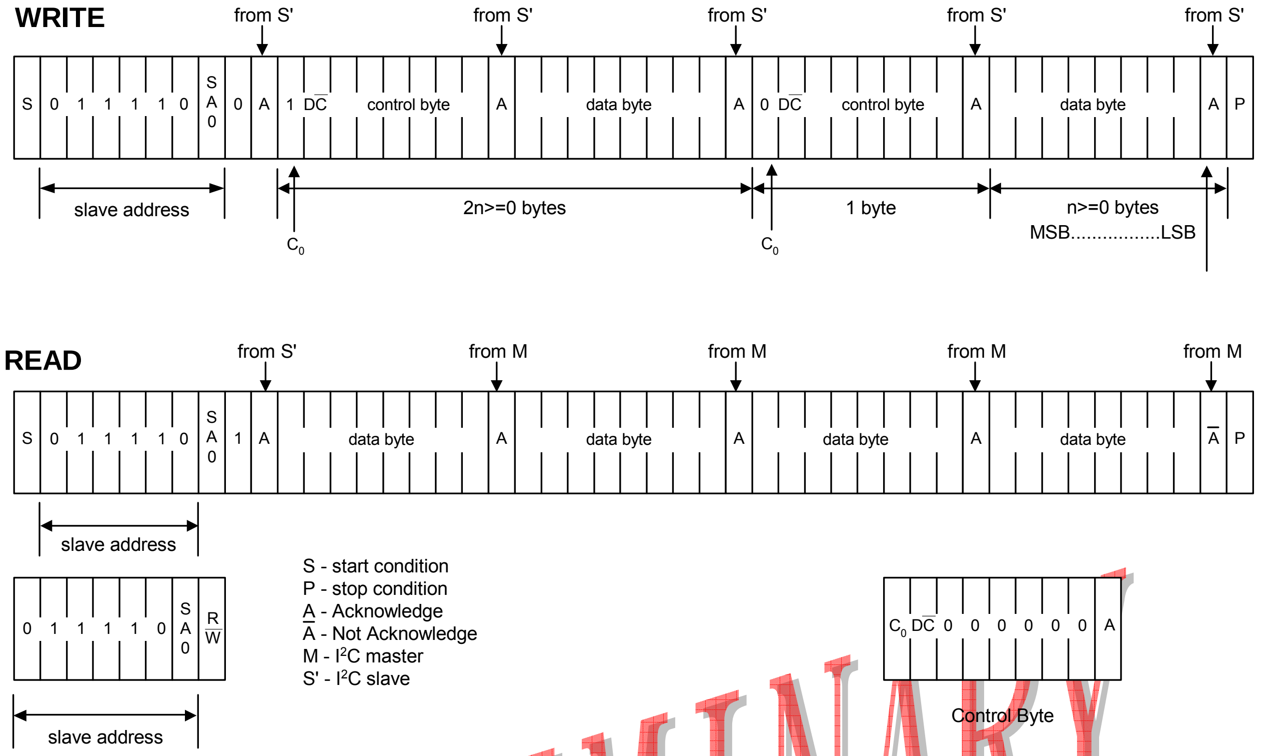


Figure 7 I²C Protocol

Note1:

1. Co＝ “0” : The last control byte , only data bytes to follow,
   Co＝ “1” : Next two bytes are a data byte and another control byte;
2. D/$\overline{\text{C}}$ ＝ “0” : The data byte is for command operation,
   D/$\overline{\text{C}}$ ＝ “1” : The data byte is for RAM operation.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = “H”, the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = “L”, the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 X 64 bits.

For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

The Page Address Circuit

As shown in Figure. 8, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Column Address

As shown in Figure. 8, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to re-specify both the page address and the column address.

Furthermore, as shown in Table. 7, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table. 7

Segment Output	SEG0		SEG131
ADC "0"	0 (H) →	Column Address	→ 83 (H)
ADC "1"	83 (H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Figure. 8, specifies the line address relating to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for SH1106, when the common output mode is reversed. The display area is a 64-line area for the SH1106 from the display start line address.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. that can be performed relationship between display data RAM and address (if initial display line is 1DH).

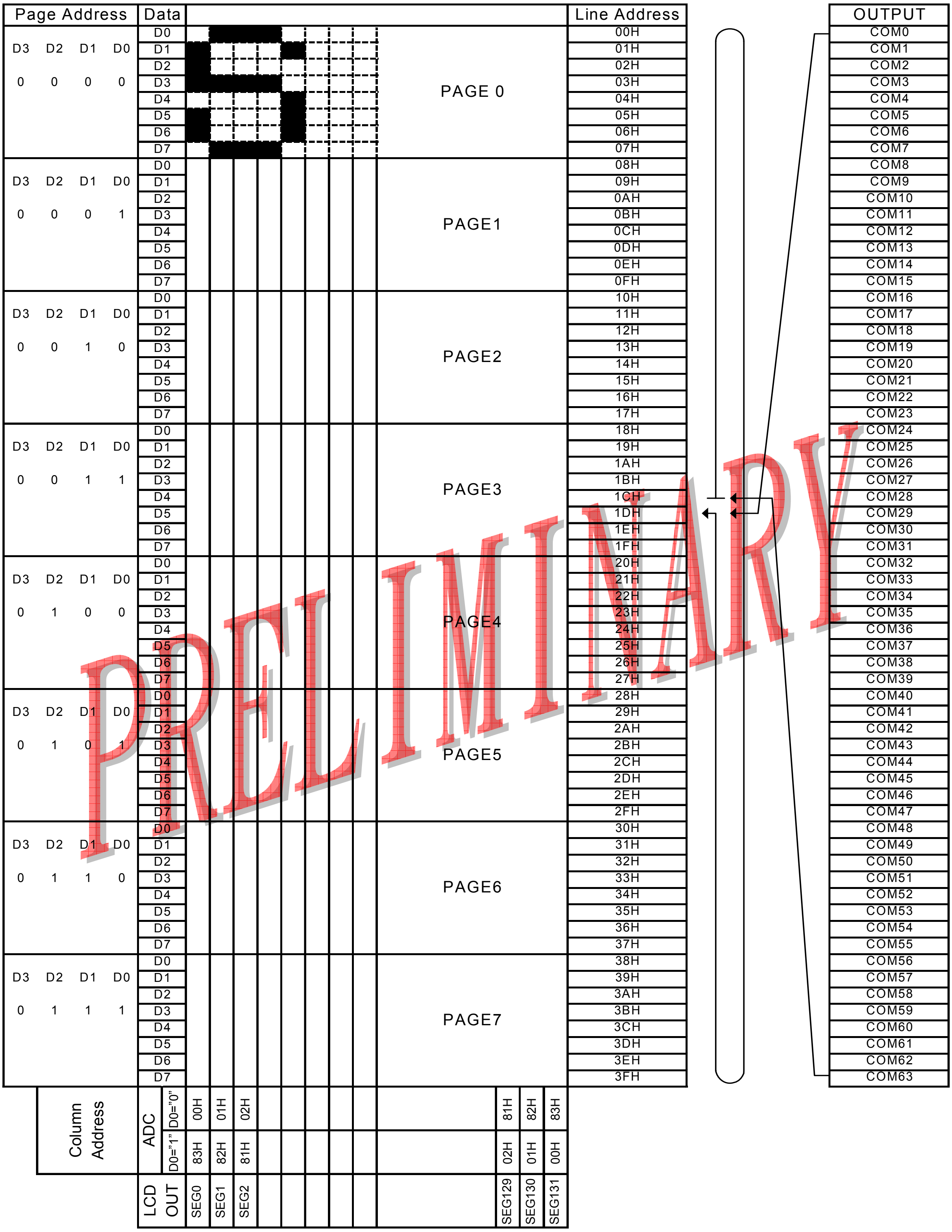

Page Address
Data
Line Address
OUTPUT
D3 D2 D1 D0
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
D0 D1 D2 D3 D4 D5 D6 D7
PAGE 0
PAGE1
PAGE2
PAGE3
PAGE4
PAGE5
PAGE6
PAGE7
00H 01H 02H 03H 04H 05H 06H 07H 08H 09H 0AH 0BH 0CH 0DH 0EH 0FH
10H 11H 12H 13H 14H 15H 16H 17H 18H 19H 1AH 1BH 1CH 1DH 1EH 1FH
20H 21H 22H 23H 24H 25H 26H 27H 28H 29H 2AH 2BH 2CH 2DH 2EH 2FH
30H 31H 32H 33H 34H 35H 36H 37H 38H 39H 3AH 3BH 3CH 3DH 3EH 3FH
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15
COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31
COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39 COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47
COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55 COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63
Column Address
ADC
D0="0"
00H 01H 02H 81H 82H 83H
D0="1"
83H 82H 81H 02H 01H 00H
LCD OUT
SEG0 SEG1 SEG2 SEG129 SEG130 SEG131

Figure. 8

The Oscillator Circuit

This is a RC type oscillator (Figure. 9) that produces the display clock. The oscillator circuit is only enabled when CLS = "H". When CLS = "L", the oscillation stops and the display clock is inputted through the CL terminal.

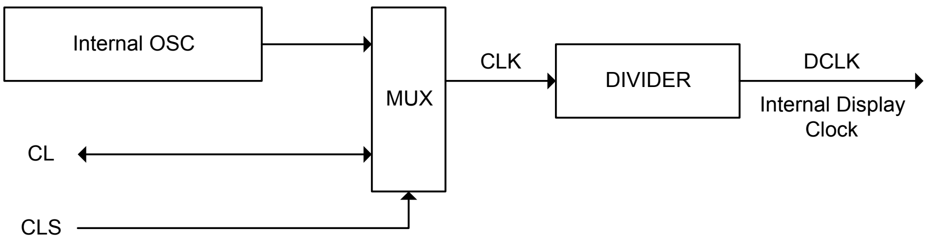


Figure. 9

Charge Pump Regulator

This block accompanying only 2 external capacitors, is used to generate a 9.0V voltage for OLED panel. This regulator can be turned ON/OFF by software command 8Bh setting.

Charge Pump output voltage control

This block is used to set the voltage value of charger pump output. The driving voltage can be adjusted from 6.4V up to 9.0V. This used to meet different demand of the panel.

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. VPP and VDD2 are external power supplies. IREF is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 132 current sources to drive OLED panel. The driving current can be adjusted up to 200μA with 256 steps. Common drivers generate voltage scanning pulses.

Reset Circuit

When the $\overline{\text{RES}}$ input falls to "L", these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 132 X 64 Display mode.
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM line address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.

Commands

The SH1106 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/$\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address: (00H - 0FH)
2. Set Higher Column Address: (10H - 1FH)

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
			:					:
1	0	0	0	0	0	1	1	131

Note: Don't use any commands not mentioned above.

3. Set Pump voltage value: (30H~33H)

Specifies output voltage (V_{PP}) of the internal charger pump.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	0	A1	A0

A1	A0	Pump output voltage (V_{PP})
0	0	6.4
0	1	7.4
1	0	8.0(Power on)
1	1	9.0

4. Set Display Start Line: (40H - 7FH)

Specifies line address (refer to Figure. 8) to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

5. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: ISEG = α/256 X IREF X scale factor

Where: α is contrast step; IREF is reference current equals 10μA; Scale factor = 32.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.
When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	ISEG
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	1	0	
0	1	0	0	0	0	0	0	0	1	1	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

6. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of Figure. 8. When display data is written or read, the column address is incremented by 1 as shown in Figure. 1.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = “L”, the right rotates (normal direction). (POR)

When ADC = “H”, the left rotates (reverse direction).

7. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = “L”, the normal display status is provided. (POR)

When D = “H”, the entire display ON status is provided.

8. Set Normal/Reverse Display: (A6H -A7H)

Reverses the display ON/OFF status without rewriting the contents of the display data RAM.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = “L”, the RAM data is high, being OLED ON potential (normal display). (POR)

When D = “H”, the RAM data is low, being OLED ON potential (reverse display)

9 Set Multiplex Ration: (Double Bytes Command)

This command switches default 64 multiplex modes to any multiplex ratio from 1 to 64. The output pads COM0-COM63 will be switched to corresponding common signal.

- Multiplex Ration Mode Set: (A8H)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

- Multiplex Ration Data Set: (00H - 3FH)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	*	*	0	0	0	0	0	0	1
0	1	0	*	*	0	0	0	0	1	0	2
0	1	0	*	*	0	0	0	0	1	1	3
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	63
0	1	0	*	*	1	1	1	1	1	1	64 (POR)

10. Set DC-DC OFF/ON: (Double Bytes Command)

This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then display ON command. The panel display must be off while issuing this command.

- DC-DC Control Mode Set: (ADH)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

- DC-DC ON/OFF Mode Set: (8AH - 8BH)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	1	0	1	D

When D = “L”, DC-DC is disable.

When D = “H”, DC-DC will be turned on when display on. (POR)

Table. 8

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External VPP must be used.
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display

11. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	E $\overline{RD}$	R / $\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = “L”, Display OFF OLED. (POR)

When D = “H”, Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

1) Stops the oscillator circuit and DC-DC circuit.
2) Stops the OLED drive and outputs HZ as the segment/common driver output.
3) Holds the display data and operation mode provided before the start of the sleep mode.
4) The MPU can access to the built-in display RAM.

12. Set Page Address: (B0H - B7H)

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

A0	E $\overline{RD}$	R / $\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

Note: Don’t use any commands not mentioned above for user.

13. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = “L”, Scan from COM0 to COM [N -1]. (POR)

When D = “H”, Scan from COM [N -1] to COM0.

14. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-63 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (64-16), so the second byte should be 100000.

- Display Offset Mode Set: (D3H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

- Display Offset Data Set: (00H~3FH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	*	*	0	0	0	0	0	0	0 (POR)
0	1	0	*	*	0	0	0	0	1	0	1
0	1	0	*	*	0	0	0	0	1	1	2
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	62
0	1	0	*	*	1	1	1	1	1	1	63

Note: “*” stands for “Don’t care”

15. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

- Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

- Divide Ratio/Oscillator Frequency Data Set: (00H - 3FH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

A3 - A0 defines the divide ration of the display clocks (DCLK). Divide Ration = A[3:0]+1.

A3	A2	A1	A0	Divide Ration
0	0	0	0	1 (POR)
		:		:
1	1	1	1	16

A7 - A4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A7	A6	A5	A4	Oscillator Frequency of *f*osc
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	*f*osc (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

16. Set Dis-charge/Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

- Pre-charge Period Mode Set: (D9H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

- Dis-charge/Pre-charge Period Data Set: (00H - FFH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

Pre-charge Period Adjust: (A3 - A0)

A3	A2	A1	A0	Pre-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Dis-charge Period Adjust: (A7 - A4)

A7	A6	A5	A4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

17. Set Common pads hardware configuration: (Double Bytes Command)

This command is to set the common signals pad configuration (sequential or alternative) to match the OLED panel hardware layout

- Common Pads Hardware Configuration Mode Set: (DAH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	0

- Sequential/Alternative Mode Set: (02H - 12H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	D	0	0	1	0

When D = “L”, Sequential.

COM31, 30 - 1, 0	SEG0, 1 - 130, 131	COM32, 33 - 62, 63

When D = “H”, Alternative. (POR)

COM62, 60 - 2, 0	SEG0, 1 - 130, 131	COM1, 3 - 61, 63

18. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

- VCOM Deselect Level Mode Set: (DBH)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

- VCOM Deselect Level Data Set: (00H - FFH)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{COM} = \beta \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β	A[7:0]	β
00H	0.430	20H	
01H		21H	
02H		22H	
03H		23H	
04H		24H	
05H		25H	
06H		26H	
07H		27H	
08H		28H	
09H		29H	
0AH		2AH	
0BH		2BH	
0CH		2CH	
0DH		2DH	
0EH		2EH	
0FH		2FH	
10H		30H	
11H		31H	
12H		32H	
13H		33H	
14H		34H	
15H		35H	0.770 (POR)
16H		36H	
17H		37H	
18H		38H	
19H		39H	
1AH		3AH	
1BH		3BH	
1CH		3CH	
1DH		3DH	
1EH		3EH	
1FH		3FH	
40H - FFH	1		

19. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

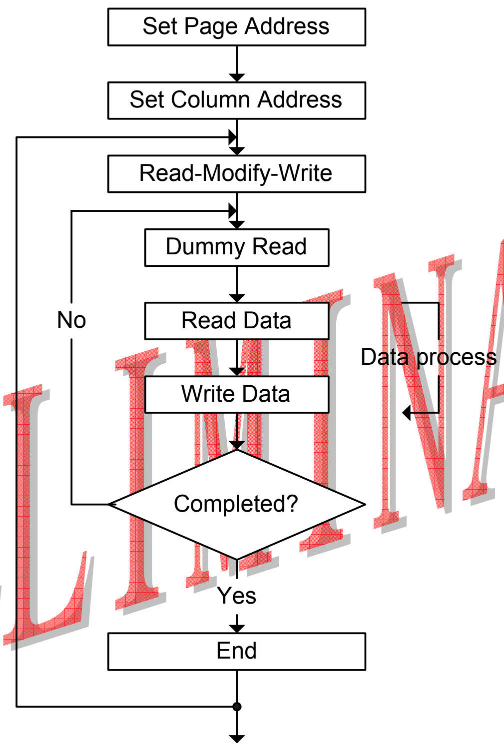


Figure. 10

20. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

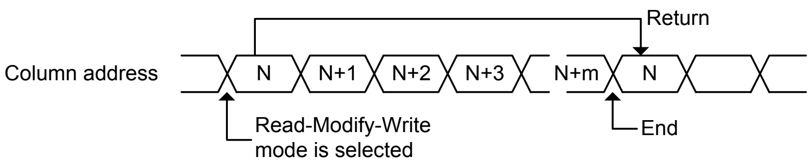


Figure. 11

21. NOP: (E3H)

Non-Operation Command.

A0	E $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

23. Read Status

A0	E $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	*	*	*	0	0	0

BUSY: When high, the SH1106 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

24. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Set Pump voltage value	0	1	0	0	0	1	1	0	0	Pump voltage value		This command is to control the DC-DC voltage output value. (POR=32H)
4. Set Display Start Line	0	1	0	0	1	Line address						Specifies RAM display line for COM0. (POR = 40H)
5. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display.
Contrast Data Register Set	0	1	0	Contrast Data								The chip has 256 contrast steps from 00 to FF. (POR = 80H)
6. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
7. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
8. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
9 Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
Multiplex Ration Data Set	0	1	0	*	*	Multiplex Ratio						
10. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	1	0	1	D	

Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
11. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
12. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
13. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
14. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H)
Display Offset Data Set	0	1	0	*	*	COMx						
15. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
16. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
17. Common Pads Hardware Configuration Mode Set	0	1	0	1	1	0	1	1	0	1	0	This command is to set the common signals pad configuration. (POR = 12H)
Sequential/Alternative Mode Set	0	1	0	0	0	0	D	0	0	1	0	
18. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM (β X VREF)								
19. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
20. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
21. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
22. Write Display Data	1	1	0	Write RAM data								
23. Read Status	0	0	1	BUSY	ON/ OFF	*	*	*	0	0	0	
24. Read Display Data	1	0	1	Read RAM data								

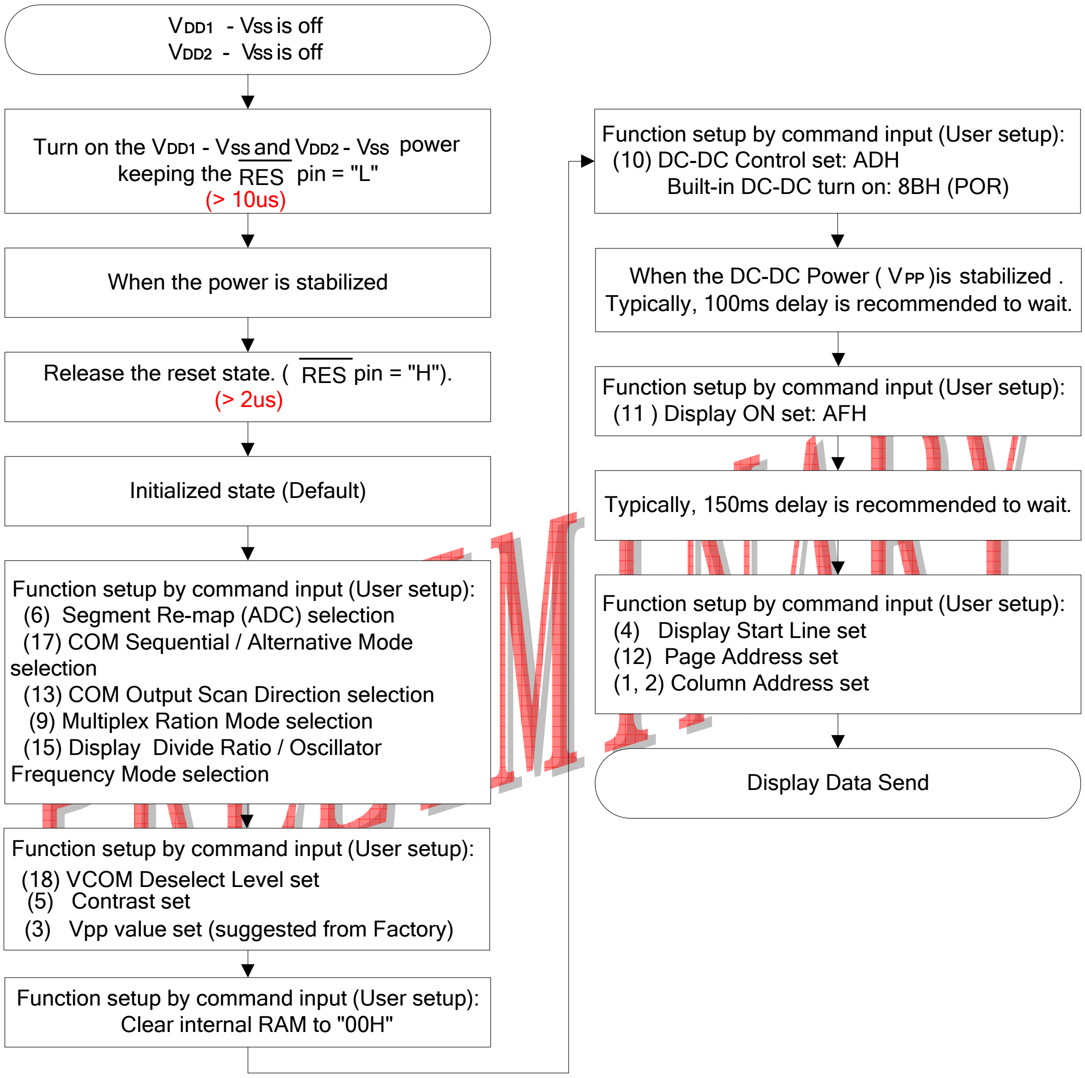
Note: Do not use any other command, or the system malfunction may result.

Command Description

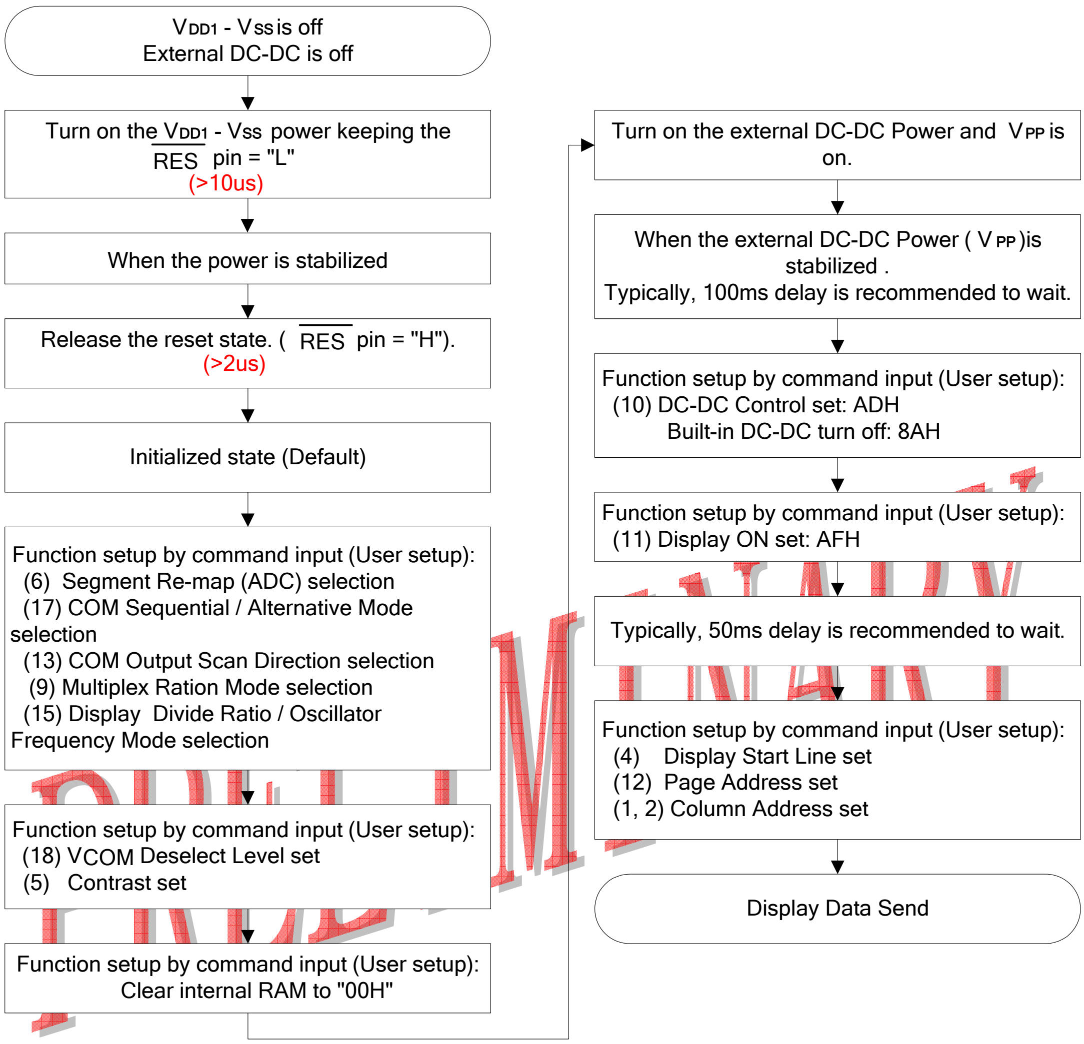
Instruction Setup: Reference

1. Power On and Initialization

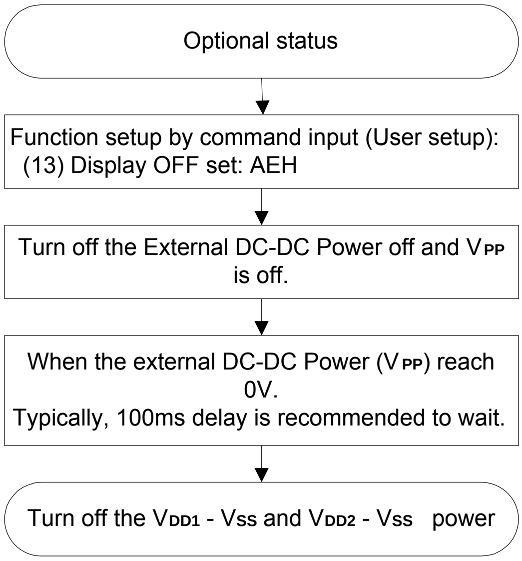
1.1. When the built-in DC-DC pump power is being used immediately after turning on the power:



1.2.When the external DC-DC pump power is being used immediately after turning on the power:



2. Power Off


Optional status
Function setup by command input (User setup):
(13) Display OFF set: AEH
Turn off the External DC-DC Power off and V_{PP} is off.
When the external DC-DC Power (V_{PP}) reach 0V.
Typically, 100ms delay is recommended to wait.
Turn off the V_{DD1} - V_{SS} and V_{DD2} - V_{SS} power

Absolute Maximum Rating*

DC Supply Voltage (V_{DD1}) . . . . -0.3V to +3.6V

DC Supply Voltage (V_{DD2}) . . . . -0.3V to +4.3V

DC Supply Voltage (V_{PP}) . . . . -0.3V to +13.5V

Input Voltage . . . . -0.3V to V_{DD1} + 0.3V

Operating Ambient Temperature . . . . -40°C to +85°C

Storage Temperature . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (V_{SS} = 0V, V_{DD1} = 1.65 - 3.5V T_A =+25°C, unless otherwise specified)

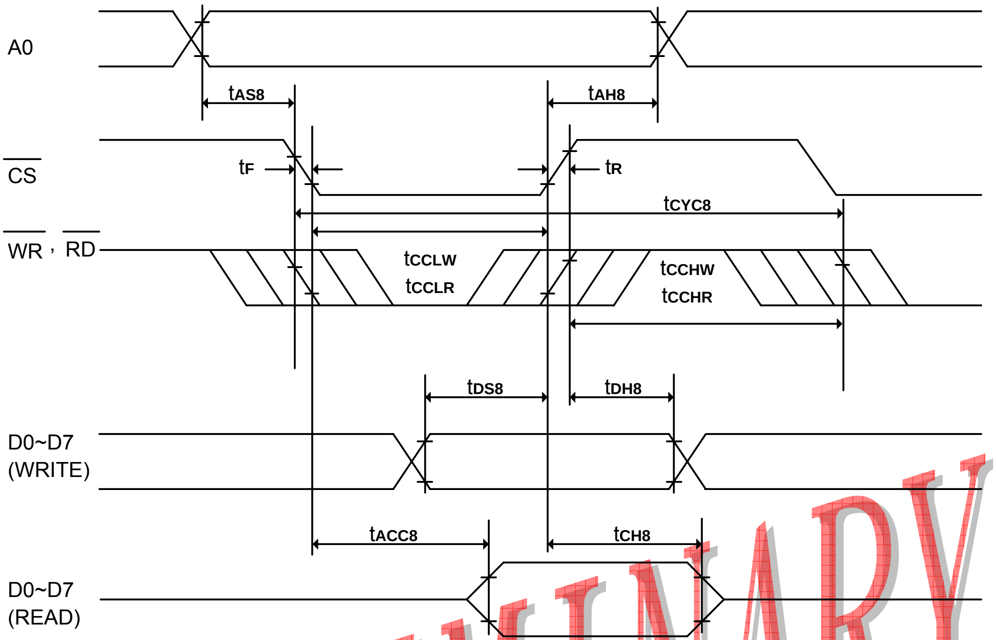
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD1}	Operating voltage	1.65	-	3.5	V	
V_{DD2}	Operating voltage	3.0	-	4.2	V	
V_{PP}	OLED Operating voltage	6.4		13.0	V	
I_{DD1}	Dynamic current consumption 1	-	-	110	μA	V_{DD1} = 3V, V_{DD2} = 3.7V, I_{REF} = 12.5μA, Contrast α = 256, Internal charge pump OFF, Display ON, display data = All ON, No panel attached.
I_{DD2}	Dynamic current consumption 2	-	-	2	mA	V_{DD1} = 3V, V_{DD2} =3.7V, I_{REF} = -12.5μA, Contrast α = 256, internal charge pump ON, Display ON, Display data = All ON, No panel attached.
I_{PP}	OLED dynamic current consumption	-	-	1.5	mA	V_{DD1} = 3V, V_{DD2} = 3.7V, V_{PP} =9V(external), I_{REF} = -12.5μA, Contrast α = 256, Display ON, display data = All ON, No panel attached.
I_{SP}	Sleep mode current consumption in V_{DD1} & V_{DD2}	-	-	5	μA	During sleep, T_A = +25°C, V_{DD1} = 3V, V_{DD2} = 3V.
	Sleep mode current consumption in V_{PP}	-	-	5	μA	During sleep, T_A = +25°C, V_{PP} = 9V (External)
I_{SEG}	Segment output current	-	-200	-	μA	V_{DD1} = 3V, V_{PP} = 9V, I_{REF} = -12.5μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 256.
		-	-25	-	μA	V_{DD1} = 3V, V_{PP} = 9V, I_{REF} = -12.5μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 32.
ΔI_{SEG1}	Segment output current uniformity	-	-	±3	%	ΔI_{SEG1} = (I_{SEG} - I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [0:131] at contrast α = 256.
ΔI_{SEG2}	Adjacent segment output current uniformity	-	-	±2	%	ΔI_{SEG2} = (I_{SEG} [N] - I_{SEG} [N+1])/(I_{SEG} [N] + I_{SEG} [N+1]) X 100% I_{SEG} [0:131] at contrast α = 256.

DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.8 X V_{DD1}	-	V_{DD1}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, IM0~2 and $\overline{RES}$.
V_{ILC}	Low-level input voltage	Vss	-	0.2 X V_{DD1}	V	
V_{OHC}	High-level output voltage	0.8 X V_{DD1}	-	V_{DD1}	V	I_{OH} = -0.5mA (D0 - D7, and CL).
V_{OLC}	Low -level output voltage	Vss	-	0.2 X V_{DD1}	V	I_{OL} = 0.5mA (D0, D2 - D7, and CL)
V_{OLCS}	SDA low -level output voltage	Vss	-	0.2 X V_{DD1}	V	VDD1<2V; I_{OL}=3mA (SDA)
				0.4		VDD1>2V
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD1} or Vss (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, IM0~2 and $\overline{RES}$).
I_{HZ}	HZ leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance.
fosc	Oscillation frequency	315	360	420	kHz	T_A = +25°C.
f_{FRM}	Frame frequency for 64 Commons	-	104	-	Hz	When fosc = 360kHz, Divide ratio = 1, common width = 54 DCLKs.

AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



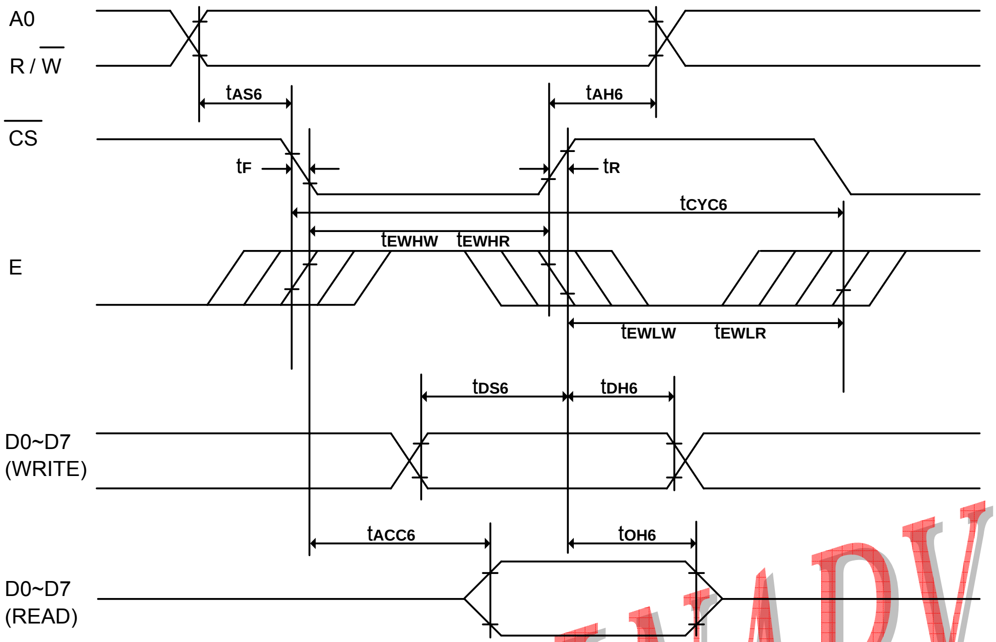
(VDD1 = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	600	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	80	-	-	ns	
t_{DH8}	Data hold time	30	-	-	ns	
t_{CH8}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	280	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	200	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	240	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	200	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	15	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



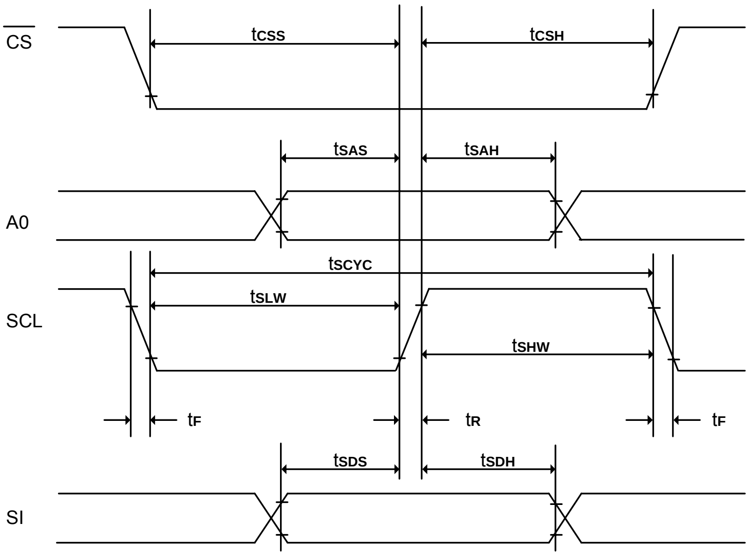
(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	600	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	80	-	-	ns	
t_{DH6}	Data hold time	30	-	-	ns	
t_{OH6}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	200	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	240	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	200	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	15	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(3) System buses Write characteristics 3 (For 4 wire SPI)



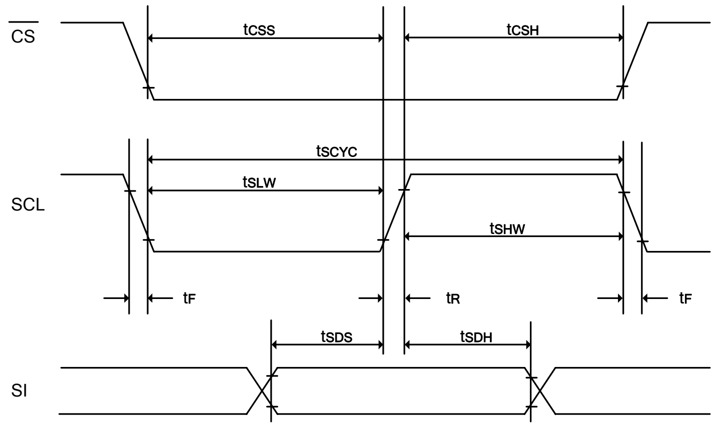
(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SAS}	Address setup time	300	-	-	ns	
t_{SAH}	Address hold time	300	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SAS}	Address setup time	150	-	-	ns	
t_{SAH}	Address hold time	150	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(4) System buses Write characteristics 4(For 3 wire SPI)



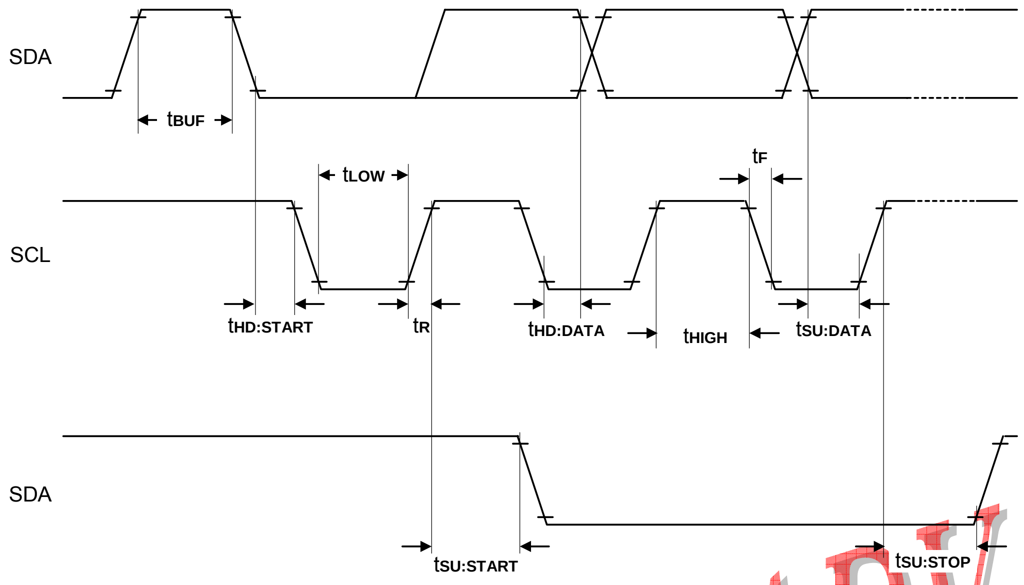
(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

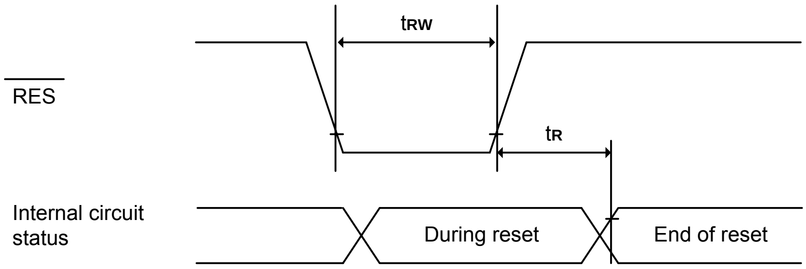
(5) I²C interface characteristics



(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	uS	
THIGH	SCL clock H pulse width	0.6	-	-	uS	
TSU:DATA	data setup time	100	-	-	nS	
THD:DATA	data hold time	0	-	0.9	uS	
TR	SCL，SDA rise time	20+0.1Cb	-	300	nS	
TF	SCL，SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
TSU:START	Setup timefor re-START	0.6	-	-	uS	
THD:START	START Hold time	0.6	-	-	uS	
TSU:STOP	Setup time for STOP	0.6	-	-	uS	
TBUF	Bus free times between STOP and START condition	1.3	-	-	uS	

(6) Reset Timing



(V_{DD1} = 1.65 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	µs	
t_{RW}	Reset low pulse width	10.0	-	-	µs	

(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	1.0	µs	
t_{RW}	Reset low pulse width	5.0	-	-	µs	

Application Circuit (for reference only)

Reference Connection to MPU:

1. 8080 series interface: (Internal oscillator, Built-in DC-DC)

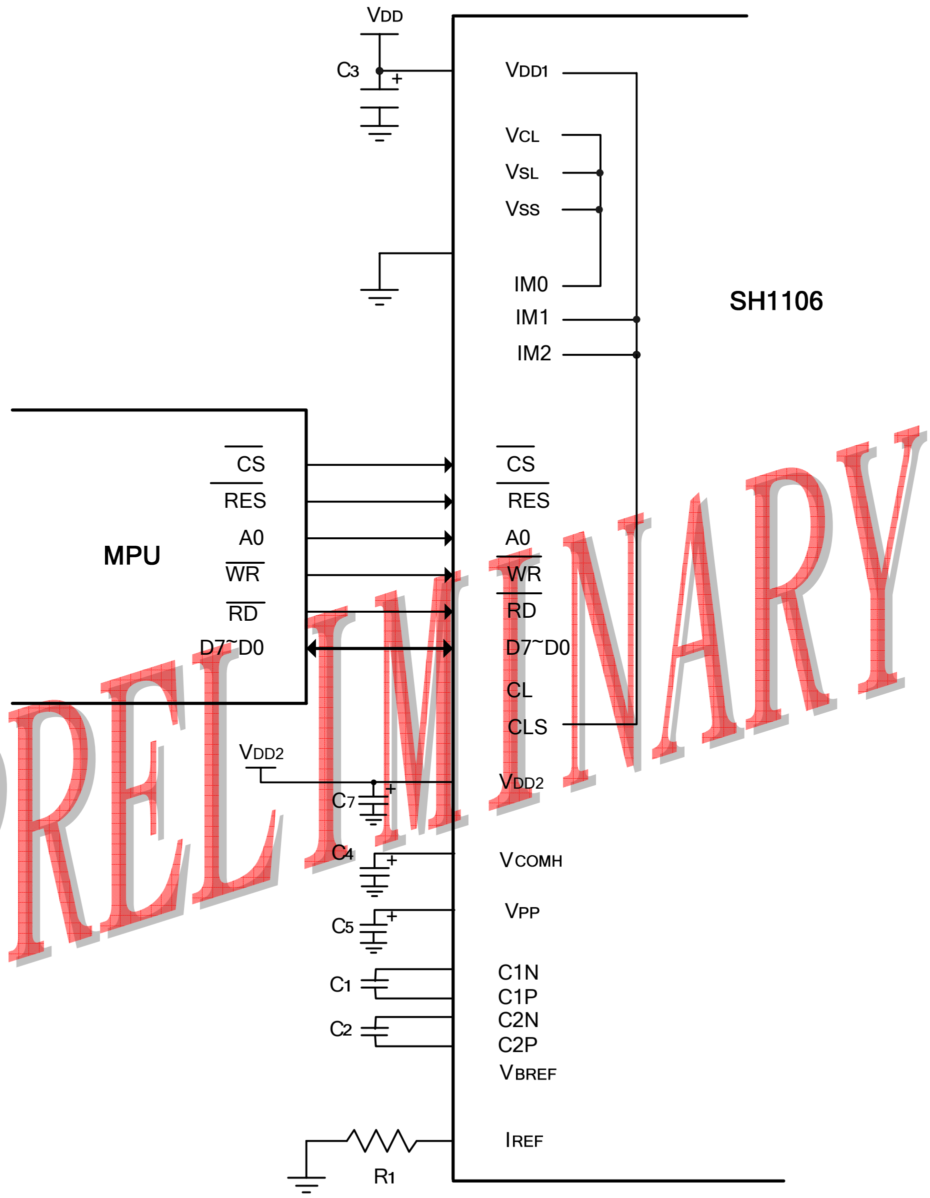


Figure. 12

Note:

C_3 - C_5, C_7: 4.7µF. C_1, C_2 : 0.22 ~ 1µF.
R_1: about 510kΩ, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

2. 6800 Series Interface: (Internal oscillator, Built-in DC-DC)

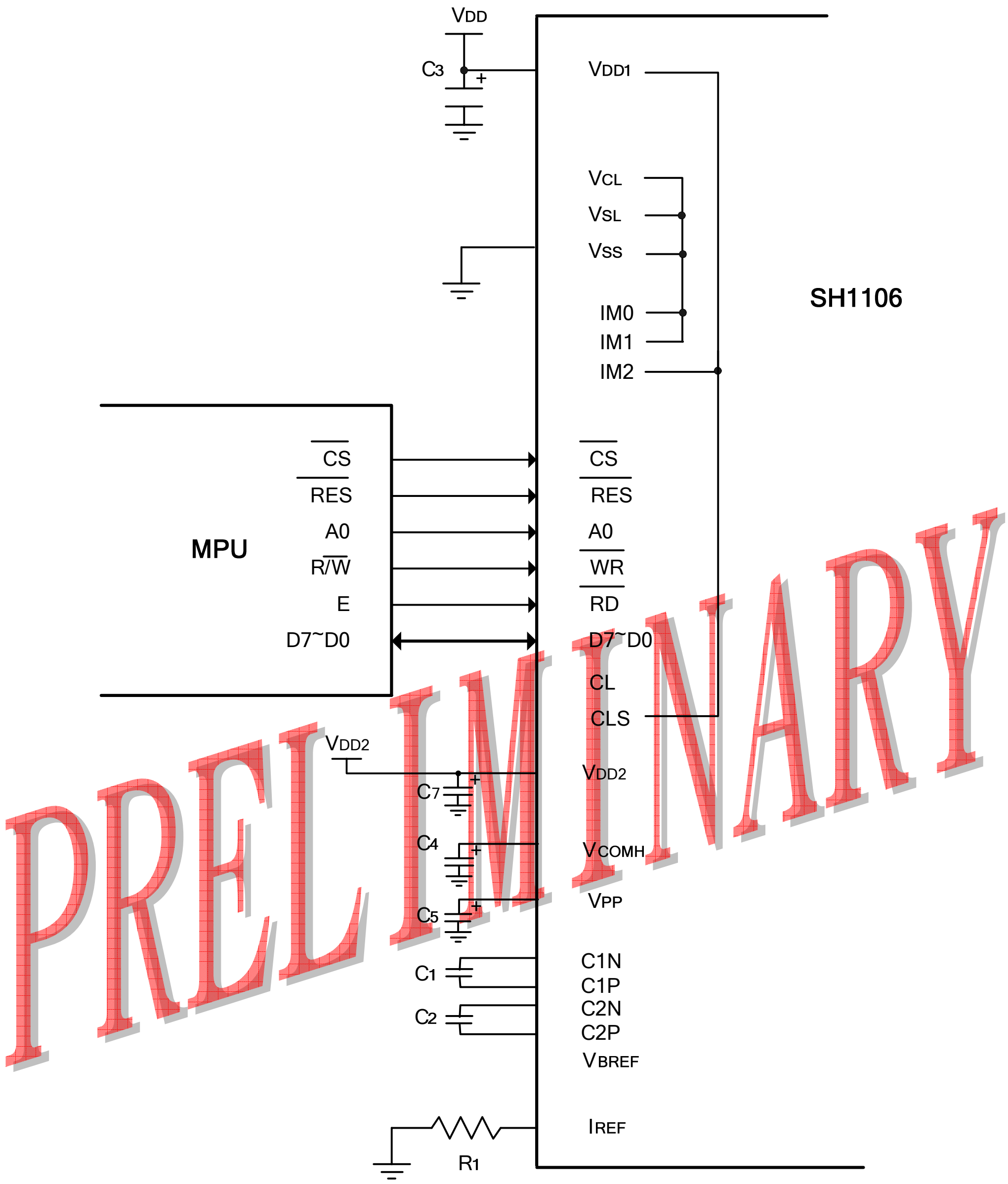


Figure. 13

Note:
C_3 - C_5, C_7: 4.7µF. C_1, C_2 : 0.22 ~1µF
R_1: about 510kΩ, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

3. Serial Interface(3-wire or 4-wire SPI): (External oscillator, External VPP , Max 13.0V)

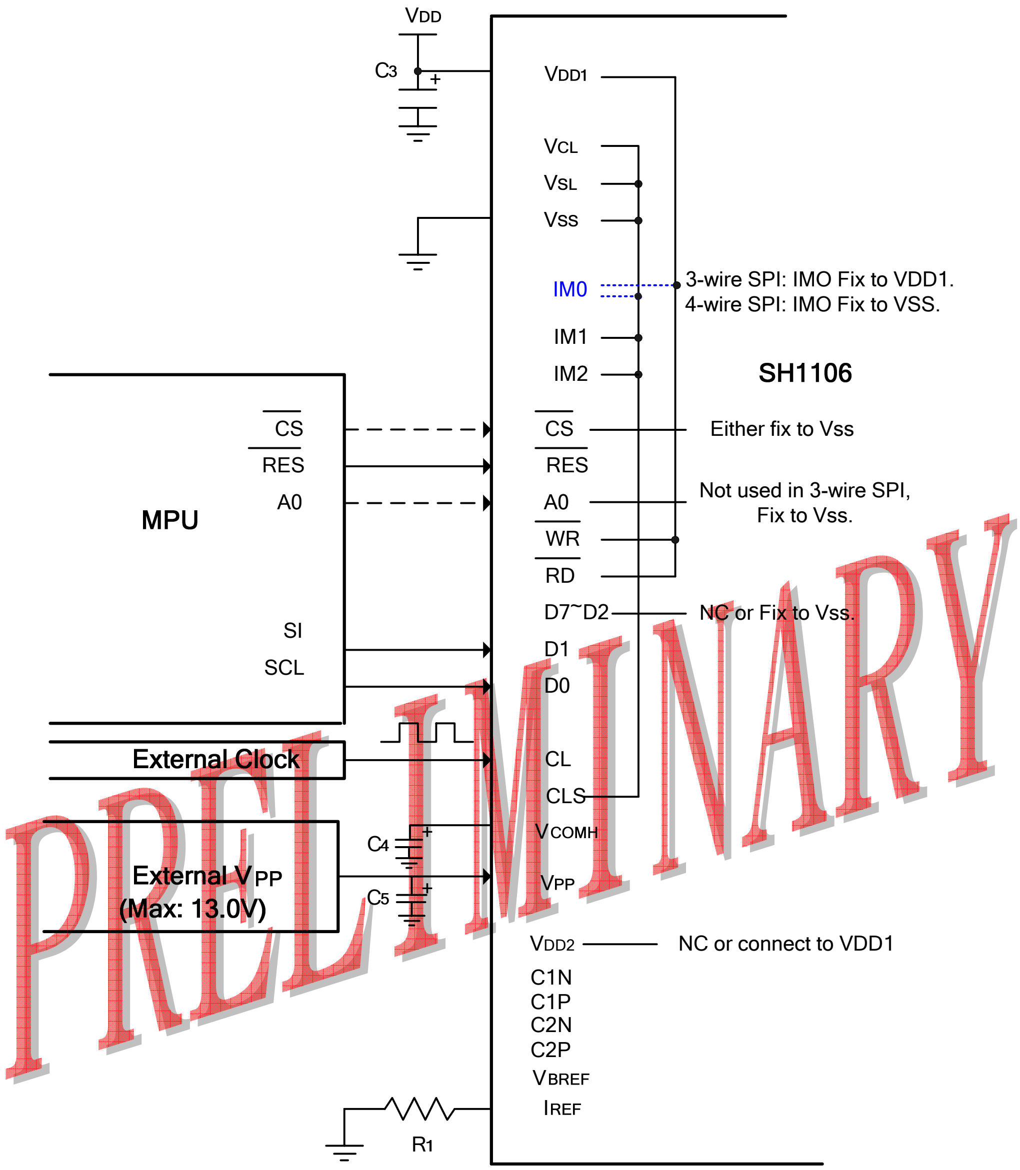


Figure. 14

Note:

C3 - C5: 4.7µF
R1: about 510kΩ, R1 = (Voltage at IREF - Vss)/IREF

$\overline{\text{WR}}$ and $\overline{\text{RD}}$ are not used in SPI mode, should fix to VSS or VDD1.

$\overline{\text{CS}}$ can fix to VSS in SPI mode.

4. I^{2}C Interface: (Internal oscillator, Built-in DC-DC)

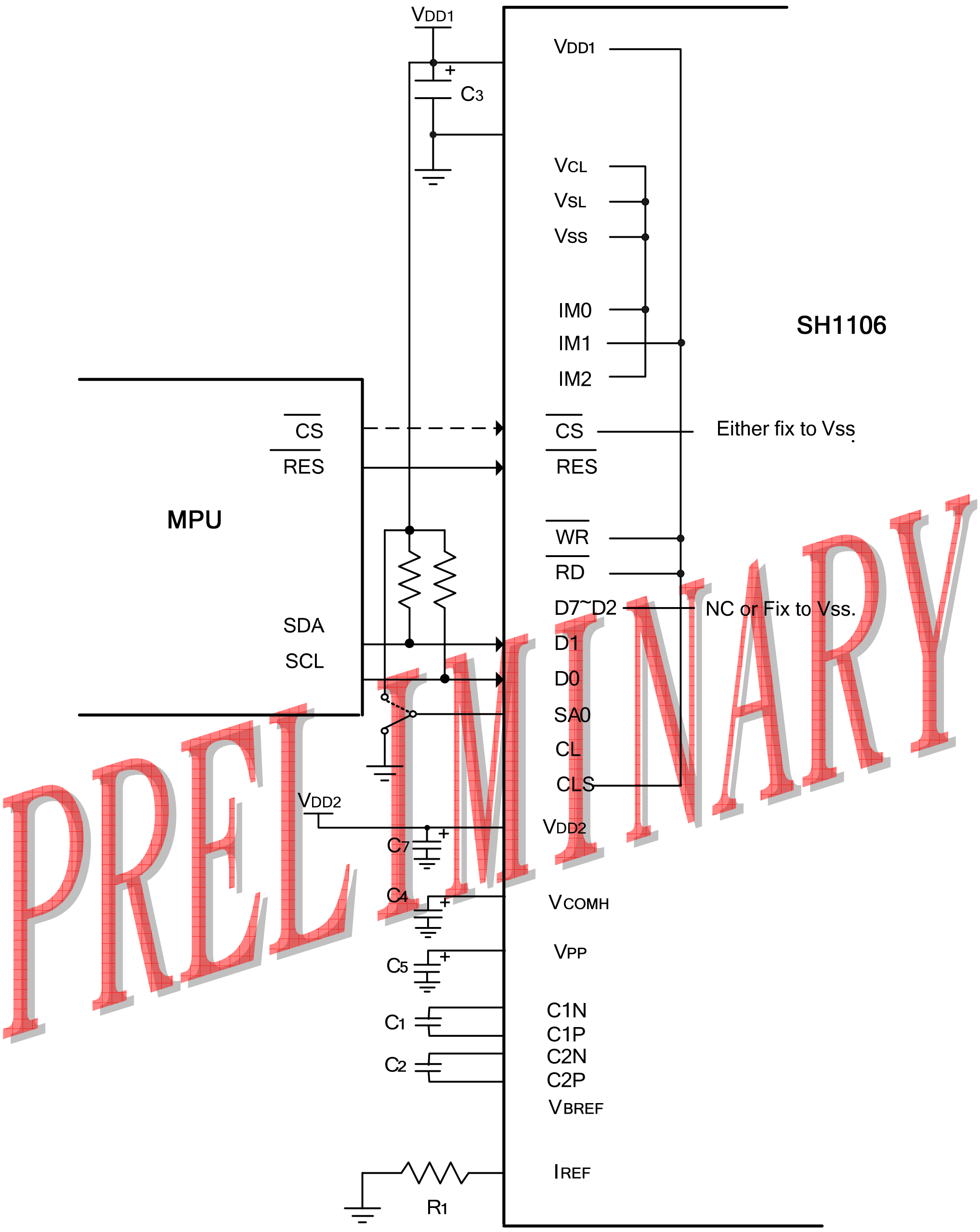


Figure. 15

Note:

C3 - C5, C7: 4.7µF. C1, C2: 0.22 ~1µF.
R1: about 510kΩ, R1 = (Voltage at IREF - Vss)/IREF
The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(VSS) or 1 (VDD1).
WR and RD are not used in I^{2}C mode, should fix to VSS or VDD1.
CS can fix to VSS in I^{2}C mode.
The positive supply of pull-up resistor must equal to the value of VDD1.

Ordering Information

Part No.	Package
SH1106G	Gold bump on chip tray

Spec Revision History

Version	Content	Date
0.0	1. Original	Sep.2011
0.1	1. Add 3-wire SPI. 2. Interface select pin rename to IM0~2. (C86 rename to IM1, P/S rename to IM2.) 3. Update Application Circuit. 4. Add Set Pump voltage value command. (Page 17,18,29)	OCT.2011
0.2	1. Change the voltage output value of Set Pump voltage value command. 2. Add pad location and diagram. 3. Add AC Characteristics of 3-wire SPI. (Page 42)	Nov.2011