An FPGA-Based Time-Domain Frequency Shifter with Application to LTE and LTE-A Systems

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***Abstract*—This paper presents the hardware architecture and the corresponding implementation details of a configurable and optimized FPGA-based time-domain frequency shifter with application to Long Term Evolution (LTE) and Long Term Evolution-Advanced (LTE-A) systems. The architecture is mainly based on a customized Numerically Controlled Oscillator (NCO) that is used for generating complex exponentials employing only adders, a Look-Up Table (LUT) and plain logic resources.**

***Keywords*—** LTE, LTE-A, PRACH, NCO, time-domain frequency shift, FPGA.

I. Introduction

The mobile communications market has found on 3GPP technology roadmap an end-to-end convergent solution to deploy 4G cellular services that can benefit from the economies of large scale. The LTE technology is already mainstream in countries like USA, Korea and Japan, and it is the first step towards 4G networks based on LTE-Advanced technologies.

In LTE and LTE-A, the user equipment (UE) can use the uplink physical random access channel (PRACH) to request initial access to a target cell in the radio access network (RAN) [1], [2]. In this scenario, the UE transmits a random access (RA) preamble within a PRACH transmission opportunity set by higher layers (L2/L3) [3]. This preamble is detected at the eNodeB side, which estimates both the identification (ID) of the transmitted preamble and the propagation delay between UE and eNodeB. This latter information is then transmitted back to the UE as a timing advance command that enables the UE to synchronize its transmissions to the uplink frame structure.

Higher layers also determine the frequency location of the random access preamble within the physical resource blocks. In this way, at eNodeB side, a fundamental operation before any attempt to detect random access preambles takes place is the translation of the PRACH signal back to baseband through the use of a time-domain frequency shift operation.

This paper presents an efficient Time-domain Frequency Shifter (TDFS) hardware architecture for PRACH receivers with low-computational complexity. Implementation aspects and results are discussed here for FPGA devices, considering resource utilization and speed. Performance results are also presented considering the average error between time-domain frequency shift operations carried out by a floating-point model and by the fixed-point FPGA implementation of the proposed architecture.

The remainder of the paper is organized as follows. Section II presents important practical considerations on the implementation of the proposed architecture as well as detailed description of the units composing it. Test methodology, simulation and implementation results are then presented in Section III. Finally, Section IV provides some concluding remarks.

II. Implementation Aspects and Background Information

The proposed architecture is suitable for implementation on devices that employ hardware description language (HDL) as part of its design process such as Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC). Figure 1 shows the hardware architecture of the TDFS module, which employs only one LUT and exploits quarter wave symmetry for shortening the table length.

The architecture works with two different system clocks, the first one of 30.72 MHz, is the clock used by the ADC unit and therefore dictates the rate the complex multiplication must be carried out. Only two units run at this rate, namely, Complex Multiplier and Phase to Value Mapper. The second system clock, 61.44 MHz, is employed so that two samples of the complex exponential can be retrieved from the same LUT within the period of one sample coming from the ADC. This double system clock mechanism further reduces the amount of RAM needed. All units run at this rate with only one exception, the Complex Multiplier unit.

The input parameters $frequency\_offset$ and $bandwidth$ are static parameters, since they are fed into the module only when the eNodeB is initialized. The input signal $config\_present$ is asserted by higher layers during the initialization process to inform when the input parameter values are valid.

The TDFS module needs to be informed by means of the $ce\_61MHz44$ signal when the sequence part of the preamble starts so that it can be multiplied by the complex exponential the Customized NCO unit generates. Signal $ce\_61MHz44$ is asserted by the PRACH receiver module after it discards the CP part of the preamble and must stay

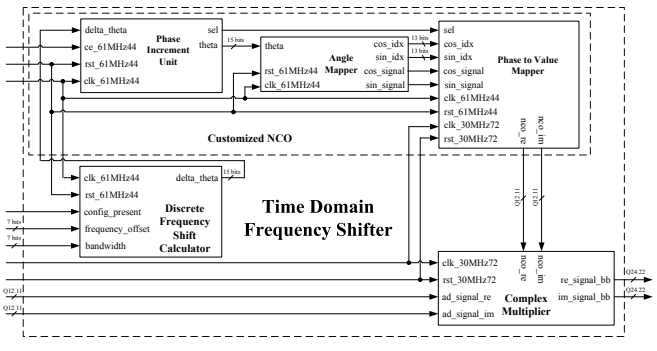

Figure 1. Blocks composing the Time-Domain Frequency Shifter module.

high for the whole duration of the sequence part, for example, for format-0 it must stay asserted for 24576 30.72 MHz-clock cycles, $i.e.$, 2*24576 when the 61.44 MHz system clock is considered. Once all units have registered outputs some latency is expected and then must be accounted for by the PRACH receiver when asserting the chip enable signal.

Other characteristic of the architecture is that it uses a total of 4 multipliers, which are employed in the Complex Multiplier unit. Besides that, the architecture only employs bit-shift and add operations to evaluate trigonometric functions, $i.e.$, complex exponentials, turning it into a very efficient hardware architecture in terms of logic resource usage.

The proposed architecture can have its outputs and inputs totally configured, $i.e.$, input and output widths can be configured for one of the following options: 8, 12, 16 and 24 bits. In our case we are using an ADC which outputs 12 bits for each one of the quadrature components I and Q and has fixed-point representation (Q Format) Q12.11, $i.e.$, 1 integer bit and 11 fractional bits.

The quadrature components of the complex exponential generated by the Customized NCO have the same fixed-point representation of the input. In this regard, after the complex multiplication between ADC and NCO quadrature samples, which involves multiplication and subsequent addition, the fixed-point representation of the output is Q25.22. As the maximum possible value produced by the complex multiplication operation is 2, the integer part only needs 2 bits instead of 3. In this way, depending on the configuration the fixed-point representation of the output complex signal can be set to Q8.6, Q12.10, Q16.14 and Q24.22.

A. Discrete Frequency Shift Calculator Unit

Figure 2 shows the architecture of the Discrete Frequency Shift Calculator unit. This unit is used to calculate the frequency shift, m, given by Equation 1, that must be applied to the received PRACH signal in order to bring it to baseband.

$$m = 13 + 144n_{PRB}^{RA} - 72N_{RB}^{UL}. \quad (1)$$

The parameter n_{PRB}^{RA} controls the PRACH location in the frequency domain. It corresponds to the input $frequency\_offset\_i$ of the TDFS module and is expressed as a resource block number configure by higher layers. The N_{RB}^{UL} gives the uplink system bandwidth in terms of Resource Blocks (RB).

All multiplications are performed through bit-shifting the input values n_{PRB}^{RA} and N_{RB}^{UL} by the constant values 144 and -72 respectively and then adding the result to the constant 13. Before feeding m into the Customized NCO unit it is necessary to check if the resulting value is negative, if so, the constant value N is summed to the resulting value then turning m into a positive value. It is done because the Phase

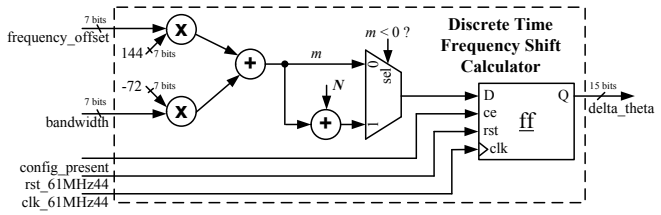

Figure 2. Architecture of the Discrete Frequency Shift Calculator unit.

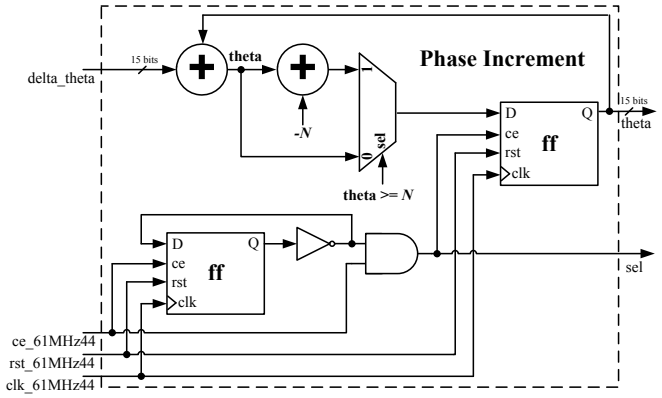

Figure 3. Architecture of the Phase Increment unit.

Increment Unit composing the Customized NCO expects only positive values. It can be easily proven that the discrete frequency shift, m is equal to $\Delta\theta$ that is the input value necessary for the Customized NCO to operate.

B. Customized Numerically Controlled Oscillator

As can be seen in Figure 1 the Customized NCO unit is made up of three blocks, namely, Phase Increment, Angle Mapper and Phase to Value Mapper. The first two units operate at 61.44 MHz and the last one operates at 30.72 and 61.44 MHz as it is the unit responsible for retrieving both quadrature values I and Q from the LUT within one period of the 30.72 MHz system clock.

Figure 3 shows the architecture of the Phase Increment unit. This unit implements a digital integrator which generates the phase argument, θ, fed into the Angle Mapper unit. At each iteration $\Delta\theta$ is added to θ which starts with 0. If the resulting θ value is greater than $N+1$ the constant value $-N$ is added to it, so that it stays less than N and thus can be correctly mapped into a valid value. This procedure is the direct implementation of a module operation, $\text{mod}(\theta, N)$. The unit only outputs a valid θ value when the selection, sel, signal is asserted. The

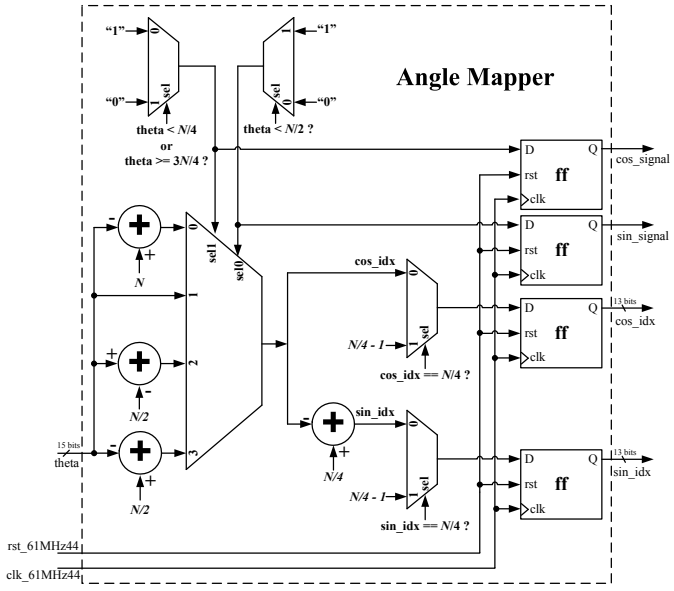

Figure 4. Architecture of the Angle Mapper unit.

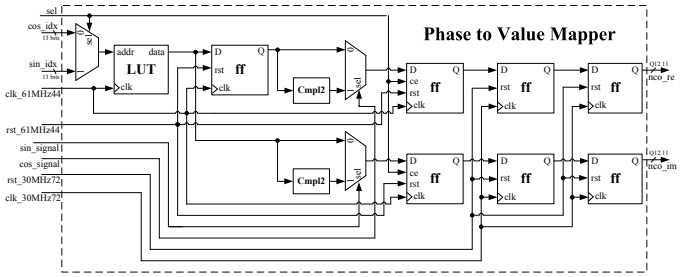

Figure 5. Architecture of the Phase to Value Mapper unit.

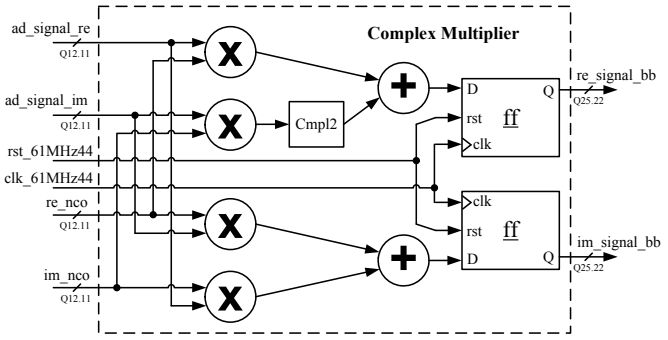

Figure 6. Architecture of the Complex Multiplier unit.

sel signal is generated by a clock divisor which divides the 61.44 MHz clock by 2, $i.e.$, the unit outputs a valid value at a rate of 30.72 MHz. The selection signal is also output by the unit in order to feed the Phase To Value Mapper unit. Once N is not a power of 2, the data width of the Phase Increment unit, $B_{\Theta(n)}$, should be ceiled, resulting in 15 bits.

Figure 4 depicts the architecture of the Angle Mapper unit. This unit is responsible for translating the phase argument, θ, which can vary between 0 and $2*\pi$ (0 to N) into a phase value within the first quadrant, $i.e.$, a value between 0 and $pi/2$ (0 and $N/4$). The resulting value gives the cosine index which is used as address to access one of the $N/4$ values stored in the LUT. In order to get the sine index a constant phase offset of $pi/2$ $i.e.$, $N/4$, is applied to the cosine index. As the value corresponding to $\cos(\pi/2)$, $i.e.$, 0, is not stored in the LUT whenever either cosine or sine indexes are equal to $N/4$ their values are changed to $(N/4)-1$, which is the closest value to zero.

The unit is also in charge of tracking the signals that must be applied to the quadrature values I and Q at the output of the Phase to Value Mapper unit. These signals translate the phase argument, represented by the cosine and sine indexes, back to its original quadrant. At the input of this unit the phase argument, θ, has a data width of 15 bits so that it could access N samples, $i.e.$, all the four quadrants, however, as the Angle Mapper unit translates θ to the first quadrant the data width can be reduced to 13 bits, which is the number of bits necessary to access the $N/4$ samples of the 1st quadrant (quarter wave symmetry) and which are stored in the LUT. It runs at 61.44 MHz and generates two new indexes, cosine and sine, at a 30.72 MHz rate once the phase argument θ is fed into the unit at that rate.

Figure 5 shows the architecture of the Phase to Value Mapper unit which is responsible for the mapping from phase-space to time. The cosine and sine indexes are used as addresses to access positions of the LUT. It is the LUT that performs the translation from phase-space to time. The LUT stores only 1/4, $i.e.$, $N/4$, of the cosine signal used as basis waveform. The selection, sel, signal chooses whether cosine or sine index is used to read the LUT. As can be seen in Figure 5 the cosine index is used as address when sel is low and the sine index when it is high.

Both cosine and sine indexes stay constant for a 30.72 MHz clock cycle. As the LUT operates at a rate of 61.44 MHz and both indexes are simultaneously present at its input it is possible to retrieve 2 samples within one period of the 30.72 MHz clock. By creating a delayed data path (with the use of a register) at the output of the LUT, it is possible to divert the in-phase (I) and quadrature (Q) samples to two different data paths and thus generating the complex exponential necessary to shift the received PRACH preamble to baseband. At this point, the generated quadrature signal is synchronized to the 61.44 MHz system clock, however, each quadrature pair lasts for one period of the 30.72 MHz system clock. It is explained by the two registers with chip enable inputs driven by the sel signal positioned at the output of the signal changing multiplexers.

In order to translate the quadrature samples to their original quadrants, the cosine and sine signals generated by the Angle Mapper unit are applied to their respective data paths. When necessary, the signal change is easily performed by applying the two's complement to the sample value.

Finally, as the ADC has a data rate of $30.72\text{x}10^6$ samples per second it is necessary to change the clock domain of the complex exponential signal, even tough its samples lasts for the correct period, they are not synchronized to the 30.72 MHz system clock. A simple way to perform this crossing of clock domains is to employ two registers at the desired clock rate. As we have a complex signal we use a pair of double registers for each of the quadrature components. Now the complex exponential signal is ready to be multiplied by the incoming PRACH preamble.

C. Complex Multiplier Unit

Figure 6 depicts the architecture devised for the Complex Multiplier unit. Once samples coming from both NCO and ADC are complex, it is necessary a complex multiplier to multiply then and perform the necessary frequency shift in time domain. The complex multiplier, also known as mixer, multiplies the ADC samples, $i.e.$, the PRACH signal, by the complex exponential samples generated by the Customized NCO unit. The complex multiplication requires 4 multiplications and 2 additions, as we consider a subtraction as being an addition in 2's complement. The Complex Multiplier unit operates at the system clock of 30.72 MHz once we must always respect the data rate dictated by the ADC.

III. Implementation Results

This section presents results regarding the implementation of the TDFS architecture which will be referred as device under test (DUT) from now on. We also assess the efficiency of the proposed circuitry by carrying out some simulations. The proposed architecture was developed in VHSIC Hardware Description Language (VHDL) and a corresponding bit-accurate Matlab model, referred here as Golden Model (GM), was developed for verification. The full design was targeted to a Xilinx Virtex 6 xc6vlx240t FPGA.

Table I presents information about the resource utilization

Table I. RESOURCE UTILIZATION

Part number	XC6VLX240T-1ff1156 (Virtex 6)
Number of Slice Registers	170 out of 301440 0%
Number of Slice LUTs	215 out of 150720 0%
Number of Occupied Slices	84 out of 37,680 0%
Number of RAMB36E1/FIFO36E1s	3 out of 416 0%
Number of DSP48E1s	4 out of 768 0%
Maximum Frequency	**239.981 MHz**

of the proposed TDFS module. It summarizes the main results obtained from the implementation of the proposed architecture on a FPGA device. The number of registers, occupied slices, LUTs, memory resources and Digital Signal Processor (DSP) resource blocks are presented. The maximum operation frequency reached by the module is 239.981 MHz.

From the results of Table I, it can be noticed that 3 Block RAM (BRAM) memories are used instead of the 2 mentioned earlier. The synthesis tool maps the content of the LUT to 3 BRAMs because the number of bits used to address the LUT is 13, therefore, $\text{ceil}((2^{13} * 12)/36K) = 3$ instead of 2. Note that each position of the BRAM stores a 12-bit value sampled from the basis waveform. The 4 instantiated Xilinx's DSP48 resources are employed by the Complex Multiplier unit.

In Virtex 6 family, 1 slice corresponds to 4 LUTs and 8 flip-flops. Block RAM/FIFOs are embedded resources of 36-bit memory. DSP48 is an embedded processing resource equivalent to 1 multiplier with two 18-bit inputs and one accumulator of 48 bits.

The reuse of DSP48 resources is a feasible strategy that can further optimize FPGA area at the expense of an increased clock operation and additional control logic. For example, the four full-parallel multiplications present in the Complex Multiplier unit can be serialized saving 3 out of the 4 DSP48 already in use.

As can be noticed by analyzing Table I, the proposed architecture occupies less than 1% of all Virtex 6 logic resources. The use of low cost FPGAs is allowed once the implementation of the proposed architecture on FPGA presents a very low occupancy rate. There are two points to take into account when choosing a low-cost FPGA: 1) the maximum achievable frequency, since low-cost FPGAs tend to have worse timing characteristics and 2) slice count could increase for technologies below Virtex-6, once other families may use 4-bit LUT instead of the 6-bit LUT per slice.

Figure 7 shows the average error between frequency shifted preambles produced by the GM and DUT. In order to get a concise plot, the average error for a given preamble is averaged over all possible offsets applied to that preamble, $i.e.$, Figure 7 presents the average of the average error over all possible offsets applied to a given preamble. The Figure shows the average error for some Q-formats when the bandwidth parameter, N_{RB}^{UL}, is set to 25 and 50 RBs, $i.e.$, bandwidths of 5 and 10 MHz respectively, and the offset parameter, n_{PRB}^{RA}, is varied along all possible values. It is clearly seen that the error has a very small variation, almost constant, along the preambles.

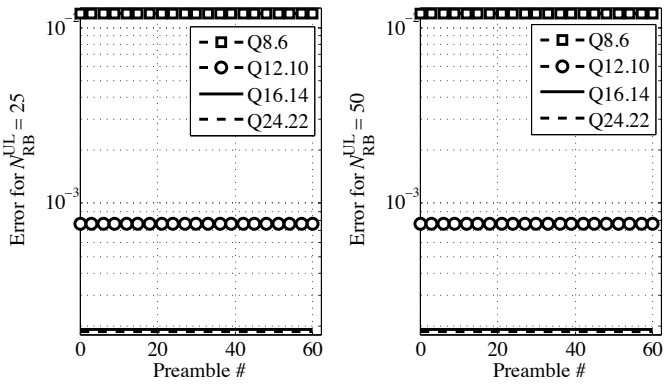

Figure 7. Average error between GM and DUT.

IV. CONCLUSIONS

A hardware-efficient architecture used for translating PRACH preambles into baseband featuring high-accuracy and low complexity characteristics has been presented. The proposed architecture is optimized to shorten the use of BRAMs, multipliers and logic resources. The low resource utilization demonstrates the feasibility of using this hardware architecture as part of a larger physical layer project comprising LTE downlink transmitter and uplink receiver at base station side.

ACKNOWLEDGMENT

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