

Reading Assignment 2

A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance

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This paper presents a design framework of the run-time Dynamic Voltage and Frequency Scaling (DVFS) optimizer in a general dynamic compilation system. DVFS is an effective technique for controlling microprocessor energy and performance.

It deals with how Operating System (OS) based DVFS practices are very limited and how their implementation can improve them. DVFS during run time or during program execution can help us save a lot of energy and perform better. They consider the phase changes in the program, defining where they can relax by clocking the microcontrollers at a lower speed. This is called as clock gating. It involves code insertion during compile time based on the hardware. This is because DVFS decisions are dependent on the program's memory boundedness i.e. the CPU can be slowed down if it is waiting for memory operation completion. The program behavior in term of memory boundedness is in turn dependent on run-time system settings such as machine configuration, program input size and patterns.

The same kind of application of DVFS is used in power capping for HPC and in data centers which require control over how the systems are being used and when to use maximum power and when not to. Using DVFS we can analyze when they require maximum computational power based on load and when they can switch of certain parts of the data center and save power. Overall, Dynamic Frequency Scaling and Dynamic Voltage and Frequency Scaling are the two most predictable power control mechanisms in terms of effects both on performance and power consumption.