ECE 451-LAB5

Fall 2019

Ram Rohit Gannavarapu

Contents

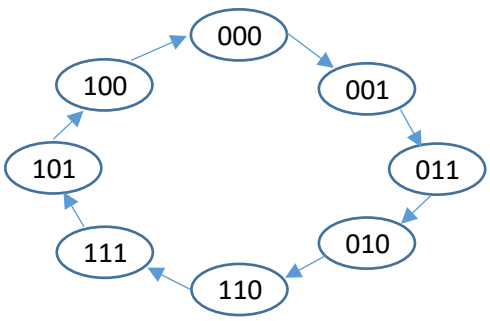
List of Figures

1. List of items completed

a) Design of positive edge triggered D-Flip Flop
b) Design of Grey Code Counter
c)

2. Lab Procedures

a. Grey code Counter state transition diagram



b. State transition table

Present State		
Q2	**Q1**	**Q0**
0	0	0
0	0	1
0	1	1
0	1	0
1	1	0
1	1	1
1	0	1
1	0	0

Next State		
Q2	**Q1**	**Q0**
0	0	1
0	1	1
0	1	0
1	1	0
1	1	1
1	0	1
1	0	0
0	0	0

c. K-maps for D in put of the flip flop

D2

Q2\Q1,Q0	00	01	11	10
0	0	1	1	0
1	0	0	1	1

$$\overline{Q_0}Q_1 + Q_0Q_2 = D_2$$

D1

Q2\Q1,Q0	00	01	11	10
0	0	1	1	1
1	0	0	0	1

$$\overline{Q_0}Q_1 + Q_0\overline{Q_2} = D_1$$

D0

Q2\Q1,Q0	00	01	11	10
0	1	1	0	0
1	0	0	1	1

$$\overline{Q_2Q_1} + Q_1Q_2 = D_0$$

The lab design starts with designing of a D- Flip Flop. Then followed by creating a combinational logic based on the equation generated in above table

3. Schematics/Verilog models

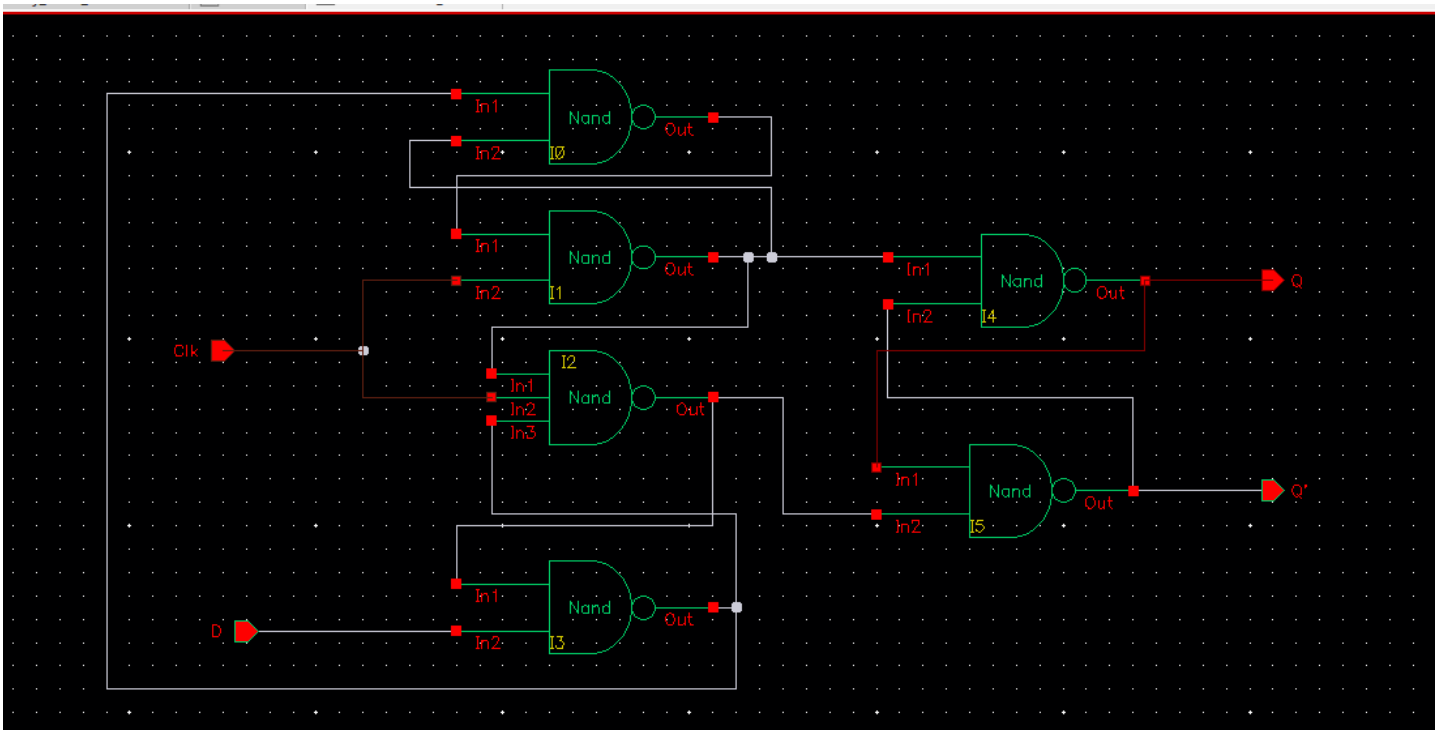


Figure 1: D-Flip Flop Schematic using gates

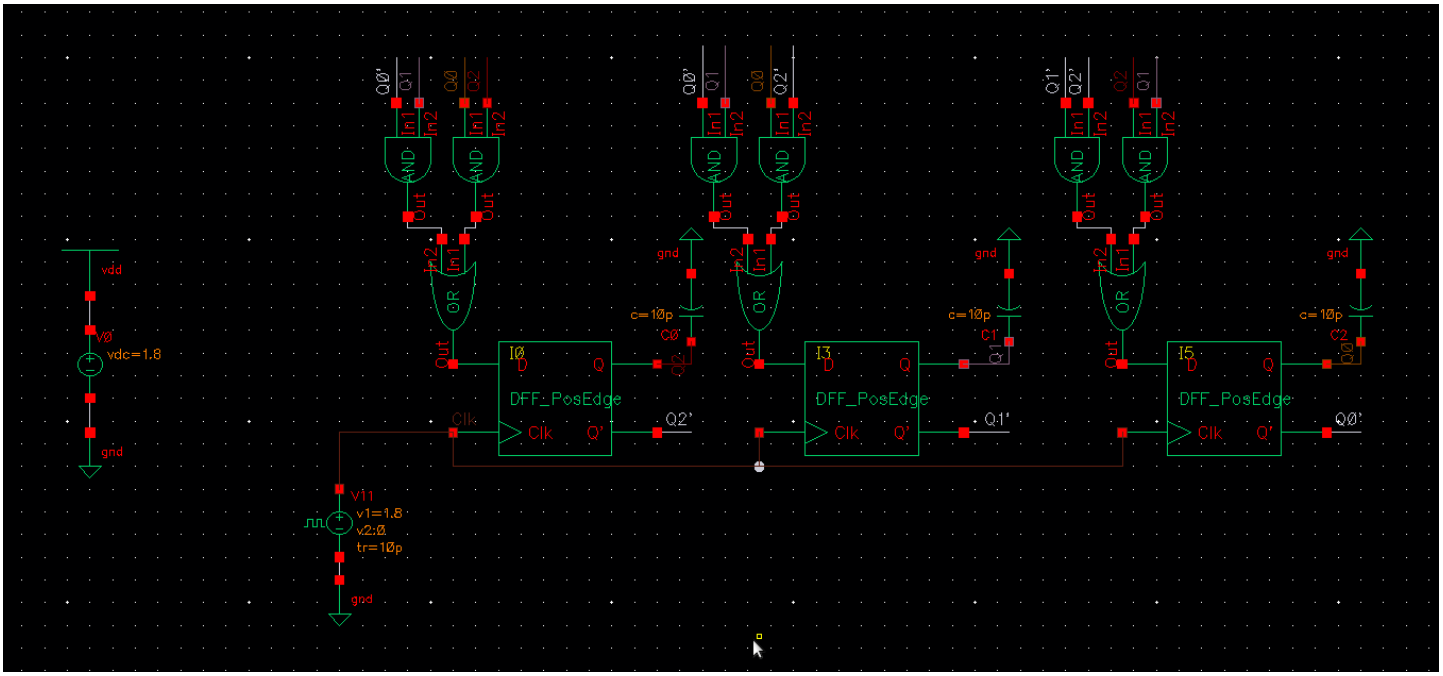


Figure 2: Grey Code Counter using D-Flip Flop

4. Simulation Results

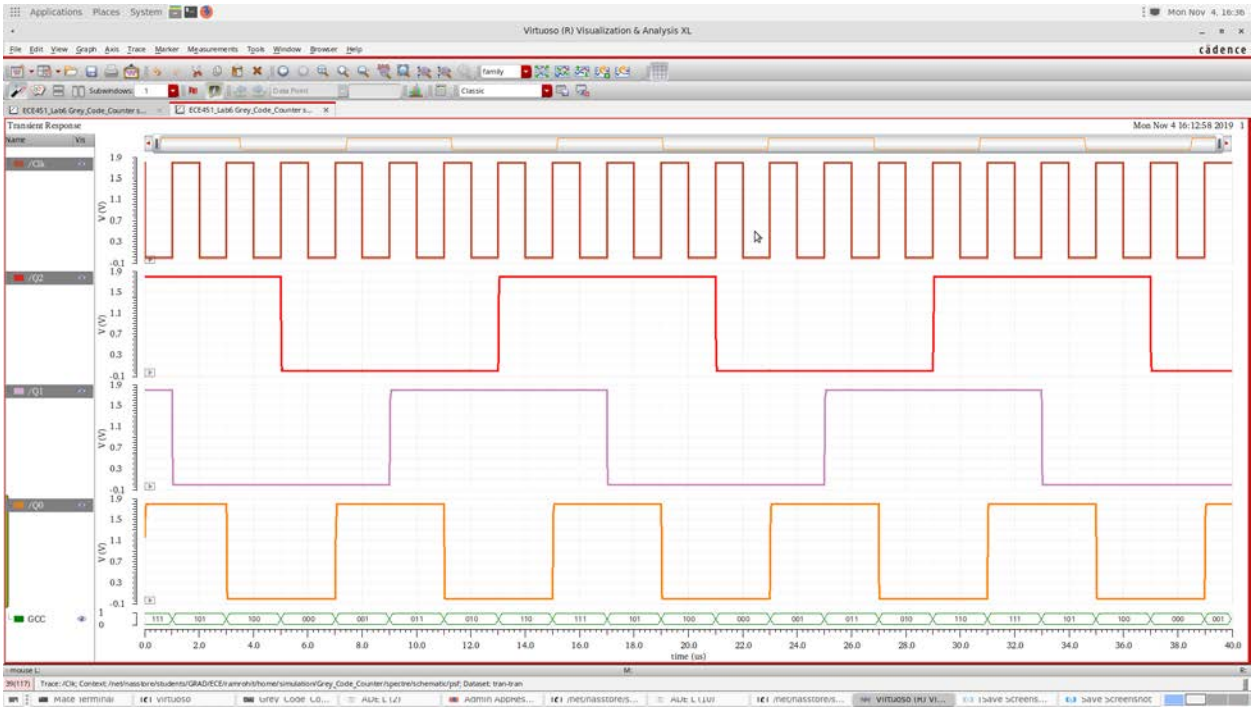


Figure 3: Simulation Results

5. Analysis and Explanations

The simulation results clearly follow the grey code counter sequence. As we didn't design a condition for initial state, the counter randomly enters a state and starts up counting from that state following the Grey code counter sequence.

6. Conclusion

In this LAB we have successfully designed a 3-bit grey code counter using D-Flip Flops and understand the concept of sequential circuit design.

7. Answers to questions posted in the lab

Q) What is Moore Finite State Machine(FSM)?

Moore finite state machine is a system whose outputs are decided only based on its current state. The outputs are decided based on the state.

Q) What is Mealy FSM?

Mealy FSM is a system whose outputs are decided based on the inputs and the current state. The outputs are set on the transition between states.