ECE 451-LAB2

Fall 2019

Ram Rohit Gannavarapu

Contents

[List of Figures 1](#_Toc20757140)

[1. List of items completed 2](#_Toc20757141)

[2. Lab Procedures 2](#_Toc20757142)

[3. Schematics/Verilog models 2](#_Toc20757143)

[4. Simulation Results 2](#_Toc20757144)

[5. Analysis and Explanations 2](#_Toc20757145)

[6. Conclusion 2](#_Toc20757146)

[7. Answers to questions posted in the lab 2](#_Toc20757147)

# List of Figures

[Figure 1: Verilog Code of 3-Bit ALU 2](#_Toc20756945)

[Figure 2: Verilog code for dispaly module 3](#_Toc20756946)

[Figure 3: Waveform output of the Logic 3](#_Toc20756947)

# List of items completed

* 1. 3-Bit ALU Verilog code
  2. Code to display Output F on 7-Segment Display

# Lab Procedures

# Schematics/Verilog models

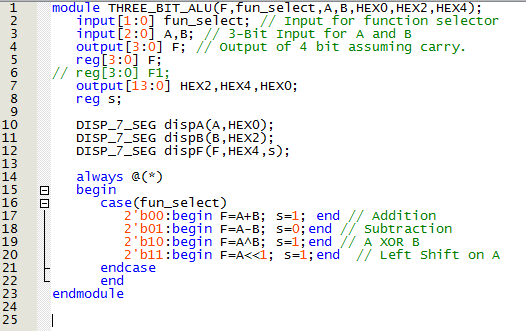


Figure 1: Verilog Code of 3-Bit ALU

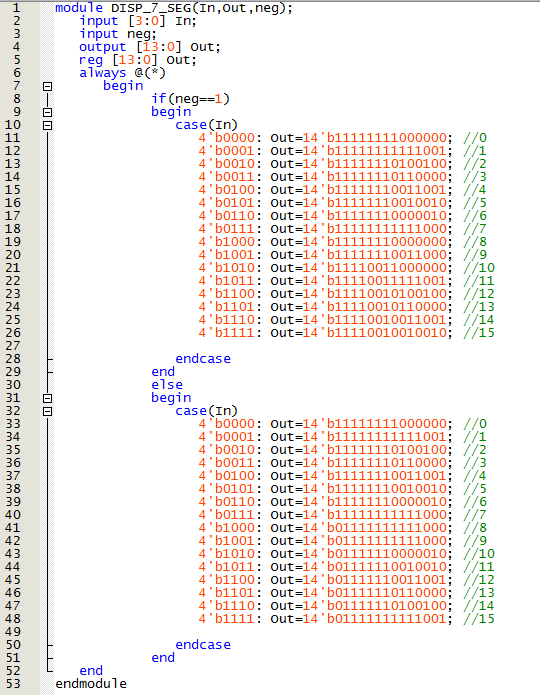


Figure 2: Verilog code for dispaly module

# Simulation Results

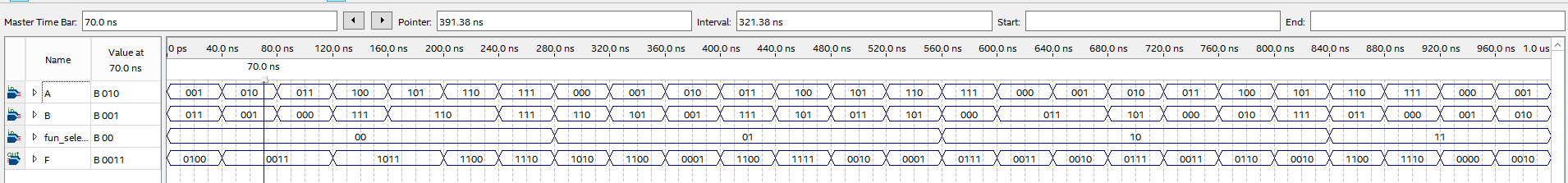


Figure 3: Waveform output of the Logic

# Analysis and Explanations

It is evident from the simulation results that all the operations are working as expected.

# Conclusion

Verilog Code for 3-bit ALU is working as expected and the output is also displayed on the 7-segment display properly.

# Answers to questions posted in the lab

Q) Discuss the advantages of a Hardware Descriptive Language (HDL).

A) It is easier to implement/Model a Design in Verilog. It also saves a lot of time in both Verification through simulation and debugging issues.