# VC Verification IP
# UART
# Release Notes

Version O-2018.09, September 2018

SYNOPSYS®

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# Contents

# 1 Product Updates

VC VIP for UART supports the verification of SoC designs that include interfaces implementing UART specifications. UART VIP supports Universal Verification Methodology (UVM) or Open Verification Methodology (OVM). It provides the following feature set:

- Protocol features
- Verification features
- Methodology features
- VIP features
- Transaction features
- Ease-of-use features

This chapter discusses new features and enhancements of VC Verification IP for UART release. This chapter consists of the following topics:

- "New and Changed Features" on page 7
- "Fixes/B-STARs" on page 8

## 1.1 New and Changed Features

This release provides the following changes:

- Added a configuration attribute `pkt_cnt_to_send_xoff_pattern` in `svt_uart_configuration` class which defines the threshold of receiving packets after which XOFF will be sent by DCE in software handshaking. It has to be less than or equal to `receiver_buffer_size`.
- The `+incdir+` flow is an alternative to the existing flow (design directory flow). This alternative flow eliminates the dependency on design directory. As for the usage, provide the path to the VIP's package directory. For example,

  *DESIGNWARE_HOME/vip/svt/uart_svt/version/sverilog/include*

Table 1-1 lists the new and changed features in this release.

**Table 1-1 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001374512 | UART data transmit/receive behavior in sotware hndshk need enhancement |

## 1.2 Fixes/B-STARs

Table 1-2 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 1-2 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001378910 | Uart VIP checker missing start bit sampling in one of software handshake scenario |

# 2 Known Issues and Limitations

This chapter discusses known issues and limitations of the Verification IP. This chapter consists of the following topics:



## 2.1 Protocol Limitations

- Configuring XON and XOFF packets via sequence is not recommended when `pkt_cnt_to_send_xoff_pattern` is set to non-zero value.

## 2.2 Verification and Methodology Limitations

- MTI and VCSMX ares not supported with Verilog mode.

# 3 Supported Platforms, Models, and Software

This chapter discusses supported platforms, models, and software of VC Verification IP for UART.

This chapter consists of the following topics:



## 3.1 Supported Methodologies

Table 3-1 lists the methodologies supported with simulators.

**Table 3-1 Supported Methodologies With Simulators**

| Methodology | VCS | IUS | MTI |
|---|---|---|---|
| UVM | Supported | Supported | Supported |
| OVM | Supported | Supported | Supported |
| VMM | Not supported | Not supported | Not supported |
| VLOG | Supported | Supported | Supported |

## 3.2 Supported OS and Simulator Platforms

The simulator matrix table is available at the following location:

VC VIP Library page

https://solvnet.synopsys.com/dow_retrieve/latest/snps_vip_lib/doc/simulator_matrix.pdf

This version of UART VIP is qualified with version O-2018.09 of the SystemVerilog Verification Technology (SVT). The SVT is an internal portion of the VIP and provides base VIP functionality, some utilities, and support for installation and licensing.

This version supports SVT O-2018.09. The version of the SVT is the key for determining which versions of platform/OS and simulators have been qualified with this VIP. Whenever a new version of the SVT is released, this VIP is qualified with it.

To determine the version of the SVT in an existing DESIGNWARE_HOME installation, use the following command:

```
$DESIGNWARE_HOME/bin/dw_vip_setup -i home
```

## 3.3 Software Tools Support

Following are the supported tool sets that work with this version of the VIP:

- Protocol Analyzer: Version O-2018.09

## 3.4 Licensing Information

You can enable UART VIP by performing the license check in the order listed below. Once a required feature or a set of features are successfully checked-out, the VIP stops looking for other licenses. The type of license depends on product and portfolio type. You can use one of the following set of hierarchies:

- `VIP-UART-SVT`
- `VIP-PROTOCOL-SVT`
- `VIP-SOC-LIBRARY-SVT`
- `VIP-LIBRARY-SVT + DesignWare-Regression`

**Note**

Licensing is needed if the VIP component classes are instantiated in the design. This includes envs, agents, drivers, monitors, sequencers, and components in UVM/OVM. This includes groups, subenvs, and xactors in VMM.

# 4 Documentation

This chapter discusses the documentation of VC Verification IP for UART.

This chapter consists of the following topics:



**Attention**

Beginning in December 2014 with the J-2014.12 release, Synopsys Verification IP products adopt the release version format recommended by the company. The new version format is:
<alphabet>-<year>.<month>

<alphabet> is a single letter corresponding to the QSC foundation that the release is compliant with.
<year> is a 4-digit number corresponding to the year of the release.
<month> is a 2-digit number corresponding to the month of the release.

For patch releases, a "-<patch_number>" is appended to the release version.
For Service Pack releases, a "-SP<number>" is appended to the release version.

For example:
J-2014.12: Release in December 2014 that is compliant with the J foundation.
J-2014.12-1: First patch on the J-2014.12 release.
J-2014.12-SP1: First Service Pack release for J-2014.12.

**Note**

1.41a was the last release before the version change.

## 4.1 Protocol

- PC16550D Universal Asynchronous Receiver/Transmitter with FIFOs

## 4.2 Methodology

- Universal Verification Methodology (UVM) 1.1 User's Guide May 18, 2011d
- Universal Verification Methodology (UVM) 1.2 User's Guide June, 2014
- Open Verification Methodology (OVM) 2.1.2 User's Guide June, 2011

## 4.3 Product Guides and Online Help

After UART VIP is downloaded and installed, its documentation set resides at the following location:

```
$DESIGNWARE_HOME/vip/svt/uart_svt/latest/doc/
```

VC VIP for UART documentation set includes the following documents:

- UART VIP UVM User Guide - A document to guide you on the installation, usage, and feature set of VC VIP for UART UVM. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/doc/uart_svt_uvm_user_guide.pdf
  ```

- UART VIP OVM User Guide - A document to guide you on the installation, usage, and feature set of VC VIP for UART OVM. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/doc/uart_svt_ovm_user_guide.pdf
  ```

- UART VIP HDL User Guide - A document to guide you on the installation, usage, and feature set of VC VIP for UART HDL. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/doc/uart_svt_hdl_user_guide.pdf
  ```

- UART VIP UVM Getting Started Guide - A document to guide you on integrating VC VIP for UART into testbenches that are compliant with the SystemVerilog UVM. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/doc/uart_svt_uvm_getting_started.pdf
  ```

Online HTML reference documentation consists of the following:

- UART VIP UVM Class Reference - A HTML-based reference help, which provides information about classes, functions, and member variables. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/doc/uart_svt_uvm_class_reference/html/index.
  html
  ```

- UART VIP OVM Class Reference - A HTML-based reference help, which provides information about classes, functions, and member variables. It is installed at the following location:

```
$DESIGNWARE_HOME/vip/svt/uart_svt/latest/doc/uart_svt_ovm_class_reference/html/index.
html
```

## 4.4 Quickstart Examples

The VIP provides various levels of quickstart tutorials for each methodology. A complete list of available tutorials and their associated examples is as follows:

- UART VIP UVM Basic QuickStart - An example to demonstrate the usage of the VIP in the SV-UVM environment. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/examples/sverilog/tb_uart_svt_uvm_basic_sys/
  doc/tb_uart_svt_uvm_basic_sys/index_basic.html
  ```

- UART VIP UVM Intermediate QuickStart - An example to demonstrate the usage of the VIP in the SV-UVM environment. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/examples/sverilog/tb_uart_svt_uvm_intermedia
  te_sys/doc/tb_uart_svt_uvm_intermediate_sys/index_intermediate.html
  ```

- UART VIP OVM Basic QuickStart - An example to demonstrate the usage of the VIP in the SV-OVM environment. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/examples/sverilog/tb_uart_svt_ovm_basic_sys/
  doc/tb_uart_svt_ovm_basic_sys/index_basic.html
  ```

- UART VIP OVM Intermediate QuickStart - An example to demonstrate the usage of the VIP in the SV-OVM environment. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/examples/sverilog/tb_uart_svt_ovm_intermedia
  te_sys/doc/tb_uart_svt_uvm_intermediate_sys/index_intermediate.html
  ```

- UART VIP HDL Basic QuickStart - An example to demonstrate the usage of the VIP in the HDL environment. It is installed at the following location:

  ```
  $DESIGNWARE_HOME/vip/svt/uart_svt/latest/examples/verilog/tb_uart_svt_verilog_basic_s
  ys/doc/tb_uart_svt_verilog_basic_sys/index_basic.html
  ```

# 5 Customer Support

This chapter discusses customer support provided for VC VIP for UART.

This chapter consists of the following topics:



## 5.1 SolvNet

Synopsys SolvNet resides at the following location:

http://solvnet.synopsys.com

It provides you with the following features:

- Download Center for all VIPs <*should we include download instructions?*>
- Support
- Training
- Reference Methodology Retrieval System
- Hundreds of articles on VIP usage
- Register problem reports

## 5.2 Registering a Problem

To register a problem, perform any of the following tasks:

- Enter a call through SolvNet:
  - Go to http://solvnet.synopsys.com/EnterACall
    and click the Open A Support Case link to enter a call. Provide the following requested information:
    - Product: **Verification IP**
    - Sub Product 1: **UART SVT**
    - Product Version: **O-2018.09**

    Fill in the remaining fields according to your environment and your issue.
- Send an e-mail message to support_center@synopsys.com
  - Include the Product name, Sub Product name, and Product version as discussed previously.

## 5.3 Reporting a Problem

To report a problem, keep the following information ready before you contact technical support:

- Provide a description of the following:
  - The issue under investigation
  - Your verification environment
- Create a Value Change Dump (VCD) file.
- Generate a log file for the simulation.
- Provide other files such as translation logs.

For information on reporting a problem for each methodology, see the following sections in the respective user guide:

- Chapter A, “Appendix A: Reporting Problems”, in the VC Verification IP UART UVM user guide
- Chapter A, “Appendix A: Reporting Problems”, in the VC Verification IP UART OVM user guide
- Chapter A, “Appendix A: Reporting Problems”, in the VC Verification IP UART Verilog user guide

## 5.4 Telephone Support

Telephone your local support center:

- North America:

  Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday

- All other countries:

  http://www.synopsys.com/support/support_ctr

# 6
# Previous Release Notes

This chapter lists product update for the following previous releases:

✦ "Notes for Release 0.10a" on page 37

## 6.1 Notes for Release O-2018.06-1

### 6.1.1 New and Changed Features

This release provides the following changes:

- Added the `deassert_autoflow_hndshk_before_stop_bit` configuration in `svt_uart_configuration` class for rts/cts de-assertion to happen before middle of stop bit in autoflow mode.
- Added the `is_valid` function check in runtime reconfiguration via task. Warnings will be printed in case of violation. These warnings will be converted to fatal errors in the O-2018.09 release.
- Added the `UV_CHK_RTS_DEASSERT_DURING_HNDSHK` checker rule as warning.

Table 6-1 lists the new and changed features in this release.

**Table 6-1 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001354103 | Way to pullback RTS going high little bit early then original implementation |

### 6.1.2 Fixes/B-STARs

Table 6-2 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-2 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.2 Notes for Release O-2018.06

### 6.2.1 New and Changed Features

This release provides the following changes:

- Added the RAL based reference public example *uart_svt/tb_uart_svt_uvm_basic_ral_sys*.

Table 6-3 lists the new and changed features in this release.

**Table 6-3 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001330410 | UART VIP False reporting issue when RTS is Z before clock stop |

### 6.2.2 Fixes/B-STARs

Table 6-4 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-4 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.3 Notes for Release N-2018.03-3

### 6.3.1 New and Changed Features

This release provides the following changes:

- Added specification version references in checker rules.
- Added few checks with respect to X and Z value check on data and handshake interface signals.

Table 6-5 lists the new and changed features in this release.

**Table 6-5 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001330410 | UART VIP False reporting issue when RTS is Z before clock stop |

### 6.3.2 Fixes/B-STARs

Table 6-6 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-6 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.4 Notes for Release N-2018.03-2

### 6.4.1 New and Changed Features

This release provides the following changes:

- Added the `transmitted_packet` variable in `svt_uart_transaction` class to indicate packet transmitted on bus for monitoring and response object capturing.

Table 6-7 lists the new and changed features in this release.

**Table 6-7 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001316224 | Add variable in Uart transaction to indicate transmit packet on bus @ rsp object |

### 6.4.2 Fixes/B-STARs

Table 6-8 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-8 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.5 Notes for Release N-2018.03-1

### 6.5.1 New and Changed Features

This release provides the following changes:

- Added support for RS485 mode checking.

Table 6-9 lists the new and changed features in this release.

**Table 6-9 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001298010 | UART VIP to be enhanced for RS485 mode support for passive dte agent. |

### 6.5.2 Fixes/B-STARs

Table 6-10 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-10 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.6 Notes for Release N-2018.03

### 6.6.1 New and Changed Features

This release provides the following changes:

- Moved interface definition from *svt_uart_if.sv* file to *svt_uart_if.svi* file as per SVT guidelines.

Table 6-11 lists the new and changed features in this release.

**Table 6-11 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.6.2 Fixes/B-STARs

Table 6-12 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-12 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.7 Notes for Release N-2017.12-2

### 6.7.1 New and Changed Features

Table 6-15 lists the new and changed features in this release.

**Table 6-13 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.7.2 Fixes/B-STARs

Table 6-16 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-14 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.8 Notes for Release N-2017.12-1

### 6.8.1 New and Changed Features

Table 6-15 lists the new and changed features in this release.

**Table 6-15 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.8.2 Fixes/B-STARs

Table 6-16 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-16 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001280615 | UART VIP 2017.06 version hangs with VCS-2015.09-SP2 but 2016.03 works well |

## 6.9 Notes for Release N-2017.12

### 6.9.1 New and Changed Features

Table 6-17 lists the new and changed features in this release.

**Table 6-17 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001158891 | svt_vip_writer class giving Error w.r.t svt_uart_transaction |

### 6.9.2 Fixes/B-STARs

Table 6-18 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-18 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001252371 | NOA in user SB resulted with UART VIP due to sampling issue while autoflow ctrl |

## 6.10 Notes for Release N-2017.09-1

### 6.10.1 New and Changed Features

This release provides the following changes:

- Added a runtime argument `svt_uart_disable_registry_chk` which must be set to 1 to disable registry checks if either of UART BFM wrapper or UART agent is not created.

Table 6-19 lists the new and changed features in this release.

**Table 6-19 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001236270 | To bypass agent registry checks using $valuplusargs in UART VIP. |

### 6.10.2 Fixes/B-STARs

Table 6-20 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-20 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.11 Notes for Release N-2017.09-T20170906

### 6.11.1 New and Changed Features

Table 6-21 lists the new and changed features in this release.

**Table 6-21 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001233770 | UART VIP shall not toggle RTS & CTS pins while enable_rts_cts_handshake is 0. |
| 9001233823 | UARTn_CTS must be released before the middle of last STOP bit. |

### 6.11.2 Fixes/B-STARs

Table 6-22 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-22 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.12 Notes for Release N-2017.09

### 6.12.1 New and Changed Features

Table 6-23 lists the new and changed features in this release.

**Table 6-23 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.12.2 Fixes/B-STARs

Table 6-24 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-24 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001230018 | do_is_valid shall only be checked for FBRD only when enable_fractional_brd =1 |

## 6.13 Notes for Release M-2017.06-T-20170811

### 6.13.1 New and Changed Features

This release provides the following changes:

- Added support for DVT Eclipse version 16.1.14.

Table 6-25 lists the new and changed features in this release.

**Table 6-25 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.13.2 Fixes/B-STARs

Table 6-26 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-26 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001227992 | VIP sampling issue in case of fractional baud divisor having minor clock tolerance |

## 6.14 Notes for Release M-2017.06-T-20170802

### 6.14.1 New and Changed Features

This release provides the following changes:

- Added support for DVT Eclipse version 16.1.14.

Table 6-27 lists the new and changed features in this release.

**Table 6-27 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.14.2 Fixes/B-STARs

Table 6-28 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-28 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001222646 | UART VIP parity reconfiguration issue |
| 9001223847 | VIP RTS de-assertion is taking 1 or 2 clocks while receiver buffer gets full |

## 6.15 Notes for Release M-2017.06

### 6.15.1 New and Changed Features

This release provides the following changes:

- Added support for DVT Eclipse version 16.1.14.

Table 6-29 lists the new and changed features in this release.

**Table 6-29 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.15.2 Fixes/B-STARs

Table 6-30 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-30 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001133529 | Dependent configuration setting causing NOA error instead VIP failure message |

## 6.16 Notes for Release M-2017.03

### 6.16.1 New and Changed Features

Table 6-31 lists the new and changed features in this release.

**Table 6-31 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001150335 | UART VIP: Dynamic licensing support requirement{checkout while traffic to send } |

### 6.16.2 Fixes/B-STARs

Table 6-32 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-32 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.17 Notes for Release M-2016.12-T0119

### 6.17.1 New and Changed Features

Table 6-33 lists the new and changed features in this release.

**Table 6-33 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.17.2 Fixes/B-STARs

Table 6-34 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-34 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001145687 | UART VIP: fractional baud rate functional issue during reconfiguration call |

## 6.18 Notes for Release M-2016.12

None

## 6.19 Notes for Release L-2016.09

### 6.19.1 New and Changed Features

Table 6-35 lists the new and changed features in this release.

**Table 6-35 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001060156 | UART: 1.5 STOP bit requirement |

### 6.19.2 Fixes/B-STARs

Table 6-36 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-36 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.20 Notes for Release L-2016.06-T0624

### 6.20.1 New and Changed Features

Table 6-37 lists the new and changed features in this release.

**Table 6-37 New and Changed Features**

| E-STAR | Title |
|---|---|
| None | |

### 6.20.2 Fixes/B-STARs

Table 6-38 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-38 Fixed STARs**

| B-STAR | Title |
|---|---|
| 9001049088 | UART VIP:Using reconfigure_via_task() VIP RTS pin gets de-asserted for full simu |

## 6.21 Notes for Release L-2016.06

None

## 6.22 Notes for Release L-2016.03-2

None

## 6.23 Notes for Release L-2016.03-1

This release provides the following changes:

- Enhancement for programmable sample rate other than 16.
- Added the `sample_rate` variable in the *svt_uart_configuration.sv* file to set different sample rates.
- Added the `resync_rx_at_each_byte` variable in the *svt_uart_configuration.sv* file to support sample rate other than 16.
- Added the *tb_uart_svt_uvm_diff_top_clock_intermediate_sys* example in UVM for configurations `resync_rx_at_each_byte` and `sample_rate`.

Table 6-39 lists the new and changed features in this release.

**Table 6-39 New and Changed Features**

| E-STAR | Title |
|---|---|
| 9001014564 | UART VIP: Enhancement to support programmable sample rate other than 16 |

### 6.23.1 Fixes/B-STARs

Table 6-40 lists the Synopsys Technical Action Requests (STARs) fixed in this release.

**Table 6-40 Fixed STARs**

| B-STAR | Title |
|---|---|
| None | |

## 6.24 Notes for Release L-2016.03

None

## 6.25 Notes for Release K-2015.12

None

## 6.26 Notes for Release K-2015.09

STAR fixes.

## 6.27 Notes for Release J-2014.12-SP3

None

## 6.28 Notes for Release J-2014.12-SP2

None

## 6.29 Notes for Release J-2014.12-SP1-2

Added tests to achieve 100% coverage in the UVM example.

## 6.30 Notes for Release J-2014.12-SP1

None

## 6.31 Notes for Release J-2014.12-1

This release provides the following changes:

- Updated examples to generate FSDB dump (WAVES =fsdb target).

## 6.32 Notes for Release J-2014.12

This release provides the following changes:

- Enhanced the VIP to run UVM examples in Partition Compile and Precompiled IP flows. For this, added additional targets, namely, `vcspcvlog`, `vcsmxpcvlog`, and `vcsmxpipvlog`).
- Added the verification plan in the `.hvp` format to leverage the Verdi planning and management solutions.
- Added reference program block examples.
- Added the getting started guide, namely `uart_nvs_uvm_getting_started.pdf`, for the VIP.
- Changed the naming convention of documents. The format of the naming convention is as follows:
- 
```
<component_name>_<uvm/ovm/hdl>_user_guide.pdf
<component_name>_release_notes.pdf
<component_name>_uvm_getting_started.pdf
```

## 6.33 Notes for Release 1.41a

This release provides the following changes:

- Supports UVM version 1.2
- STAR fixes.

## 6.34 Notes for Release 1.40a

This release provides the following changes:

- Added support for the back annotation of verification plans in Verdi. A new set of `.hvp` files are provide to work with Verdi.
- STAR fixes.

## 6.35 Notes for Release 1.35a

The release provides the following features:

- Added quickstart for verilog basic example to cover different uart scenarios.
- Added support for the Verification Compiler licensing. For more information, see "Licensing Information" on page 12

## 6.36 Notes for Release 1.30a

The release provides the following features:

- Added new tests in verilog basic example to cover different possible uart scenarios.
- Added new UART subscriber class and test in OVM and UVM intermediate example to read the received data back from the VIP.
- Updated OVM and UVM Quickstart guides with resect to uart_subscriber class.
- Updated OVM,UVM and HDL userguide with Usage notes section.

## 6.37 Notes for Release 1.25a

The release provides the following feature:

- Updated OVM and UVM Quickstart guides with new tests.

## 6.38 Notes for Release 1.16a

The release provides the following feature:

- Added the functionality to add the fractional-baud-rate-divisor value.
- Added new configuration attributes, namely enable_fractional_brd, fractional_divisor, fractional_divisor_period, and fractional_mult_median, for the fractional-baud-rate-divisor implementation in the svt_uart_configuration.sv class.

## 6.39 Notes for Release 1.15a

The release provides the following feature:

- Added a quickstart for an OVM intermediate example.

- Added few new tests in intermediate examples for both OVM and UVM.
- Added two examples in both OVM and UVM for the configuration of `enable_tx_rx_handshake=0`.

## 6.40 Notes for Release 1.10a

The release provides the following feature:

- Added the `checks_coverage_enable` variable in the `svt_uart_agent_configuration.sv` file to enable or disable protocol checks-related functional coverage.

## 6.41 Notes for Release 1.06a

The release provides the following feature:

- Added a basic-example environment for a new Verilog interface
- Added a user guide for the Verilog interface.

## 6.42 Notes for Release 1.05a

The release provides the following feature:

- Added a quickstart guide for a UVM intermediate example.
- Updated both OVM and UVM user guides with the Flow Control description in the Usage Notes chapter.
- Supports version 2.10a of the SVT.
- Supports version 1.10a of the Protocol Analyzer.

## 6.43 Notes for Release 1.01a

The release provides the following feature:

- Updated the `valid_ranges` constraint for the `data_pattern_xon` and `data_pattern_xoff` variables in the `svt_uart_configuration` class to limit the length of their values within the selected data width. Also, updated the `do_is_valid` function in the `svt_uart_configuration` class to check whether `data_pattern_xon` and `data_pattern_xoff` cross the length of the selected data width.
- Modified the logic of the `svt_uart_dce_soft_handshake_send_xoff_xon_sequence` sequence in the `body` task in the `svt_uart_dce_transaction_sequence_collection.sv` file.

- Set the default values of the `inter_cycle_delay` and `packet_count` variables to `200` and `10` respectively of the `svt_uart_dce_soft_handshake_packet_with_xoff_xon_sequence` class in the `svt_uart_dce_transaction_sequence_collection.sv` file.
- Modified the `reasonable_sequence_length` constraint on the `sequence_length` variable in the basic and intermediate example environment.

## 6.44 Notes for Release 1.00a

The release provides the following features:

- Updated the sequence collection.
- Updated the intermediate example.
- Changed licensing to support the `VIP-LIBRARY-SVT` feature.
- Updated the driver of the DTE and DCE agent to provide a response to the sequencer. For this, use the `get_response()` task in the sequence. If you do not want the driver to provide a response to the sequencer then set the `enable_put_response` property of the configuration class to `0`.
- Added Clock as an argument of the `svt_uart_if` interface. Now, you need to create an instance of `svt_uart_if` as shown here:

```
svt_uart_if uart_dte_if(SystemClock);
```

- Changed the type for the two properties, namely `received_parity` and `received_packet`, of the `svt_uart_transaction` class as shown here:

```
bit received_parity [];
bit [12:0] received_packet[] ;
```

(In the last release, it was `logic received+_parity = 1'b0`)
(In the last release, it was `logic [12:0] received_packet = 'b0;`)

Since these properties are of the array type, you need to access them by `received_parity[0]` and `received_packet[0]`, if you are using these properties in your scoreboard.

## 6.45 Notes for Release 0.13a

The release provides the following features:

- Support for the MTI simulator
- Functional coverage
- Sequence collection
- Error injections
- Callbacks
- Source code visibility
- Configuration creator

- An intermediate example

## 6.46 Notes for Release 0.11a

The release provides the following features:

- Support for OVM.
- The IUS support for UVM and OVM.

## 6.47 Notes for Release 0.10a

The release provides the following features:

- Supports the UVM methodology running over VCS.
- Provides the functionality based on 16550 industry standard, such as programmable data width (5-9), programmable parity bit (Even, Odd, Stick Parity, and No parity), and Line-break generation and detection.
- Provides a quickstart example to highlight the use model and to show how to configure and run a test using VIP.
- Integrates Protocol Analyzer - a GUI-based tool - to view transaction values across transactions during the simulation run.