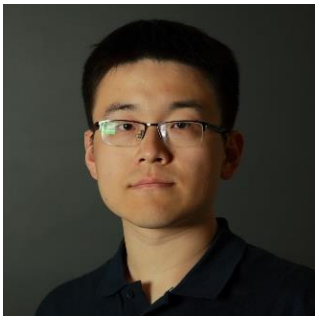
Chang Gao



Ph.D. Student

Institute of Neuroinformatics, University of Zürich and ETH Zürich

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LinkedIn: www.linkedin.com/in/gaochangw

Google Scholar: https://scholar.google.ch/citations?user=sQ9N7dsAAAAJ&hl=en

General Information

Nationality:	Chinese
Marital Status:	Single
Date of Birth:	22 April 1992
Languages:	Chinese (Native), English (Fluent)

Education

University of Zürich & ETH Zürich — Ph.D. in Neuroscience — **Jan 2017 - present**, Zürich, Switzerland

- **Focus:** Energy-efficient deep neural network accelerator design for edge inference, training and relevant applications.
- **Grants:** Fully funded (50,040 CHF/year) by Samsung Advanced Institute of Technology (SAIT) and Swiss National Science Foundation (SNSF).
- **Teaching:** INI-502: Basics of instrumentation, measurement and analysis
  ETH Course 402-0248-00L: Electronics for Physicists II (Digital)
- **Advisors:** Prof. Dr. Shih-Chii Liu & Prof. Dr. Tobi Delbrück

Imperial College London — M.Sc. in Analog and Digital Integrated Circuit Design — **Sept 2015 - Sept 2016**, London, UK

- **Grade:** Distinction (equivalent GPA: 4.00/4.25; Rank: #1)
- **Thesis:** Full-custom design of a mixed-signal physical unclonable function in 350 nm technology. Published in ISCAS 2017.

University of Liverpool — B.Eng. in Electronics — **Sept 2013 - Sept 2015**, Liverpool, UK

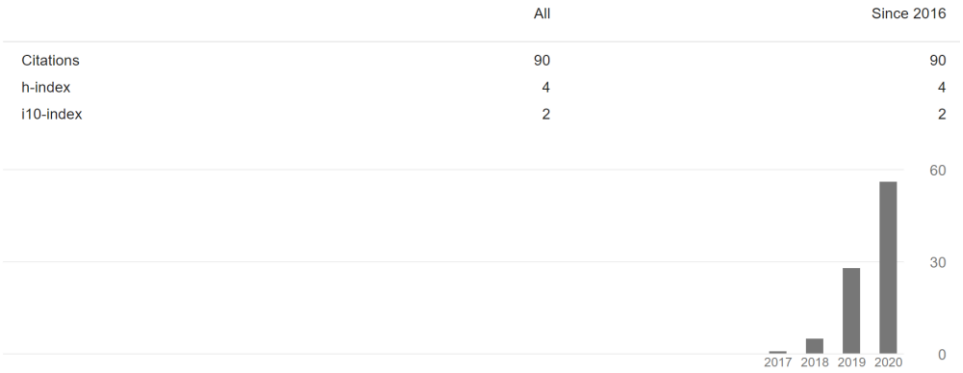
- **Grade:** First-Class Honors (equivalent GPA: 4.00/4.00)
- **Thesis:** Simulation & Measurement of Zinc Oxide Thin-film Transistors

Xi'an Jiaotong-Liverpool University — B.Eng. in Electronic Science and Technology — **Sept 2011 - Sept 2015**, Suzhou, China

- **Degree:** 2+2 Joint Degree with University of Liverpool

Highlight of Research

Interest	Digital Circuit Design, Computer Architecture, Artificial Intelligence
Expertise	Recurrent Neural Networks ASIC design from RTL to GDS FPGA design from RTL to implementation & real-world demonstration
Best Papers	IEEE AICAS 2020
Bibliometrics	Google scholar metrics as of 10 Jan 2021:



Publications

2020

[1] C. Gao, A. Rios-Navarro, X. Chen, S.-C. Liu, and T. Delbruck, "EdgeDRNN: Recurrent Neural Network Accelerator for Edge Inference," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, 10(4):419-432, 2020 **(Demo)**

[2] C. Gao*, R. Gehlhar*, A. D. Ames, S. C. Liu, and T. Delbruck, "Recurrent Neural Network Control of a Hybrid Dynamical Transfemoral Prosthesis with EdgeDRNN Accelerator," in *IEEE International Conference on Robotics and Automation (ICRA)*, pp. 5460–5466, 2020 **(Talk, Demo)**

[3] C. Gao, A. Rios-Navarro, X. Chen, T. Delbruck, and S. C. Liu, "EdgeDRNN: Enabling Low-latency Recurrent Neural Network Edge Inference," in *IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, pp. 41–45, 2020 **(Talk, Best Paper Award)**

2019

[4] C. Gao, S. Braun, I. Kiselev, J. Anumula, T. Delbruck, and S. C. Liu, "Real-time speech recognition for iot purpose using a delta recurrent neural network accelerator," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, 2019 **(Demo)**

[5] C. Gao, S. Braun, I. Kiselev, J. Anumula, T. Delbruck, and S. C. Liu, "Live demonstration: Real-time spoken digit recognition using the DeltaRNN accelerator," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–1, 2019 **(Demo)**

2018

[6] C. Gao, D. Neil, E. Ceolini, S.-C. Liu, and T. Delbruck, "DeltaRNN: A Power-efficient Recurrent Neural Network Accelerator," in *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 21-30, 2018 **(Acceptance Rate: 9%)**

2017

[7] C. Gao, S. Ghoreishizadeh, Y. Liu, and T. Constandinou, "On-chip ID generation for multi-node implantable devices using SA-PUF," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–4, 2017

2015

[8] A. Shaw, C. Gao, J. D. Jin, I. Z. Mitrovic, and S. Hall, "Characterisation and modelling of Mg doped ZnO TFTs," in *11th Conference on Ph.D. Research in Microelectronics and Electronics, PRIME 2015*, pp. 153–156, 2015

Honors & Achievements

Misha Mahowald Prize for Neuromorphic Engineering — **Dec 2020**, Misha Mahowald Prize Committee

Awarded to the team led by Prof. Shih-Chii Liu for their pioneering "Dynamic Audio Sensor, DAS" that emulates processing principles found in the biological hearing sensors. Team members who contributed to this project are: Minhao Yang, **Chang Gao**, Enea Ceolini, Adrian Huber, Jithendar Anumula, Ilya Kiselev, Daniel Neil, Tobi Delbruck, and Shih-Chii Liu.

Best Paper Award of IEEE AICAS 2020 — **Sept 2020**, IEEE

Awarded to my paper "EdgeDRNN: Enabling Low-latency Recurrent Neural Network Edge Inference" presented in the 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS).

GRC Travel Grant — **July 2019**, University of Zürich

1,900 CHF travel grant for my participance in the 2019 Telluride Neuromorphic Cognition Engineering Workshop in Telluride, Colorado, USA.

Outstanding Achievement in MSc Analogue and Digital Integrated Circuit Design — **Oct 2016**, Imperial College London

The prize acknowledges the top student achieving high standard of work in MSc Analogue and Digital Integrated Circuit Design at the Department of Electrical and Electronic Engineering

Scholarship for International Undergraduate Students from XJTLU — **Sep 2013**, University of Liverpool

50% discount of the tuition fees (~£8,000) awarded to the top student in the program

Progression Scholarship in XJTLU — **Sep 2013**, Xi'an Jiaotong-Liverpool University

Academic Excellence Award for Top 5% students in XJTLU in each program.

Review Appointments

Journals

- IEEE Transactions on Circuits and Systems I: Regular Papers
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems
- Neural Networks

Conferences

- IEEE International Symposium on Circuits and Systems
- IEEE International Conference on Artificial Intelligence Circuits and Systems

Technical Skills

Hardware	FPGA, ASIC, Microcontrollers
Coding	SystemVerilog, Python, PyTorch, C/C++, MATLAB, VHDL, Perl, TensorFlow
Tools	Vivado, ModelSim, Design Compiler, Innovus, Xilinx HLS, Virtuoso

References

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IEEE Senior Member

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