

# CHANG GAO

Ph.D. Student at the Institute of Neuroinformatics  
University of Zurich & ETH Zurich

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## EDUCATION

Ph.D. in Neuroscience

Institute of Neuroinformatics, University of Zurich & ETH Zurich

Jan 2017 – Ongoing Zurich, Switzerland

- Focused on designing **energy-efficient** recurrent neural network (RNN) accelerators for **edge** inference & training.
- Published in **FPGA & ICRA**, top conferences in the field of FPGA and robotics.
- **FPGA development experience** from RTL design to implementation and hardware debugging.
- **ASIC development experience** from RTL design to layout and GDS.
- Have used my accelerators to solve challenging **real-time tasks**, i.e. **speech recognition** and **human-in-the-loop control**.

MSc in Analog and Digital Integrated Circuit Design

Imperial College London

Sept 2015 – Sept 2016 London, United Kingdom

- Distinction Degree; GPA: 4.00 out of 4.25; Rank in program: Top #1
- **Full-custom design experience** of mixed-signal circuits.
- Thesis on full-custom design of a mixed-signal random number generator using sense-amplifiers using 350 nm tech node.
- Thesis scored the highest in my MSc program and a related paper published in ISCAS 2017.

BEng in Electronics

University of Liverpool & Xi'an Jiaotong-Liverpool University

Sept 2011 – June 2015 Liverpool, United Kingdom

- First Class Honor Degree; GPA: 4.00 out of 4.25
- Joint bachelor degrees from both universities
- Thesis on establishing mathematical models to predict voltage-current characteristics of thin-film transistors

## SELECTED PUBLICATIONS

DeltaRNN: A Power-efficient Recurrent Neural Network Accelerator

ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2018), as the first author

- Google Scholar Citation: 55
- First hardware accelerator to exploit temporal sparsity of RNNs.
- Achieved 1.2 TOPS throughput and 166 GOPS/W energy efficiency without batching in GRU-RNN inference, which is the state-of-the-art at the time.

Recurrent Neural Network Control of a Hybrid Dynamic Transfemoral Prosthesis with EdgeDRNN Accelerator

## BASIC INFORMATION

Nationality: Chinese  
Date of Birth: 22/04/1992  
Marital Status: Single  
Mobile: +41 78 652 66 72  
Skype: chang.gao1992  
LinkedIn: https://cutt.ly/oyLmLmu  
Google Scholar: https://cutt.ly/vyLmSLN  
Personal Website: https://changgao.site

## PERSONAL STATEMENT

I am a fourth-year PhD student at the Institute of Neuroinformatics, UZH & ETHZ supervised by Prof. Dr. Shih-Chii Liu and Prof. Dr. Tobi Delbruck. I am working on the Neuromorphic Processor Project sponsored by the Samsung Advanced Institute of Technology. My research interest is on hardware acceleration of deep neural networks computation and its applications on edge devices.

## STRENGTHS

Hard-working Self-motivated  
Problem Solving Time Management  
Good Presenter Teamwork Leader

## AWARDS

**Best Paper Award at AICAS 2020**  
For our paper "EdgeDRNN: Enabling Low-latency Recurrent Neural Network Edge Inference" with \$800 cash prize.

**GRC Travel Grant**  
1,900 CHF travel grant for participating in the 2019 Telluride Neuromorphic Cognition Engineering Workshop in Telluride, Colorado, USA.

**Outstanding Achievement in MSc Analogue and Digital Integrated Circuit Design**  
To acknowledge the top 1 student in the MSc program by Imperial College London

**Scholarship from University of Liverpool**  
50% discount of the tuition fees (£8,000) awarded to the top student in the program

## IEEE International Conference on Robotics and Automation (ICRA 2020), as the co-first author

- Google Scholar Citation: 2
- End-to-end RNN control of a robotic prosthesis functioning with a human in the real-world
- First work to use a hardware-accelerated RNN for real-time control

## Real-Time Speech Recognition for IoT Purpose Using a Delta Recurrent Neural Network Accelerator

### IEEE International Symposium on Circuits and Systems (ISCAS 2019), as the first author

- Google Scholar Citation: 10
- The first instance of a continuous speech recognition system using event-drive silicon cochlea based audio front-end.

## [Best Paper Award] EdgeDRNN: Enabling Low-latency Recurrent Neural Network Edge Inference

### IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2020), as the first author

- Google Scholar Citation: 4
- A delta GRU-RNN accelerator for edge applications
- Achieved sub-millisecond latency for large multi-layer GRU-RNN inference; faster with low power versus various commercial products including NVIDIA Jetson Nano, Jetson TX2, Google Edge TPU & Intel Neural Compute Stick.

## On-chip ID generation for multi-node implantable devices using SA-PUF

### IEEE International Symposium on Circuits and Systems (ISCAS 2017), as the first author

- Google Scholar Citation: 1
- Paper based on my MSc thesis.
- Design of a physical unclonable function mixed-signal circuit using sense-amplifiers for identifying implantable chips.

## REVIEW APPOINTMENTS

### Journals

- IEEE Transactions on Circuits and Systems I: Regular Papers
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems
- Neural Networks

### Conferences

- IEEE International Symposium on Circuits and Systems
- IEEE International Conference on Artificial Intelligence Circuits and Systems



### XJTLU Progression Scholarship

Academic Excellence Award for  
Top 5% students in Xi'an Jiaotong-  
Liverpool University

## SKILLS

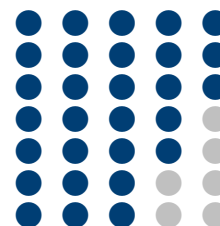
### Hardware

FPGA  
Microcontroller  
PCB



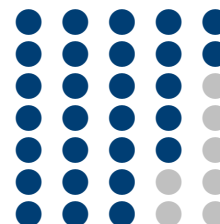
### Coding

SystemVerilog  
Python  
PyTorch  
C/C++  
MATLAB  
VHDL  
TensorFlow



### Tools

Linux  
Xilinx Vivado  
ModelSim  
Design Compiler  
Innovus  
Xilinx HLS  
KiCad



### Languages

Chinese  
English



## REFEREES

### Prof. Dr. Shih-Chii Liu

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