EE 599 Spring 2020

Homework1

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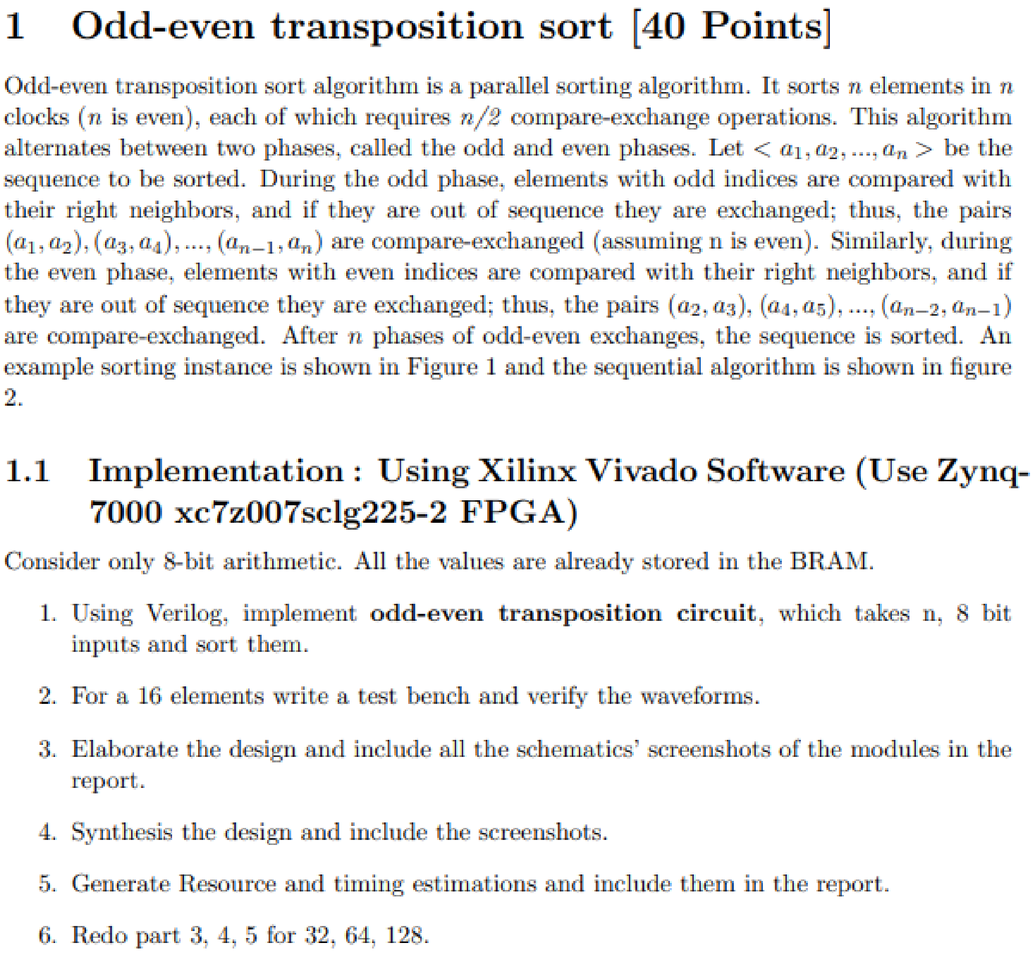
2020/03/05

https://github.com/gaochaousc/EE-599_-gaoc-_-4458723430-



1 Odd-even transposition sort [40 Points]

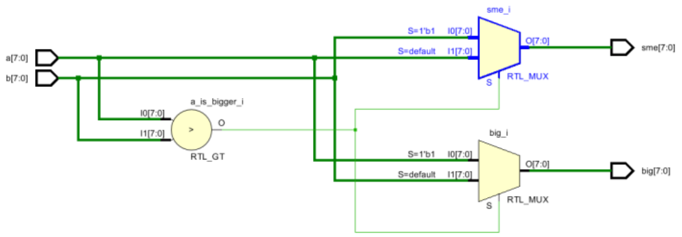
Odd-even transposition sort algorithm is a parallel sorting algorithm. It sorts n elements in n clocks (n is even), each of which requires $n/2$ compare-exchange operations. This algorithm alternates between two phases, called the odd and even phases. Let $< a_1, a_2, ..., a_n >$ be the sequence to be sorted. During the odd phase, elements with odd indices are compared with their right neighbors, and if they are out of sequence they are exchanged; thus, the pairs $(a_1, a_2), (a_3, a_4), ..., (a_{n-1}, a_n)$ are compare-exchanged (assuming n is even). Similarly, during the even phase, elements with even indices are compared with their right neighbors, and if they are out of sequence they are exchanged; thus, the pairs (a_2, a_3), (a_4, a_5), ..., (a_{n-2}, a_{n-1}) are compare-exchanged. After n phases of odd-even exchanges, the sequence is sorted. An example sorting instance is shown in Figure 1 and the sequential algorithm is shown in figure 2.

1.1 Implementation : Using Xilinx Vivado Software (Use Zynq-7000 xc7z007sclg225-2 FPGA)

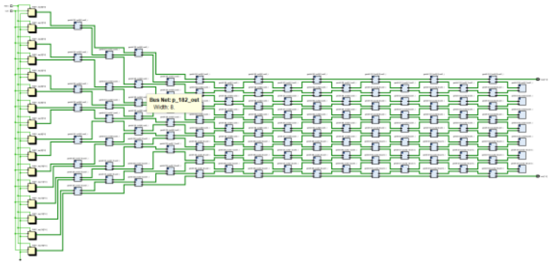
Consider only 8-bit arithmetic. All the values are already stored in the BRAM.

1. Using Verilog, implement **odd-even transposition circuit**, which takes n, 8 bit inputs and sort them.
2. For a 16 elements write a test bench and verify the waveforms.
3. Elaborate the design and include all the schematics' screenshots of the modules in the report.
4. Synthesis the design and include the screenshots.
5. Generate Resource and timing estimations and include them in the report.
6. Redo part 3, 4, 5 for 32, 64, 128.

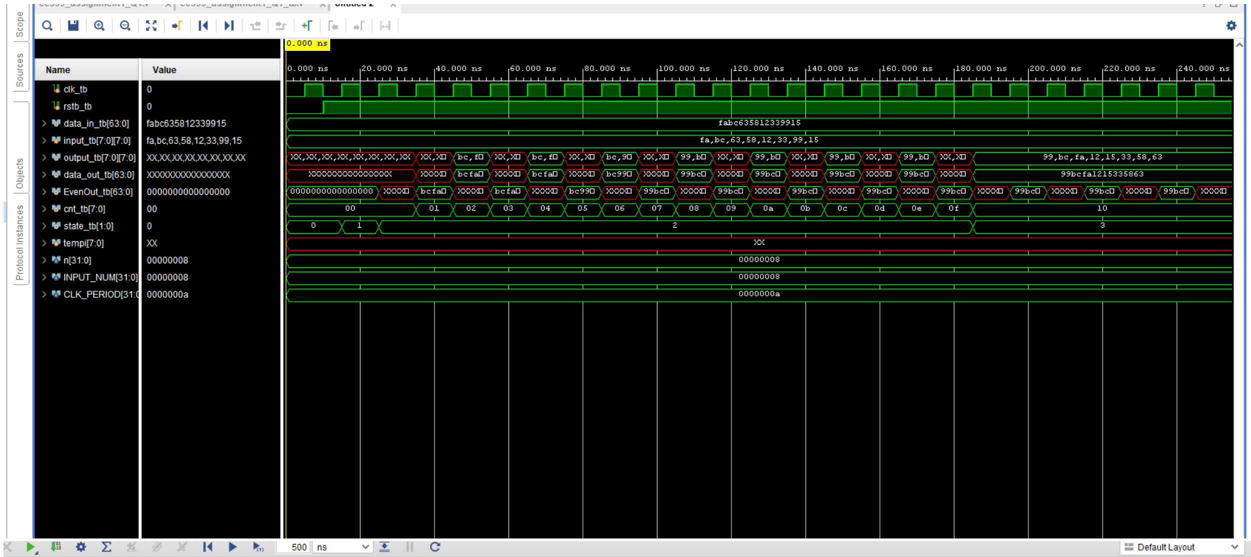
1. Schematic's screenshots
    a. CaS model: this is the model that compare two 8-bit number A and B, and sort them in the order of magnitude.



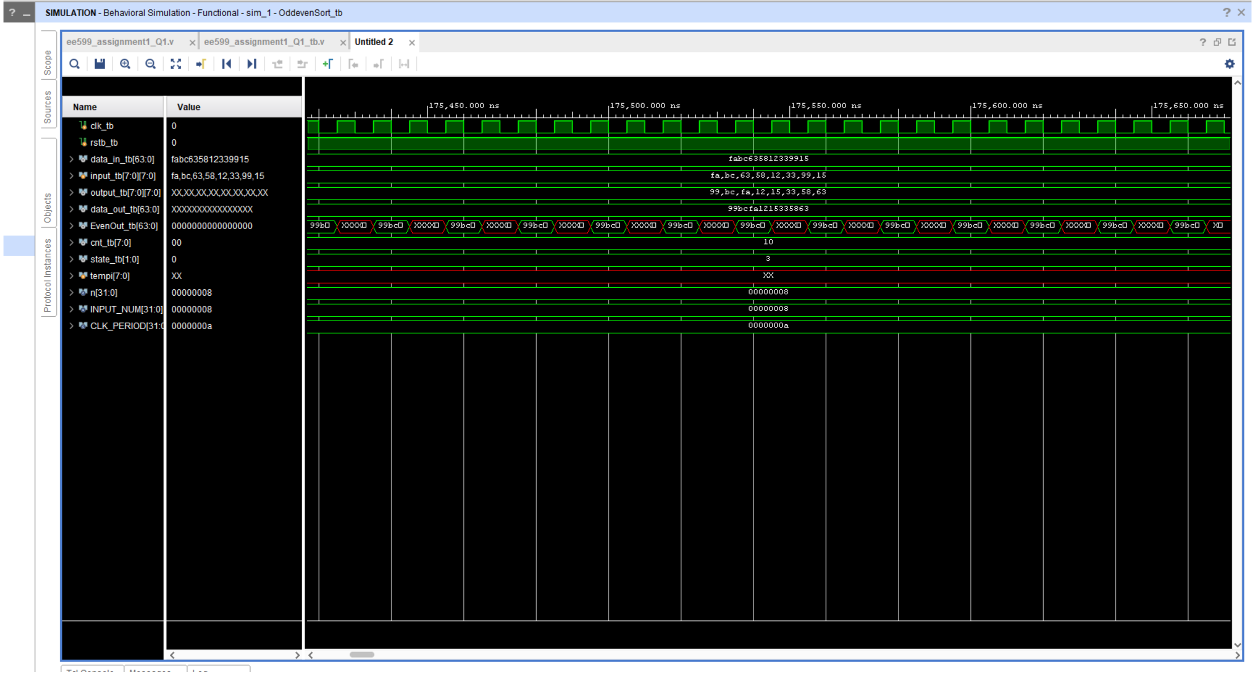
b. OES is the top module of the design (the schematic of 32,64,128 will be included in the later part of the report)



c. Function waveform
In this simulation, we can get the output in order of big and small



```
Name                 Value
clk_tb               0
rstb_tb              0
data_in_tb[63:0]     fabc635812339915
input_tb[7:0][7:0]   fa,bc,63,58,12,33,99,15
output_tb[7:0][7:0]  XX,XX,XX,XX,XX,XX,XX,XX
data_out_tb[63:0]    XXXXXXXXXXXXXXXX
EvenOut_tb[63:0]     0000000000000000
cnt_tb[7:0]          00
state_tb[1:0]        0
tempi[7:0]           XX
n[31:0]              00000008
INPUT_NUM[31:0]      00000008
CLK_PERIOD[31:0      0000000a
```

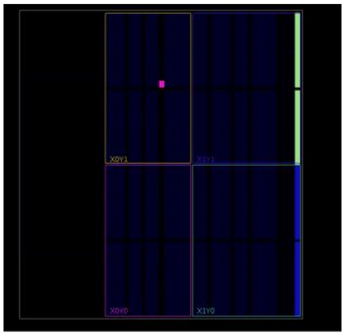


SIMULATION - Behavioral Simulation - Functional - sim_1 - OddevenSort_tb

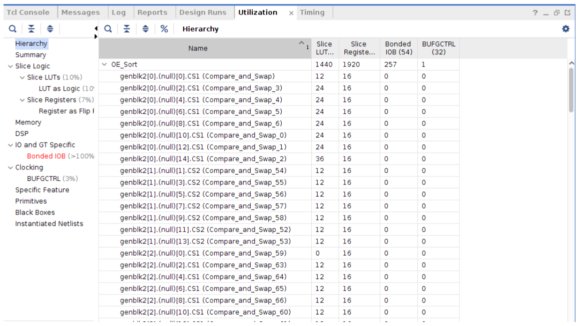
```
Name                 Value
clk_tb               0
rstb_tb              0
data_in_tb[63:0]     fabc635812339915
input_tb[7:0][7:0]   fa,bc,63,58,12,33,99,15
output_tb[7:0][7:0]  XX,XX,XX,XX,XX,XX,XX,XX
data_out_tb[63:0]    XXXXXXXXXXXXXXXX
EvenOut_tb[63:0]     0000000000000000
cnt_tb[7:0]          00
state_tb[1:0]        0
tempi[7:0]           XX
n[31:0]              00000008
INPUT_NUM[31:0]      00000008
CLK_PERIOD[31:0      0000000a
```

d. Simulation Report for 16 elements:

Synthesis and report:

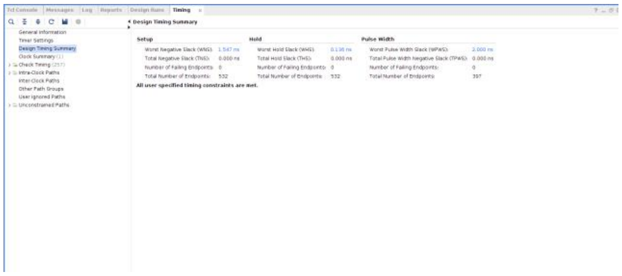


1. Resource estimation



Name	Slice LUT...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
OE_Sort	1440	1920	257	1
genblk2[0].(null)[0].CS1 (Compare_and_Swap)	12	16	0	0
genblk2[0].(null)[2].CS1 (Compare_and_Swap_3)	24	16	0	0
genblk2[0].(null)[4].CS1 (Compare_and_Swap_4)	24	16	0	0
genblk2[0].(null)[6].CS1 (Compare_and_Swap_5)	24	16	0	0
genblk2[0].(null)[8].CS1 (Compare_and_Swap_6)	24	16	0	0
genblk2[0].(null)[10].CS1 (Compare_and_Swap_0)	24	16	0	0
genblk2[0].(null)[12].CS1 (Compare_and_Swap_1)	24	16	0	0
genblk2[0].(null)[14].CS1 (Compare_and_Swap_2)	36	16	0	0
genblk2[1].(null)[1].CS2 (Compare_and_Swap_54)	12	16	0	0
genblk2[1].(null)[3].CS2 (Compare_and_Swap_55)	12	16	0	0
genblk2[1].(null)[5].CS2 (Compare_and_Swap_56)	12	16	0	0
genblk2[1].(null)[7].CS2 (Compare_and_Swap_57)	12	16	0	0
genblk2[1].(null)[9].CS2 (Compare_and_Swap_58)	12	16	0	0
genblk2[1].(null)[11].CS2 (Compare_and_Swap_52)	12	16	0	0
genblk2[1].(null)[13].CS2 (Compare_and_Swap_53)	12	16	0	0
genblk2[2].(null)[0].CS1 (Compare_and_Swap_59)	0	16	0	0
genblk2[2].(null)[2].CS1 (Compare_and_Swap_63)	12	16	0	0
genblk2[2].(null)[4].CS1 (Compare_and_Swap_64)	12	16	0	0
genblk2[2].(null)[6].CS1 (Compare_and_Swap_65)	12	16	0	0
genblk2[2].(null)[8].CS1 (Compare_and_Swap_66)	12	16	0	0
genblk2[2].(null)[10].CS1 (Compare_and_Swap_60)	12	16	0	0

2. Timing estimation

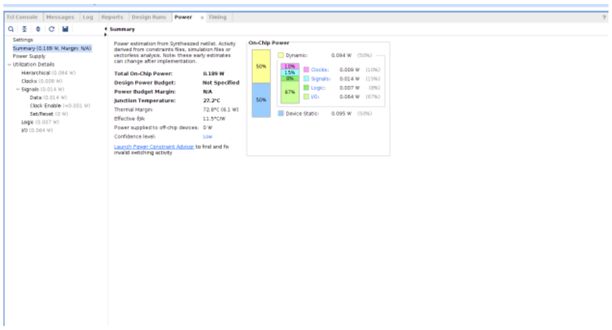


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.547 ns	Worst Hold Slack (WHS):	0.136 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	532	Total Number of Endpoints:	532	Total Number of Endpoints:	397

All user specified timing constraints are met.

3. Power estimation



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.189 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.2°C**
Thermal Margin:	72.8°C (6.1 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

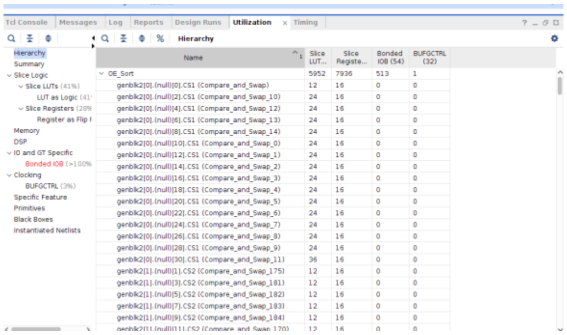
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.094 W	(50%)
Clocks:	0.009 W	(10%)
Signals:	0.014 W	(15%)
Logic:	0.007 W	(8%)
I/O:	0.064 W	(67%)
Device Static:	0.095 W	(50%)

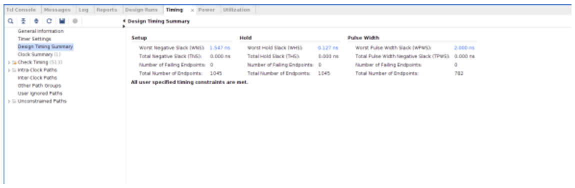
e. Simulation for 32 elements

1. Resource estimation



Name	Slice LUT...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
OE_Sort	5952	7936	513	1
genblk2[0].(null)[0].CS1 (Compare_and_Swap)	12	16	0	0
genblk2[0].(null)[2].CS1 (Compare_and_Swap_10)	24	16	0	0
genblk2[0].(null)[4].CS1 (Compare_and_Swap_12)	24	16	0	0
genblk2[0].(null)[6].CS1 (Compare_and_Swap_13)	24	16	0	0
genblk2[0].(null)[8].CS1 (Compare_and_Swap_14)	24	16	0	0
genblk2[0].(null)[10].CS1 (Compare_and_Swap_0)	24	16	0	0
genblk2[0].(null)[12].CS1 (Compare_and_Swap_1)	24	16	0	0
genblk2[0].(null)[14].CS1 (Compare_and_Swap_2)	24	16	0	0
genblk2[0].(null)[16].CS1 (Compare_and_Swap_3)	24	16	0	0
genblk2[0].(null)[18].CS1 (Compare_and_Swap_4)	24	16	0	0
genblk2[0].(null)[20].CS1 (Compare_and_Swap_5)	24	16	0	0
genblk2[0].(null)[22].CS1 (Compare_and_Swap_6)	24	16	0	0
genblk2[0].(null)[24].CS1 (Compare_and_Swap_7)	24	16	0	0
genblk2[0].(null)[26].CS1 (Compare_and_Swap_8)	24	16	0	0
genblk2[0].(null)[28].CS1 (Compare_and_Swap_9)	24	16	0	0
genblk2[0].(null)[30].CS1 (Compare_and_Swap_11)	36	16	0	0
genblk2[1].(null)[1].CS2 (Compare_and_Swap_175)	12	16	0	0
genblk2[1].(null)[3].CS2 (Compare_and_Swap_181)	12	16	0	0
genblk2[1].(null)[5].CS2 (Compare_and_Swap_182)	12	16	0	0
genblk2[1].(null)[7].CS2 (Compare_and_Swap_183)	12	16	0	0
genblk2[1].(null)[9].CS2 (Compare_and_Swap_184)	12	16	0	0
genblk2[1].(null)[11].CS2 (Compare_and_Swap_170)	12	16	0	0

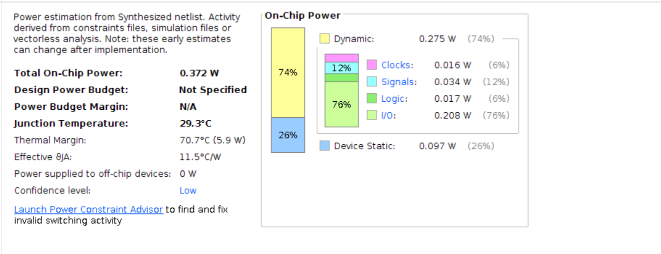
2. Timing estimation



```
Design Timing Summary

Setup                                       Hold                                        Pulse Width
  Worst Negative Slack (WNS):     1.547 ns    Worst Hold Slack (WHS):         0.127 ns    Worst Pulse Width Slack (WPWS):            2.000 ns
  Total Negative Slack (TNS):     0.000 ns    Total Hold Slack (THS):         0.000 ns    Total Pulse Width Negative Slack (TPWS):   0.000 ns
  Number of Failing Endpoints:    0           Number of Failing Endpoints:    0           Number of Failing Endpoints:               0
  Total Number of Endpoints:      1045        Total Number of Endpoints:      1045        Total Number of Endpoints:                 782
All user specified timing constraints are met.
```

3. Power estimation



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.372 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**29.3°C**
Thermal Margin:	70.7°C (5.9 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

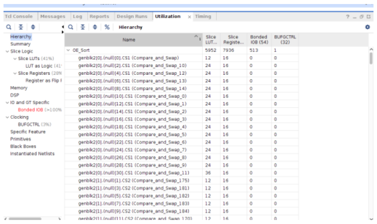
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.275 W	(74%)
Clocks:	0.016 W	(6%)
Signals:	0.034 W	(12%)
Logic:	0.017 W	(6%)
I/O:	0.208 W	(76%)
Device Static:	0.097 W	(26%)

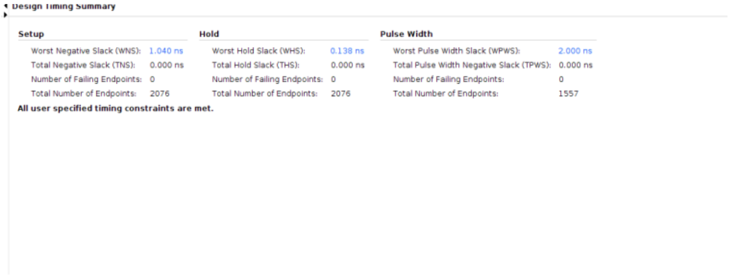
f. Simulation for 64 elements

1. Resource estimation



Name	Slice LUT...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
OE_Sort	5952	7936	513	1
genblk2[0].(null)[0].CS1 (Compare_and_Swap)	12	16	0	0
genblk2[0].(null)[2].CS1 (Compare_and_Swap_10)	24	16	0	0
genblk2[0].(null)[4].CS1 (Compare_and_Swap_12)	24	16	0	0
genblk2[0].(null)[6].CS1 (Compare_and_Swap_13)	24	16	0	0
genblk2[0].(null)[8].CS1 (Compare_and_Swap_14)	24	16	0	0
genblk2[0].(null)[10].CS1 (Compare_and_Swap_0)	24	16	0	0
genblk2[0].(null)[12].CS1 (Compare_and_Swap_1)	24	16	0	0
genblk2[0].(null)[14].CS1 (Compare_and_Swap_2)	24	16	0	0
genblk2[0].(null)[16].CS1 (Compare_and_Swap_3)	24	16	0	0
genblk2[0].(null)[18].CS1 (Compare_and_Swap_4)	24	16	0	0
genblk2[0].(null)[20].CS1 (Compare_and_Swap_5)	24	16	0	0
genblk2[0].(null)[22].CS1 (Compare_and_Swap_6)	24	16	0	0
genblk2[0].(null)[24].CS1 (Compare_and_Swap_7)	24	16	0	0
genblk2[0].(null)[26].CS1 (Compare_and_Swap_8)	24	16	0	0
genblk2[0].(null)[28].CS1 (Compare_and_Swap_9)	24	16	0	0
genblk2[0].(null)[30].CS1 (Compare_and_Swap_11)	36	16	0	0
genblk2[1].(null)[1].CS2 (Compare_and_Swap_175)	12	16	0	0
genblk2[1].(null)[3].CS2 (Compare_and_Swap_181)	12	16	0	0
genblk2[1].(null)[5].CS2 (Compare_and_Swap_182)	12	16	0	0
genblk2[1].(null)[7].CS2 (Compare_and_Swap_183)	12	16	0	0
genblk2[1].(null)[9].CS2 (Compare_and_Swap_184)	12	16	0	0
genblk2[1].(null)[11].CS2 (Compare_and_Swap_170)	12	16	0	0

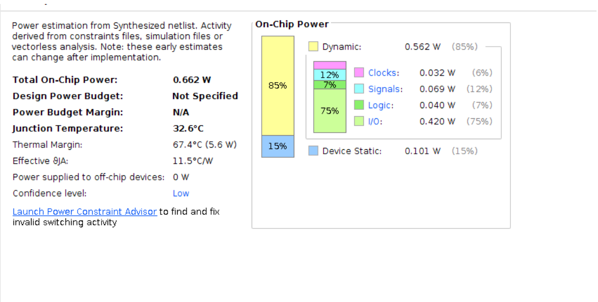
2. Timing estimation



```
Design Timing Summary

Setup                                       Hold                                        Pulse Width
  Worst Negative Slack (WNS):     1.040 ns    Worst Hold Slack (WHS):         0.138 ns    Worst Pulse Width Slack (WPWS):            2.000 ns
  Total Negative Slack (TNS):     0.000 ns    Total Hold Slack (THS):         0.000 ns    Total Pulse Width Negative Slack (TPWS):   0.000 ns
  Number of Failing Endpoints:    0           Number of Failing Endpoints:    0           Number of Failing Endpoints:               0
  Total Number of Endpoints:      2076        Total Number of Endpoints:      2076        Total Number of Endpoints:                 1557
All user specified timing constraints are met.
```

3. Power estimation



Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.662 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**32.6°C**
Thermal Margin:	67.4°C (5.6 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

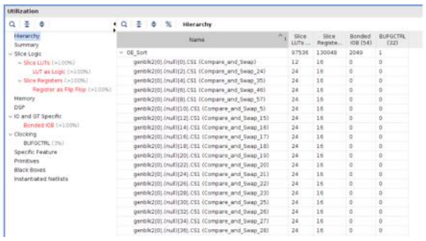
Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.562 W	(85%)
Clocks:	0.032 W	(6%)
Signals:	0.069 W	(12%)
Logic:	0.040 W	(7%)
I/O:	0.420 W	(75%)
Device Static:	0.101 W	(15%)

g. Simulation for 128 elements

1. Resource estimation

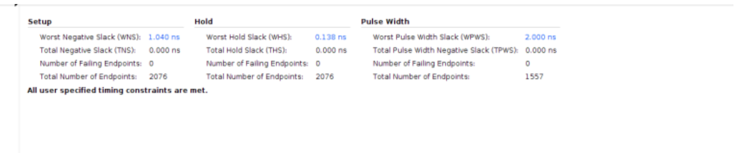

Utilization

Hierarchy
Summary
Slice Logic
Slice LUTs (>100%)
LUT as Logic (>100%)
Slice Registers (>100%)
Register as Flip Flop (>100%)
Memory
DSP
IO and GT Specific
Bonded IOB (>100%)
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
Instantiated Netlists

Hierarchy

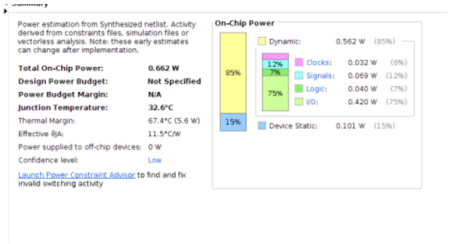
Name	Slice LUTs ...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
OE_Sort	97536	130048	2049	1
genblk2[0].(null)[0].CS1 (Compare_and_Swap)	12	16	0	0
genblk2[0].(null)[2].CS1 (Compare_and_Swap_24)	24	16	0	0
genblk2[0].(null)[4].CS1 (Compare_and_Swap_35)	24	16	0	0
genblk2[0].(null)[6].CS1 (Compare_and_Swap_46)	24	16	0	0
genblk2[0].(null)[8].CS1 (Compare_and_Swap_57)	24	16	0	0
genblk2[0].(null)[10].CS1 (Compare_and_Swap_5)	24	16	0	0
genblk2[0].(null)[12].CS1 (Compare_and_Swap_15)	24	16	0	0
genblk2[0].(null)[14].CS1 (Compare_and_Swap_16)	24	16	0	0
genblk2[0].(null)[16].CS1 (Compare_and_Swap_17)	24	16	0	0
genblk2[0].(null)[18].CS1 (Compare_and_Swap_18)	24	16	0	0
genblk2[0].(null)[20].CS1 (Compare_and_Swap_19)	24	16	0	0
genblk2[0].(null)[22].CS1 (Compare_and_Swap_20)	24	16	0	0
genblk2[0].(null)[24].CS1 (Compare_and_Swap_21)	24	16	0	0
genblk2[0].(null)[26].CS1 (Compare_and_Swap_22)	24	16	0	0
genblk2[0].(null)[28].CS1 (Compare_and_Swap_23)	24	16	0	0
genblk2[0].(null)[30].CS1 (Compare_and_Swap_25)	24	16	0	0
genblk2[0].(null)[32].CS1 (Compare_and_Swap_26)	24	16	0	0
genblk2[0].(null)[34].CS1 (Compare_and_Swap_27)	24	16	0	0
genblk2[0].(null)[36].CS1 (Compare_and_Swap_28)	24	16	0	0

2. Timing estimation


Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.040 ns	Worst Hold Slack (WHS):	0.138 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2076	Total Number of Endpoints:	2076	Total Number of Endpoints:	1557

All user specified timing constraints are met.

3. Power estimation


Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.662 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**32.6°C**
Thermal Margin:	67.4°C (5.6 W)
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.562 W	(85%)
Clocks:	0.032 W	(6%)
Signals:	0.069 W	(12%)
Logic:	0.040 W	(7%)
I/O:	0.420 W	(75%)
Device Static:	0.101 W	(15%)

2 Dense Matrix-Matrix Multiplication [60 Points]

2.1 Scalable Multiply and adder tree

If A is an $m \times n$ matrix and B is an $n \times p$ matrix, the matrix product $C = AB$ (denoted without multiplication signs or dots) is defined to be the $m \times p$ matrix such that,

$$c_{i,j} = a_{i,1}b_{1,j} + a_{i,2}b_{2,j} + ... + a_{i,n}b_{n,j} = \sum_{k=1}^{n} a_{i,k}b_{k,j};$$

where for i = 1, ..., m and j = 1, ..., p

Consider two matrices A and B, each having the size of $n \times n$ where n = 2^r.

Figure 3 shows an example design of Multiply and Adder Tree. The adder tree consists of a Multiplication Step following Adder Steps. Given the size of matrices is $n \times n$, there are n multipliers in the first stage. Assume that matrix A saved in row order, and matrix B saved in column order in the memory. In the beginning, the first row of A and the first column of B loaded and multiplied together. Then in each Adder Step, partial sums are added together until it produces the final result corresponding to an element in the output matrix. Adder steps consist of 2 element adders as shown in Figure 2. Notice that Multiply and adder tree is a pipeline process. Notice that in each step, after corresponding rows and columns of A and B going through the pipe, it produces one element of the output matrix.

2.1.1 Design Problems

Consider simple Multiply and Adder Tree design with n element multiplication,

1. How many Multiplier units needed for the entire design?

n

2. Consider an adder stage r, how many adder modules needed for the stage?

$$2^{logn-r}$$

3. If all the inputs to the design represented using k bits, how many bits are needed to represent the final result of the Multiply and Adder Tree?

$$2k\text{-}1+logn$$

4. How may Adder modules need for the entire multiply and adder tree design?

n-1

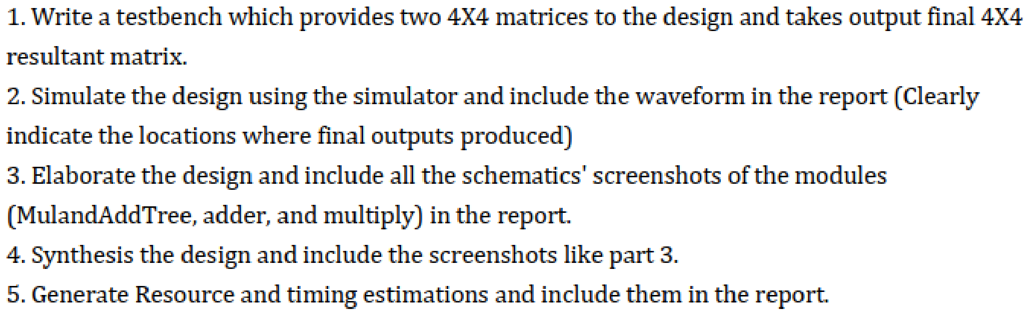
5. How many clock cycles need to produce the first output element in the adder tree?

$$logn + 1$$

6. How many clock cycles need to multiply two n× n matrices?

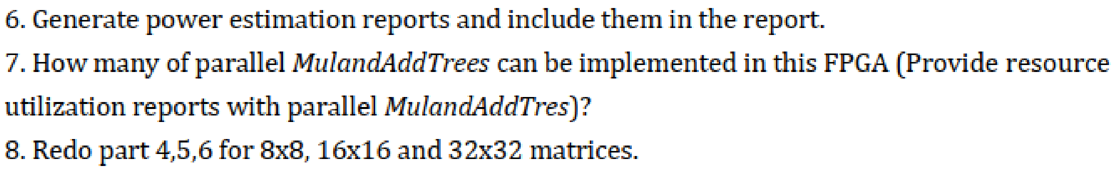
$$n^2 + logn$$

2.1.2 Implementation



1. Write a testbench which provides two 4X4 matrices to the design and takes output final 4X4 resultant matrix.
2. Simulate the design using the simulator and include the waveform in the report (Clearly indicate the locations where final outputs produced)
3. Elaborate the design and include all the schematics' screenshots of the modules (MulandAddTree, adder, and multiply) in the report.
4. Synthesis the design and include the screenshots like part 3.
5. Generate Resource and timing estimations and include them in the report.

Sche



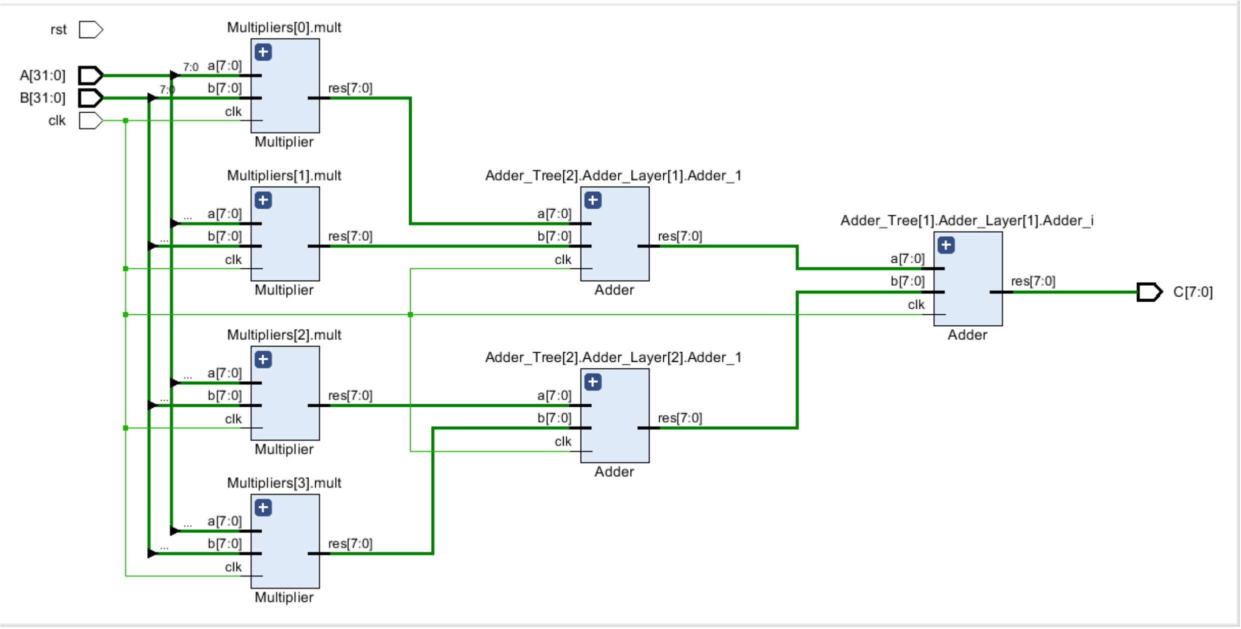
6. Generate power estimation reports and include them in the report.
7. How many of parallel *MulandAddTrees* can be implemented in this FPGA (Provide resource utilization reports with parallel *MulandAddTres*)?
8. Redo part 4,5,6 for 8x8, 16x16 and 32x32 matrices.

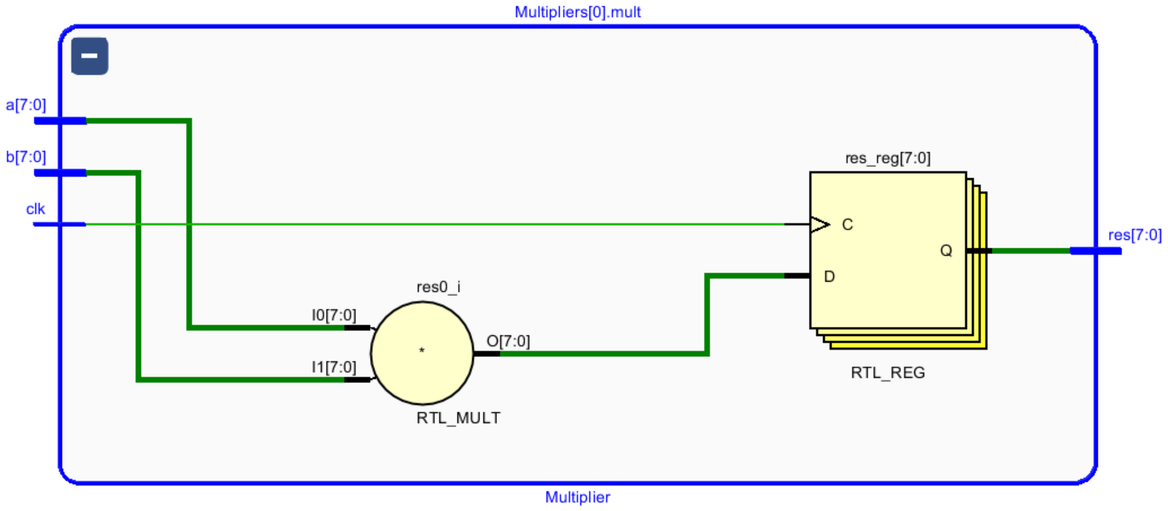
Schematic's screenshots are shown below:

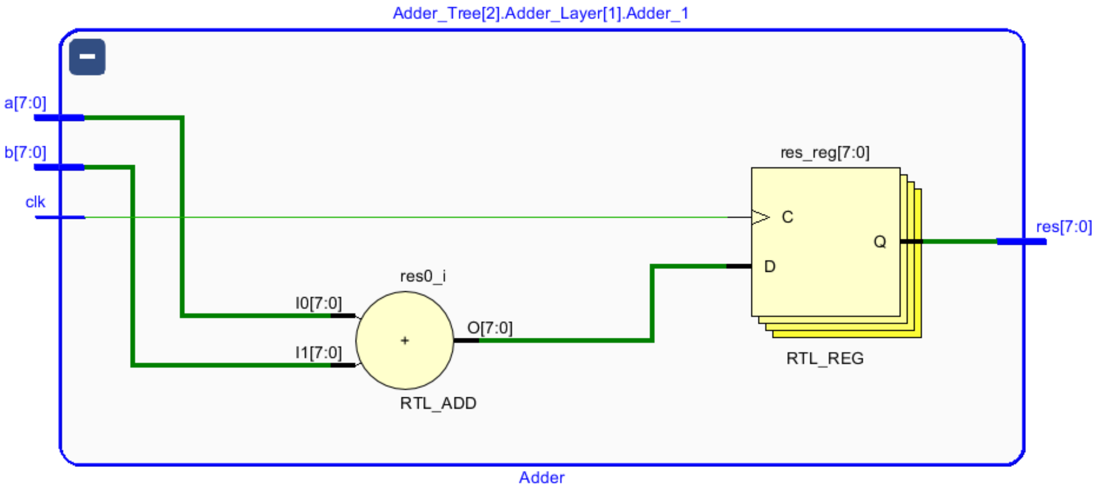
a. Multiply Unit is designed to get the product of two 8-bit number A and B.

b. And according to the number of elements of matrix, combine all the multiply units into Multiply Combination.

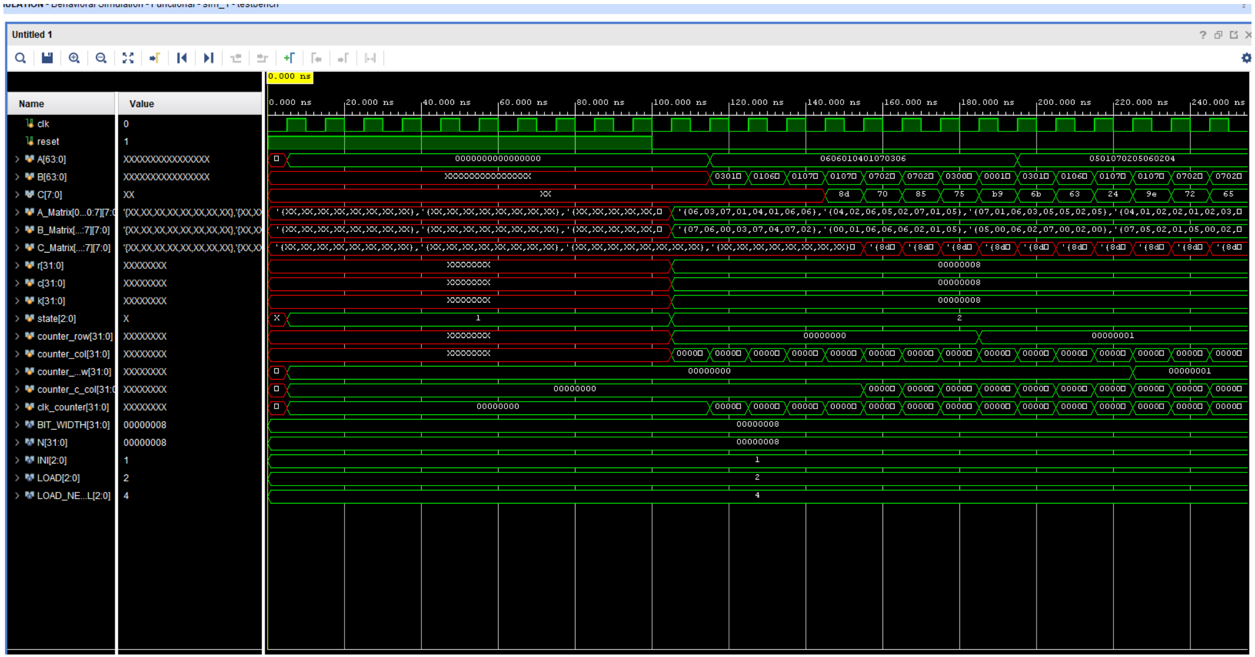
c. For adder, it computes the 4 A and B


rst
A[31:0]
B[31:0]
clk
Multipliers[0].mult
7:0
a[7:0]
b[7:0]
clk
res[7:0]
Multiplier
Multipliers[1].mult
...
a[7:0]
b[7:0]
clk
res[7:0]
Multiplier
Multipliers[2].mult
a[7:0]
b[7:0]
clk
res[7:0]
Multiplier
Multipliers[3].mult
a[7:0]
b[7:0]
clk
res[7:0]
Multiplier
Adder_Tree[2].Adder_Layer[1].Adder_1
a[7:0]
b[7:0]
clk
res[7:0]
Adder
Adder_Tree[2].Adder_Layer[2].Adder_1
a[7:0]
b[7:0]
clk
res[7:0]
Adder
Adder_Tree[1].Adder_Layer[1].Adder_i
a[7:0]
b[7:0]
clk
res[7:0]
Adder
C[7:0]

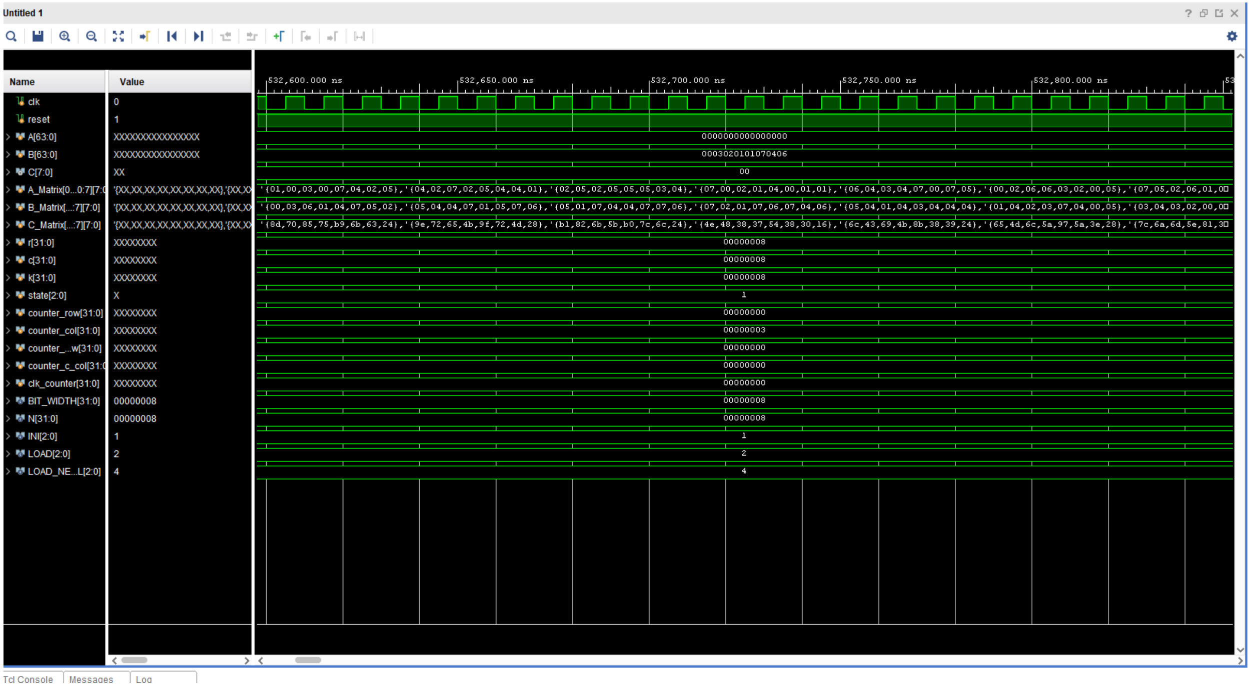




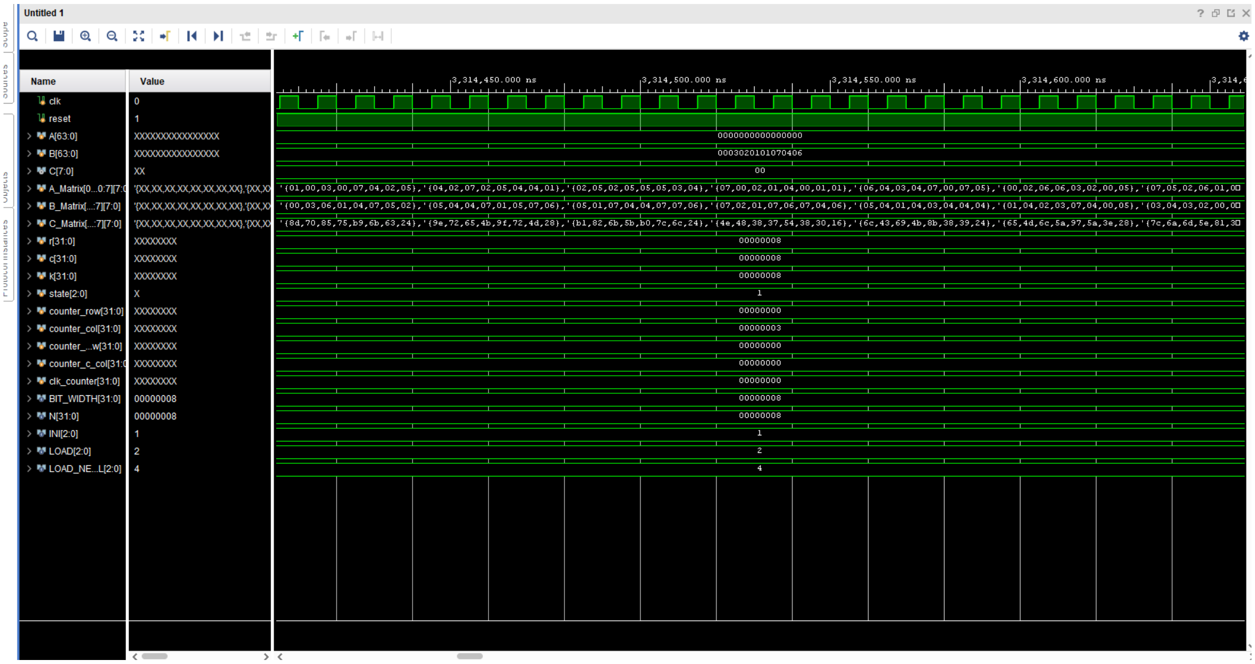
d. Function waveform



Name	Value
clk	0
reset	1
A[63:0]	XXXXXXXXXXXXXXXX
B[63:0]	XXXXXXXXXXXXXXXX
C[7:0]	XX
A_Matrix[0...0:7][7:0	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX
B_Matrix[...:7][7:0]	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX
C_Matrix[...:7][7:0]	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX
r[31:0]	XXXXXXXX
c[31:0]	XXXXXXXX
k[31:0]	XXXXXXXX
state[2:0]	X
counter_row[31:0]	XXXXXXXX
counter_col[31:0]	XXXXXXXX
counter_...w[31:0]	XXXXXXXX
counter_c_col[31:0	XXXXXXXX
clk_counter[31:0]	XXXXXXXX
BIT_WIDTH[31:0]	00000008
N[31:0]	00000008
INI[2:0]	1
LOAD[2:0]	2
LOAD_NE...L[2:0]	4

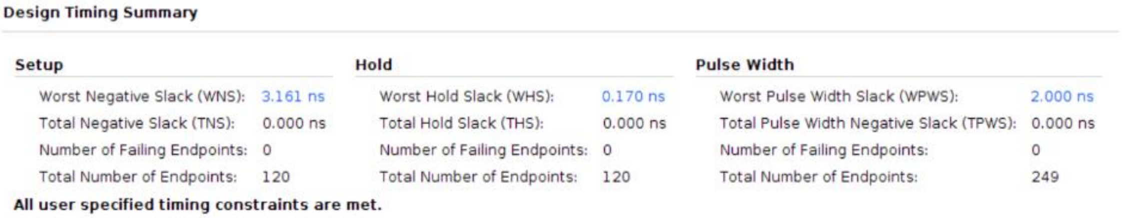


Name	Value
clk	0
reset	1
A[63:0]	XXXXXXXXXXXXXXXX
B[63:0]	XXXXXXXXXXXXXXXX
C[7:0]	XX
A_Matrix[0...0:7][7:0	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX
B_Matrix[...:7][7:0]	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX
C_Matrix[...:7][7:0]	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX
r[31:0]	XXXXXXXX
c[31:0]	XXXXXXXX
k[31:0]	XXXXXXXX
state[2:0]	X
counter_row[31:0]	XXXXXXXX
counter_col[31:0]	XXXXXXXX
counter_...w[31:0]	XXXXXXXX
counter_c_col[31:0	XXXXXXXX
clk_counter[31:0]	XXXXXXXX
BIT_WIDTH[31:0]	00000008
N[31:0]	00000008
INI[2:0]	1
LOAD[2:0]	2
LOAD_NE...L[2:0]	4



Name	Value	
clk	0	
reset	1	
A[63:0]	XXXXXXXXXXXXXXXX	0000000000000000
B[63:0]	XXXXXXXXXXXXXXXX	0003020101070406
C[7:0]	XX	00
A_Matrix[0...0:7][7:0	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX	'{01,00,03,00,07,04,02,05},'{04,02,07,02,05,04,04,01},'{02,05,02,05,05,05,03,04},'{07,00,02,01,04,00,01,01},'{06,04,03,04,07,00,07,05},'{00,02,06,06,03,02,00,05},'{07,05,02,06,01,00
B_Matrix[...:7][7:0]	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX	'{00,03,06,01,04,07,05,02},'{05,04,04,07,01,05,07,06},'{05,01,07,04,04,07,07,06},'{07,02,01,07,06,07,04,06},'{05,04,01,04,03,04,04,04},'{01,04,02,03,07,04,00,05},'{03,04,03,02,00,00
C_Matrix[...:7][7:0]	'{XX,XX,XX,XX,XX,XX,XX,XX},'{XX,XX	'{8d,70,85,75,b9,6b,63,24},'{9e,72,65,4b,9f,72,4d,28},'{b1,82,6b,5b,b0,7c,6c,24},'{4e,48,38,37,54,38,30,16},'{6c,43,69,4b,8b,38,39,24},'{65,4d,6c,5a,97,5a,3e,28},'{7c,6a,6d,5e,81,30
r[31:0]	XXXXXXXX	00000008
c[31:0]	XXXXXXXX	00000008
k[31:0]	XXXXXXXX	00000008
state[2:0]	X	1
counter_row[31:0]	XXXXXXXX	00000000
counter_col[31:0]	XXXXXXXX	00000003
counter_...w[31:0]	XXXXXXXX	00000000
counter_c_col[31:0	XXXXXXXX	00000000
clk_counter[31:0]	XXXXXXXX	00000000
BIT_WIDTH[31:0]	00000008	00000008
N[31:0]	00000008	00000008
INI[2:0]	1	1
LOAD[2:0]	2	2
LOAD_NE...L[2:0]	4	4

e. 8-bit timing analysis



Design Timing Summary

Setup

Worst Negative Slack (WNS):	3.161 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	120

Hold

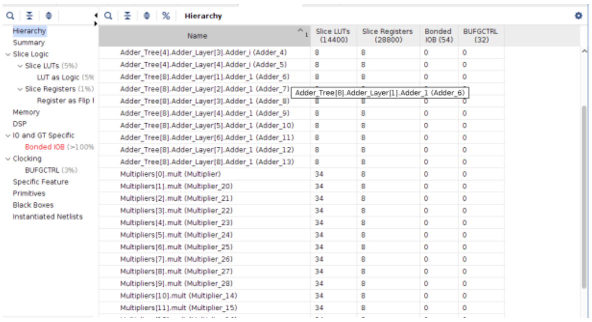
Worst Hold Slack (WHS):	0.170 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	120

Pulse Width

Worst Pulse Width Slack (WPWS):	2.000 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	249

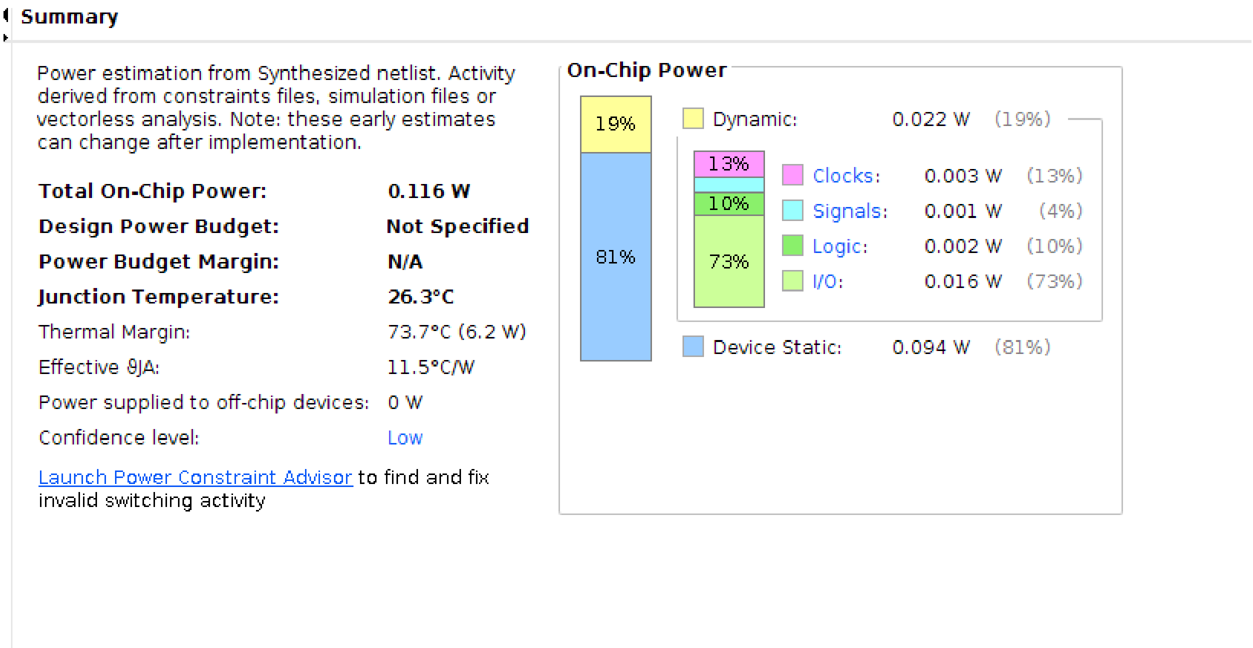
All user specified timing constraints are met.

f. 8-bit resources analysis



Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
Adder_Tree[4].Adder_Layer[3].Adder_i (Adder_4)	8	8	0	0
Adder_Tree[4].Adder_Layer[4].Adder_i (Adder_5)	8	8	0	0
Adder_Tree[8].Adder_Layer[1].Adder_1 (Adder_6)	8	8	0	0
Adder_Tree[8].Adder_Layer[2].Adder_1 (Adder_7)	[illegible]	[illegible]	[illegible]	[illegible]
Adder_Tree[8].Adder_Layer[3].Adder_1 (Adder_8)	8	8	0	0
Adder_Tree[8].Adder_Layer[4].Adder_1 (Adder_9)	8	8	0	0
Adder_Tree[8].Adder_Layer[5].Adder_1 (Adder_10)	8	8	0	0
Adder_Tree[8].Adder_Layer[6].Adder_1 (Adder_11)	8	8	0	0
Adder_Tree[8].Adder_Layer[7].Adder_1 (Adder_12)	8	8	0	0
Adder_Tree[8].Adder_Layer[8].Adder_1 (Adder_13)	8	8	0	0
Multipliers[0].mult (Multiplier)	34	8	0	0
Multipliers[1].mult (Multiplier_20)	34	8	0	0
Multipliers[2].mult (Multiplier_21)	34	8	0	0
Multipliers[3].mult (Multiplier_22)	34	8	0	0
Multipliers[4].mult (Multiplier_23)	34	8	0	0
Multipliers[5].mult (Multiplier_24)	34	8	0	0
Multipliers[6].mult (Multiplier_25)	34	8	0	0
Multipliers[7].mult (Multiplier_26)	34	8	0	0
Multipliers[8].mult (Multiplier_27)	34	8	0	0
Multipliers[9].mult (Multiplier_28)	34	8	0	0
Multipliers[10].mult (Multiplier_14)	34	8	0	0
Multipliers[11].mult (Multiplier_15)	34	8	0	0

g. 8-bit power analysis



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

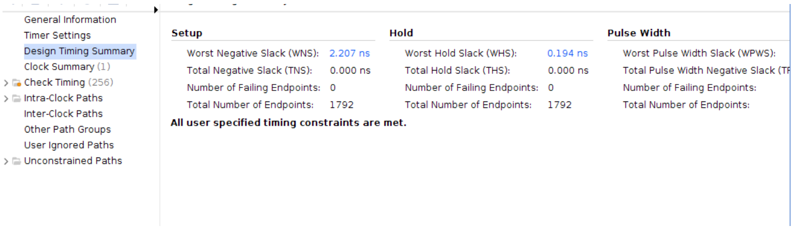
Total On-Chip Power:	**0.116 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.3°C**
Thermal Margin:	73.7°C (6.2 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.022 W	(19%)
Clocks:	0.003 W	(13%)
Signals:	0.001 W	(4%)
Logic:	0.002 W	(10%)
I/O:	0.016 W	(73%)
Device Static:	0.094 W	(81%)

h. 16 inputs timing analysis



Setup

Worst Negative Slack (WNS): 2.207 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1792

Hold

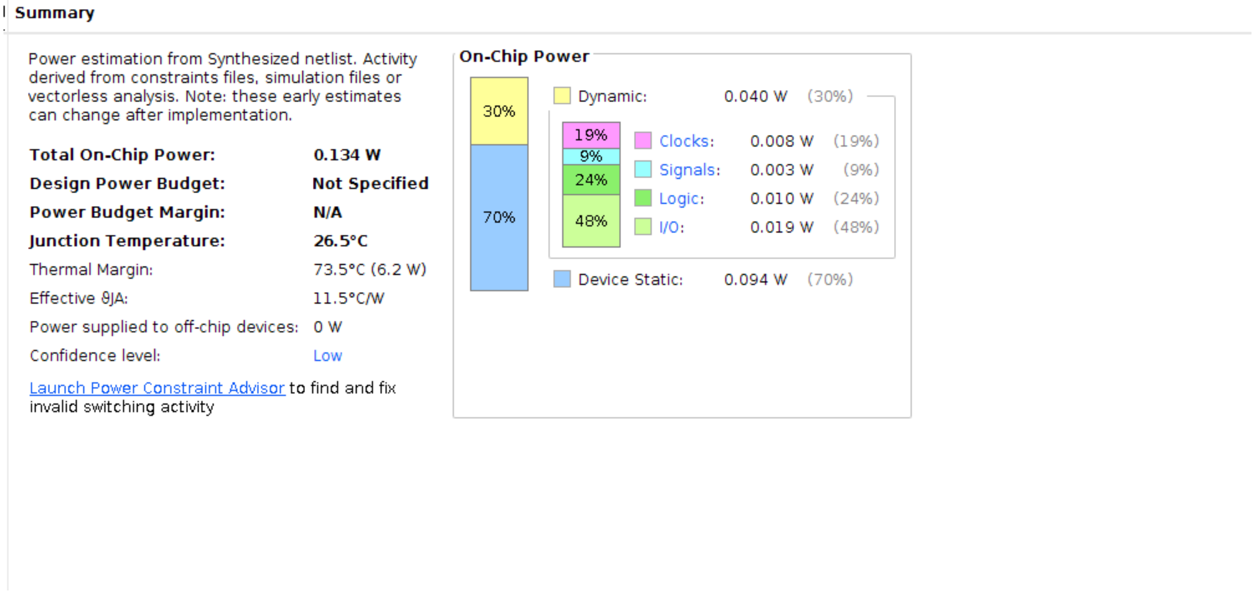
Worst Hold Slack (WHS): 0.194 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1792

Pulse Width

Worst Pulse Width Slack (WPWS):
Total Pulse Width Negative Slack (TP
Number of Failing Endpoints:
Total Number of Endpoints:

All user specified timing constraints are met.

i. 16 inputs power analysis



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

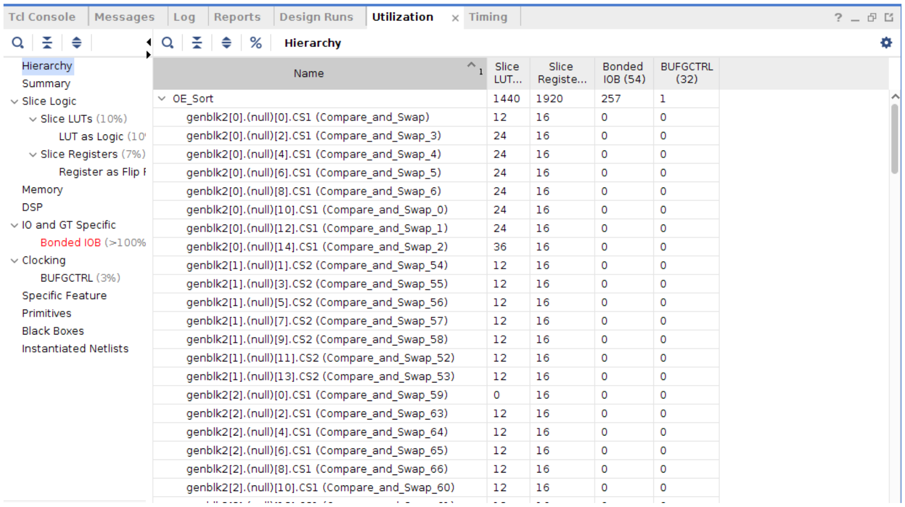
Total On-Chip Power:	**0.134 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**26.5°C**
Thermal Margin:	73.5°C (6.2 W)
Effective ϑJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

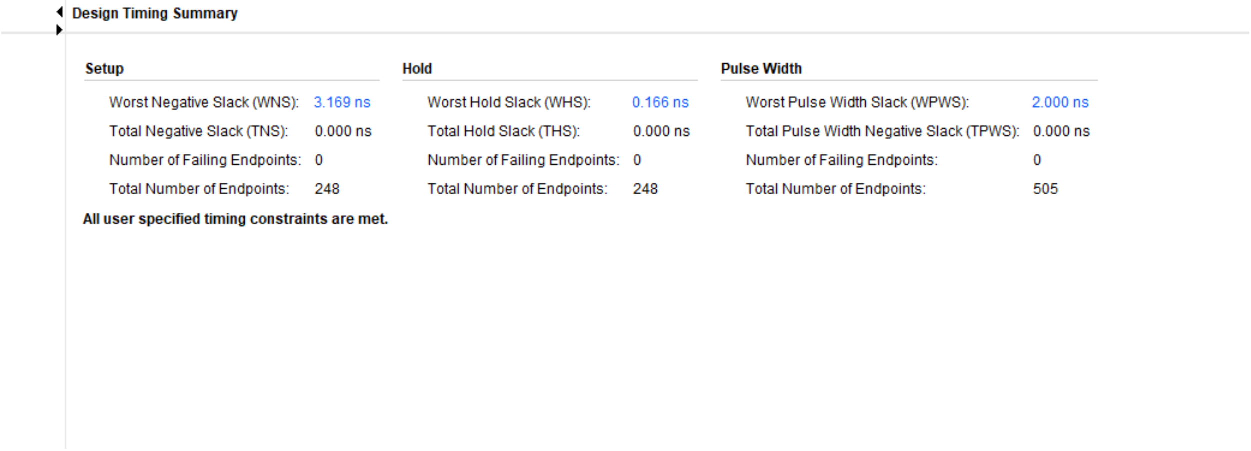
Dynamic:	0.040 W	(30%)
Clocks:	0.008 W	(19%)
Signals:	0.003 W	(9%)
Logic:	0.010 W	(24%)
I/O:	0.019 W	(48%)
Device Static:	0.094 W	(70%)

j. 16 inputs resources analysis



Name	Slice LUT...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
OE_Sort	1440	1920	257	1
genblk2[0].(null)[0].CS1 (Compare_and_Swap)	12	16	0	0
genblk2[0].(null)[2].CS1 (Compare_and_Swap_3)	24	16	0	0
genblk2[0].(null)[4].CS1 (Compare_and_Swap_4)	24	16	0	0
genblk2[0].(null)[6].CS1 (Compare_and_Swap_5)	24	16	0	0
genblk2[0].(null)[8].CS1 (Compare_and_Swap_6)	24	16	0	0
genblk2[0].(null)[10].CS1 (Compare_and_Swap_0)	24	16	0	0
genblk2[0].(null)[12].CS1 (Compare_and_Swap_1)	24	16	0	0
genblk2[0].(null)[14].CS1 (Compare_and_Swap_2)	36	16	0	0
genblk2[1].(null)[1].CS2 (Compare_and_Swap_54)	12	16	0	0
genblk2[1].(null)[3].CS2 (Compare_and_Swap_55)	12	16	0	0
genblk2[1].(null)[5].CS2 (Compare_and_Swap_56)	12	16	0	0
genblk2[1].(null)[7].CS2 (Compare_and_Swap_57)	12	16	0	0
genblk2[1].(null)[9].CS2 (Compare_and_Swap_58)	12	16	0	0
genblk2[1].(null)[11].CS2 (Compare_and_Swap_52)	12	16	0	0
genblk2[1].(null)[13].CS2 (Compare_and_Swap_53)	12	16	0	0
genblk2[2].(null)[0].CS1 (Compare_and_Swap_59)	0	16	0	0
genblk2[2].(null)[2].CS1 (Compare_and_Swap_63)	12	16	0	0
genblk2[2].(null)[4].CS1 (Compare_and_Swap_64)	12	16	0	0
genblk2[2].(null)[6].CS1 (Compare_and_Swap_65)	12	16	0	0
genblk2[2].(null)[8].CS1 (Compare_and_Swap_66)	12	16	0	0
genblk2[2].(null)[10].CS1 (Compare_and_Swap_60)	12	16	0	0

32inputs timing analysis

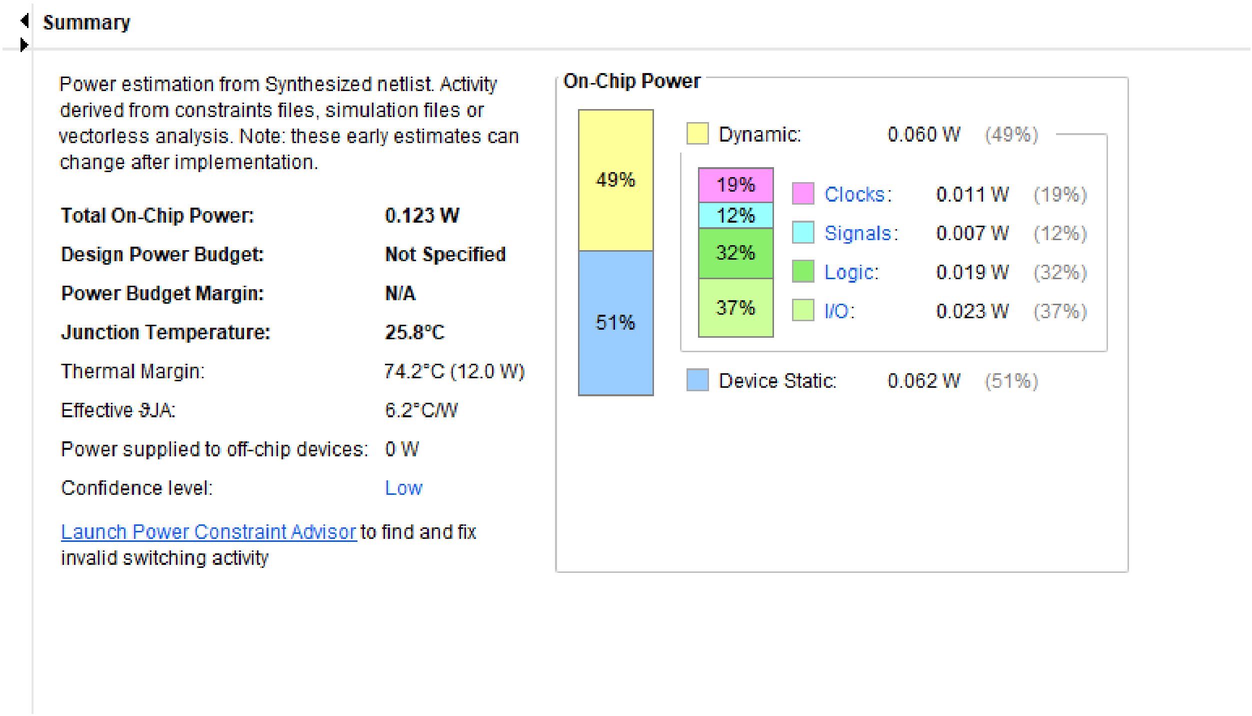


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.169 ns	Worst Hold Slack (WHS):	0.166 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	248	Total Number of Endpoints:	248	Total Number of Endpoints:	505

All user specified timing constraints are met.

32 inputs power analysis



Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

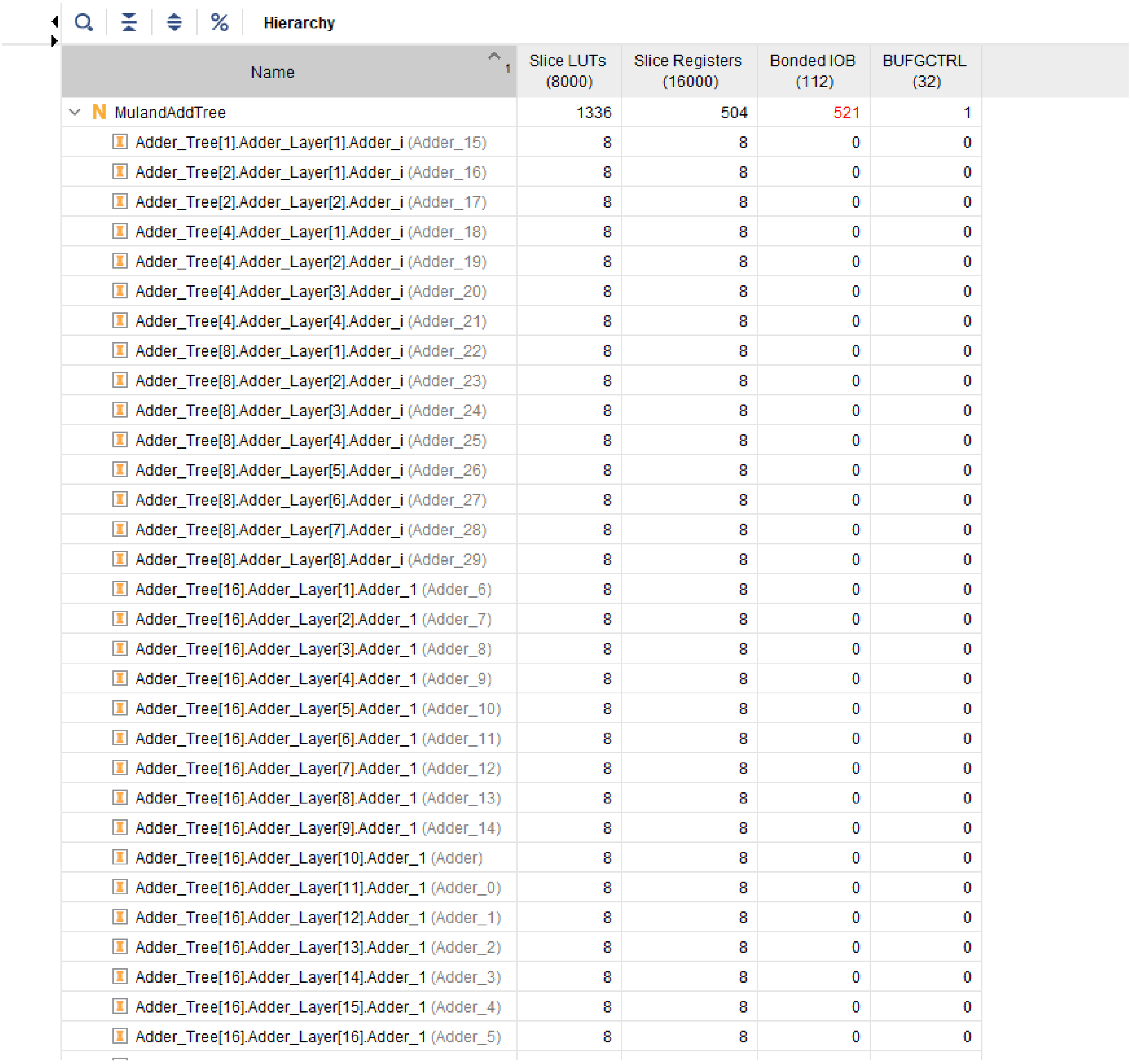
Total On-Chip Power:	**0.123 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.8°C**
Thermal Margin:	74.2°C (12.0 W)
Effective ϑJA:	6.2°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

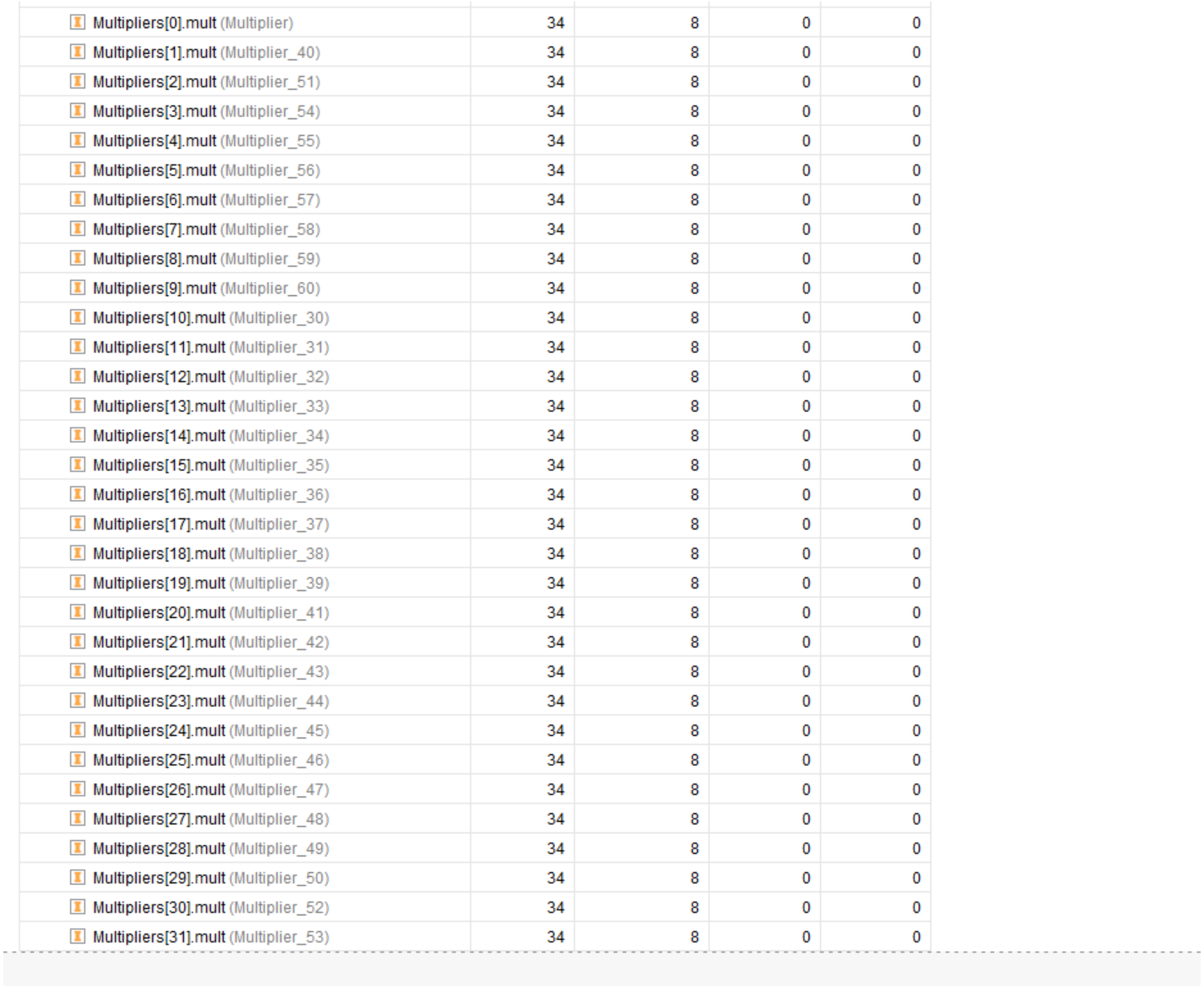
On-Chip Power

Dynamic:	0.060 W	(49%)
Clocks:	0.011 W	(19%)
Signals:	0.007 W	(12%)
Logic:	0.019 W	(32%)
I/O:	0.023 W	(37%)
Device Static:	0.062 W	(51%)

32 inputs resource analysis



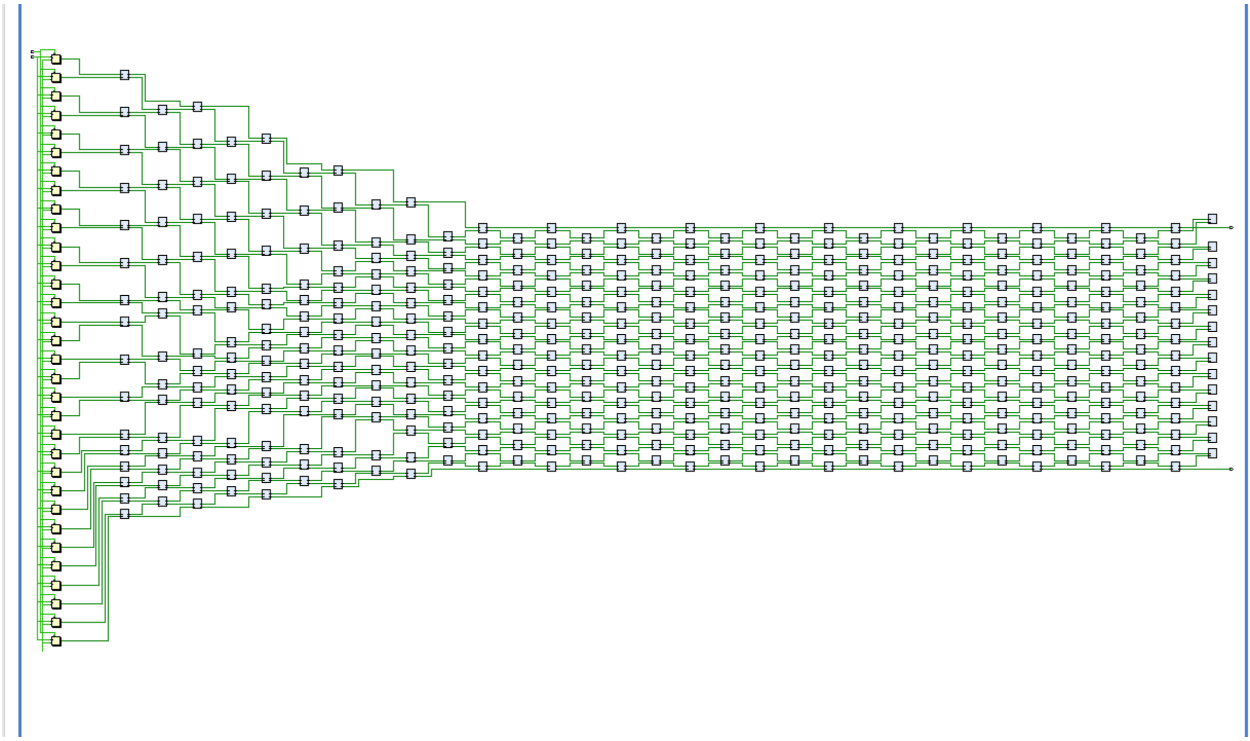
Name	Slice LUTs (8000)	Slice Registers (16000)	Bonded IOB (112)	BUFGCTRL (32)
MulandAddTree	1336	504	521	1
Adder_Tree[1].Adder_Layer[1].Adder_i (Adder_15)	8	8	0	0
Adder_Tree[2].Adder_Layer[1].Adder_i (Adder_16)	8	8	0	0
Adder_Tree[2].Adder_Layer[2].Adder_i (Adder_17)	8	8	0	0
Adder_Tree[4].Adder_Layer[1].Adder_i (Adder_18)	8	8	0	0
Adder_Tree[4].Adder_Layer[2].Adder_i (Adder_19)	8	8	0	0
Adder_Tree[4].Adder_Layer[3].Adder_i (Adder_20)	8	8	0	0
Adder_Tree[4].Adder_Layer[4].Adder_i (Adder_21)	8	8	0	0
Adder_Tree[8].Adder_Layer[1].Adder_i (Adder_22)	8	8	0	0
Adder_Tree[8].Adder_Layer[2].Adder_i (Adder_23)	8	8	0	0
Adder_Tree[8].Adder_Layer[3].Adder_i (Adder_24)	8	8	0	0
Adder_Tree[8].Adder_Layer[4].Adder_i (Adder_25)	8	8	0	0
Adder_Tree[8].Adder_Layer[5].Adder_i (Adder_26)	8	8	0	0
Adder_Tree[8].Adder_Layer[6].Adder_i (Adder_27)	8	8	0	0
Adder_Tree[8].Adder_Layer[7].Adder_i (Adder_28)	8	8	0	0
Adder_Tree[8].Adder_Layer[8].Adder_i (Adder_29)	8	8	0	0
Adder_Tree[16].Adder_Layer[1].Adder_1 (Adder_6)	8	8	0	0
Adder_Tree[16].Adder_Layer[2].Adder_1 (Adder_7)	8	8	0	0
Adder_Tree[16].Adder_Layer[3].Adder_1 (Adder_8)	8	8	0	0
Adder_Tree[16].Adder_Layer[4].Adder_1 (Adder_9)	8	8	0	0
Adder_Tree[16].Adder_Layer[5].Adder_1 (Adder_10)	8	8	0	0
Adder_Tree[16].Adder_Layer[6].Adder_1 (Adder_11)	8	8	0	0
Adder_Tree[16].Adder_Layer[7].Adder_1 (Adder_12)	8	8	0	0
Adder_Tree[16].Adder_Layer[8].Adder_1 (Adder_13)	8	8	0	0
Adder_Tree[16].Adder_Layer[9].Adder_1 (Adder_14)	8	8	0	0
Adder_Tree[16].Adder_Layer[10].Adder_1 (Adder)	8	8	0	0
Adder_Tree[16].Adder_Layer[11].Adder_1 (Adder_0)	8	8	0	0
Adder_Tree[16].Adder_Layer[12].Adder_1 (Adder_1)	8	8	0	0
Adder_Tree[16].Adder_Layer[13].Adder_1 (Adder_2)	8	8	0	0
Adder_Tree[16].Adder_Layer[14].Adder_1 (Adder_3)	8	8	0	0
Adder_Tree[16].Adder_Layer[15].Adder_1 (Adder_4)	8	8	0	0
Adder_Tree[16].Adder_Layer[16].Adder_1 (Adder_5)	8	8	0	0



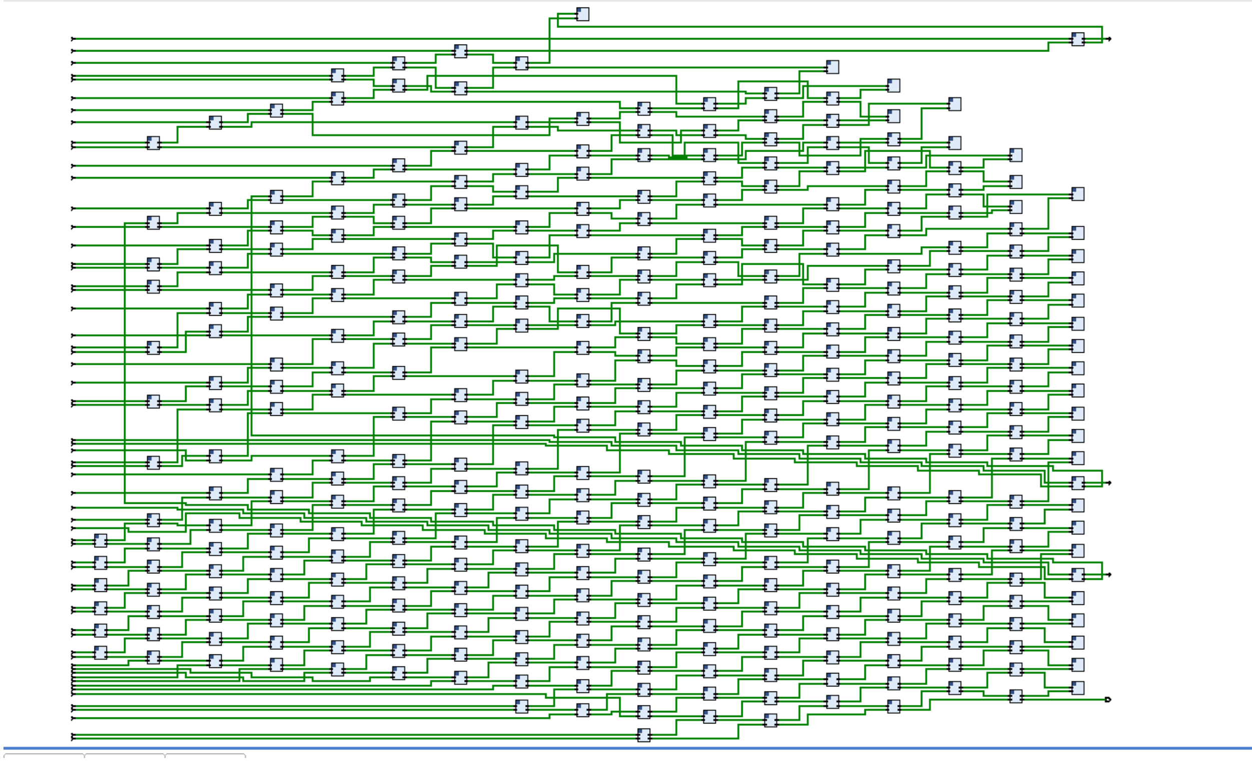
Multipliers[0].mult (Multiplier)	34	8	0	0
Multipliers[1].mult (Multiplier_40)	34	8	0	0
Multipliers[2].mult (Multiplier_51)	34	8	0	0
Multipliers[3].mult (Multiplier_54)	34	8	0	0
Multipliers[4].mult (Multiplier_55)	34	8	0	0
Multipliers[5].mult (Multiplier_56)	34	8	0	0
Multipliers[6].mult (Multiplier_57)	34	8	0	0
Multipliers[7].mult (Multiplier_58)	34	8	0	0
Multipliers[8].mult (Multiplier_59)	34	8	0	0
Multipliers[9].mult (Multiplier_60)	34	8	0	0
Multipliers[10].mult (Multiplier_30)	34	8	0	0
Multipliers[11].mult (Multiplier_31)	34	8	0	0
Multipliers[12].mult (Multiplier_32)	34	8	0	0
Multipliers[13].mult (Multiplier_33)	34	8	0	0
Multipliers[14].mult (Multiplier_34)	34	8	0	0
Multipliers[15].mult (Multiplier_35)	34	8	0	0
Multipliers[16].mult (Multiplier_36)	34	8	0	0
Multipliers[17].mult (Multiplier_37)	34	8	0	0
Multipliers[18].mult (Multiplier_38)	34	8	0	0
Multipliers[19].mult (Multiplier_39)	34	8	0	0
Multipliers[20].mult (Multiplier_41)	34	8	0	0
Multipliers[21].mult (Multiplier_42)	34	8	0	0
Multipliers[22].mult (Multiplier_43)	34	8	0	0
Multipliers[23].mult (Multiplier_44)	34	8	0	0
Multipliers[24].mult (Multiplier_45)	34	8	0	0
Multipliers[25].mult (Multiplier_46)	34	8	0	0
Multipliers[26].mult (Multiplier_47)	34	8	0	0
Multipliers[27].mult (Multiplier_48)	34	8	0	0
Multipliers[28].mult (Multiplier_49)	34	8	0	0
Multipliers[29].mult (Multiplier_50)	34	8	0	0
Multipliers[30].mult (Multiplier_52)	34	8	0	0
Multipliers[31].mult (Multiplier_53)	34	8	0	0

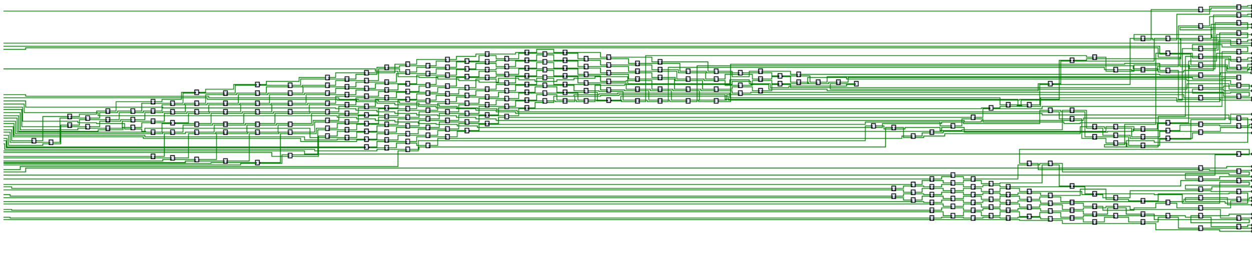
Add for more information

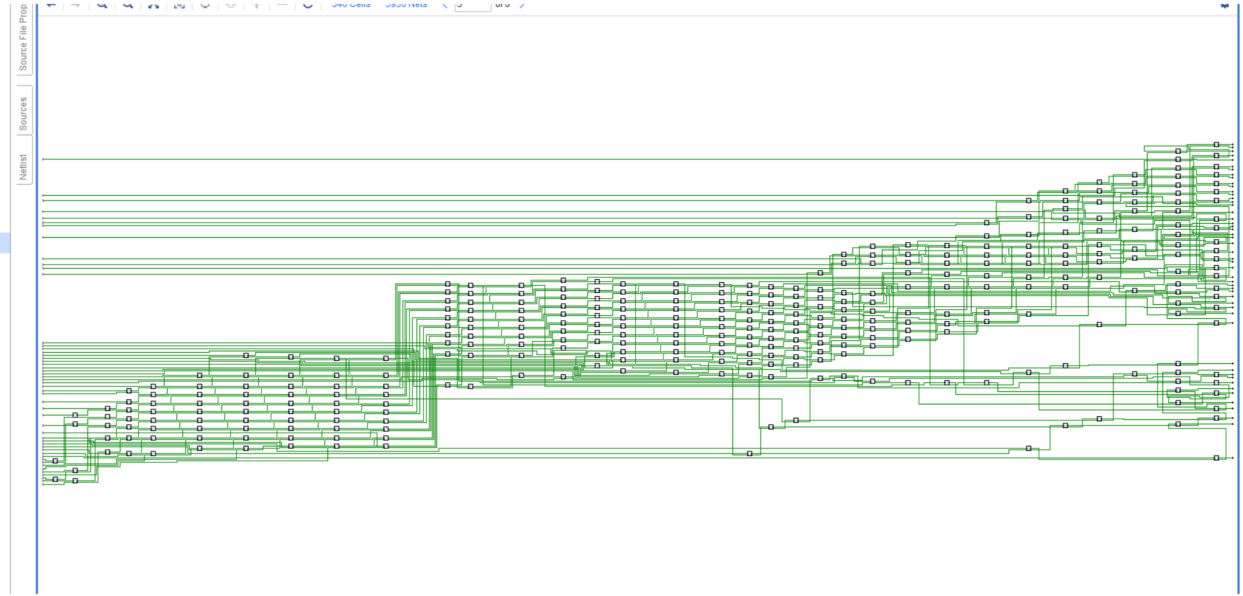
1. 32 odd-even sorting



2. 64 odd-even sorting



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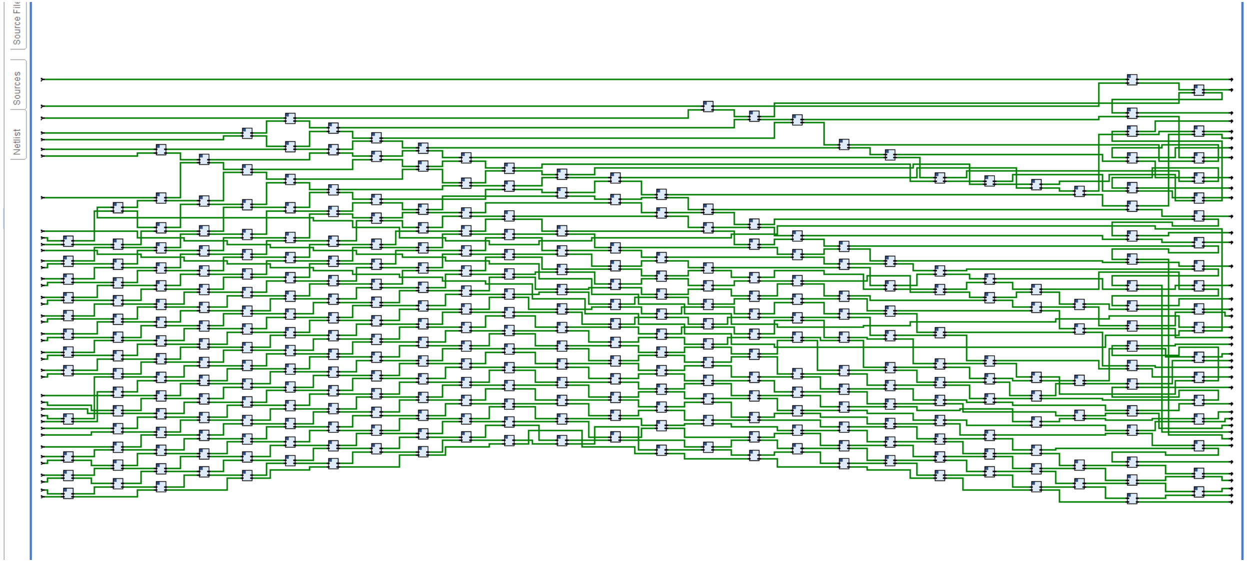
Sources
Netlist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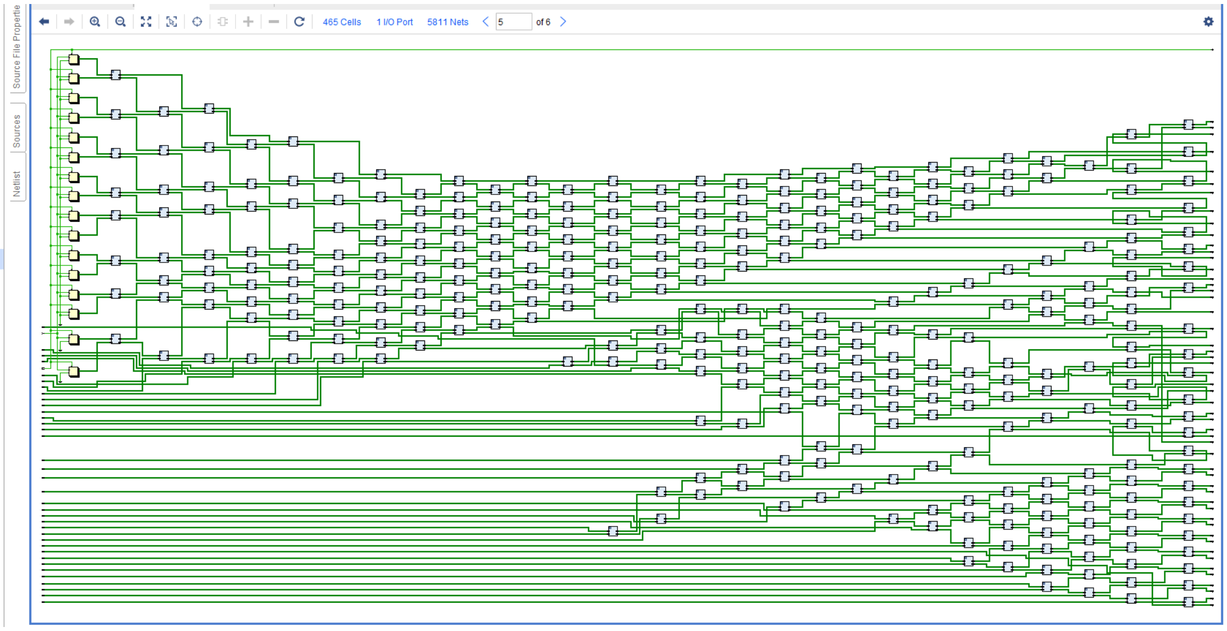
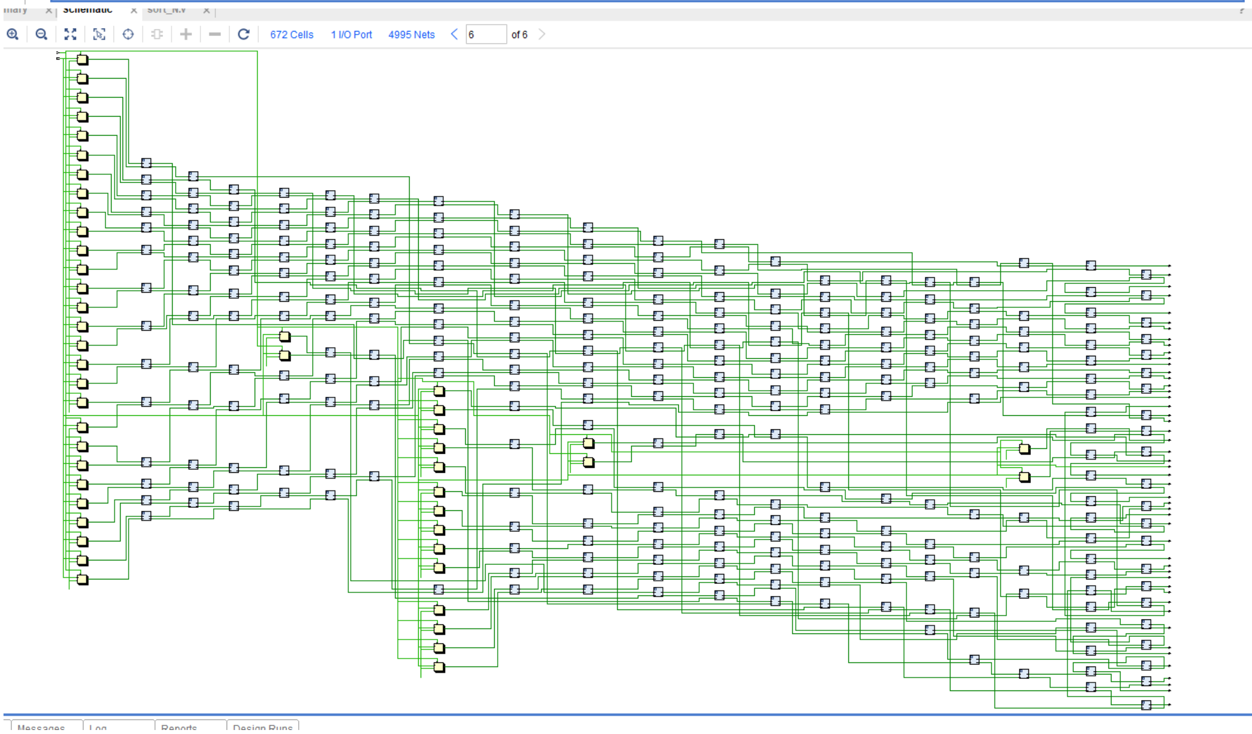
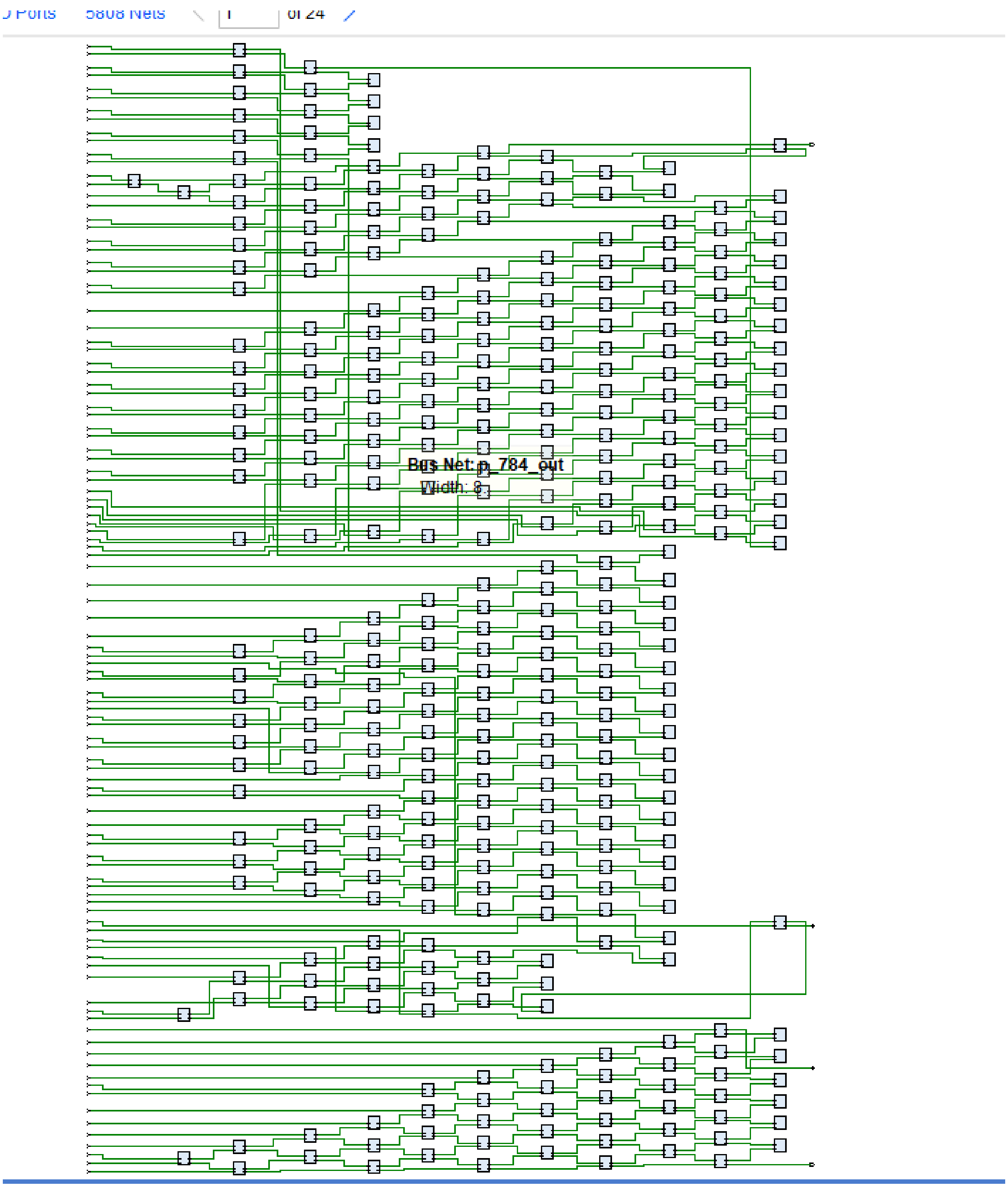




3. 128 odd-even sorting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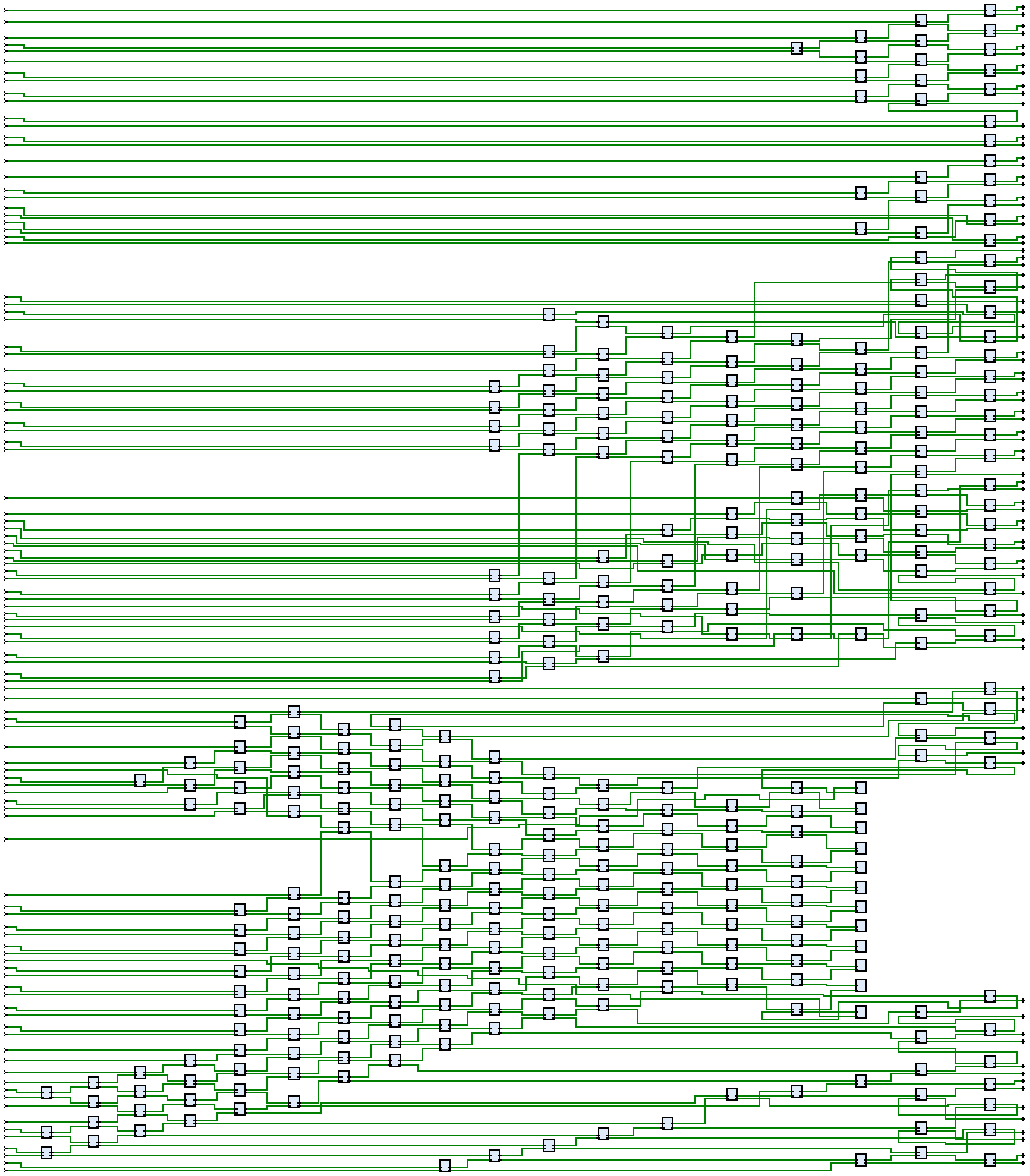
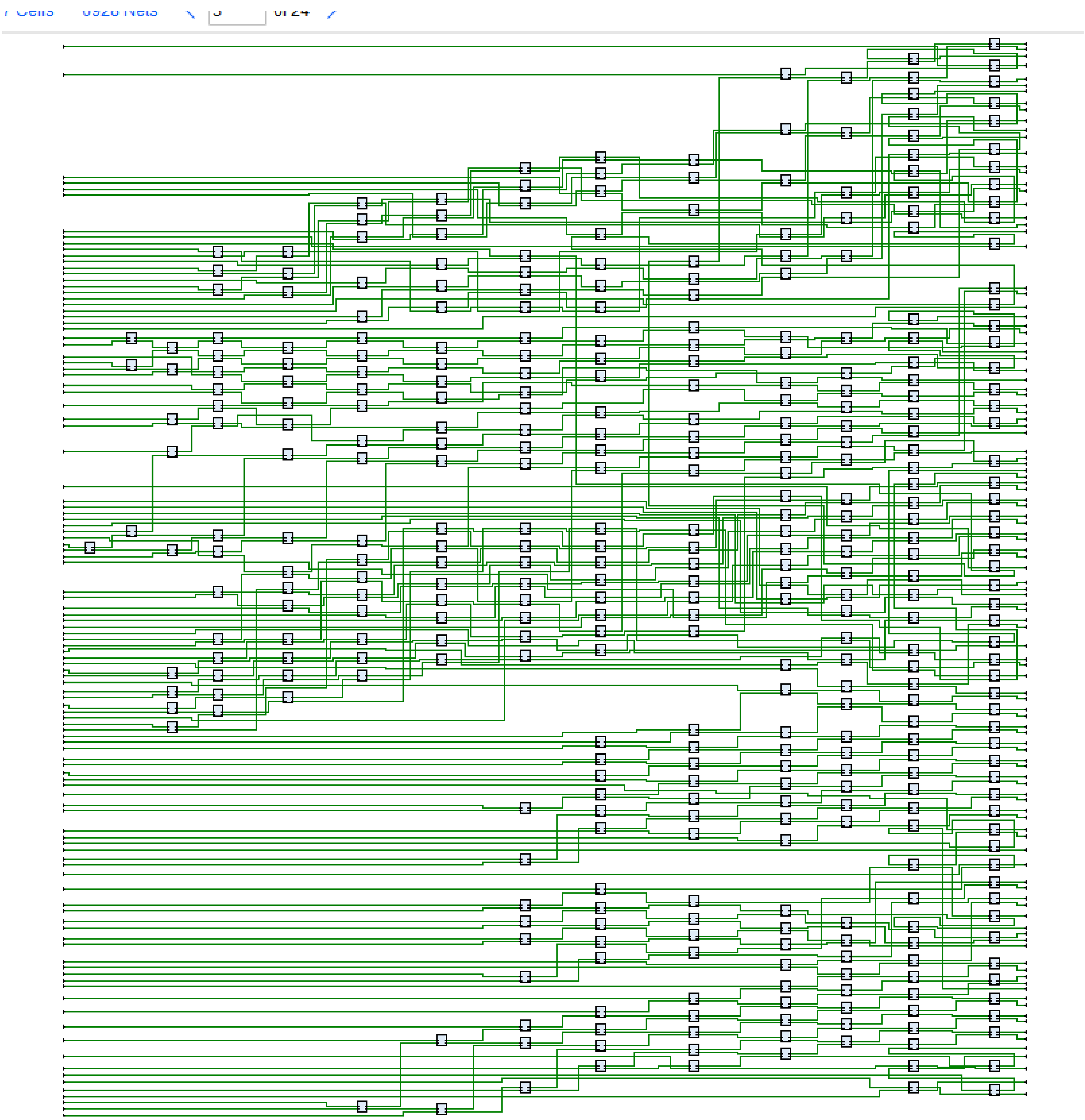
5808 Nets
1
of 24
Bus Net: n_784_out
Width: 8

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6928 Nets
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5
of 24
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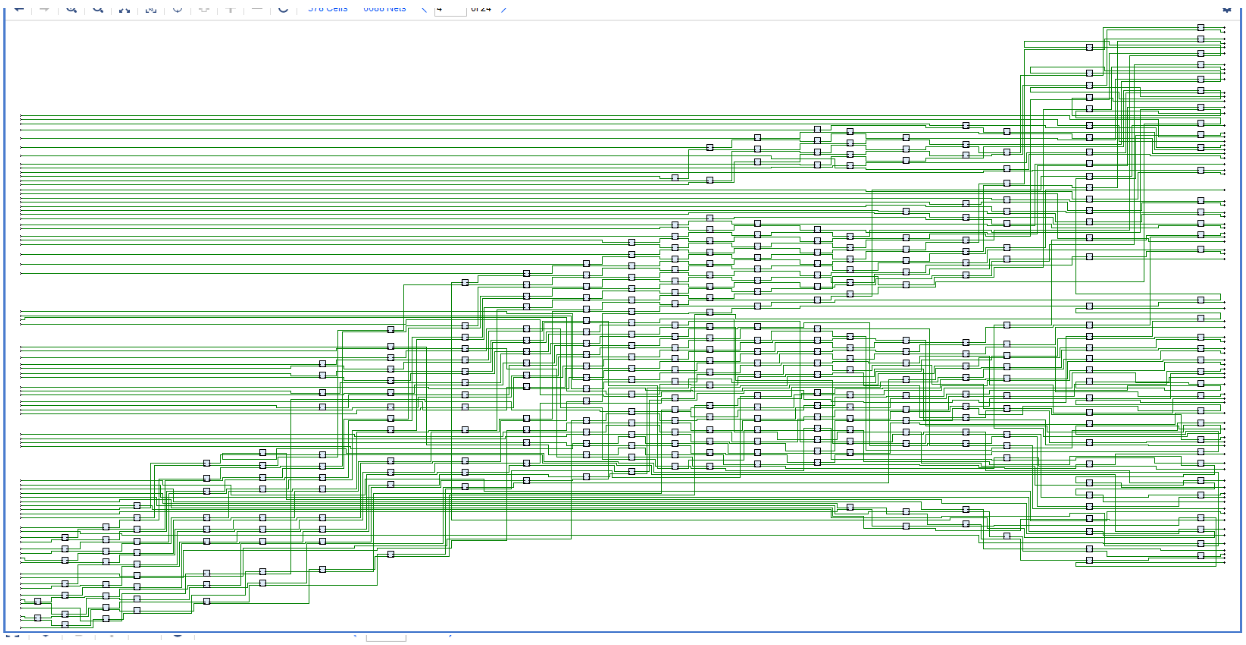
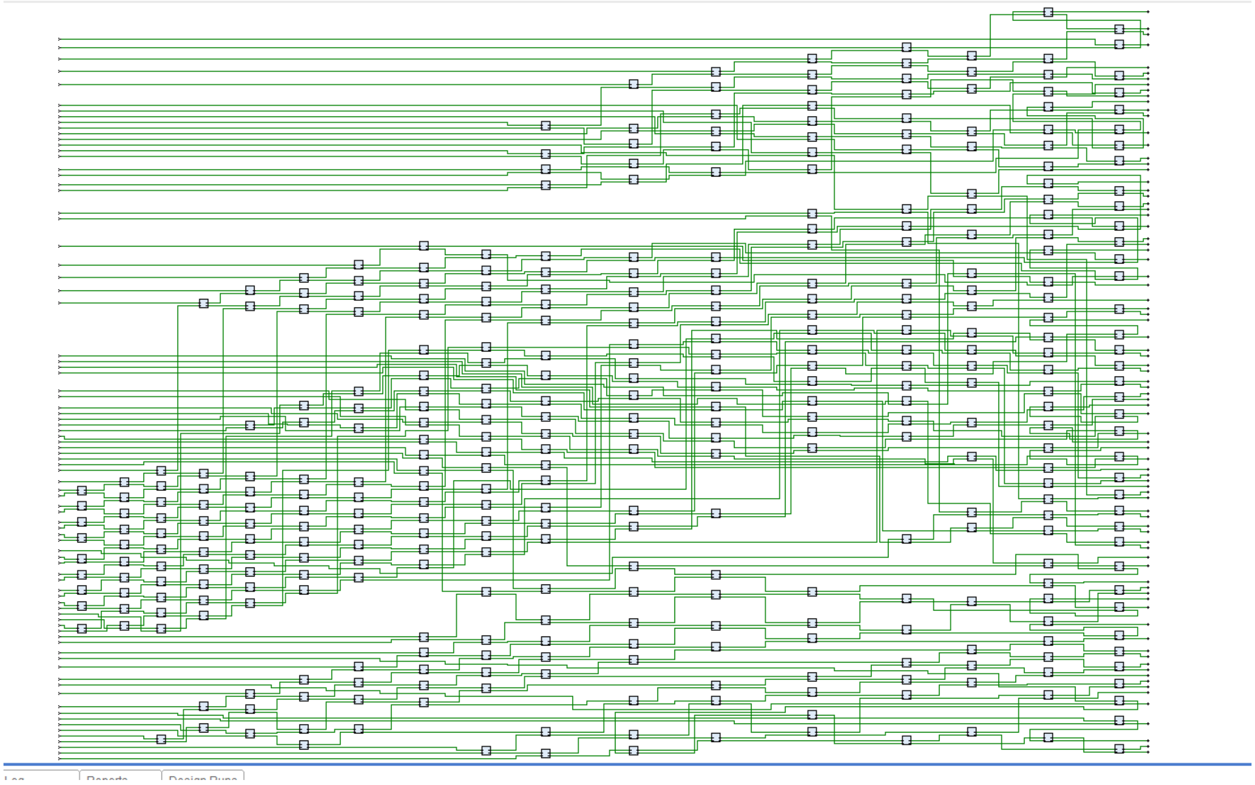
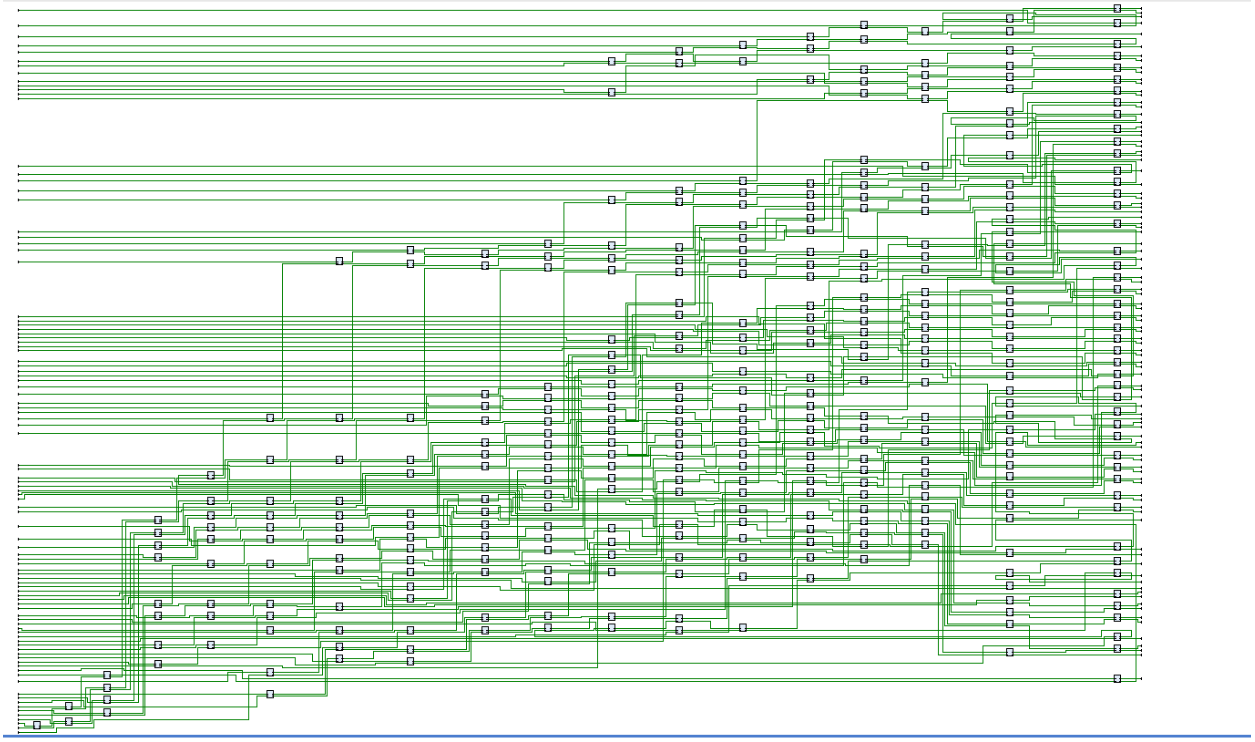
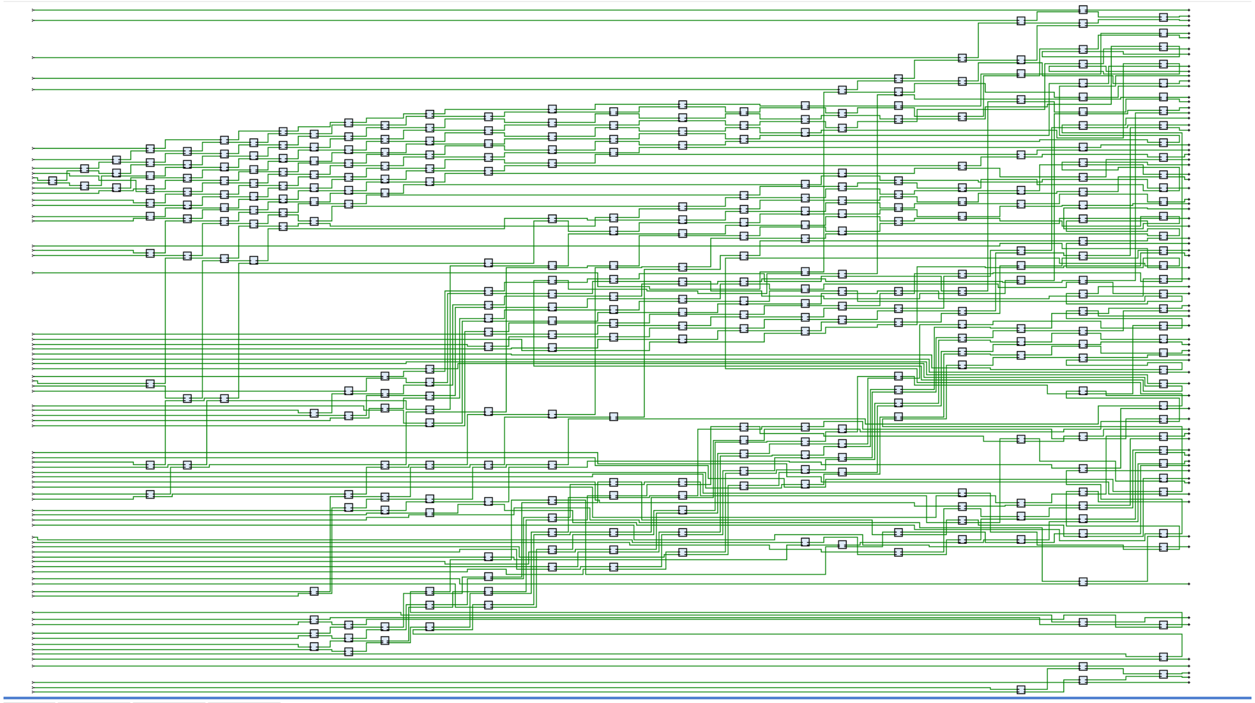
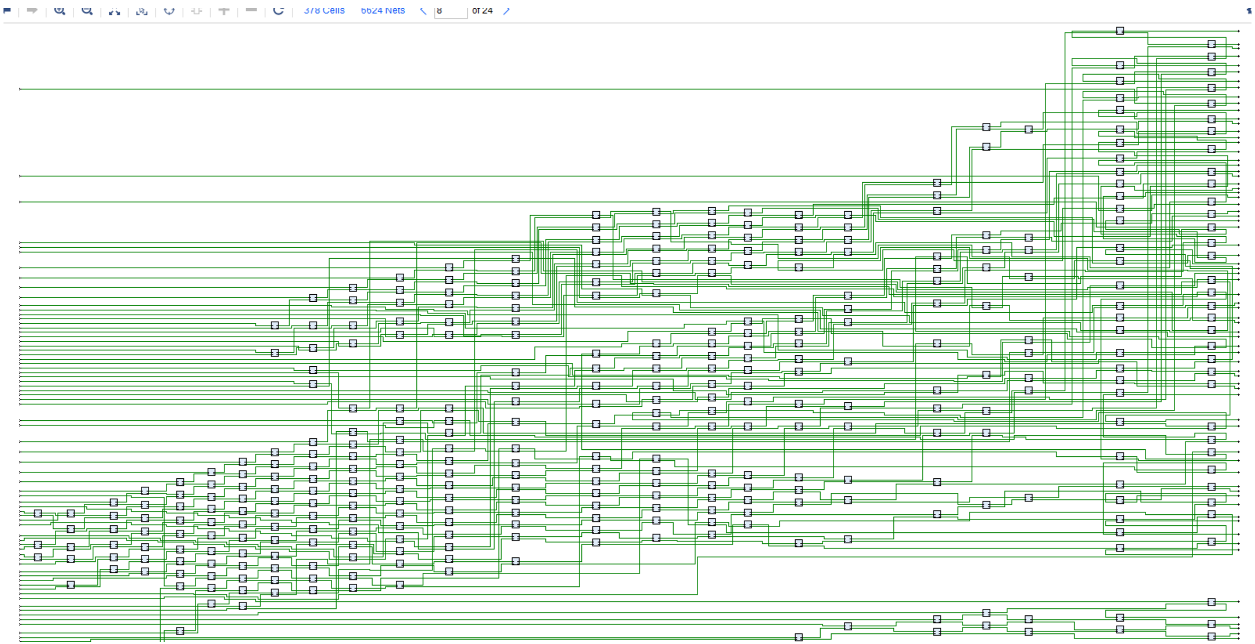
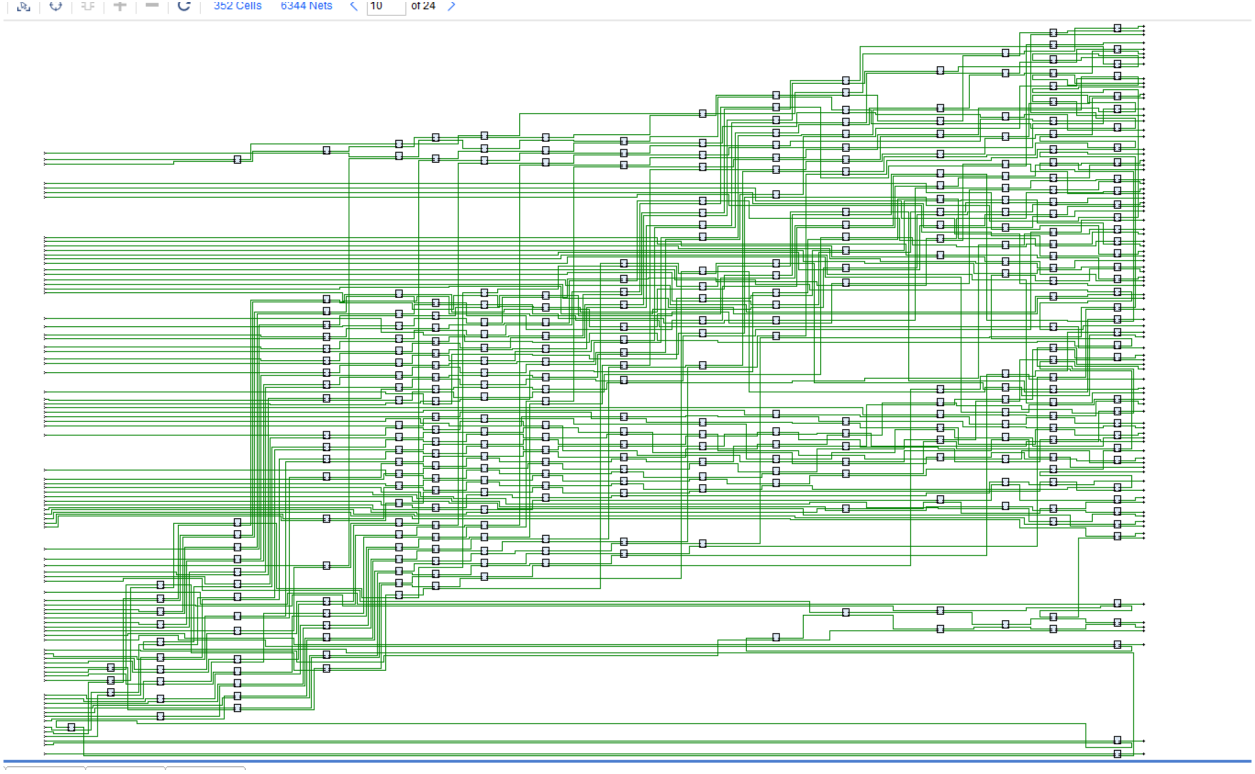

378 Cells
6068 Nets
4
of 24


Log
Reports
Design Runs






378 Cells
6624 Nets
8
of 24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6344 Nets
10
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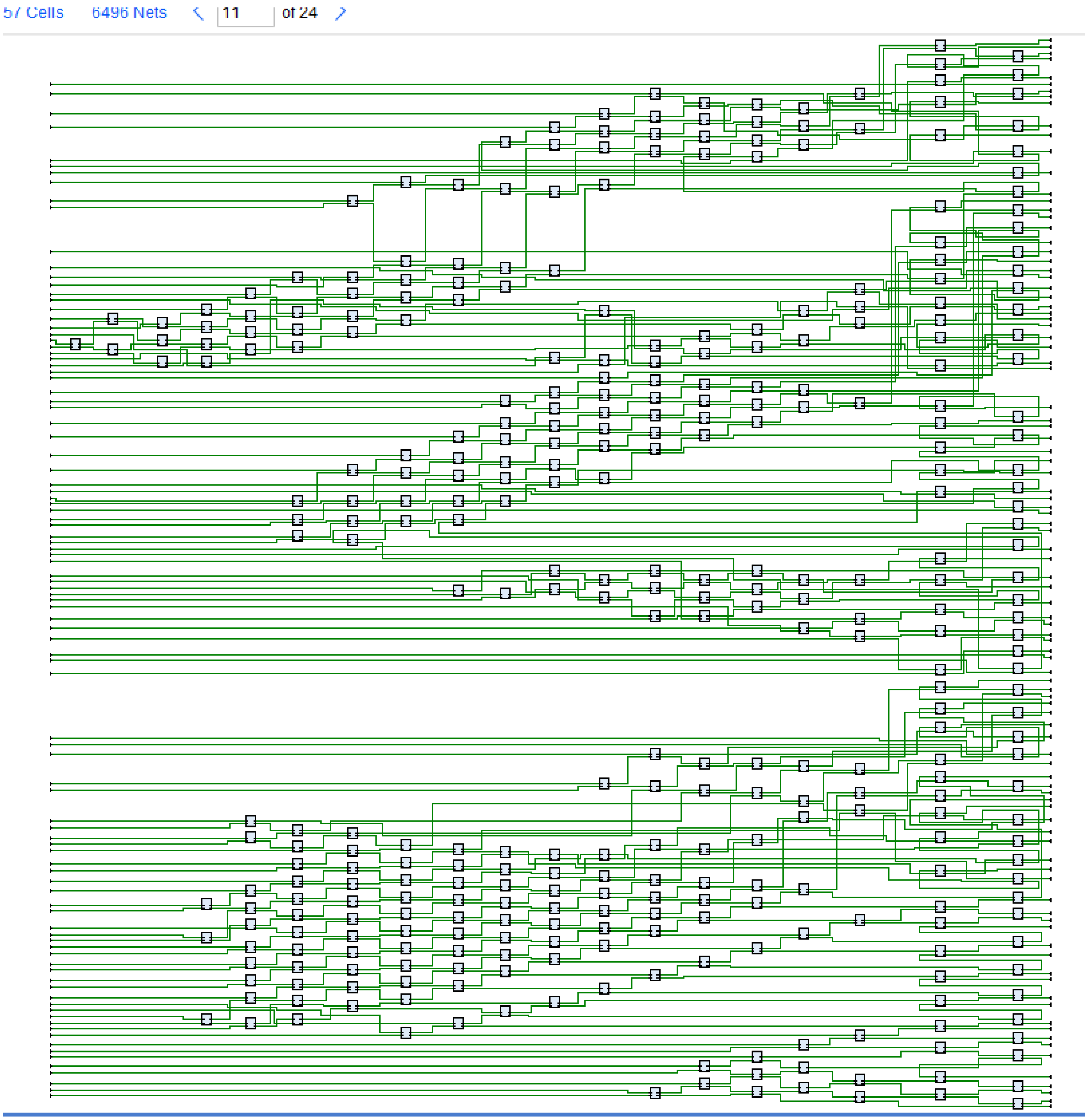
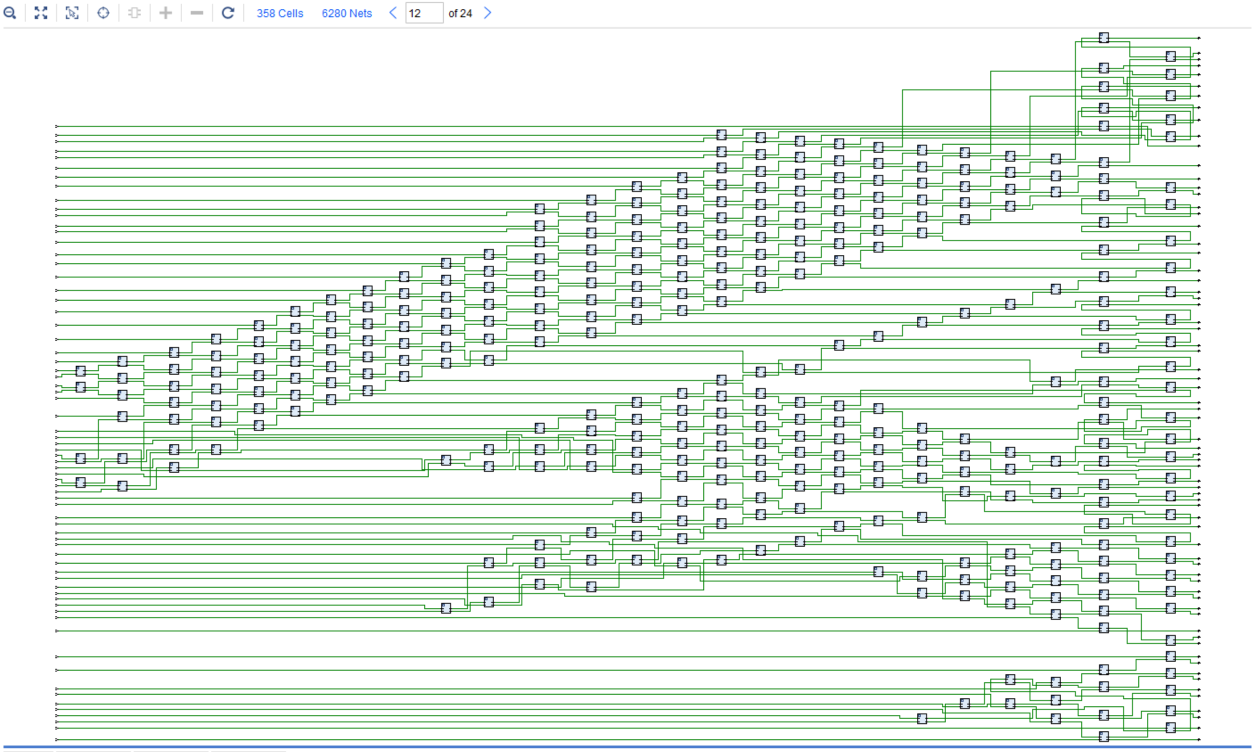


57 Cells 6496 Nets < 11 of 24 >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6280 Nets
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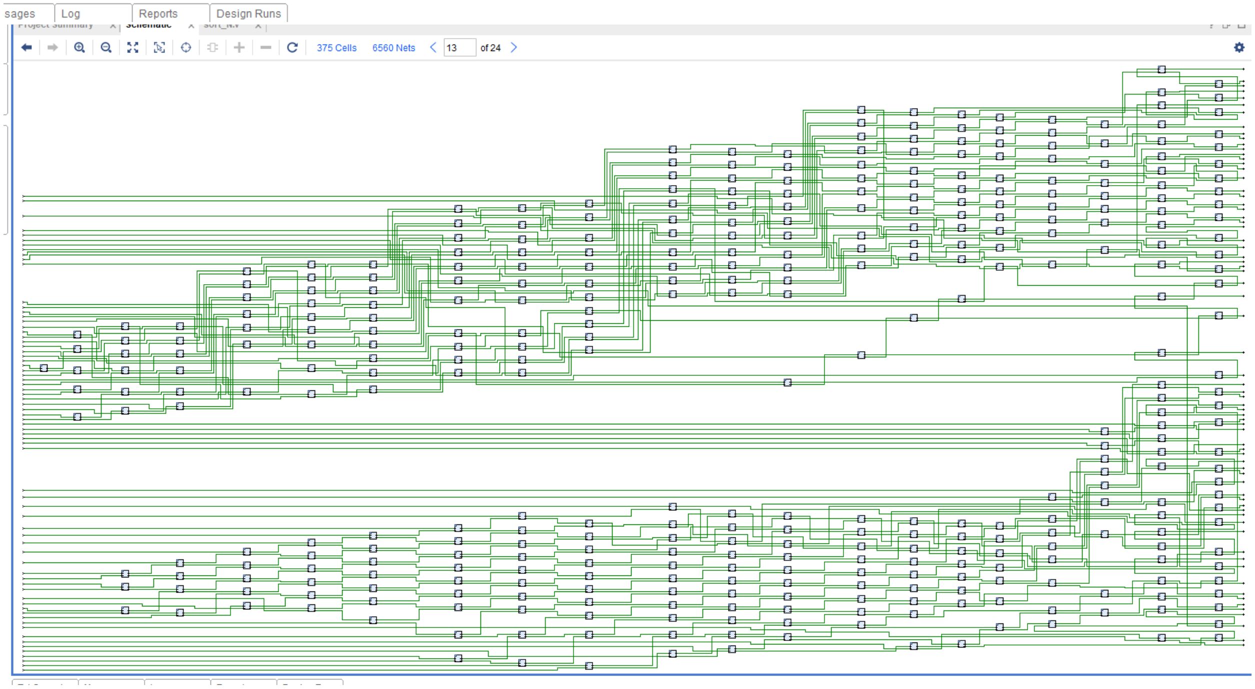
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Reports
Design Runs
Project Summary
Schematic
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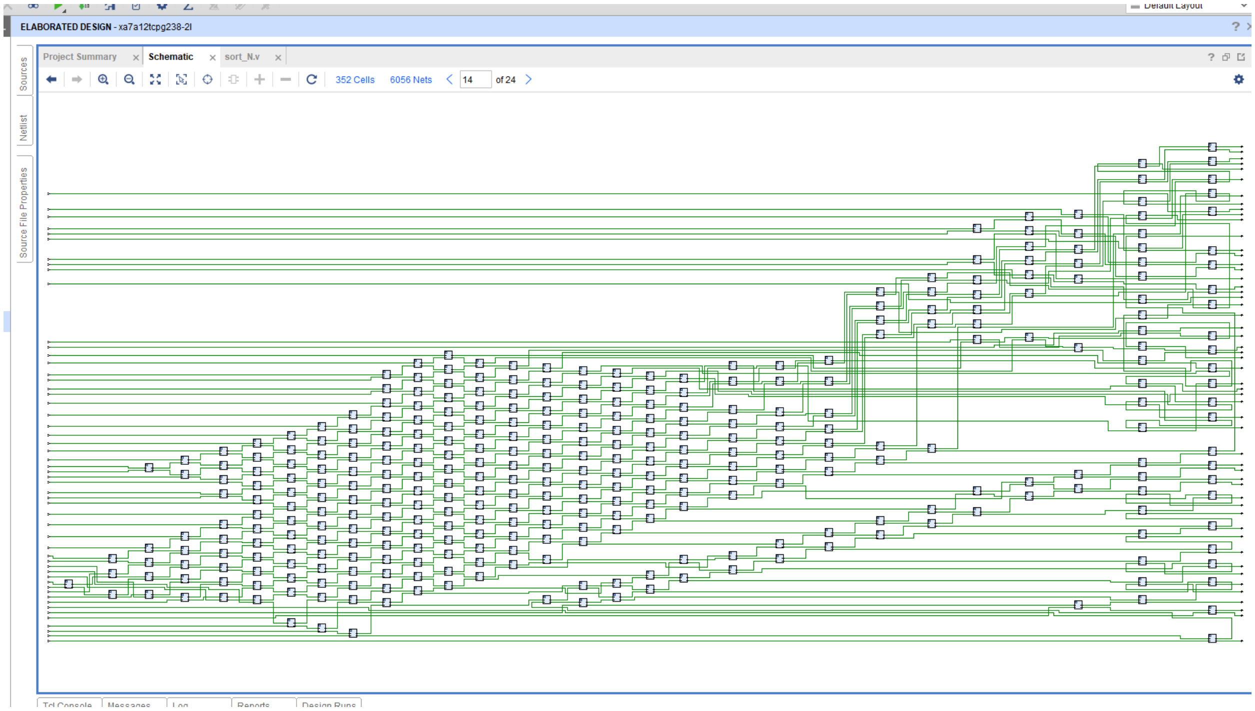
6560 Nets
13
of 24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ELABORATED DESIGN - xa7a12tcpg238-2I
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6056 Nets
14
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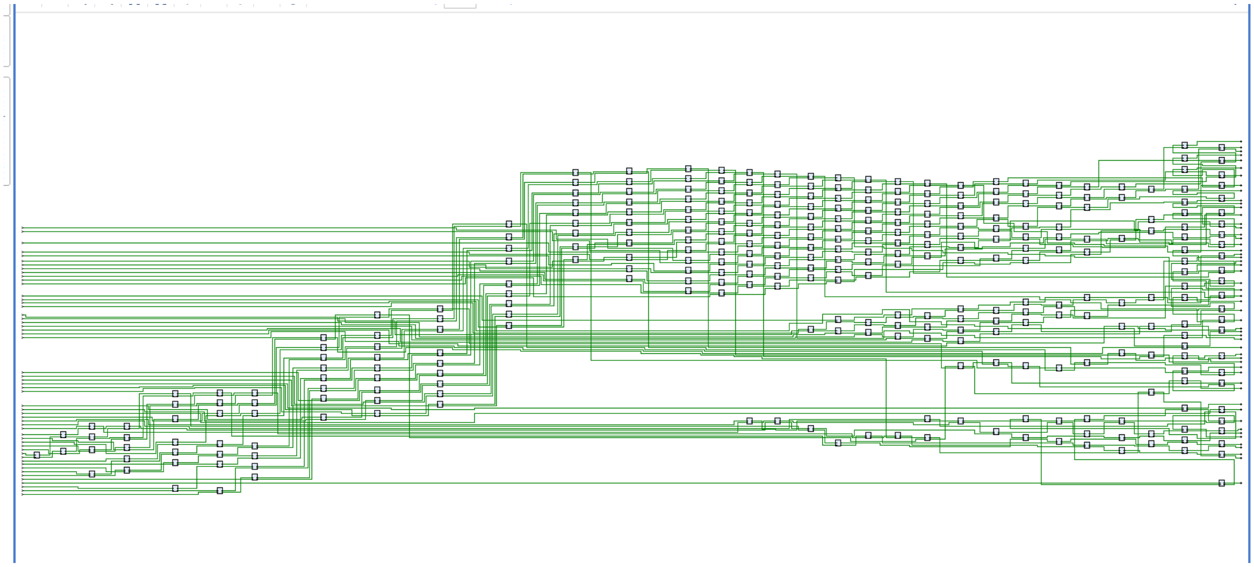
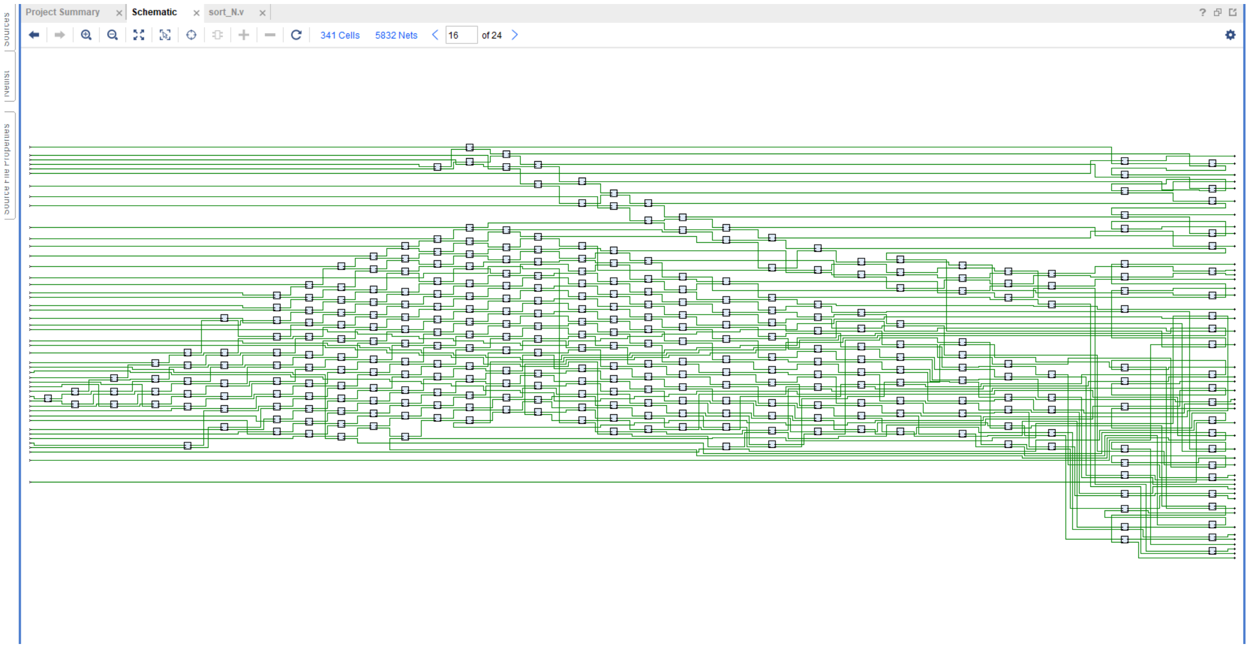
Log
Reports
Design Runs

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Source File Properties
Project Summary
Schematic
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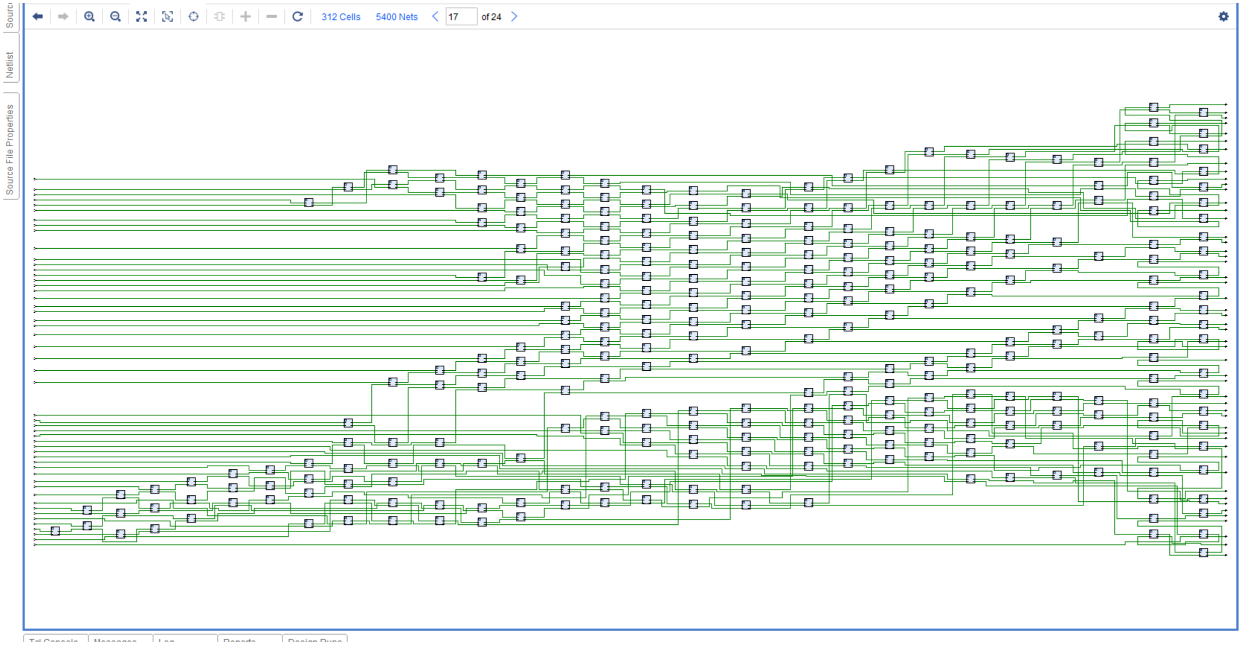
5832 Nets
16
of 24


Sources
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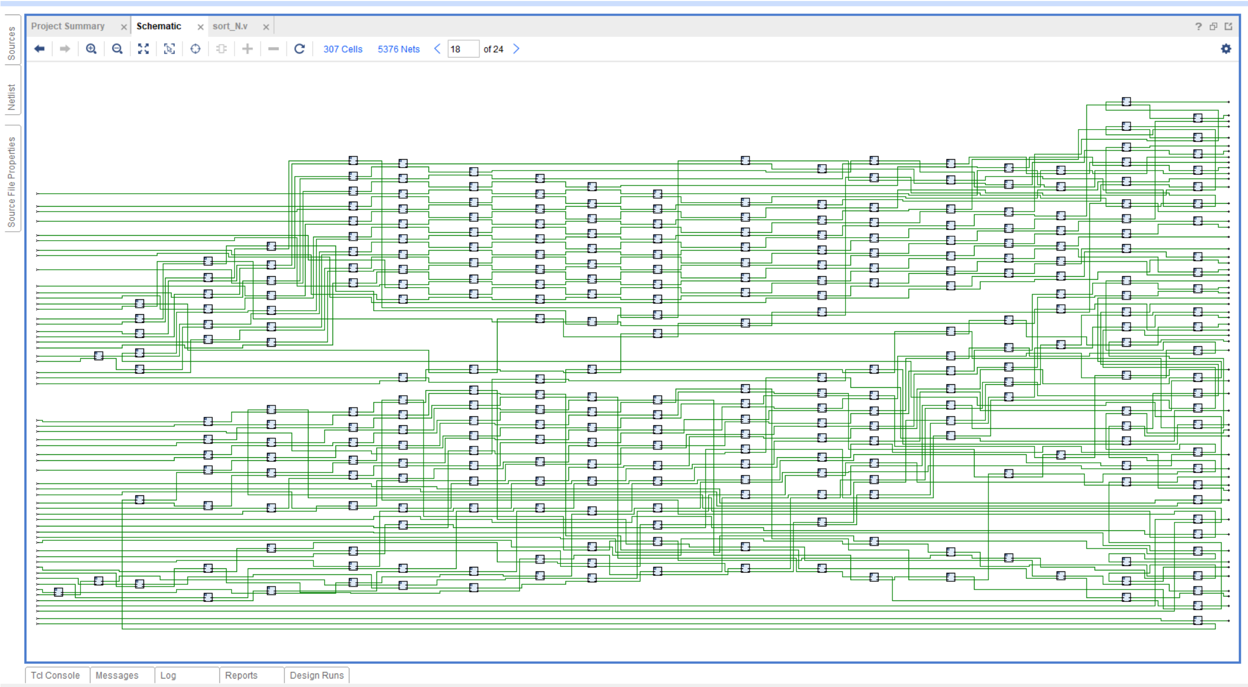
Source File Properties
312 Cells
5400 Nets
17
of 24
Tcl Console
Messages
Log
Reports
Design Runs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Messages
Log
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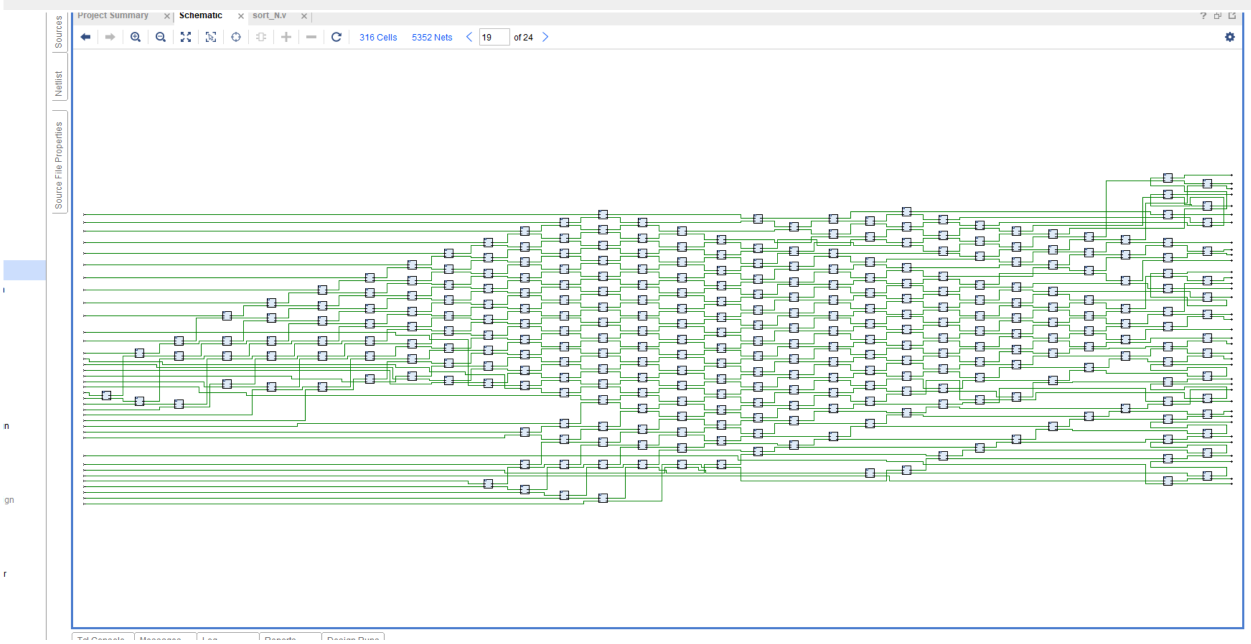
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Netlist
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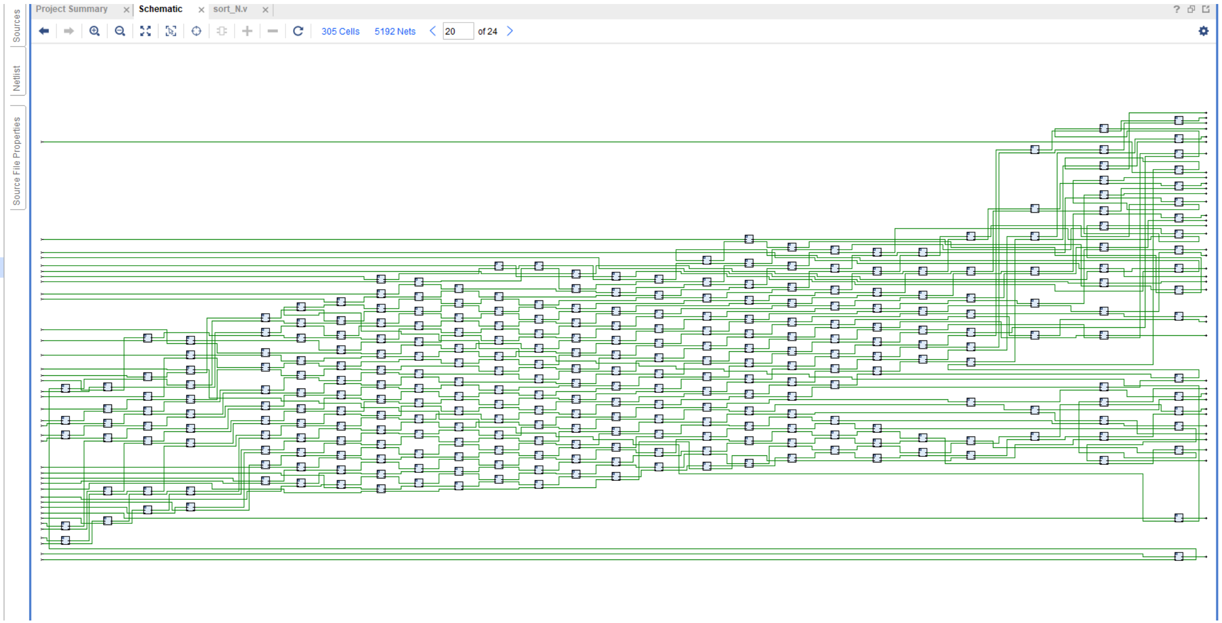
Tcl Console
Messages
Log
Reports
Design Runs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305 Cells
5192 Nets
20
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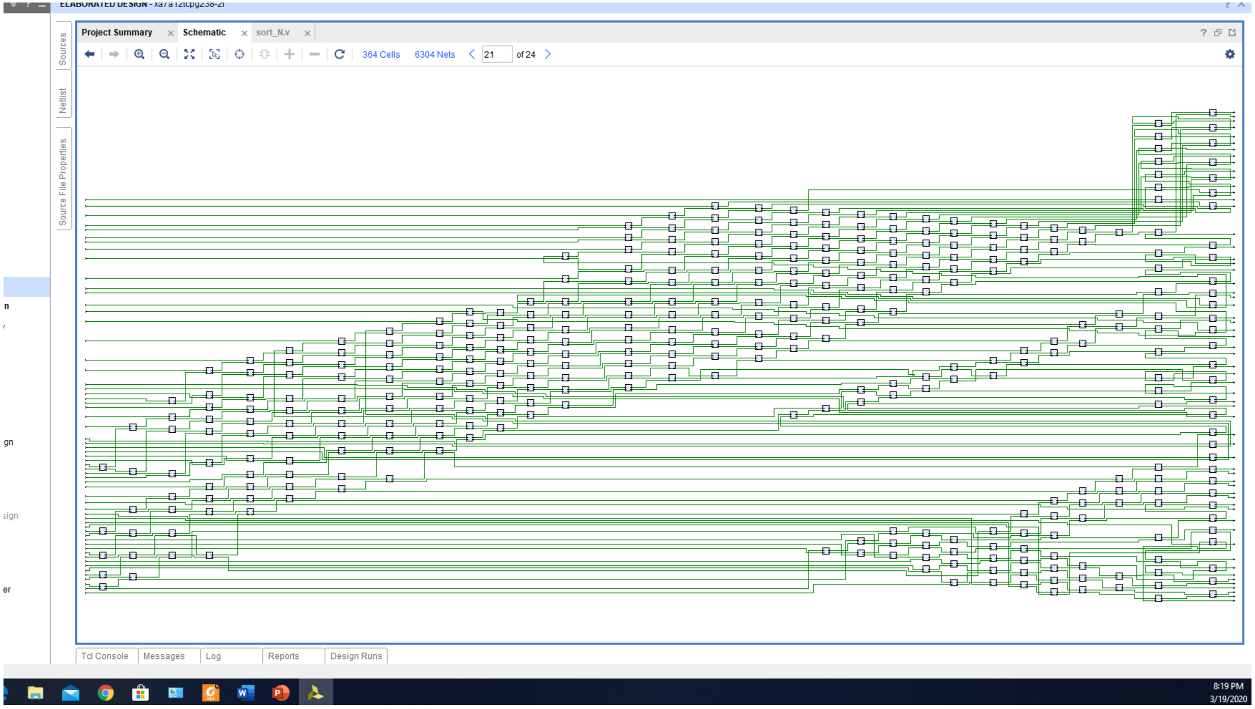
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Sources
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Source File Properties
Project Summary
Schematic
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364 Cells
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21
of 24
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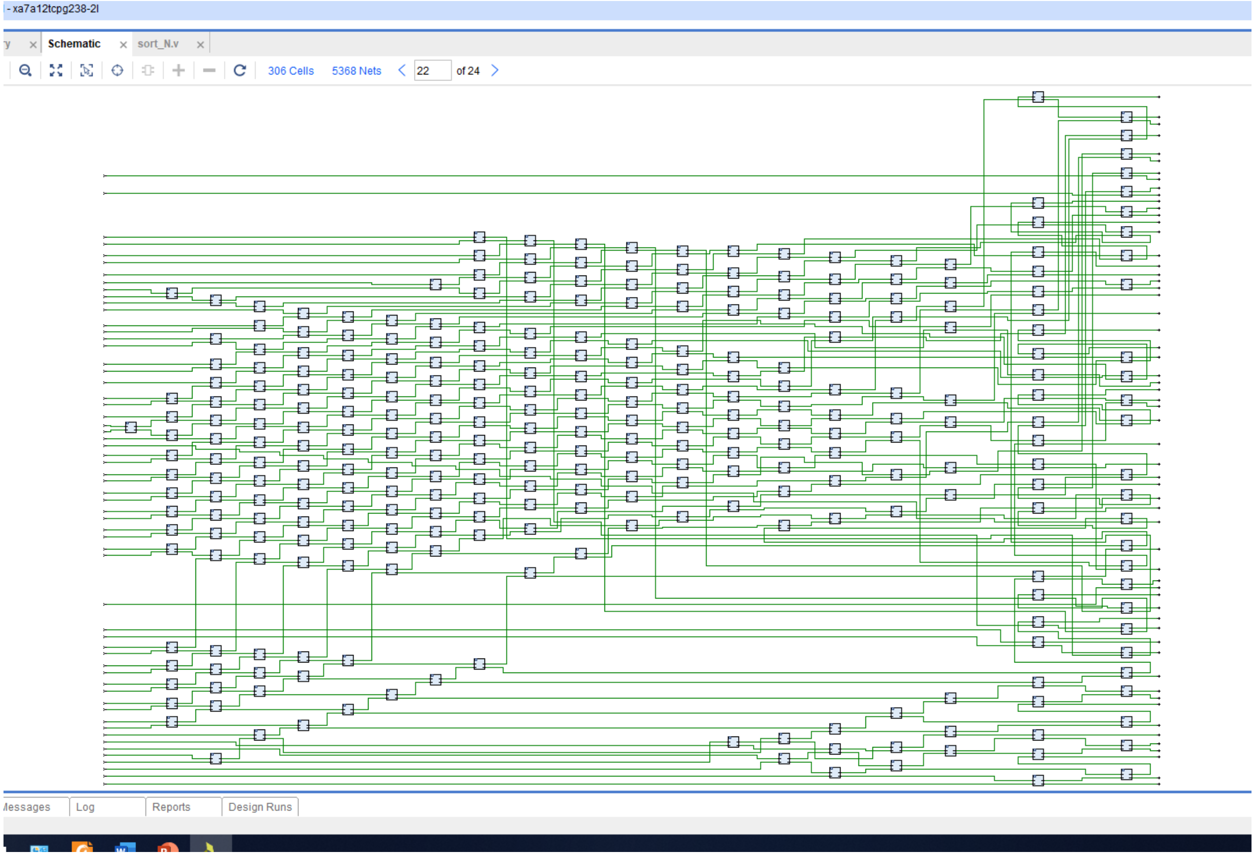
Tcl Console
Messages
Log
Reports
Design Runs
8:19 PM
3/19/2020



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Schematic
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306 Cells
5368 Nets
22
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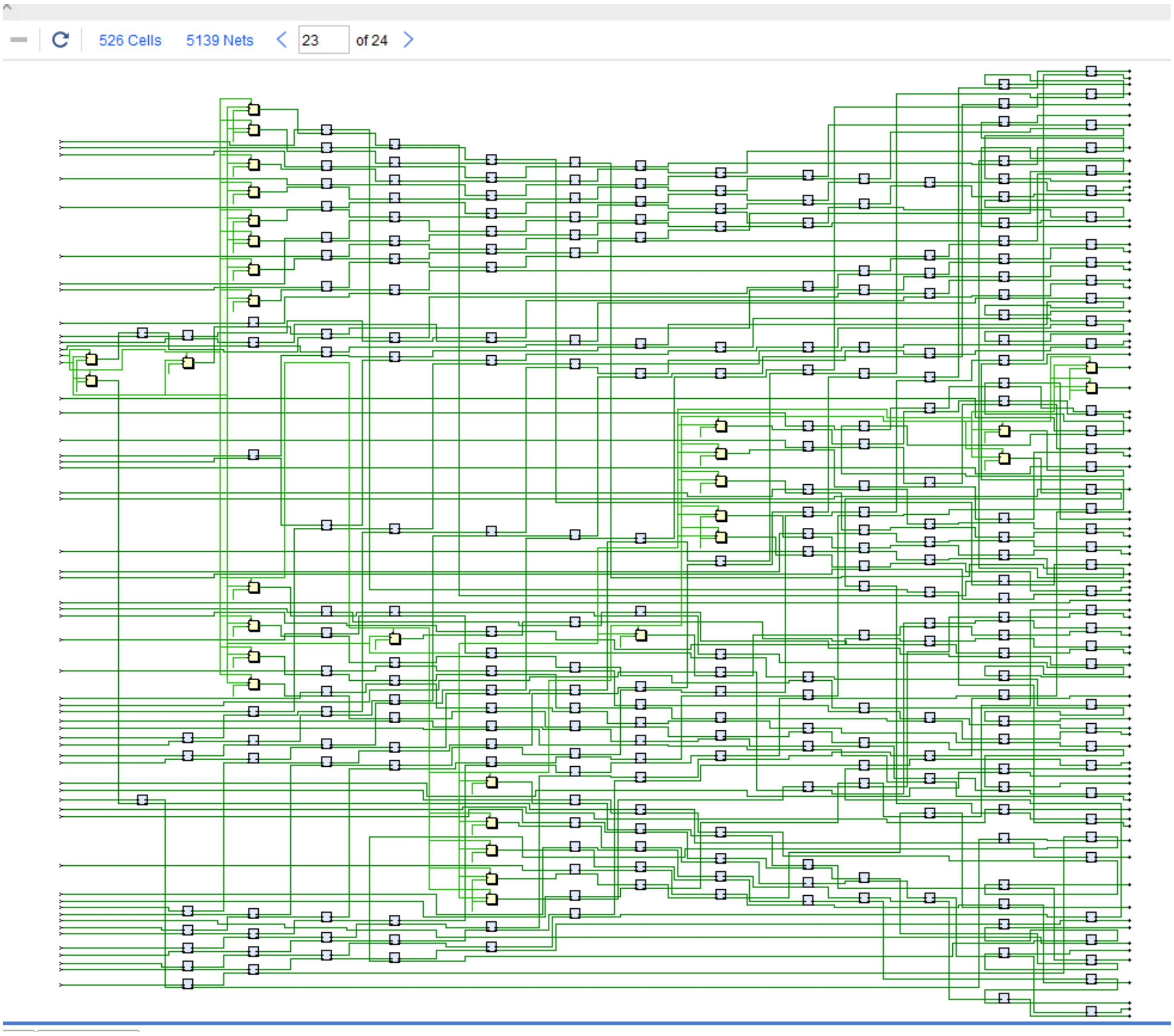
Log
Reports
Design Runs



526 Cells
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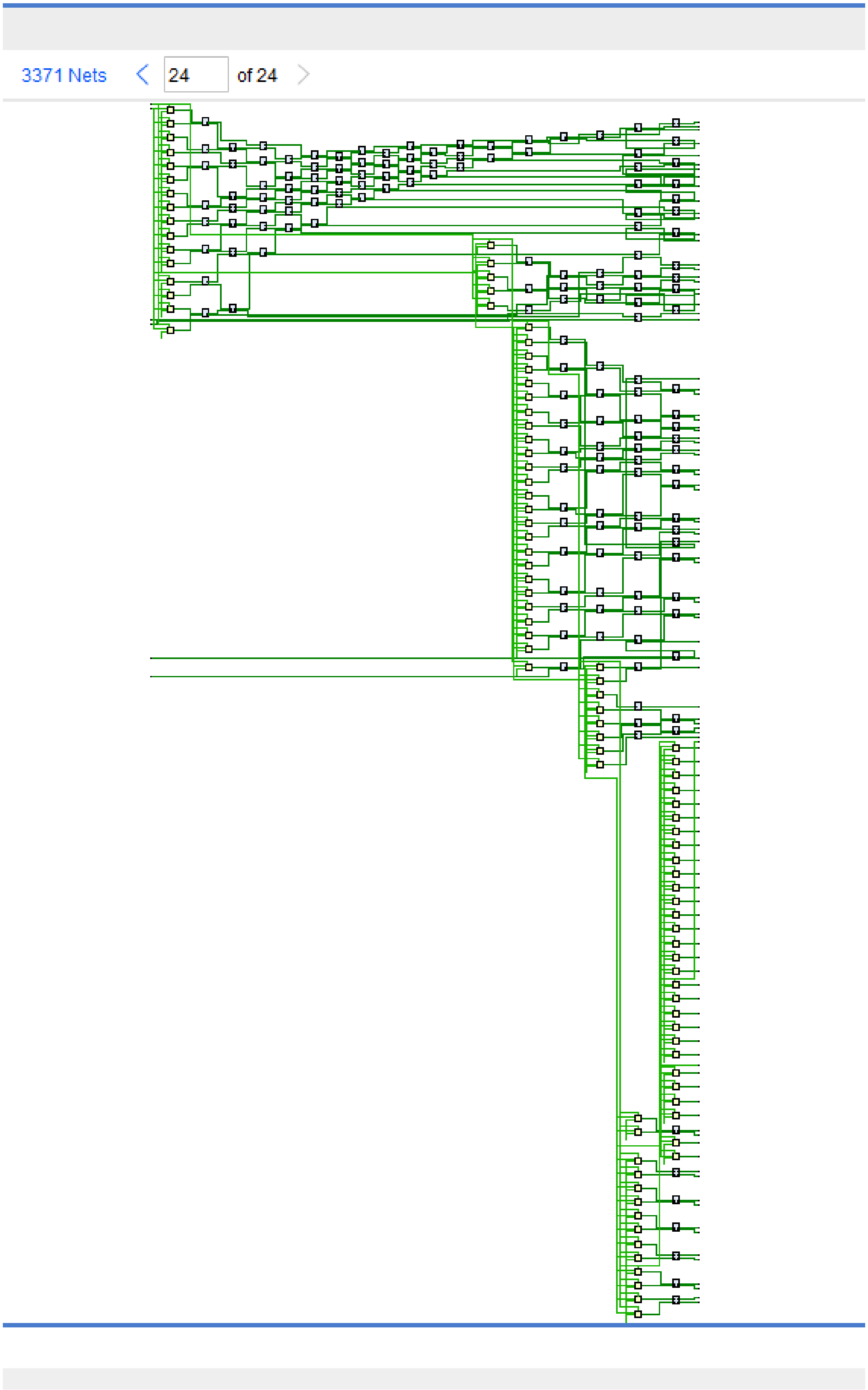
3371 Nets
24
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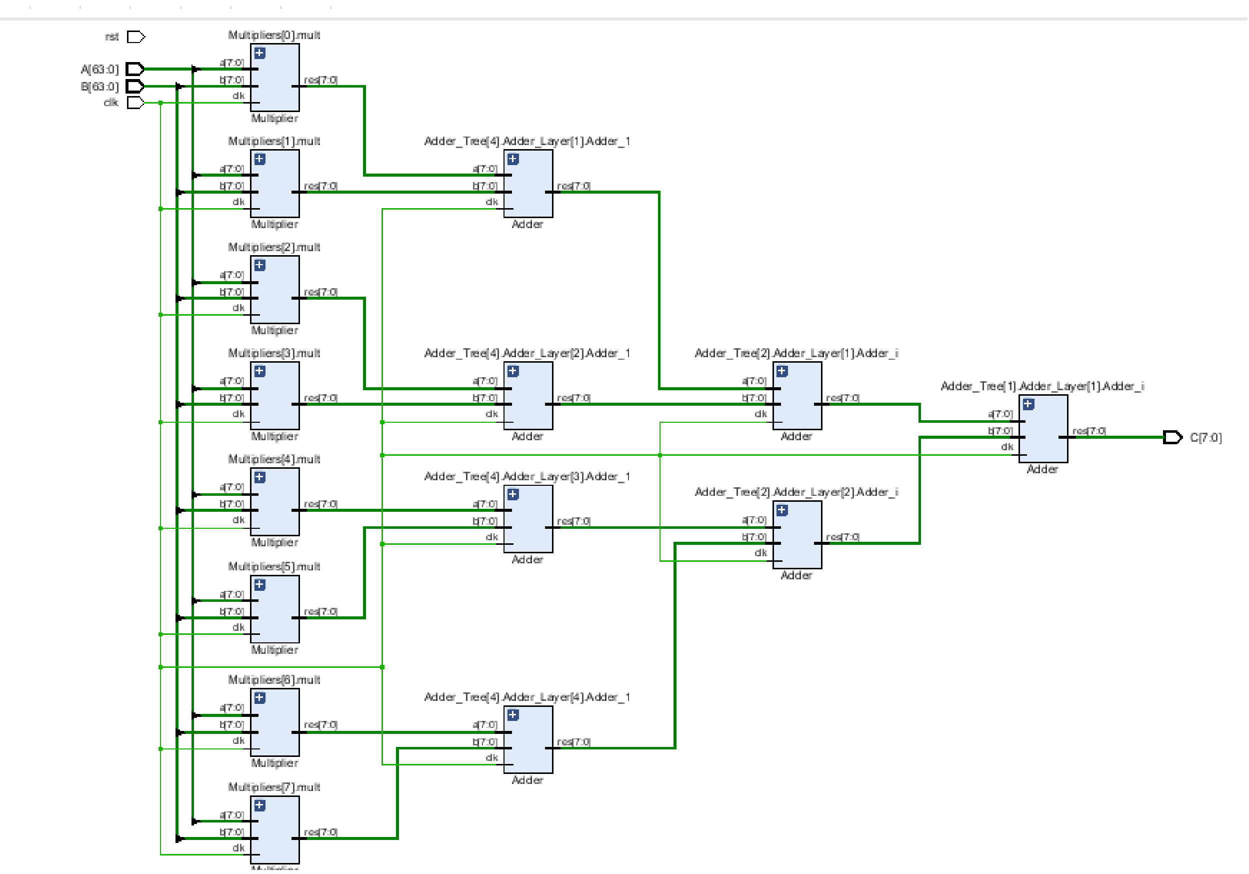
8-bit Matrix multiplier schematic


rst
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B[63:0]
clk
Multipliers[0].mult
Multipliers[1].mult
Multipliers[2].mult
Multipliers[3].mult
Multipliers[4].mult
Multipliers[5].mult
Multipliers[6].mult
Multipliers[7].mult
a[7:0]
b[7:0]
clk
res[7:0]
Multiplier
Adder_Tree[4].Adder_Layer[1].Adder_1
Adder_Tree[4].Adder_Layer[2].Adder_1
Adder_Tree[4].Adder_Layer[3].Adder_1
Adder_Tree[4].Adder_Layer[4].Adder_1
Adder_Tree[2].Adder_Layer[1].Adder_i
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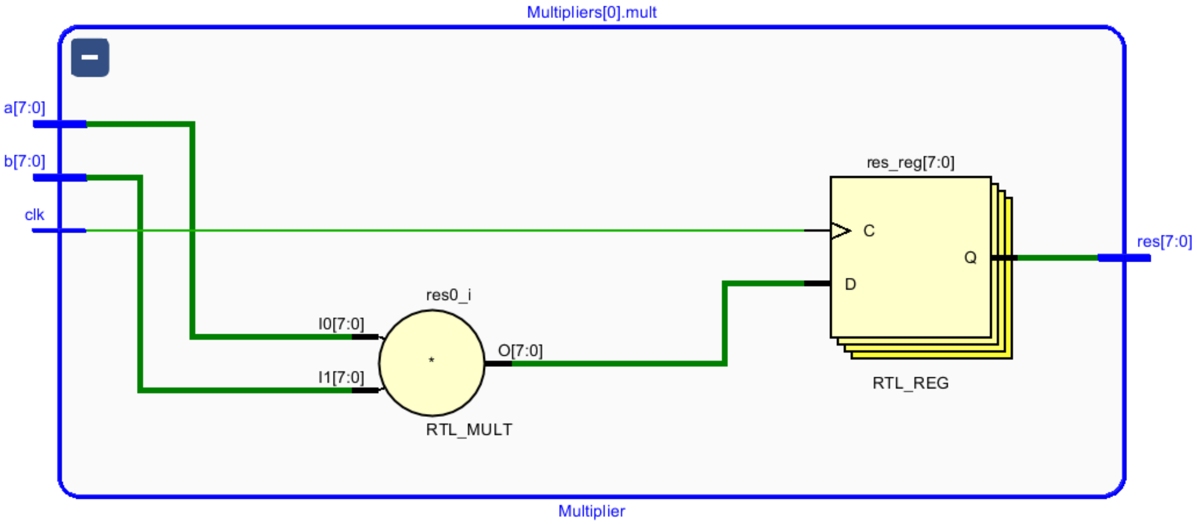
Adder_Tree[1].Adder_Layer[1].Adder_i
Adder
C[7:0]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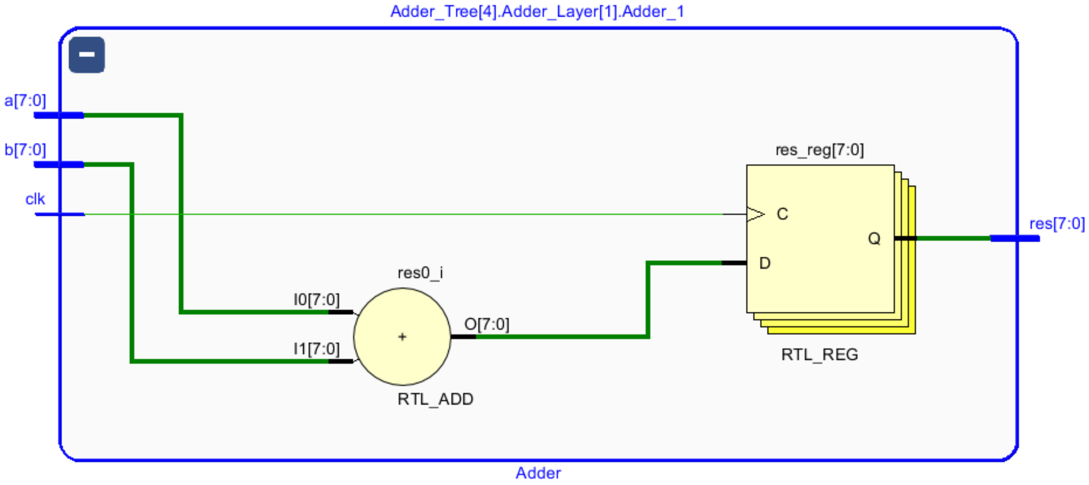
b[7:0]
clk
res_reg[7:0]
C
Q
D
RTL_REG
res[7:0]
res0_i
I0[7:0]
I1[7:0]
*
O[7:0]
RTL_MULT
Multiplier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clk
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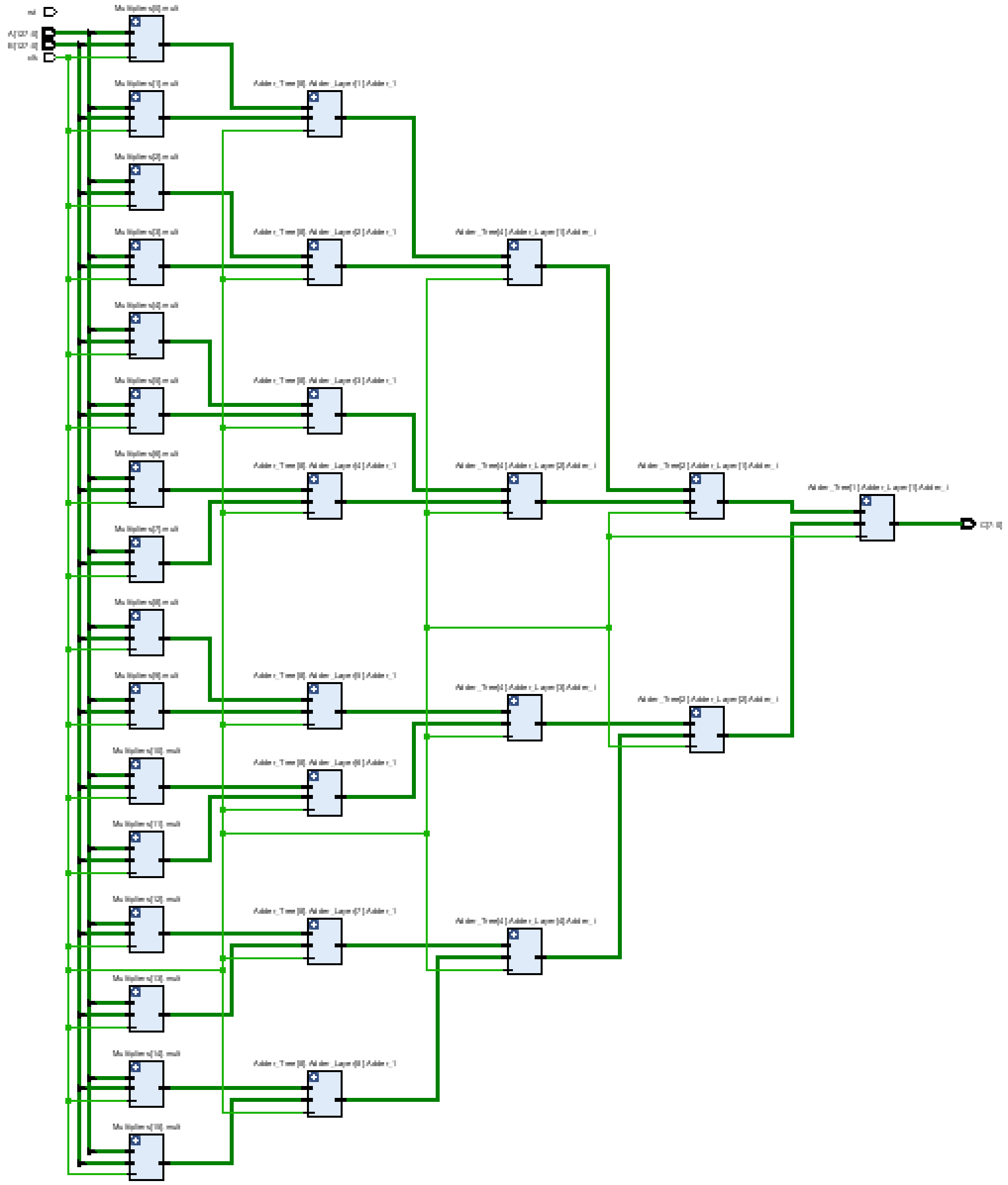
C
Q
D
RTL_REG
res[7:0]
res0_i
I0[7:0]
I1[7:0]
+
O[7:0]
RTL_ADD
Adder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Multipliers[13].mult
Multipliers[14].mult
Multipliers[15].mult
Adder_Tree[8].Adder_Layer[1].Adder_i
Adder_Tree[8].Adder_Layer[2].Adder_i
Adder_Tree[8].Adder_Layer[3].Adder_i
Adder_Tree[8].Adder_Layer[4].Adder_i
Adder_Tree[8].Adder_Layer[5].Adder_i
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Adder_Tree[1].Adder_Layer[1].Adder_i
C[7:0]