

## 1 Barrel Shifter [50 Points]

A Barrel Shifter is a logic circuit for shifting a word by a varying amount. It has a control input (select bits) that specifies the number of bit positions that it shifts. A Barrel Shifter is implemented with a sequence of shift multiplexers, each shifting a word by  $2^k$  bit positions for different values of  $k$ . The diagram below (Figure 1) shows a pipeline clock-wise barrel shifter for 8 inputs.

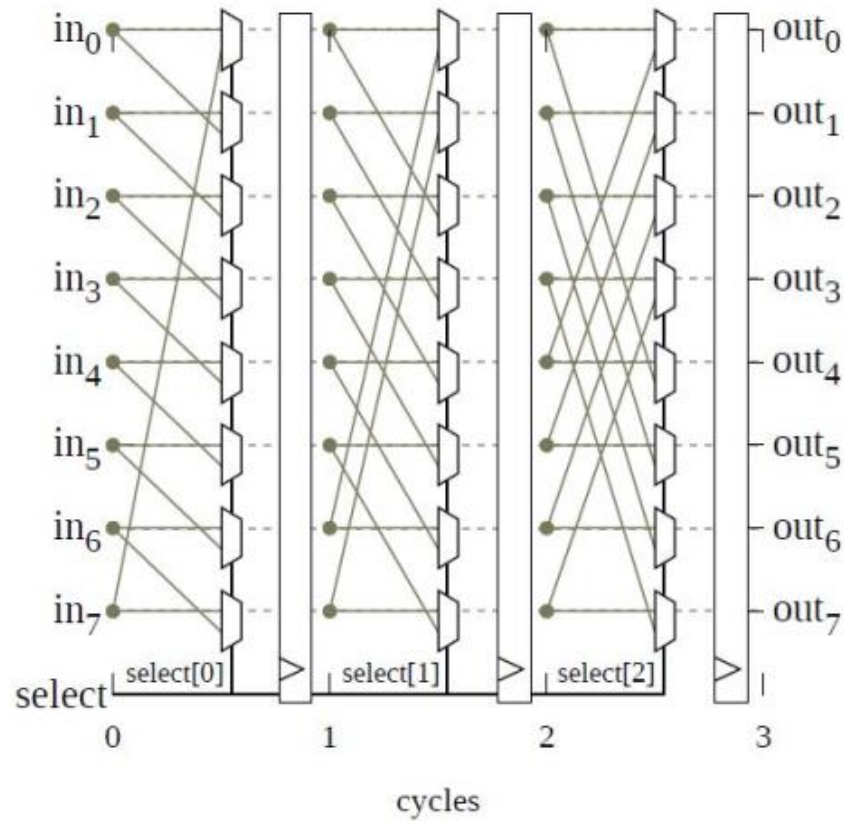


Figure 1: An Example Pipeline Barrel Shifter

Notice that we can shift the input elements by 0 - 7 elements using an implementation like Figure 1. Table 1 shows all the shifting possibilities for the above example.

Similarly, a scalable Barrel Shifter with  $N$  inputs and maximum shift of  $N-1$  can be implemented.

Table 1: All the shifting possibilities for the given example

Select[2]	Select[1]	Select[0]	Shift
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

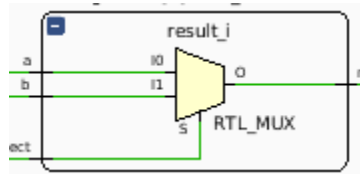
### 1.1 Implementation : Using Xilinx Vivado Software (Use Zynq-7000 xc7z007sclg225-2 FPGA)

Consider only 8-bit arithmetic. **You must implement a scalable design.**

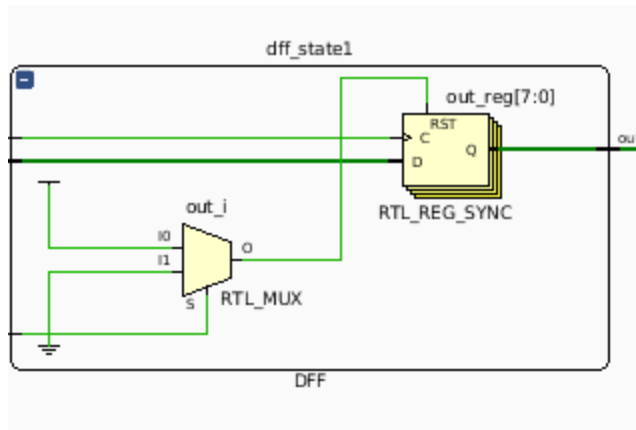
1. Implement a **barrel shifter** design in Verilog which takes  $n$  inputs with 8 bits and shift them by  $r$  (value of  $r$  is passed to select bits and  $r_{max} = (n - 1)$ ).
2. For a 16 elements design with a maximum shift of 15, write a testbench and verify the waveforms.
3. Elaborate the design and include all the schematics screenshots of the modules in the report.
4. Synthesis the design and include the schematics screenshots in the report.
5. Generate Resource and timing estimations and include them in the report.
6. Redo parts 3, 4, 5 for 64 elements (with maximum shift of 63).

#### 1. Schematic Screenshot (for 8 elements)

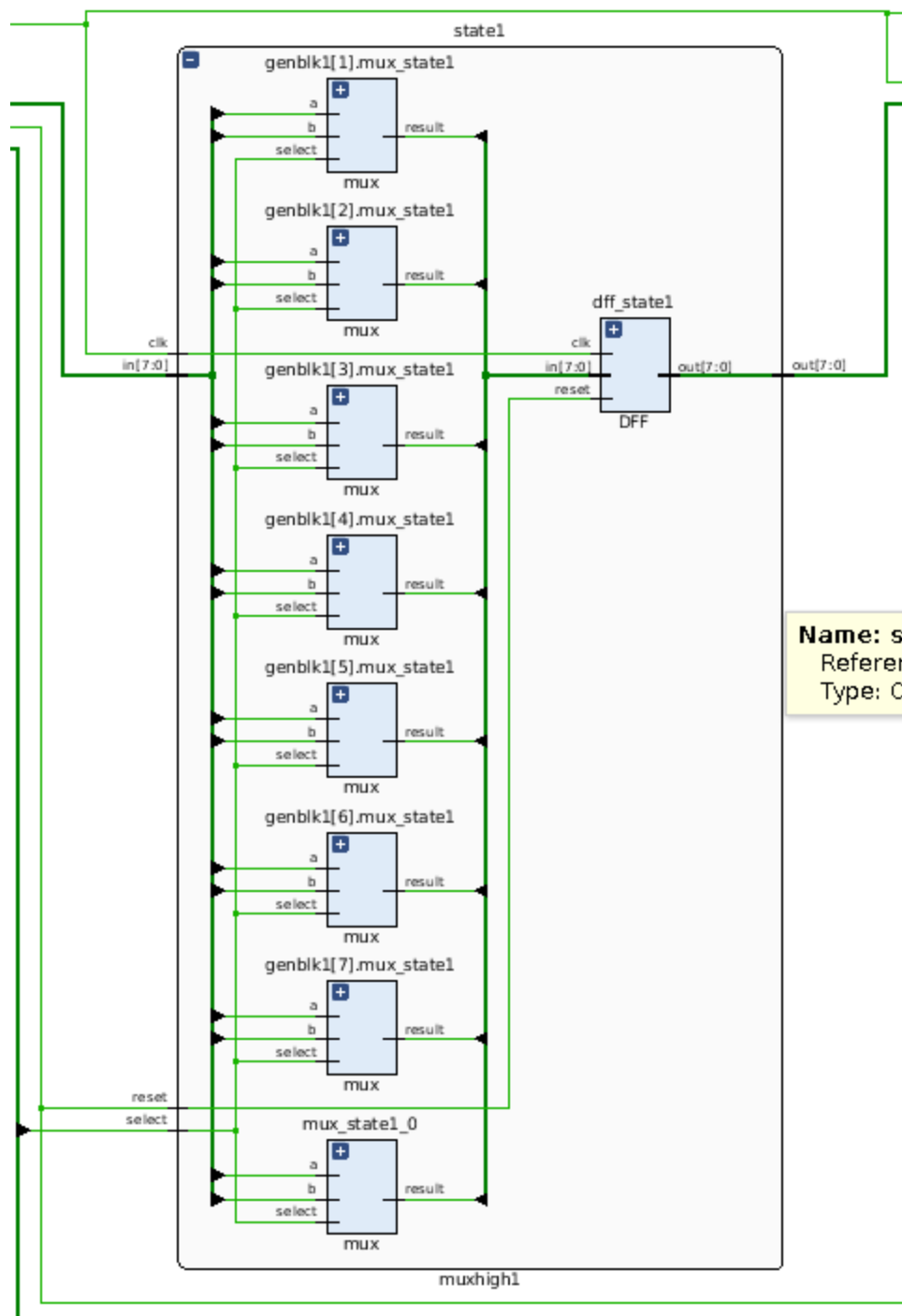
##### a. Mux



##### b. D-FF



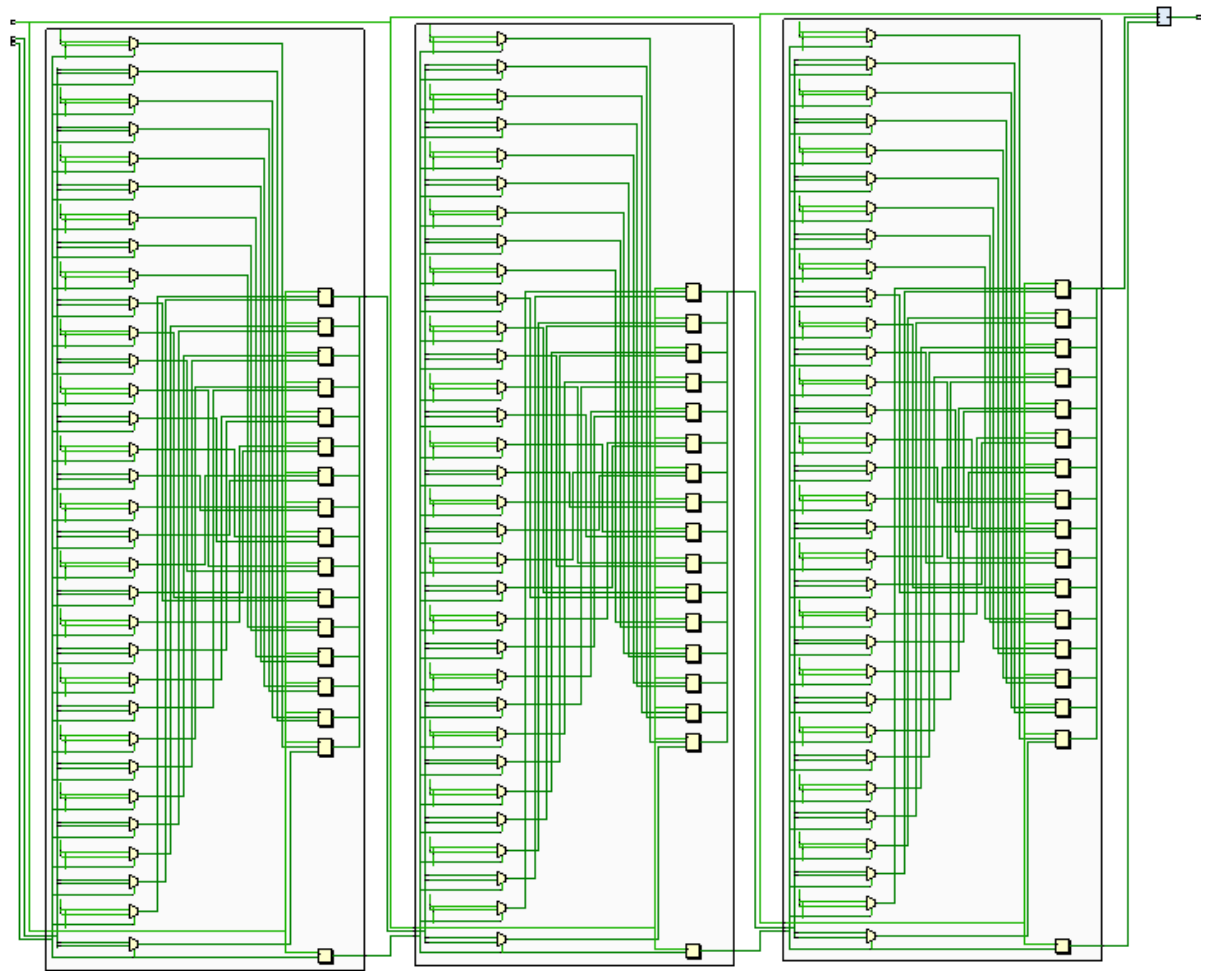
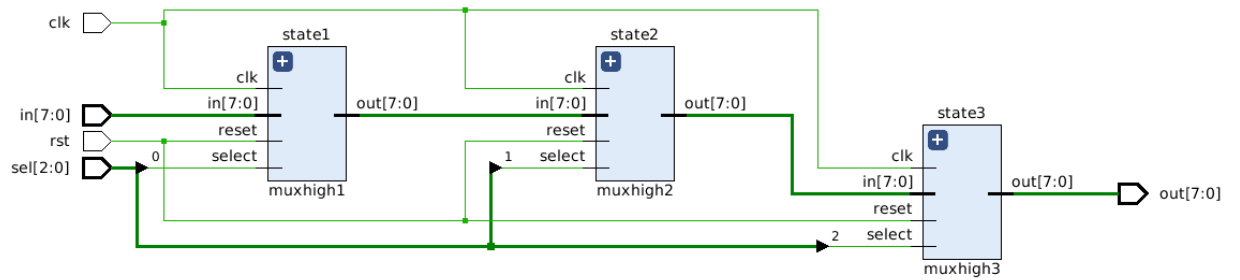
- c. State Machine
  - 1. For single input



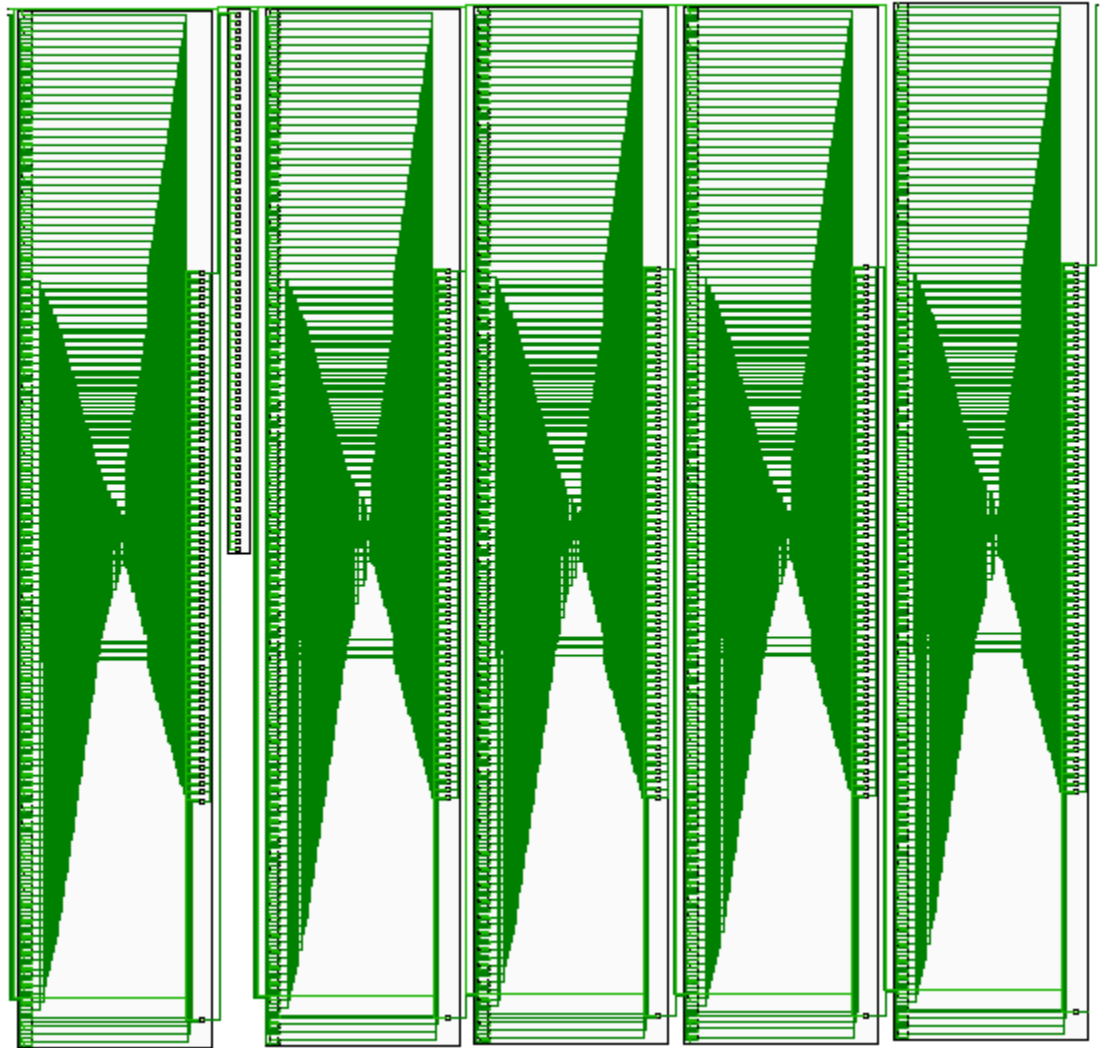
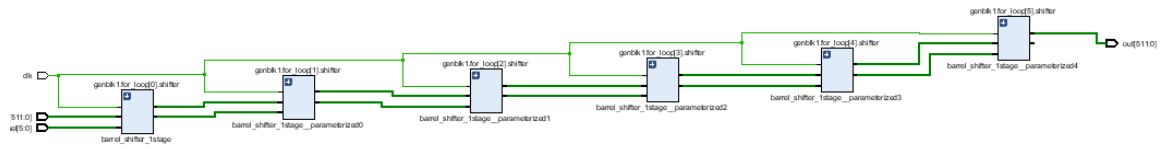
d. Whole Design

2. For multiple input data set =16,64

For data set =16:



For 64 elements:



### 3. Function Waveform Test

Here, we gave the input different value and different number for shifting and it returns different result. For single input and single output.



06	fa	0d	f8	f1	06	fb	08	0a	fa	f9	01	04	f3	0d	08	f5	f1	01	09	06	0a	0c	f9	01	02	
06	0a	f3	01	04	06	0a	f8	fc	02	0a	08	f2	f1	f9	f3	f8	0d	fb	f2	0c	0b	02	0d	08	f2	fc
0b	03	f9	0a	f1	0b	fc	01	0e	fc	03	f8	f5	fb	f1	f9	01	0d	0a	f5	0d	f9	fc	0d	f8	f5	fa
f9	ff	f1	02	fb	f9	0e	0a	06	fa	ff	01	0d	0a	04	f1	0a	f3	fc	0d	08	fa	06	01	0d	0a	
08	0d	04	fc	0a	08	06	02	06	0a	0d	0a	0d	fc	f1	04	02	f9	0e	0d	06	f8	0a	0d	0a	0d	03
f8	fe	f1	fa	fc	f8	06	fc	0b	03	fe	02	f3	0e	fb	f1	fc	f1	06	f3	0d	01	03	01	02	f3	ff
01	f2	fb	0a	0e	01	0b	fa	f9	ff	f2	fc	f9	06	0a	fb	fa	04	06	f9	01	0a	ff	f2	fc	f9	0d
0a	f5	0a	03	06	0a	f9	0a	08	0d	f5	fa	f1	06	fc	0a	0a	f1	0b	f1	f2	02	0d	f5	fa	f1	fe
02	0b	fc	ff	06	02	08	03	f8	fe	0b	0a	04	0b	0e	fc	03	fb	f9	04	f5	fc	fe	0d	0a	04	f2
fc	f3	0e	0d	0b	fc	f8	ff	01	f2	f3	03	f1	f9	06	0e	ff	0a	08	f1	0d	fa	f2	0d	03	f1	f5
fa	fd	06	fe	f9	fa	01	0d	0a	f5	fd	ff	fb	08	06	0d	fc	f8	fb	0d	0a	f5	f3	ff	fb	0b	
0a	f3	06	f2	08	0a		fe	02	0b	f3	0d	0a	f8	0b	06	fe	0e	01	0a	f3	03	0b	f9	0d	0a	f3
03	f6	0b	f5	f8	03	02	f2	fc	f3	f6	fe	fc	01	f9	0b	f2	06	0a	fc	f9	ff	f3	f1	fe	fc	fd
ff	fd	f9	0b	01	ff	fc	f5	fa	fd		f2	0e	0a	08	f9	f5	06	02	0e	f1	0d	fd	04	f2	0e	f3
0d	0a	08	f3	0a	0d	fa	0b	0a	f3	0a	f5	06	02	f8	08	0b	fc	06	04	fe	f3	f1	f5	06	f6	
fe	00	f8	fd	02	fe	0a	f3	03	f6	00	0b	06	fc	01	f8	f3	f9	fa	06	f1	f2	f6	fb	0b	06	fd
f2	00	01	f3	fc	f2	03	fd	ff	fd	00	f3	0b	fa	0a	01	fd	08	0a	0b	fb	f5	fd	0a	f3	0b	0a
f5	0a	f6	fa	f5	ff		f3	0d	0a		fd	f9	0a	02	0a	f3	f8	03	f9	0a	0b	0a	fc	fd	f9	00
0b	f3	02	fd	0a	0b	0d	f6	fe	00	f3	08	03	fc	02		f6	01	ff	08	fc	f3	00	0e	f3	08	00
f3	f5	fc	0a	03	f3	fe	fd	f2	00	f5	f6	f8	ff	fa	fc	fd	0a	0d	f8	0e	fd	00	06	f6	f8	0a
fd		fa	00	ff	fd	f2	0a	f5	0a	fd	01	0d	0a	fa		0a	02	fe	01	06	f3	0a	06	fd	01	f3
f3	fd	0a	00	0d	f3	f5	00	0b	f3	fd	0a	fe	03	0a		00	fc	f2	0a	06	f6	f3	0b	0a	f5	

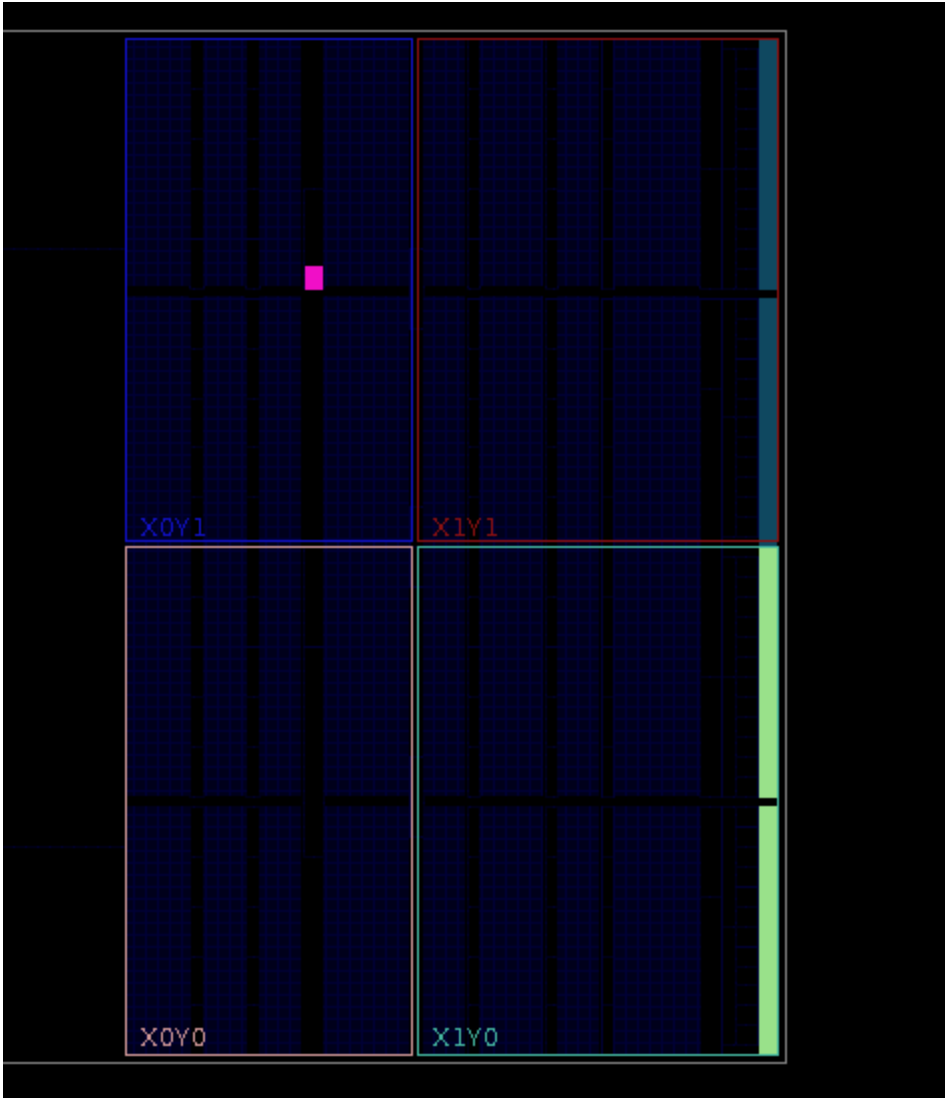


Name	Value												
> ♡ [40][7.0]	00	00	fd	f5	ff	f3	f2	fd	f3	0a	fd		f5
> ♡ [39][7.0]	00	00	0a	f8	0d		f5	0a	fd	f3	fd	f8	
> ♡ [38][7.0]	00				fe		fd	0b	00	f3			
> ♡ [37][7.0]	00			02	f2	fd	f3	00	f6		fd	f5	02
> ♡ [36][7.0]	00	00	0a	0f	f5	0c	fd	0a		fd	0a	f8	0f
> ♡ [35][7.0]	00	00	f3	f2	0b	f5		f3	0a	0c	00	fe	f2
> ♡ [34][7.0]	00	00	f5	f7	f3	f8	fd	f5	00	f5	00	02	f7
> ♡ [33][7.0]	00	00	fd	05	fd	fe		fd		f8	0a	0f	05
> ♡ [32][7.0]	00	00	fd	fa	f3	02	0a	fd	0a	fe	f3	f2	fa
> ♡ [31][7.0]	00	00	0c	f5	f6	0f	00	0c	f3	02	f5	f7	f5
> ♡ [30][7.0]	00	00	f5	f6	fd	f2	00		f5	0f	fd	05	f6
> ♡ [29][7.0]	00	00	f8	09	0a	f7	0a	f8	fd	f2	fd	fa	09
> ♡ [28][7.0]	00	00	fe	0c	00	05	f3	fe	fd	f7	0c	f5	0c
> ♡ [27][7.0]	00	00	02	0d	00	fa	f5	02	0c	05	f5	f6	0d
> ♡ [26][7.0]	00	00	0f	0d	0a	f5	fd	0f	f5	fa	f8	09	0d
> ♡ [25][7.0]	00	00	f2	06	f3	f6	fd	f2	f8	f5	fe	0c	06
> ♡ [24][7.0]	00	00	f7	0d	f5	09	0c	f7	fe	f6	02		0d
> ♡ [23][7.0]	00	00	05	01	fd	0c	f5	05	02	09	0f	0d	01
> ♡ [22][7.0]	00	00	fa	f2	fd	0d	f8	fa	0f	0c	f2	06	f2
> ♡ [21][7.0]	00	00		f5	0c	0d	fe	f5	f2	0d	f7	0d	f5
> ♡ [20][7.0]	00	00	f6	0d	f5	06	02	f6	f7	0d	05	01	0d
> ♡ [19][7.0]	00	00	09	0d	f8	0d	0f	09	05	f2	b6	fa	f2
> ♡ [18][7.0]	00	00	0c	f3	fe	01	f2	0c	fa	0d		f5	

Untitled 18

Q 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000 1001 1002 1003 1004 1005 1006 1007 1008 1009 1010 1011 1012 1013 1014 1015 1016 1017 1018 1019 1020 1021 1022 1023 1024 1025 1026 1027 1028 1029 1030 1031 1032 1033 1034 1035 1036 1037 1038 1039 1040 1041 1042 1043 1044 1045 1046 1047 1048 1049 1050 1051 1052 1053 1054 1055 1056 1057 1058 1059 1060 1061 1062 1063 1064 1065 1066 1067 1068 1069 1070 1071 1072 1073 1074 1075 1076 1077 1078 1079 1080 1081 1082 1083 1084 1085 1086 1087 1088 1089 1090 1091 1092 1093 1094 1095 1096 1097 1098 1099 1100 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110 1111 1112 1113 1114 1115 1116 1117 1118 1119 1120 1121 1122 1123 1124 1125 1126 1127 1128 1129 1130 1131 1132 1133 1134 1135 1136 1137 1138 1139 1140 1141 1142 1143 1144 1145 1146 1147 1148 1149 1150 1151 1152 1153 1154 1155 1156 1157 1158 1159 1160 1161 1162 1163 1164 1165 1166 1167 1168 1169 1170 1171 1172 1173 1174 1175 1176 1177 1178 1179 1180 1181 1182 1183 1184 1185 1186 1187 1188 1189 1190 1191 1192 1193 1194 1195 1196 1197 1198 1199 1200 1201 1202 1203 1204 1205 1206 1207 1208 1209 1210 1211 1212 1213 1214 1215 1216 1217 1218 1219 1220 1221 1222 1223 1224 1225 1226 1227 1228 1229 1230 1231 1232 1233 1234 1235 1236 1237 1238 1239 1240 1241 1242 1243 1244 1245 1246 1247 1248 1249 1250 1251 1252 1253 1254 1255 1256 1257 1258 1259 1260 1261 1262 1263 1264 1265 1266 1267 1268 1269 1270 1271 1272 1273 1274 1275 1276 1277 1278 1279 1280 1281 1282 1283 1284 1285 1286 1287 1288 1289 1290 1291 1292 1293 1294 1295 1296 1297 1298 1299 1300 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310 1311 1312 1313 1314 1315 1316 1317 1318 1319 1320 1321 1322 1323 1324 1325 1326 1327 1328 1329 1330 1331 1332 1333 1334 1335 1336 1337 1338 1339 1340 1341 1342 1343 1344 1345 1346 1347 1348 1349 1350 1351 1352 1353 1354 1355 1356 1357 1358 1359 1360 1361 1362 1363 1364 1365 1366 1367 1368 1369 1370 1371 1372 1373 1374 1375 1376 1377 1378 1379 1380 1381 1382 1383 1384 1385 1386 1387 1388 1389 1390 1391 1392 1393 1394 1395 1396 1397 1398 1399 1400 1401 1402 1403 1404 1405 1406 1407 1408 1409 1410 1411 1412 1413 1414 1415 1416 1417 1418 1419 1420 1421 1422 1423 1424 1425 1426 1427 1428 1429 1430 1431 1432 1433 1434 1435 1436 1437 1438 1439 1440 1441 1442 1443 1444 1445 1446 1447 1448 1449 1450 1451 1452 1453 1454 1455 1456 1457 1458 1459 1460 1461 1462 1463 1464 1465 1466 1467 1468 1469 1470 1471 1472 1473 1474 1475 1476 1477 1478 1479 1480 1481 1482 1483 1484 1485 1486 1487 1488 1489 1490 1491 1492 1493 1494 1495 1496 1497 1498 1499 1500 1501 1502 1503 1504 1505 1506 1507 1508 1509 1510 1511 1512 1513 1514 1515 1516 1517 1518 1519 1520 1521 1522 1523 1524 1525 1526 1527 1528 1529 1530 1531 1532 1533 1534 1535 1536 1537 1538 1539 1540 1541 1542 1543 1544 1545 1546 1547 1548 1549 1550 1551 1552 1553 1554 1555 1556 1557 1558 1559 1560 1561 1562 1563 1564 1565 1566 1567 1568 1569 1570 1571 1572 1573 1574 1575 1576 1577 1578 1579 1580 1581 1582 1583 1584 1585 1586 1587 1588 1589 1590 1591 1592 1593 1594 1595 1596 1597 1598 1599 1600 1601 1602 1603 1604 1605 1606 1607 1608 1609 1610 1611 1612 1613 1614 1615 1616 1617 1618 1619 1620 1621 1622 1623 1624 1625 1626 1627 1628 1629 1630 1631 1632 1633 1634 1635 1636 1637 1638 1639 1640 1641 1642 1643 1644 1645 1646 1647 1648 1649 1650 1651 1652 1653 1654 1655 1656 1657 1658 1659 1660 1661 1662 1663 1664 1665 1666 1667 1668 1669 1670 1671 1672 1673 1674 1675 1676 1677 1678 1679 1680 1681 1682 1683 1684 1685 1686 1687 1688 1689 1690 1691 1692 1693 1694 1695 1696 1697 1698 1699 1700 1701 1702 1703 1704 1705 1706 1707 1708 1709 1710 1711 1712 1713 1714 1715 1716 1717 1718 1719 1720 1721 1722 1723 1724 1725 1726 1727 1728 1729 1730 1731 1732 1733 1734 1735 1736 1737 1738 1739 1740 1741 1742 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752 1753 1754 1755 1756 1757 1758 1759 1760 1761 1762 1763 1764 1765 1766 1767 1768 1769 1770 1771 1772 1773 1774 1775 1776 1777 1778 1779 1780 1781 1782 1783 1784 1785 1786 1787 1788 1789 1790 1791 1792 1793 1794 1795 1796 1797 1798 1799 1800 1801 1802 1803 1804 1805 1806 1807 1808 1809 1810 1811 1812 1813 1814 1815 1816 1817 1818 1819 1820 1821 1822 1823 1824 1825 1826 1827 1828 1829 1830 1831 1832 1833 1834 1835 1836 1837 1838 1839 1840 1841 1842 1843 1844 1845 1846 1847 1848 1849 1850 1851 1852 1853 1854 1855 1856 1857 1858 1859 1860 1861 1862 1863 1864 1865 1866 1867 1868 1869 1870 1871 1872 1873 1874 1875 1876 1877 1878 1879 1880 1881 1882 1883 1884 1885 1886 1887 1888 1889 1890 1891 1892 1893 1894 1895 1896 1897 1898 1899 1900 1901 1902 1903 1904 1905 1906 1907 1908 1909 1910 1911 1912 1913 1914 1915 1916 1917 1918 1919 1920 1921 1922 1923 1924 1925 1926 1927 1928 1929 1930 1931 1932 1933 1934 1935 1936 1937 1938 1939 1940 1941 1942 1943 1944 1945 1946 1947 1948 1949 1950 1951 1952 1953 1954 1955 1956 1957 1958 1959 1960 1961 1962 1963 1964 1965 1966 1967 1968 1969 1970 1971 1972 1973 1974 1975 1976 1977 1978 1979 1980 1981 1982 1983 1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 2100 2101 2102 2103 2104 2105 2106 2107 2108 2109 2110 2111 2112 2113 2114 2115 2116 2117 2118 2119 2120 2121 2122 2123 2124 2125 2126 2127 2128 2129 2130 2131 2132 2133 2134 2135 2136 2137 2138 2139 2140 2141 2142 2143 2144 2145 2146 2147 2148 2149 2150 2151 2152 2153 2154 2155 2156 2157 2158 2





5. Timing Estimation

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.609 ns	Worst Hold Slack (WHS): 0.127 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 16	Total Number of Endpoints: 16	Total Number of Endpoints: 25
All user specified timing constraints are met.		

6. Resources Estimation

Hierarchy					
Name	^ 1	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
▼ top		13	24	21	1
> state1 (muxhigh1)		8	8	0	0
> state2 (muxhigh2)		4	8	0	0
> state3 (muxhigh3)		1	8	0	0

i)

## 7. Power Estimation

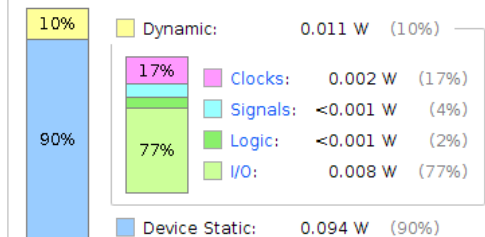
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 0.105 W  
**Design Power Budget:** Not Specified  
**Power Budget Margin:** N/A  
**Junction Temperature:** 26.2°C  
 Thermal Margin: 73.8°C (6.2 W)  
 Effective  $\theta_{JA}$ : 11.5°C/W  
 Power supplied to off-chip devices: 0 W  
 Confidence level: Low

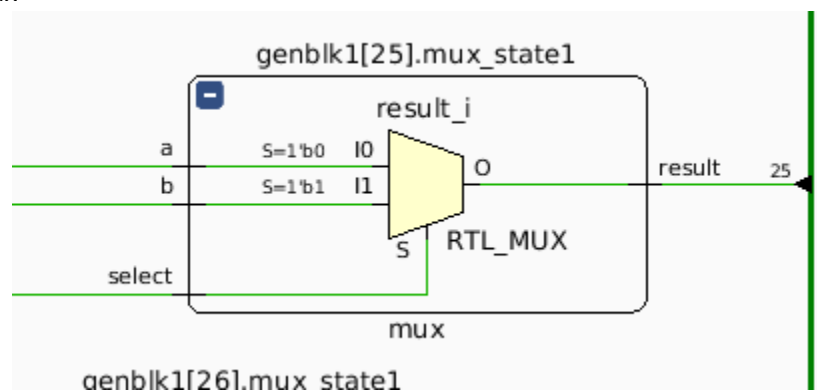
[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power

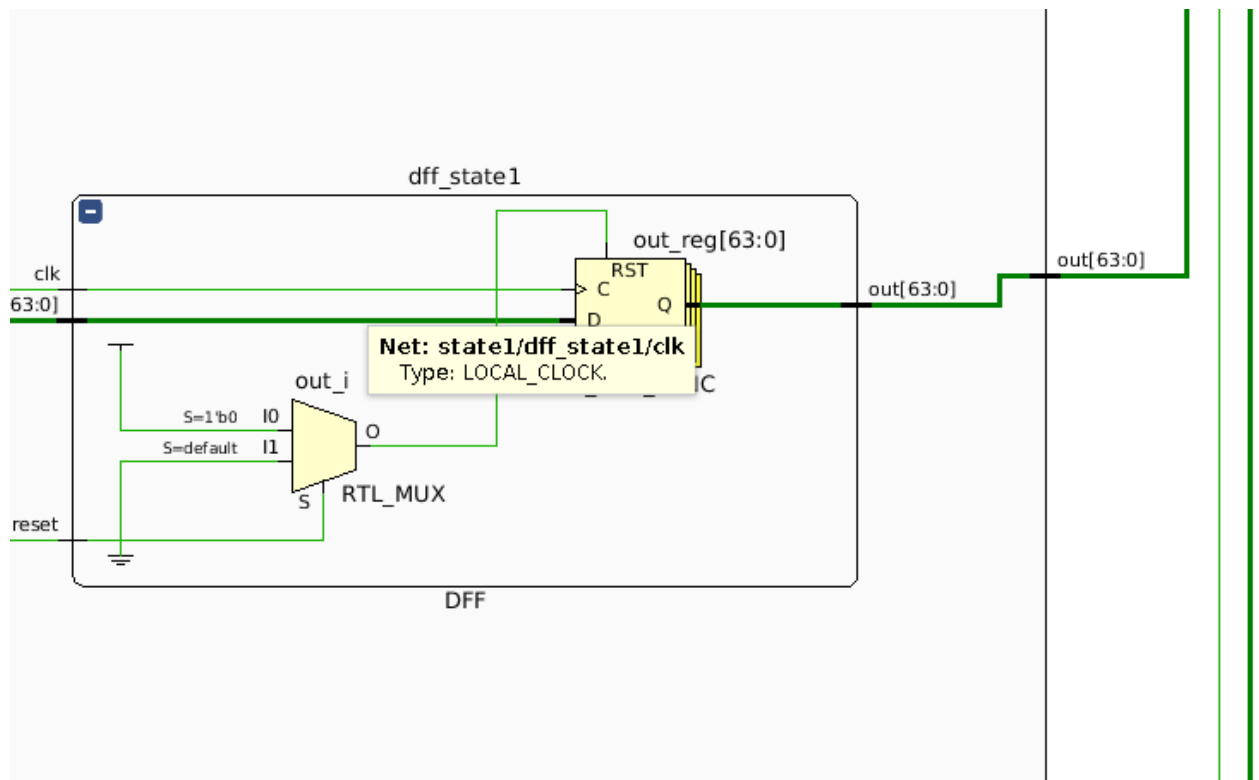


## 1. Schematic Screenshot (for 64 elements)

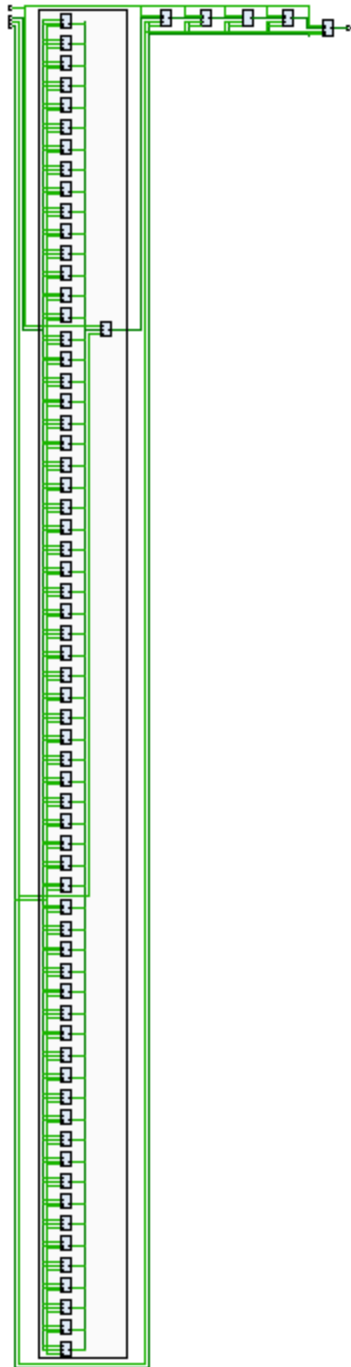
### a. Mux



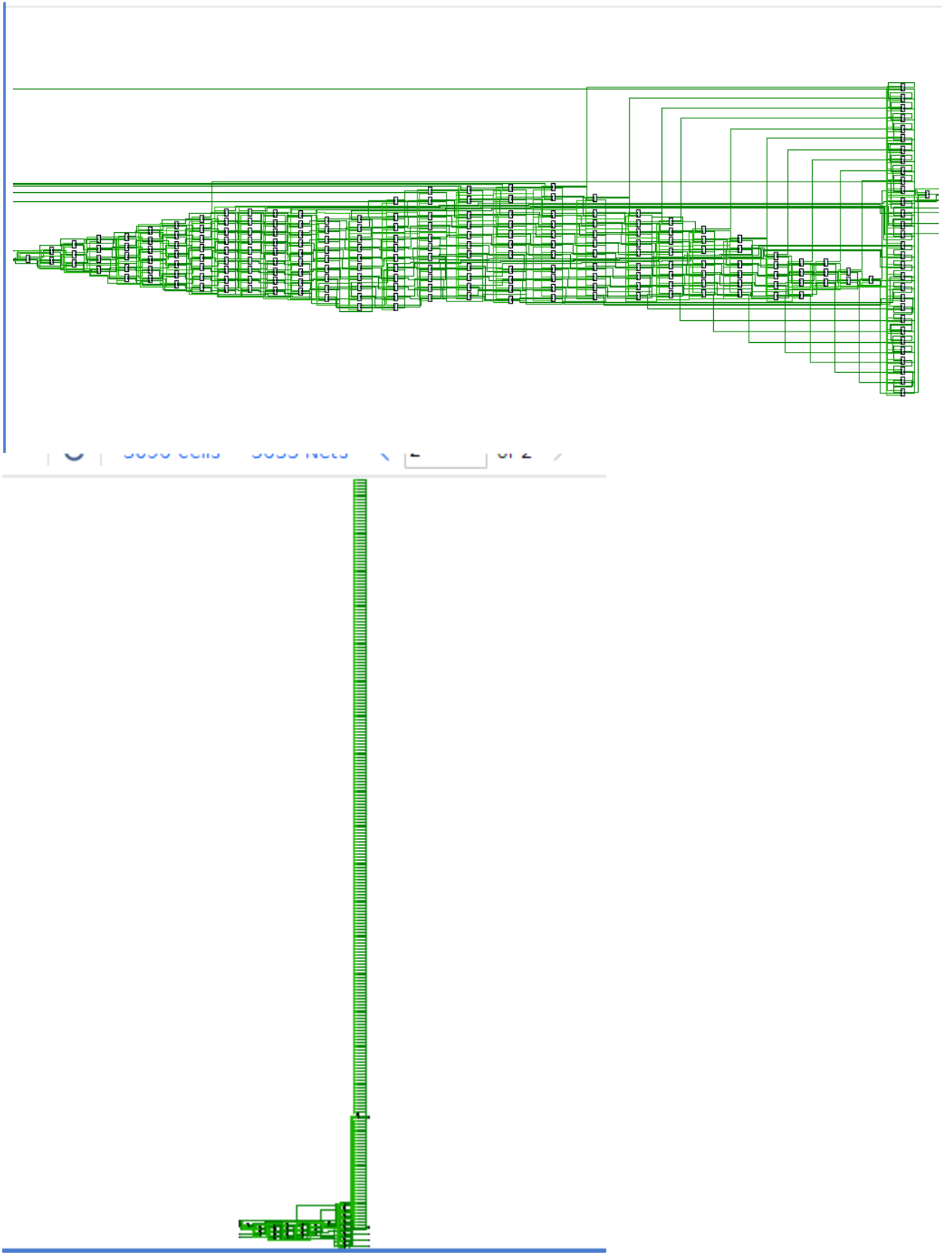
### b. D-FF



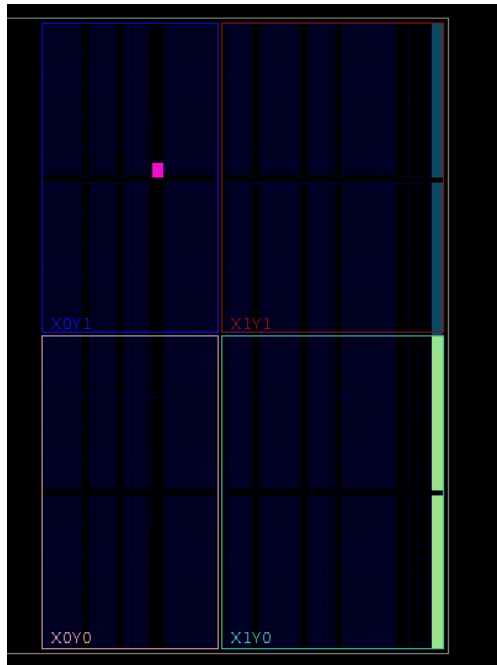
c. State Machine



d. Whole Design



## 2. Synthesis Screenshot



### 3. Timing Estimation

#### 4. Resources Estimation

Name	Slice LUTs (14400)	Slice Registers (28800)	Bonded IOB (54)	BUFGCTRL (32)
top	193	384	136	1
state1 (state1)	64	64	0	0
state2 (state2)	32	64	0	0
state3 (state3)	32	64	0	0
state4 (state4)	32	64	0	0
state5 (state5)	32	64	0	0
state6 (state6)	1	64	0	0

## 5. Power Estimation



## Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** **46.462 W (junction temp exceeded!)**

**Design Power Budget:** **Not Specified**

**Power Budget Margin:** **N/A**

**Junction Temperature:** **125.0°C**

Thermal Margin: **-460.9°C (-39.5 W)**

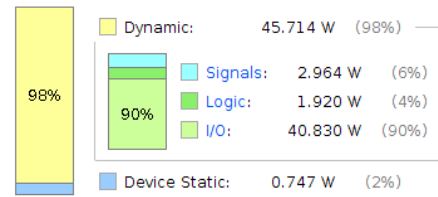
Effective  $\theta_{JA}$ : 11.5°C/W

Power supplied to off-chip devices: 0 W

Confidence level: **Low**

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

## On-Chip Power



## 2 Systolic Array for Dense Matrix-Matrix Multiplication [50 Points]

The Systolic Architecture consists of an array of processing elements, where data flows between neighboring elements, synchronously, from different directions. Processing element takes data from Top, Left, and output the results to Right, Bottom.

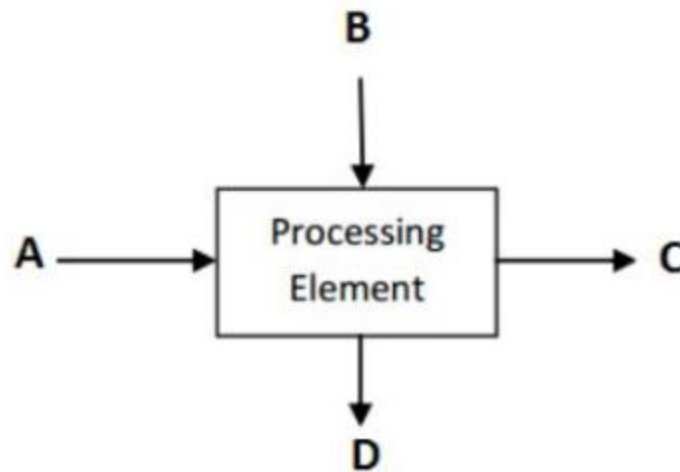


Figure 2: Inputs and outputs to the Processing Elements

One of the main applications of Systolic Architecture is matrix multiplication. As the following figure depicts,  $in\_a$ ,  $in\_b$  are inputs to the processing element and  $out\_a$ ,  $out\_b$  are output to the processing element.  $out\_c$  is to get the output result of each processing element.

Processing elements are arranged in the form of an array. In the following example, we

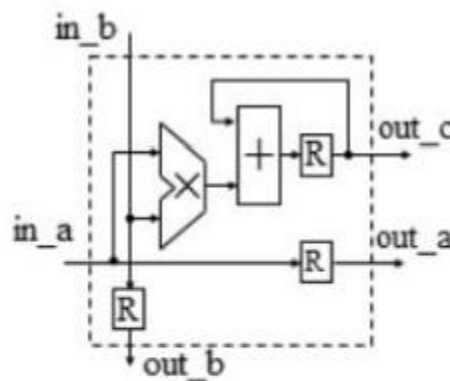


Figure 3: Internals of the PE

analyze, multiplication of  $3 \times 3$  matrices, which can be easily extended. Let say the two matrices are A and B. Figure 4 depicts how matrix A and B are fed into PE array.

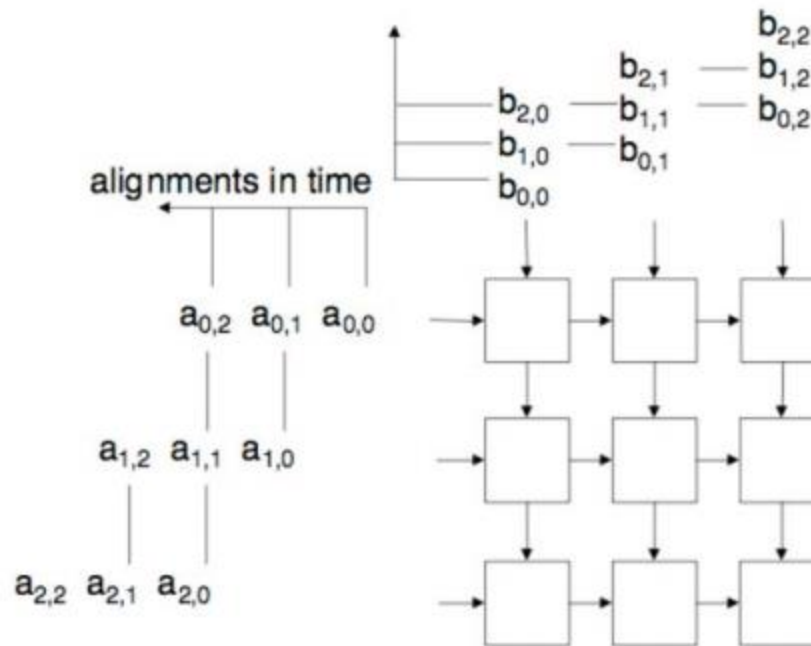


Figure 4: Example  $3 \times 3$  Systolic Array

### 2.0.1 Implementation : Using Xilinx Vivado Software (Use Zynq-7000 xc7z007sclg225-2 FPGA)

Consider only 8-bit arithmetic. All the values are already stored in the BRAM.

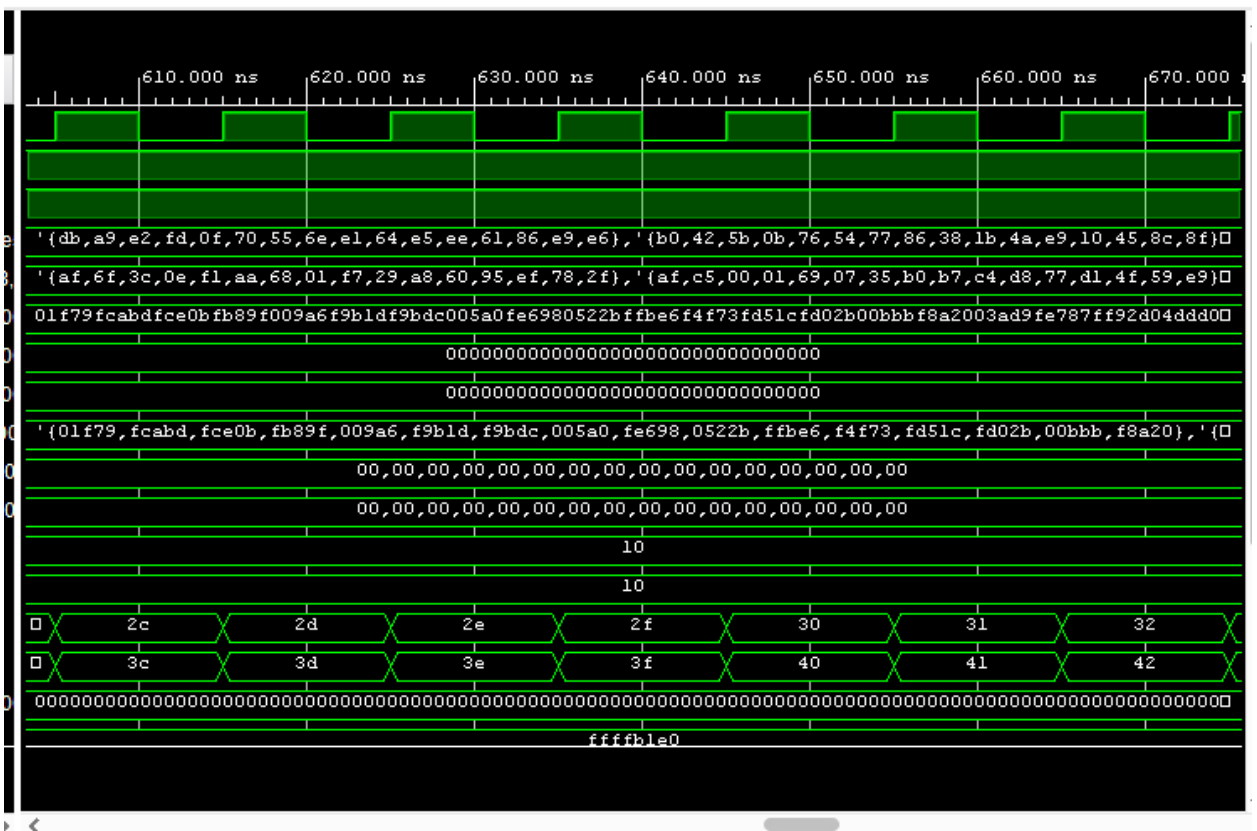
**You must implement a scalable design.**

1. Implement a **Systolic Array** design in Verilog, which takes two  $n \times n$  matrices and multiply them together.
2. Write a testbench that takes two  $16 \times 16$  matrices to the design and provide an output of  $16 \times 16$ .
3. Simulate the design using the Vivado simulator and include the waveform in the report (clearly indicate the locations where final outputs produced).
4. Elaborate the design for  $16 \times 16$  and include all the schematic screenshots of the modules in the report.
5. Synthesis the design and include the schematics screenshots in the report.
6. Generate Resource and timing estimations and include them in the report.
7. Generate power estimation reports and include them in the report.
8. Similarly provides reports for  $32 \times 32$  matrix multiplication.

#### A. 16\*16 Systolic Array

##### 1. Schematic Implementation & Function Test

Here we randomly choose number from 0-128, and generate outcome as a txt format in testbench, after that, we can compare the outcome value by writing just a simple python.



Matrix\_Result.txt - Notepad

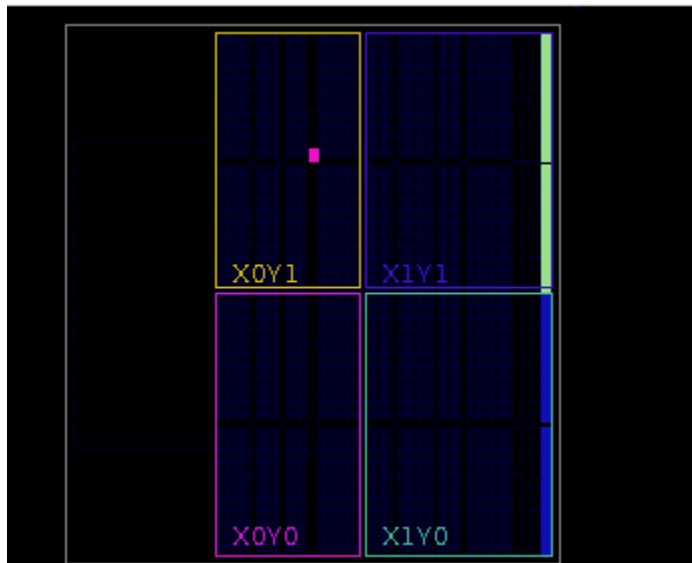
File	Edit	Format	View	Help											
3114	-10640	-27926	-13544	-16209	-1263	12293	-33605	7028	-3902	12368	-3678	5507	-18234	992	20080
10920	-22488	-33234	-31020	-35348	-7150	26906	15509	2755	-53529	34111	-21830	5012	11705	1524	3324
-17906	40885	9855	-18866	3021	-25479	9385	-32502	3997	21070	-38247	-941	19045	-7646	-11898	-13227
27949	51370	-5816	-3119	26269	-26682	12086	12738	-11100	-41620	-13960	-23479	-11838	50478	-9924	-1964
18809	56296	-10850	17478	29892	-26402	-26188	4757	14483	-2820	-50983	-25427	848	39672	17274	21739
31847	1790	4919	1981	33137	-5055	13080	11359	-28525	-23813	35856	13710	-21713	25215	-8073	-18945
-36227	4776	-6294	-11310	8916	17916	-16025	8769	13360	26046	-35808	23550	6674	-26450	19016	22804
12125	8648	-7393	22332	15958	-23286	-37675	-27645	-27212	-39425	-18406	55	-18551	21627	-35294	32473
-31557	2750	-25527	-12004	-46575	2442	-13473	10	34352	13280	-49281	-14723	17137	-16335	16825	12036
-13391	16883	22203	24910	11320	26897	1131	-27146	2056	18480	-9227	2309	-4817	-17997	-5820	5112
-4970	-3988	-6161	43121	25463	38745	2804	12475	4426	12924	-14788	14585	10028	-18794	3846	21449
12333	-41526	13528	22571	-18082	-9926	-9863	13394	-11995	8536	26373	40363	4070	-10070	1819	34060
19176	-17637	18361	8911	4845	5052	1498	-3612	-4438	25221	8006	4528	8635	587	18941	-7739
26506	-22704	14955	-15880	14619	-20331	-15743	-4646	-26791	9559	56665	31503	-24687	8602	3674	-5321
21499	11313	13196	32578	-3418	3982	16266	-4968	-2656	-5712	8891	46261	19933	-1747	-6265	15065
-30176	3003	-12245	-10980	-45197	-1050	21035	-6504	1440	-25636	-25827	2470	-18273	-12789	-13635	8057

Matrix\_A.txt - Notepad

File	Edit	Format	View	Help											
36	-119	13	-27	1	118	109	121	-59	101	-110	114	-24	92	-83	-29
0	42	-106	-115	107	-126	29	35	-54	114	65	120	107	70	-68	-117
5	-69	-2	113	98	31	120	-97	-37	-55	-41	22	-62	-9	18	109
31	5	91	-65	88	-114	122	115	-81	-33	119	-26	41	-38	-75	121
-48	43	92	-3	86	-25	54	121	20	-124	91	89	-10	54	-58	119
-76	40	-57	-120	-3	-100	-38	102	-13	94	85	-71	22	38	125	6
126	-49	-6	23	6	117	-87	-59	75	-20	78	41	14	-97	42	30
-7	74	107	54	68	18	127	122	50	4	74	-95	-5	-17	54	-113
8	27	40	75	-98	108	81	-63	88	-42	-30	115	18	-71	-95	1
39	-97	88	20	-106	85	43	45	4	-25	-55	73	-95	122	3	-14
-24	6	56	-88	-59	116	-80	42	21	23	73	37	-115	7	12	-69
-9	-36	-96	114	93	75	-98	-5	-125	29	68	-32	82	13	4	-116
23	4	124	58	-90	50	-55	-67	-36	6	-76	-84	7	17	-53	108
36	-71	-44	29	2	-39	-100	99	-56	58	-85	-110	89	-18	91	59
-113	-116	69	16	-23	74	27	56	-122	119	84	118	11	91	66	-80
-26	-23	-122	97	-18	-27	100	-31	110	85	112	15	-3	-30	-87	-37

File	Edit	Format	View	Help											
-127	-29	13	-110	13	61	12	-58	-86	-9	15	-50	-59	-67	-27	10
32	-99	-109	-45	-43	-82	-49	10	-68	10	-40	-119	54	46	42	-15
79	58	21	89	76	15	-73	-36	9	-48	-47	12	72	61	-2	57
-45	-8	73	42	-122	-100	-90	-93	-77	68	-53	90	-19	-27	-33	68
42	14	-102	-61	78	-118	-72	-72	19	-39	-51	-19	74	21	4	105
8	-83	-82	28	41	6	-67	-16	58	122	-102	55	64	-74	92	120
-37	121	-31	-95	-48	-75	65	-104	-13	-118	-88	-95	-26	42	-115	-72
72	19	-57	58	57	-76	-122	-14	-67	-28	41	14	-117	73	-11	107
-82	18	-83	-62	13	24	-122	-69	83	-37	-124	-40	-72	-27	43	72
33	-124	-106	-110	-79	-19	117	-89	-89	-71	91	81	42	-59	-4	-2
-17	112	64	118	64	57	60	98	-31	-61	-122	65	-38	44	-15	54
-98	85	-96	-76	-115	-7	-3	15	99	49	-107	-19	120	-46	70	16
106	-86	-32	-117	-91	-94	-108	75	71	-71	80	12	-22	104	115	35
73	-33	103	48	73	32	19	-86	-35	4	57	-46	-48	23	38	0
-23	89	79	-47	119	-40	-60	-73	-80	53	7	105	1	0	-59	-81
47	120	-17	-107	96	-88	41	-9	1	104	-86	-15	14	60	111	-81

## 2. Synthesis schematic

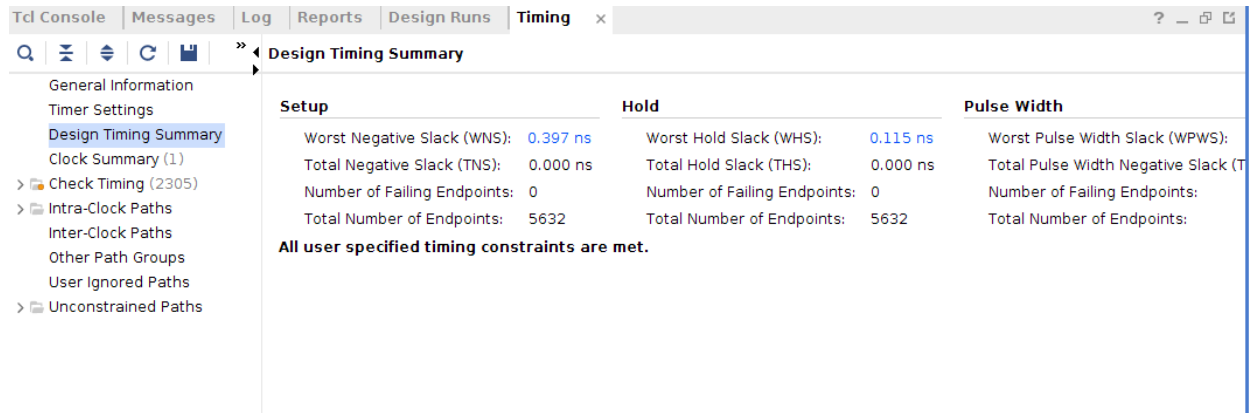


## 3. Resources Utilization

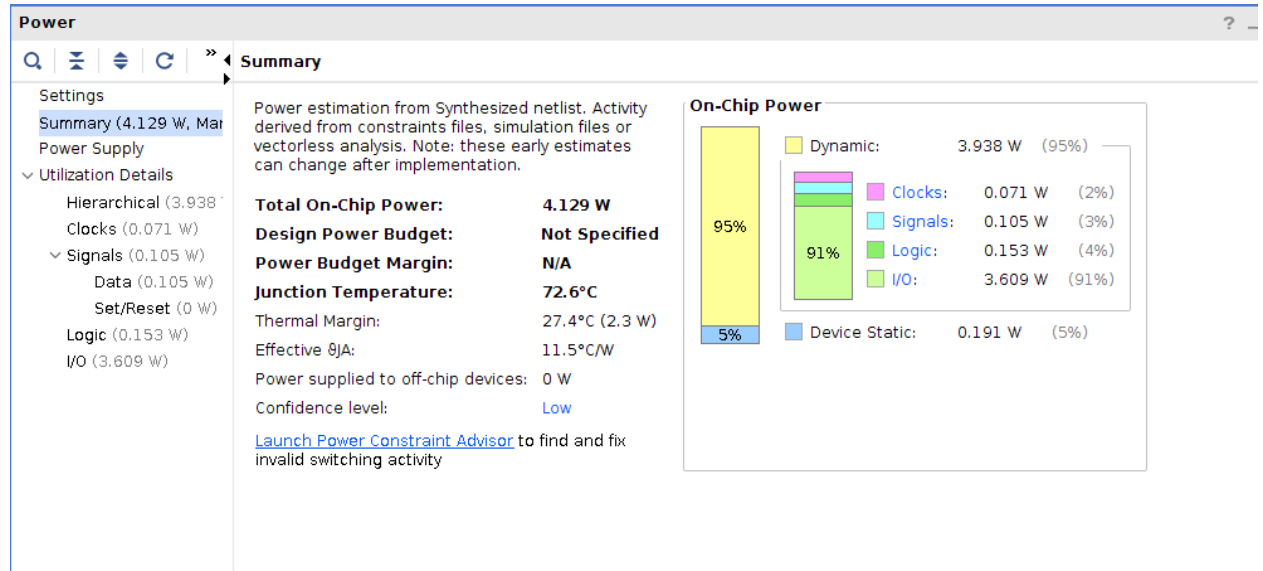
Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Timing	
Hierarchy							
Hierarchy	Name						
Summary	^ 1	Slice LUTs ...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)		
▼ Slice Logic	▼ top	11262	5888	5378	1		
▼ Slice LUTs (78%)	genblk2[0].genblk1[0].pe1 (pe_	104	24	0	0		
LUT as Logic (78	genblk2[0].genblk1[1].pe1 (pe_6)	58	24	0	0		
▼ Slice Registers (20%)	genblk2[0].genblk1[2].pe1 (pe_7)	58	24	0	0		
Register as Flip I	genblk2[0].genblk1[3].pe1 (pe_8)	58	24	0	0		
Memory	genblk2[0].genblk1[4].pe1 (pe_9)	58	24	0	0		
DSP	genblk2[0].genblk1[5].pe1 (pe_10)	58	24	0	0		
▼ IO and GT Specific	genblk2[0].genblk1[6].pe1 (pe_11)	58	24	0	0		
Bonded IOB (>100%	genblk2[0].genblk1[7].pe1 (pe_12)	58	24	0	0		
▼ Clocking	genblk2[0].genblk1[8].pe1 (pe_13)	58	24	0	0		
BUFGCTRL (3%)	genblk2[0].genblk1[9].pe1 (pe_14)	58	24	0	0		
Specific Feature	genblk2[0].genblk1[10].pe1 (pe_0)	58	24	0	0		
Primitives	genblk2[0].genblk1[11].pe1 (pe_1)	58	24	0	0		
Black Boxes	genblk2[0].genblk1[12].pe1 (pe_2)	58	24	0	0		
Instantiated Netlists	genblk2[0].genblk1[13].pe1 (pe_3)	58	24	0	0		
	genblk2[0].genblk1[14].pe1 (pe_4)	58	24	0	0		
	genblk2[0].genblk1[15].pe1 (pe_5)	27	16	0	0		
	genblk2[1].genblk1[0].pe1 (pe_111)	61	24	0	0		
	genblk2[1].genblk1[1].pe1 (pe_118)	44	24	0	0		
	genblk2[1].genblk1[2].pe1 (pe_119)	44	24	0	0		
	genblk2[1].genblk1[3].pe1 (pe_120)	44	24	0	0		
	genblk2[1].genblk1[4].pe1 (pe_121)	44	24	0	0		
	genblk2[1].genblk1[5].pe1 (pe_122)	44	24	0	0		

Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Timing	
Hierarchy							
Hierarchy	Name						
Summary	^ 1	Slice LUTs ...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)		
▼ Slice Logic	genblk2[5].genblk1[15].pe1 (pe_181)	27	16	0	0		
▼ Slice LUTs (78%)	genblk2[6].genblk1[0].pe1 (pe_191)	61	24	0	0		
LUT as Logic (78	genblk2[6].genblk1[1].pe1 (pe_198)	44	24	0	0		
▼ Slice Registers (20%)	genblk2[6].genblk1[2].pe1 (pe_199)	44	24	0	0		
Register as Flip I	genblk2[6].genblk1[3].pe1 (pe_200)	44	24	0	0		
Memory	genblk2[6].genblk1[4].pe1 (pe_201)	44	24	0	0		
DSP	genblk2[6].genblk1[5].pe1 (pe_202)	44	24	0	0		
▼ IO and GT Specific	genblk2[6].genblk1[6].pe1 (pe_203)	44	24	0	0		
Bonded IOB (>100%	genblk2[6].genblk1[7].pe1 (pe_204)	44	24	0	0		
▼ Clocking	genblk2[6].genblk1[8].pe1 (pe_205)	44	24	0	0		
BUFGCTRL (3%)	genblk2[6].genblk1[9].pe1 (pe_206)	44	24	0	0		
Specific Feature	genblk2[6].genblk1[10].pe1 (pe_192)	44	24	0	0		
Primitives	genblk2[6].genblk1[11].pe1 (pe_193)	44	24	0	0		
Black Boxes	genblk2[6].genblk1[12].pe1 (pe_194)	44	24	0	0		
Instantiated Netlists	genblk2[6].genblk1[13].pe1 (pe_195)	44	24	0	0		
	genblk2[6].genblk1[14].pe1 (pe_196)	44	24	0	0		
	genblk2[6].genblk1[15].pe1 (pe_197)	27	16	0	0		
	genblk2[7].genblk1[0].pe1 (pe_207)	61	24	0	0		
	genblk2[7].genblk1[1].pe1 (pe_214)	44	24	0	0		
	genblk2[7].genblk1[2].pe1 (pe_215)	44	24	0	0		
	genblk2[7].genblk1[3].pe1 (pe_216)	44	24	0	0		
	genblk2[7].genblk1[4].pe1 (pe_217)	44	24	0	0		
	genblk2[7].genblk1[5].pe1 (pe_218)	44	24	0	0		

#### 4. Timing Report



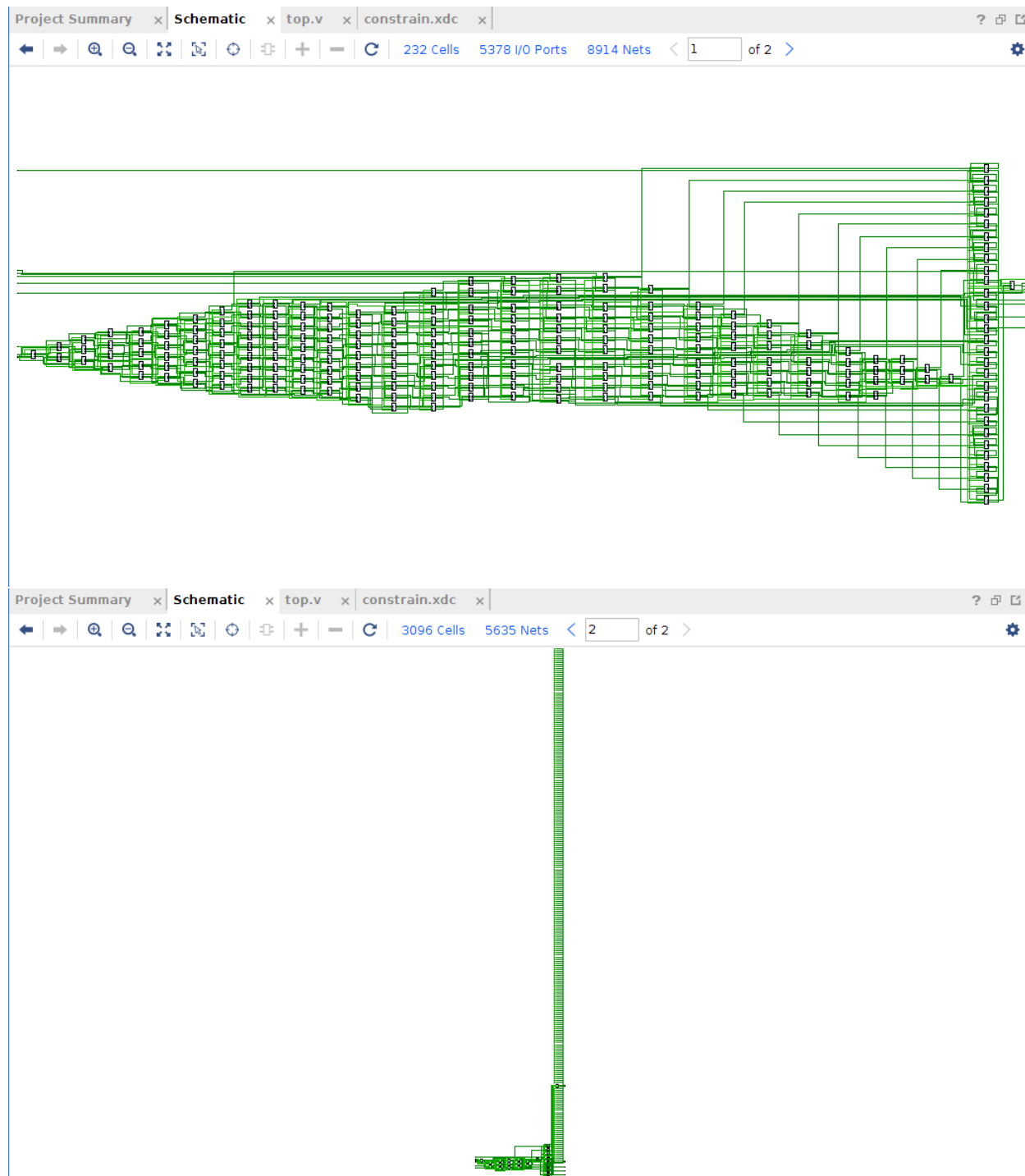
## 5. Power Report



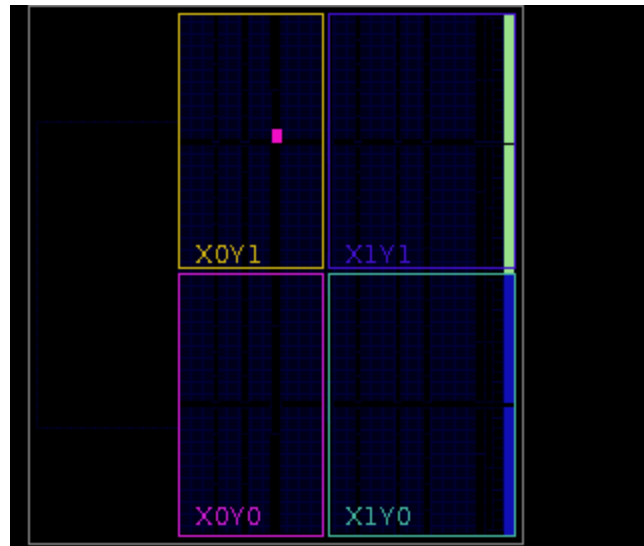
## B. 32\*32 16\*16 Systolic Array

### 1. Schematic and Function Wave form





## 2. Synthesis schematic



### 3. Resources Utilization

Tcl ConsoleMessagesLogReportsDesign RunsUtilization x?

HierarchyHierarchySummary

▼ Slice Logic

▼ Slice LUTs (78%)

LUT as Logic (78%)

▼ Slice Registers (20%)

Register as Flip I

Memory

DSP

▼ IO and GT Specific

Bonded IOB (>100%)

▼ Clocking

BUFGCTRL (3%)

Specific Feature

Primitives

Black Boxes

Instantiated Netlists

Name

^1

▼ top

genblk2[0].genblk1[0].pe1 (pe\_)

genblk2[0].genblk1[1].pe1 (pe\_6)

genblk2[0].genblk1[2].pe1 (pe\_7)

genblk2[0].genblk1[3].pe1 (pe\_8)

genblk2[0].genblk1[4].pe1 (pe\_9)

genblk2[0].genblk1[5].pe1 (pe\_10)

genblk2[0].genblk1[6].pe1 (pe\_11)

genblk2[0].genblk1[7].pe1 (pe\_12)

genblk2[0].genblk1[8].pe1 (pe\_13)

genblk2[0].genblk1[9].pe1 (pe\_14)

genblk2[0].genblk1[10].pe1 (pe\_0)

genblk2[0].genblk1[11].pe1 (pe\_1)

genblk2[0].genblk1[12].pe1 (pe\_2)

genblk2[0].genblk1[13].pe1 (pe\_3)

genblk2[0].genblk1[14].pe1 (pe\_4)

genblk2[0].genblk1[15].pe1 (pe\_5)

genblk2[1].genblk1[0].pe1 (pe\_111)

genblk2[1].genblk1[1].pe1 (pe\_118)

genblk2[1].genblk1[2].pe1 (pe\_119)

genblk2[1].genblk1[3].pe1 (pe\_120)

genblk2[1].genblk1[4].pe1 (pe\_121)

Slice LUTs ...

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Tcl Console		Messages		Log		Reports		Design Runs		Utilization			
Q		≡		≡		%		Hierarchy				⚙	
Hierarchy		Summary		Name		^ 1		Slice LUTs ...		Slice Registe...		Bonded IOB (54)	
												BUFGCTRL (32)	
▼ Slice Logic		genblk2[4].genblk1[1].pe1 (pe_166)		44		24		0		0			
▼ Slice LUTs (78%)		genblk2[4].genblk1[2].pe1 (pe_167)		44		24		0		0			
LUT as Logic (78)		genblk2[4].genblk1[3].pe1 (pe_168)		44		24		0		0			
▼ Slice Registers (20%)		genblk2[4].genblk1[4].pe1 (pe_169)		44		24		0		0			
Register as Flip I		genblk2[4].genblk1[5].pe1 (pe_170)		44		24		0		0			
Memory		genblk2[4].genblk1[6].pe1 (pe_171)		44		24		0		0			
DSP		genblk2[4].genblk1[7].pe1 (pe_172)		44		24		0		0			
▼ IO and GT Specific		genblk2[4].genblk1[8].pe1 (pe_173)		44		24		0		0			
Bonded IOB (>100%)		genblk2[4].genblk1[9].pe1 (pe_174)		44		24		0		0			
▼ Clocking		genblk2[4].genblk1[10].pe1 (pe_160)		44		24		0		0			
BUFGCTRL (3%)		genblk2[4].genblk1[11].pe1 (pe_161)		44		24		0		0			
Specific Feature		genblk2[4].genblk1[12].pe1 (pe_162)		44		24		0		0			
Primitives		genblk2[4].genblk1[13].pe1 (pe_163)		44		24		0		0			
Black Boxes		genblk2[4].genblk1[14].pe1 (pe_164)		44		24		0		0			
Instantiated Netlists		genblk2[4].genblk1[15].pe1 (pe_165)		27		16		0		0			
		genblk2[5].genblk1[0].pe1 (pe_175)		61		24		0		0			
		genblk2[5].genblk1[1].pe1 (pe_182)		44		24		0		0			
		genblk2[5].genblk1[2].pe1 (pe_183)		44		24		0		0			
		genblk2[5].genblk1[3].pe1 (pe_184)		44		24		0		0			
		genblk2[5].genblk1[4].pe1 (pe_185)		44		24		0		0			
		genblk2[5].genblk1[2].pe1 (pe_183)		44		24		0		0			
		genblk2[5].genblk1[3].pe1 (pe_184)		44		24		0		0			
		genblk2[5].genblk1[4].pe1 (pe_185)		44		24		0		0			

Tcl Console Messages Log Reports Design Runs Utilization x						
Hierarchy						
	Name	^ 1	Slice LUTs ...	Slice Registe...	Bonded IOB (54)	BUFGCTRL (32)
Hierarchy						
Summary						
✓ Slice Logic	genblk2[7].genblk1[4].pe1 (pe_217)		44	24	0	0
✓ Slice LUTs (78%)	genblk2[7].genblk1[5].pe1 (pe_218)		44	24	0	0
LUT as Logic (78)	genblk2[7].genblk1[6].pe1 (pe_219)		44	24	0	0
✓ Slice Registers (20%)	genblk2[7].genblk1[7].pe1 (pe_220)		44	24	0	0
Register as Flip I	genblk2[7].genblk1[8].pe1 (pe_221)		44	24	0	0
Memory	genblk2[7].genblk1[9].pe1 (pe_222)		44	24	0	0
DSP	genblk2[7].genblk1[10].pe1 (pe_208)		44	24	0	0
✓ IO and GT Specific	genblk2[7].genblk1[11].pe1 (pe_209)		44	24	0	0
Bonded IOB (>100%)	genblk2[7].genblk1[12].pe1 (pe_210)		44	24	0	0
✓ Clocking	genblk2[7].genblk1[13].pe1 (pe_211)		44	24	0	0
BUFGCTRL (3%)	genblk2[7].genblk1[14].pe1 (pe_212)		44	24	0	0
Specific Feature	genblk2[7].genblk1[15].pe1 (pe_213)		27	16	0	0
Primitives	genblk2[8].genblk1[0].pe1 (pe_223)		61	24	0	0
Black Boxes	genblk2[8].genblk1[1].pe1 (pe_230)		44	24	0	0
Instantiated Netlists	genblk2[8].genblk1[2].pe1 (pe_231)		44	24	0	0
	genblk2[8].genblk1[3].pe1 (pe_232)		44	24	0	0
	genblk2[8].genblk1[4].pe1 (pe_233)		44	24	0	0
	genblk2[8].genblk1[5].pe1 (pe_234)		44	24	0	0
	genblk2[8].genblk1[6].pe1 (pe_235)		44	24	0	0
	genblk2[8].genblk1[7].pe1 (pe_236)		44	24	0	0
	genblk2[8].genblk1[8].pe1 (pe_237)		44	24	0	0
	genblk2[8].genblk1[9].pe1 (pe_238)		44	24	0	0
	genblk2[8].genblk1[10].pe1 (pe_224)		44	24	0	0

#### 4. Timing Report

Tcl ConsoleMessagesLogReportsDesign RunsTiming xUtilization

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Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (2305)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

> Unconstrained Paths

Setup

Worst Negative Slack (WNS): 0.397 ns

Total Negative Slack (TNS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 5632

Hold

Worst Hold Slack (WHS): 0.115 ns

Total Hold Slack (THS): 0.000 ns

Number of Failing Endpoints: 0

Total Number of Endpoints: 5632

Pulse Width

Worst Pulse Width Slack (WPWS):

Total Pulse Width Negative Slack (TPWS):

Number of Failing Endpoints:

Total Number of Endpoints:

All user specified timing constraints are met.

#### 5. Power Report

