|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | M1M2 | M3 | M4 | M5 | M6 |
| SHT\_EN |  |  | SHT | SHT |  |
| INTR | INT(M1) |  |  |  |  |
| PC\_INC | M2 | P\_IRET+JMPR | SET+JMPI  +( LAD+STO) | (AND+ADD+SUB+OR+XOR)I |  |
| LDPC | INT(M2) | P\_IRET+JMPR | JMPI |  |  |
| PC\_BUS | #INT(M1) | SET+JMPI+ (LAD+STO) | (AND+ADD+SUB+OR+XOR)I |  |  |
| MEM\_OE | M2 |  | SET+JMPI +( LAD+STO+POP) | LAD +  (AND+ADD+SUB+OR+XOR)I |  |
| RAM\_WE |  |  | PUSH | STO |  |
| RA\_BUS |  | SHT+OUT+SOP+  (AND+ADD+SUB++OR+XOR) | PUSH | STO |  |
| RB\_BUS |  | MOV+ JMPR +  (PUSH+POP) | (AND+ADD+SUB+OR+XOR)R |  |  |
| ALU\_BUS |  |  | SOP | SHT+ (AND+ADD+SUB+OR+XOR)R | (AND+ADD+SUB+OR+XOR)I |
| LDAR | M1 | SET+JMPI+  (LAD+STO+PUSH+POP) | (LAD+STO)+ (AND+ADD+SUB+OR+XOR)I |  |  |
| LDD |  | SHT+ SOP+  (AND+ADD+SUB+OR+XOR) | SHT+ (AND+ADD+SUB+OR+XOR)R | (AND+ADD+SUB+OR+XOR)I |  |
| LDR |  | IN+MOV | SET+SOP+POP | LAD+ SHT+  (AND+ADD+SUB+OR+XOR)R | (AND+ADD+SUB+OR+XOR)I |
| IRET |  | RET |  |  |  |
| IO\_W |  | OUT |  |  |  |
| IO\_R |  | IN |  |  |  |
| LDIR | #INT(M2) |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| 1111 | OR 3/ORI 4 | 1011 | XOR 3/XORI 4 |
| 1110 | AND 3/ANDI 4 | 1010 | SHT 3 |
| 1101 | ADD 3/ADDI 4 | 1001 | STO 3/PUSH 2 |
| 1100 | SUB 3/SUBI 4 | 1000 | LAD 3/POP 2 |
|  |  |  |  |
| 0011 | SET 2 | 0111 | IRET 1 |
| 0010 | SOP 2 | 0110 | MOV 1 |
| 0001 | JMPI 2/JMPR 1 | 0101 | OUT 1 |
| 0000 | NOP\_HLT 0 | 0100 | IN 1 |