Shengzhen RERVISION Technology GO., LTD

A33 Core Board Schematic V1.0

INDEX

P01: INDEX

P02: BLOCK DIAGRAM

P03: POWER TREE

P04: GPIO ASSIGNMENT

P05: DRAM DDR3 8bitX2_16bitx1

P06: CPU

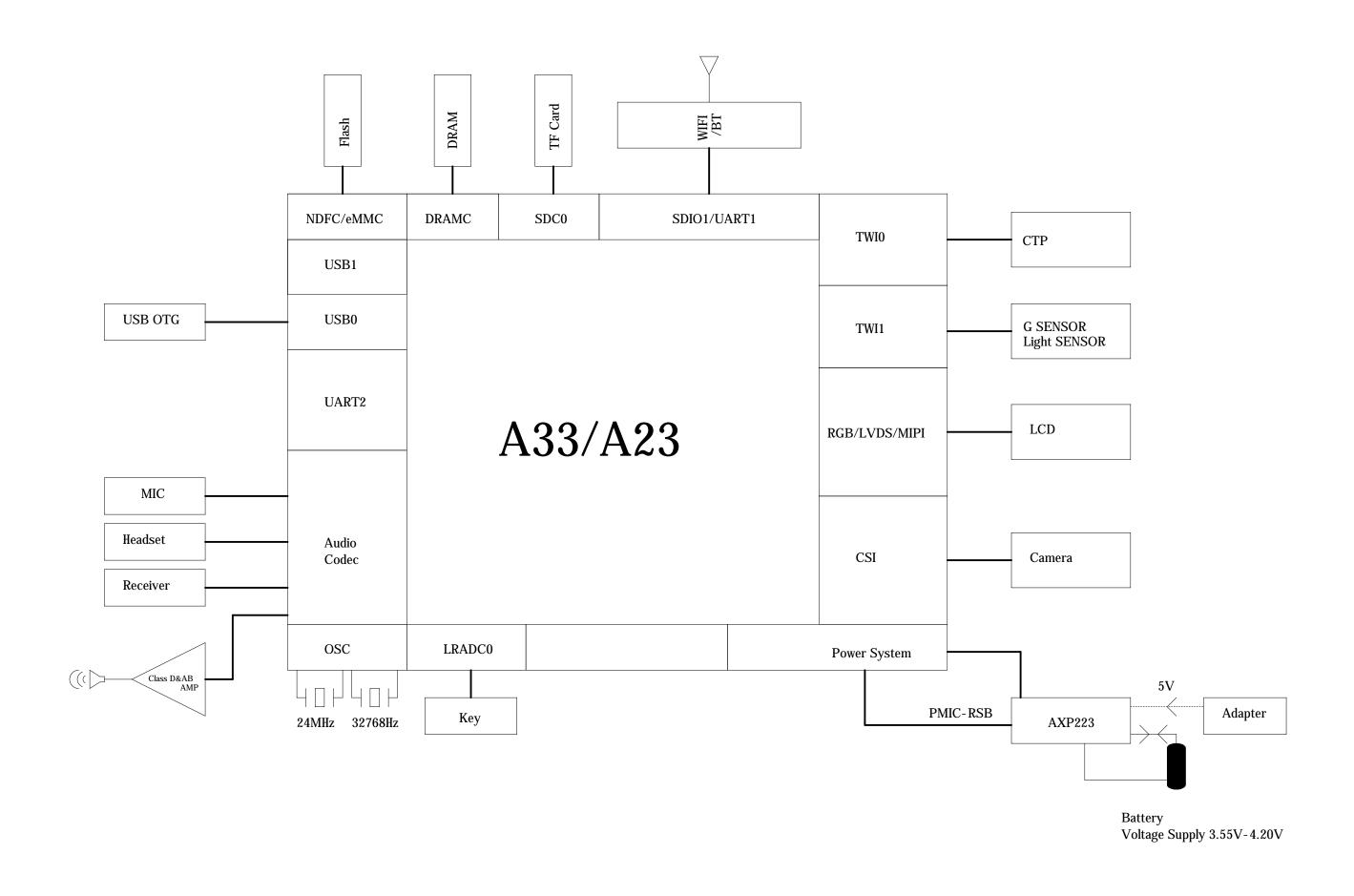
P07: POWER

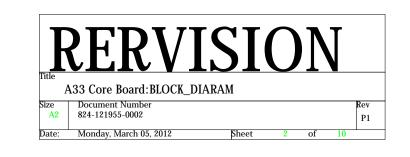
P08: NAND

P09: AUDIO(DIRECT)

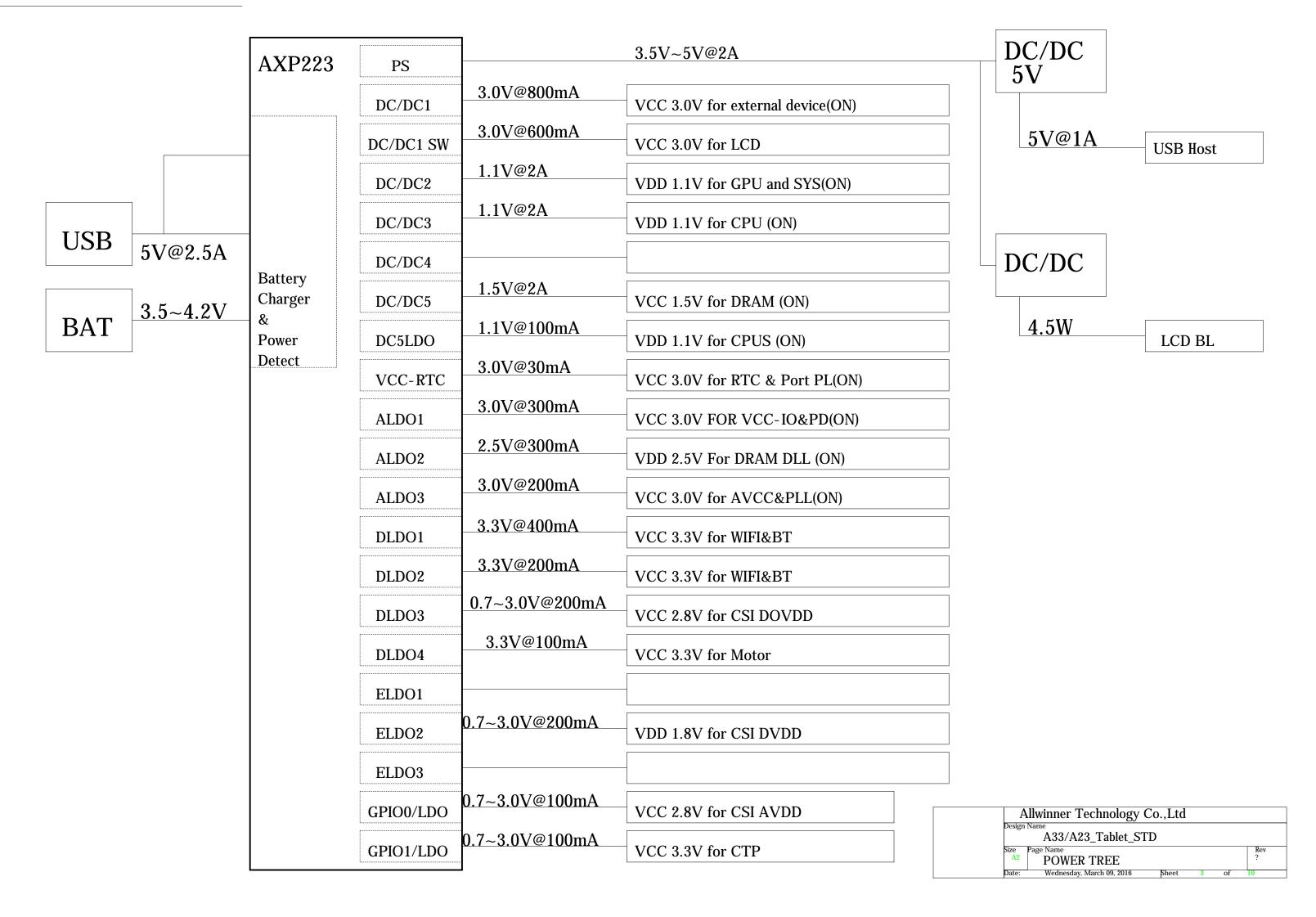
P10: CONNECT

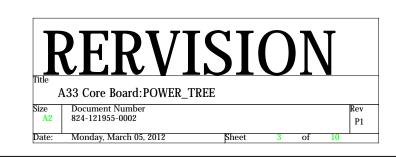
BLOCK DIAGRAM





POWER TREE





GPIO ASSIGNMENT

PIN	Name	Function
PB0	AP-UART2-TX	
PB1	AP-UART2-RX	
PB2	AP-UART2-RTS	MODEM
PB3	AP-UART2-CTS	
PB4	T-CARD-DET	T CARD
PB5	TP-INT	TP
PB6	GS-INT	GSENSOR
PB7	LS-INT	ALS

PIN	Name	Function
PH0	LCD-PWM	LCM
PH1	TP-RST	
PH2	TP-SCK	TP
РН3	TP-SDA	
PH4	SENSOR-SCK	CENCOD
PH5	SENSOR-SDA	SENSOR
РН6	LCD-BL-EN	LCM
PH7	LCD-RST	LCWI
РН8	USB-ID	USB
РН9	PA-SHDN	AUDIO PA

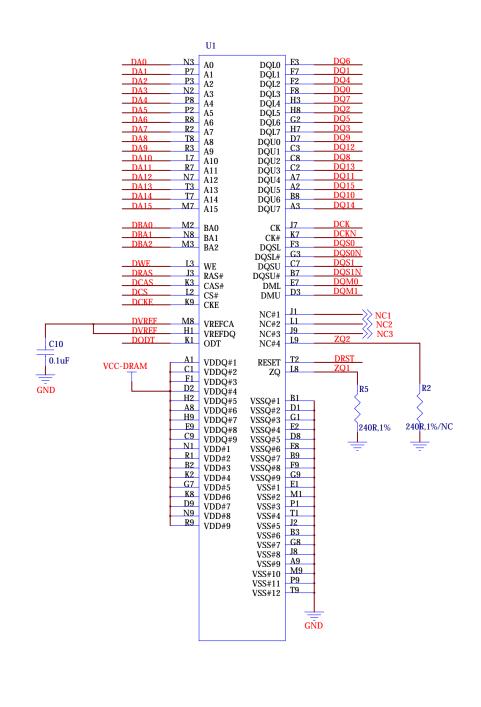
PIN	Name	Function
PL0	PMIC-SCK	PMIC
PL1	PMIC-SDA	FWIIC
PL2	BB-WAKE-AP	
PL3	BB-PWREN	MODEM
PL4	BB-PWR-BAT	MODEM
PL5	BB-RST	
PL6	WL-PMU-EN	
PL7	WL-WAKE-AP	
PL8	BT-RST-N	WLAN
PL9	BT-WAKE-AP	BT
PL10	AP-WAKE-BT	
PL11	WL-BT-ENABLE	

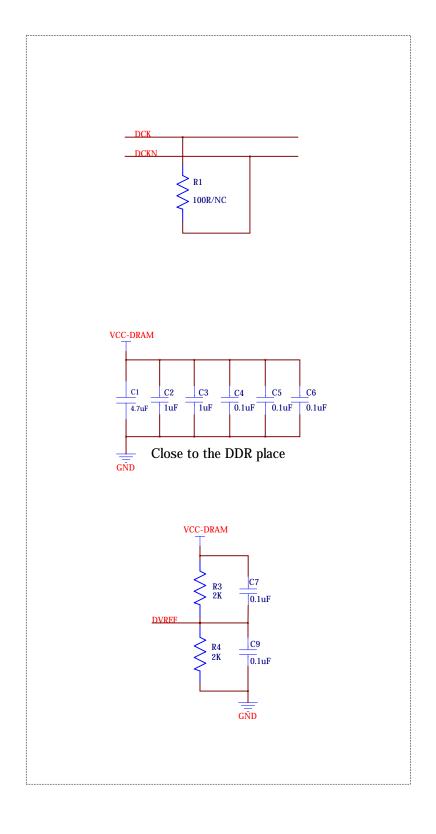
PIN	Name	Function
PG0	WL-SDIO-CLK	
PG1	WL-SDIO-CMD	
PG2	WL-SDIO-D0	
PG3	WL-SDIO-D1	WLAN
PG4	WL-SDIO-D2	
PG5	WL-SDIO-D3	
PG6	AP-UART1-TX	
PG7	AP-UART1-RX	
PG8	AP-UART1-RTS	BT
PG9	AP-UART1-CTS	
PG10	AP-WAKE-BB	
PG11		
PG12		
PG13		



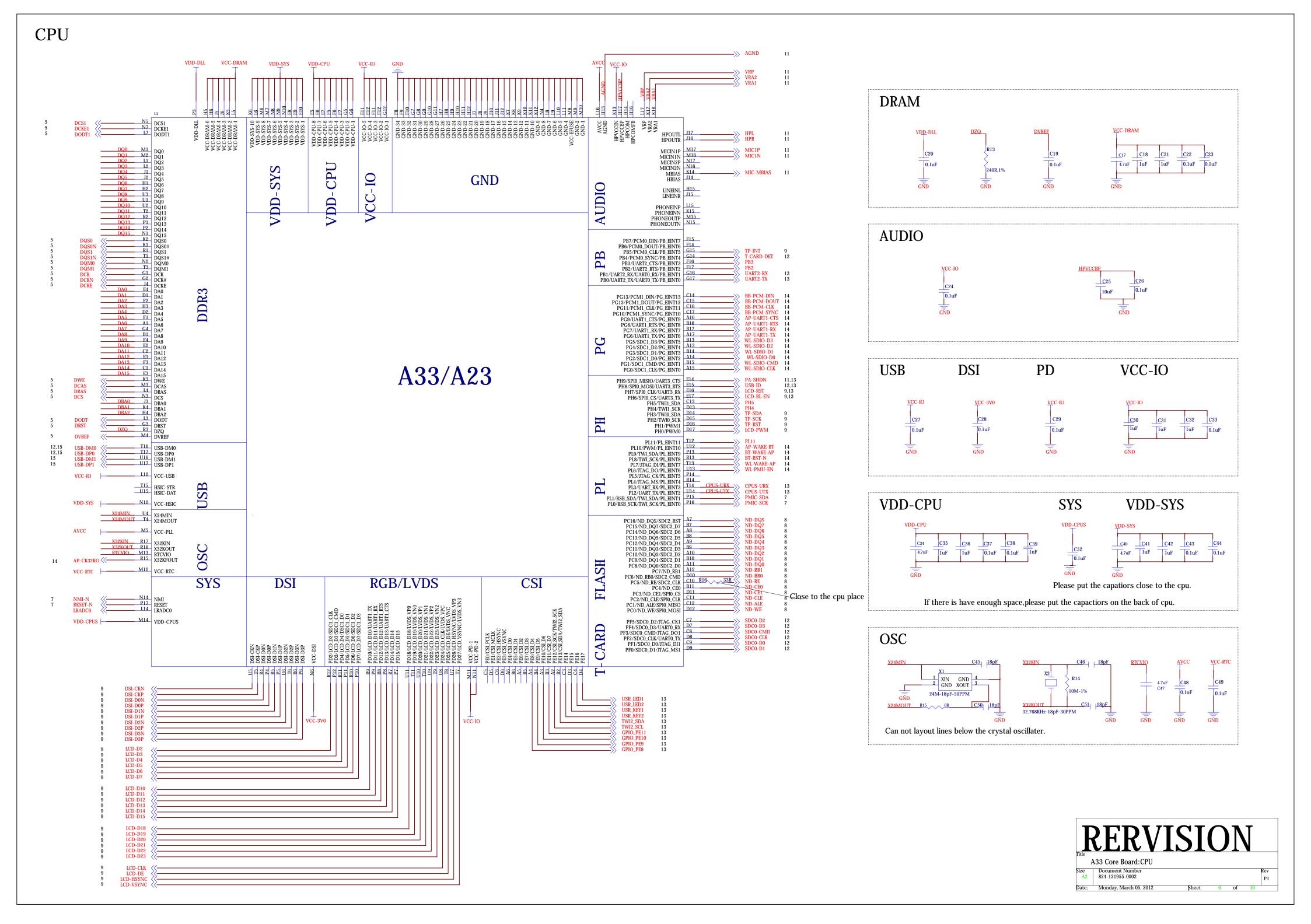
Date: Monday, March 05, 2012

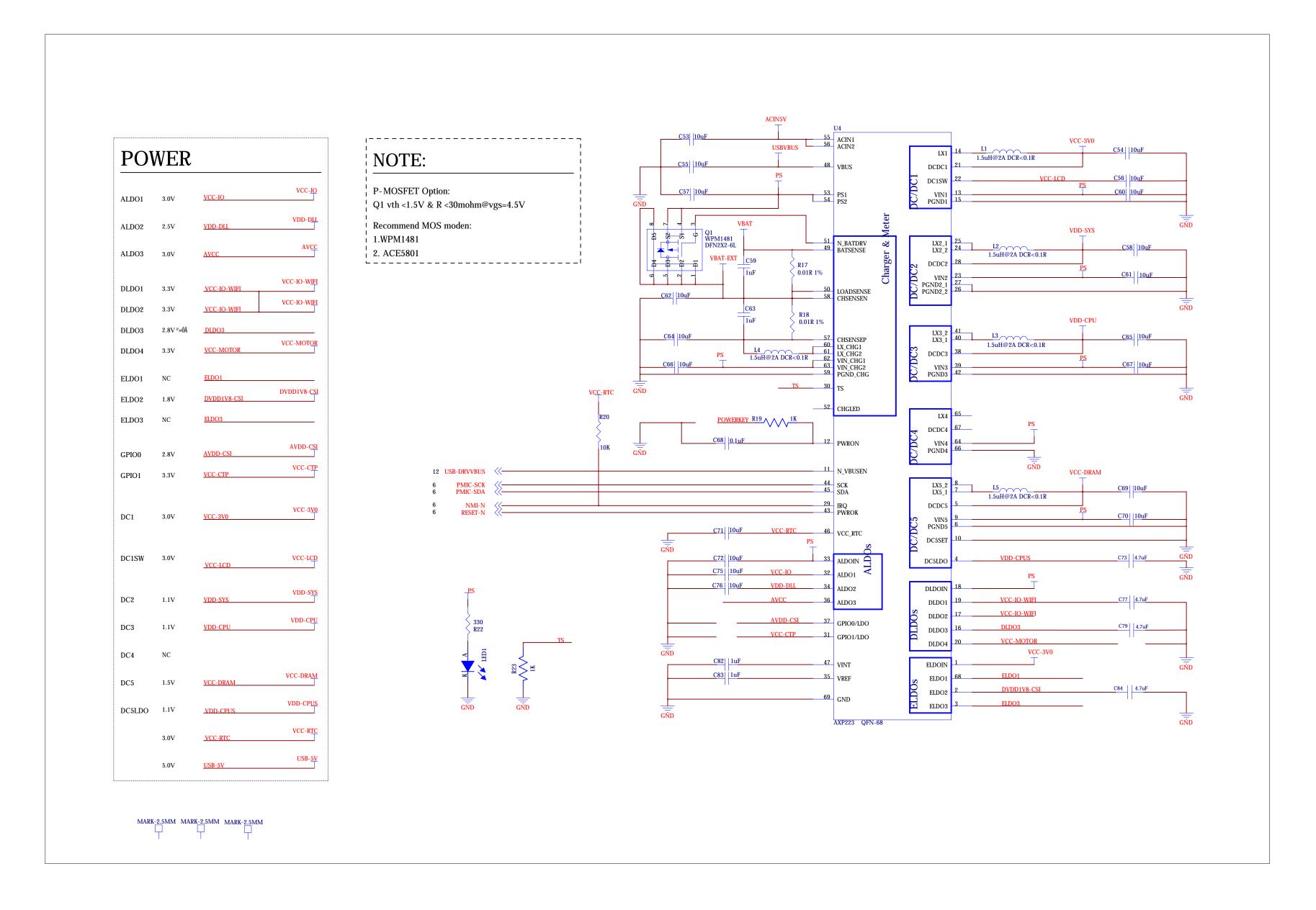
DRAM_DDR3_8BIT*2_16BIT*1



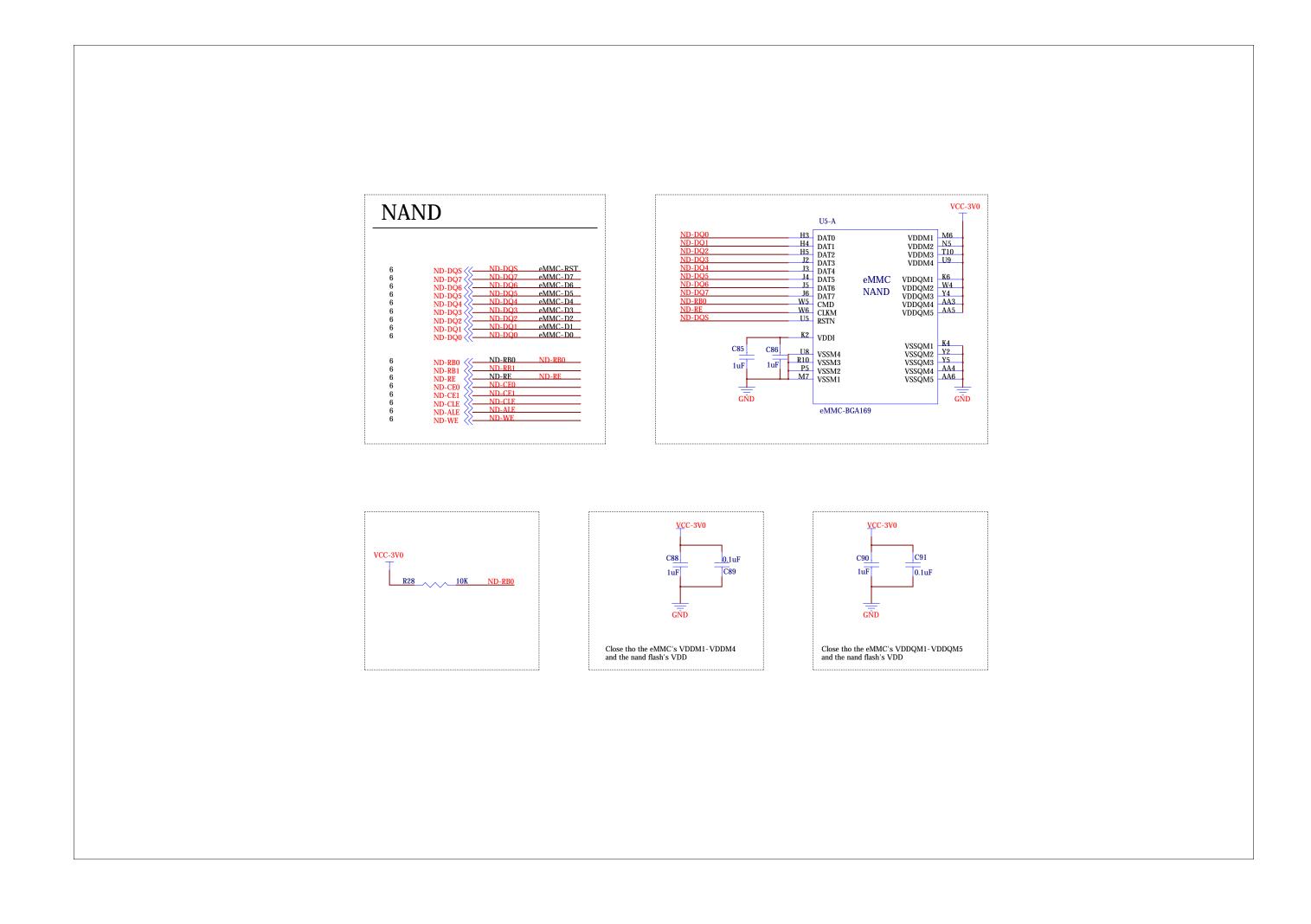


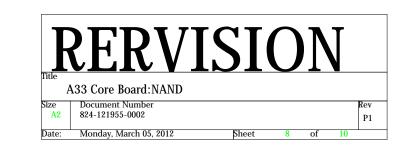
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Title	A33 Core Board:DRAM_DD	DR3 SRIT*9 16RIT	'*1
1	100 COIC DOMA.DIM MI_DD	'NO_ODII ≈_IODII	-
Size A2	Document Number 824-121955-0002	7K3_0DII	I











AUDIO(DIRECT)

