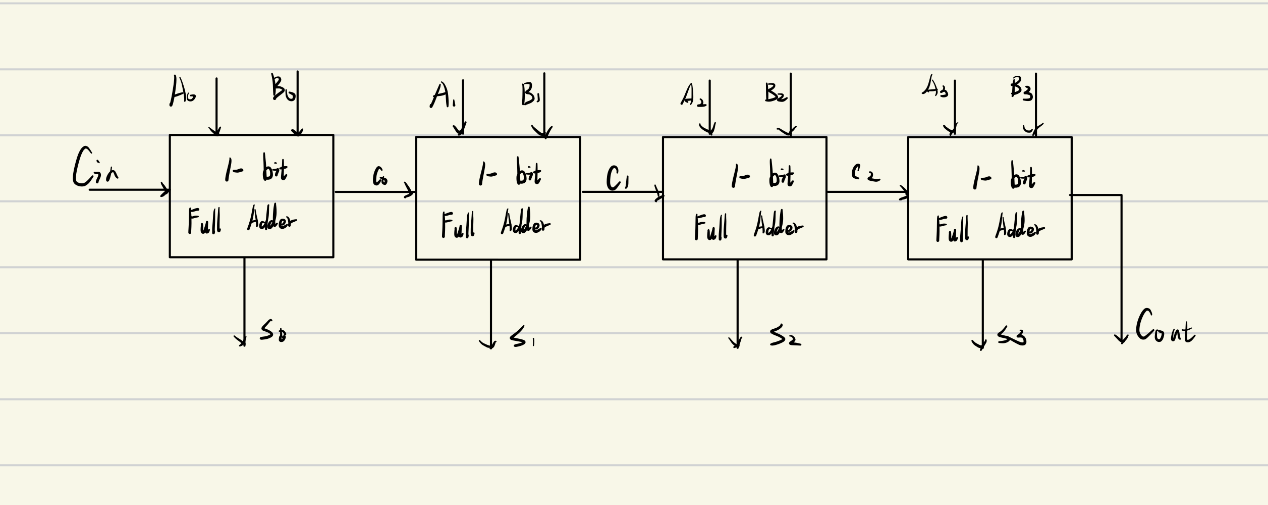
**电路结构：**



**VHDL代码：**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

Use IEEE.Std\_Logic\_Unsigned.All;

entity four\_adder is

Port ( A :in std\_logic\_vector(3 downto 0);

B :in std\_logic\_vector(3 downto 0);

Cin : in STD\_LOGIC;

S :out std\_logic\_vector(3 downto 0);

Cout : out STD\_LOGIC);

end four\_adder;

architecture Behavioral of four\_adder is

SIGNAL c0,c1,c2:std\_logic;

begin

S(0) <= A(0) xor B(0) xor Cin;

c0 <= (A(0) and B(0)) or (A(0) and Cin) or (B(0) and Cin);

S(1) <= A(1) xor B(1) xor c0;

c1 <= (A(1) and B(1)) or (A(1) and c0) or (B(1) and c0);

S(2) <= A(2) xor B(2) xor c1;

c2 <= (A(2) and B(2)) or (A(2) and c1) or (B(2) and c1);

S(3) <= A(3) xor B(3) xor c2;

Cout <= (A(3) and B(3)) or (A(3) and c2) or (B(3) and c2);

end Behavioral;

**testbench代码：**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity tb\_four\_adder is

end tb\_four\_adder;

architecture Behavioral of tb\_four\_adder is

component four\_adder

port(A,B: in std\_logic\_vector;

Cin: in std\_logic;

S: out std\_logic\_vector;

Cout: out std\_logic

);

end component;

signal A: std\_logic\_vector (3 downto 0);

signal B: std\_logic\_vector (3 downto 0);

signal Cin: std\_logic:='0';

signal S: std\_logic\_vector (3 downto 0);

signal Cout: std\_logic:='0';

constant period : time := 20ns;

begin

uut: four\_adder port map(

A => A,

B => B,

Cin => Cin,

S => S,

Cout => Cout

);

A0\_process:process

begin

A(0) <= '0';

wait for period/2;

A(0) <= '1';

wait for period/2;

end process;

B0\_process:process

begin

B(0) <= '0';

wait for period;

B(0) <= '1';

wait for period;

end process;

A1\_process:process

begin

A(1) <= '0';

wait for period\*2;

A(1) <= '1';

wait for period\*2;

end process;

B1\_process:process

begin

B(1) <= '0';

wait for period\*4;

B(1) <= '1';

wait for period\*4;

end process;

A2\_process:process

begin

A(2) <= '0';

wait for period\*8;

A(2) <= '1';

wait for period\*8;

end process;

B2\_process:process

begin

B(2) <= '0';

wait for period\*16;

B(2) <= '1';

wait for period\*16;

end process;

A3\_process:process

begin

A(3) <= '0';

wait for period\*32;

A(3) <= '1';

wait for period\*32;

end process;

B3\_process:process

begin

B(3) <= '0';

wait for period\*64;

B(3) <= '1';

wait for period\*64;

end process;

Cin\_process:process

begin

Cin <= '0';

wait for period\*128;

Cin <= '1';

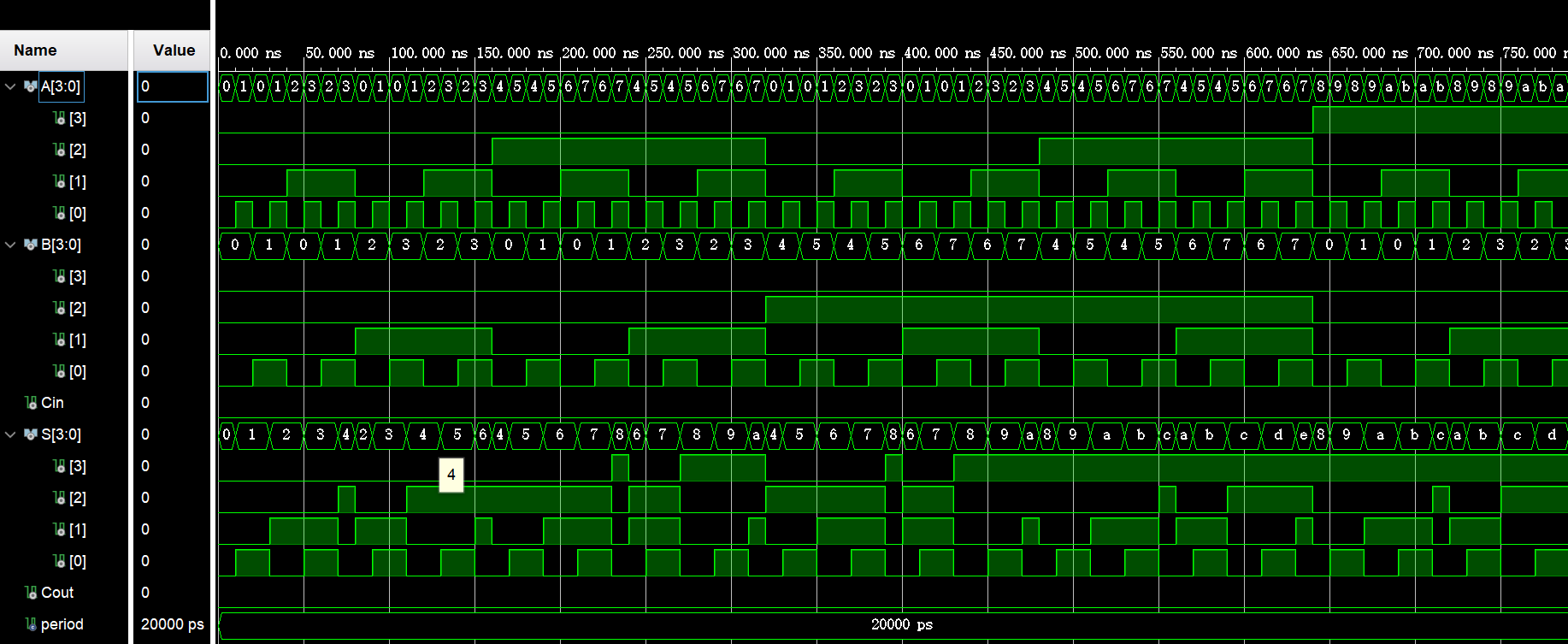
wait for period\*128;

end process;

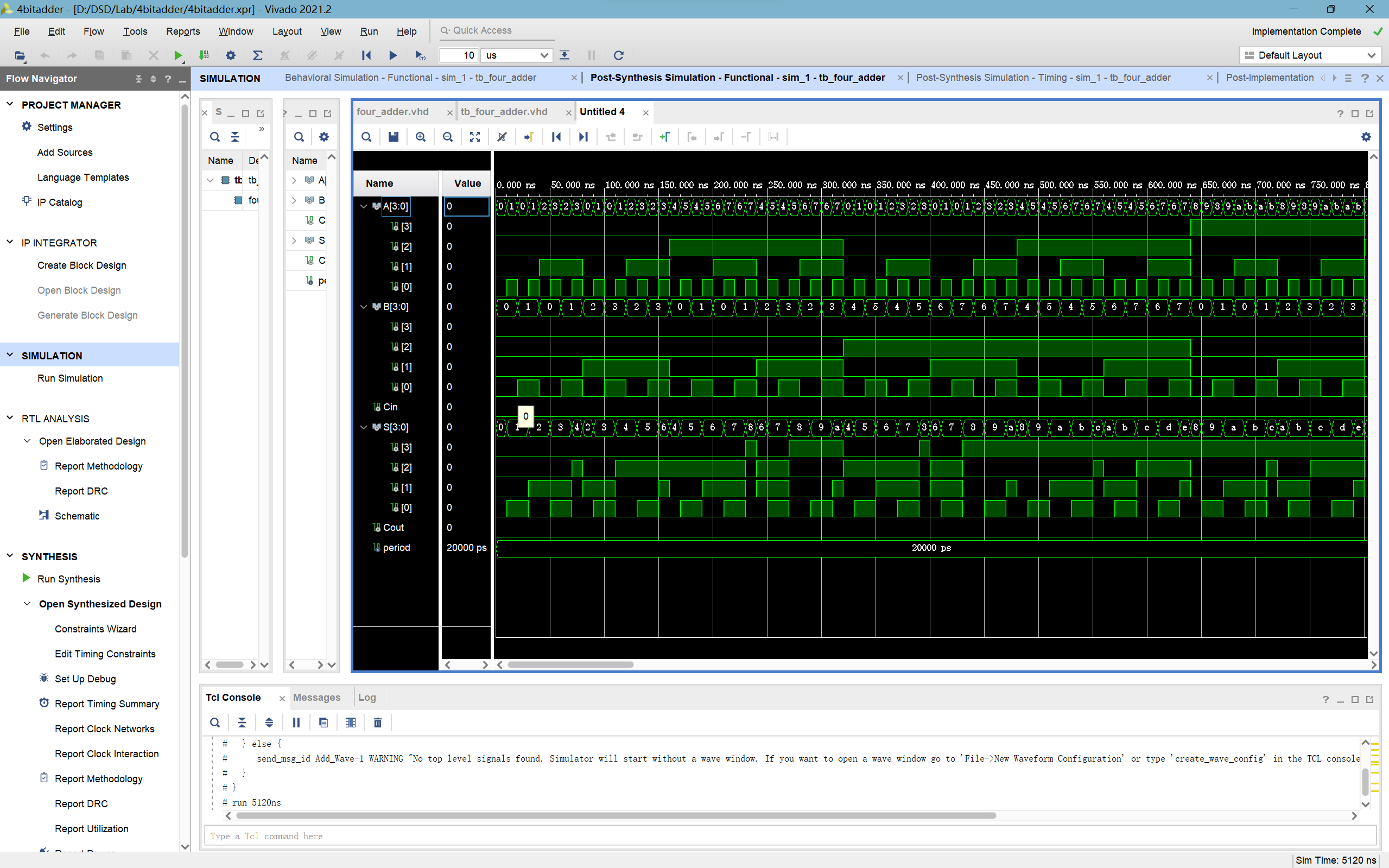
end Behavioral;

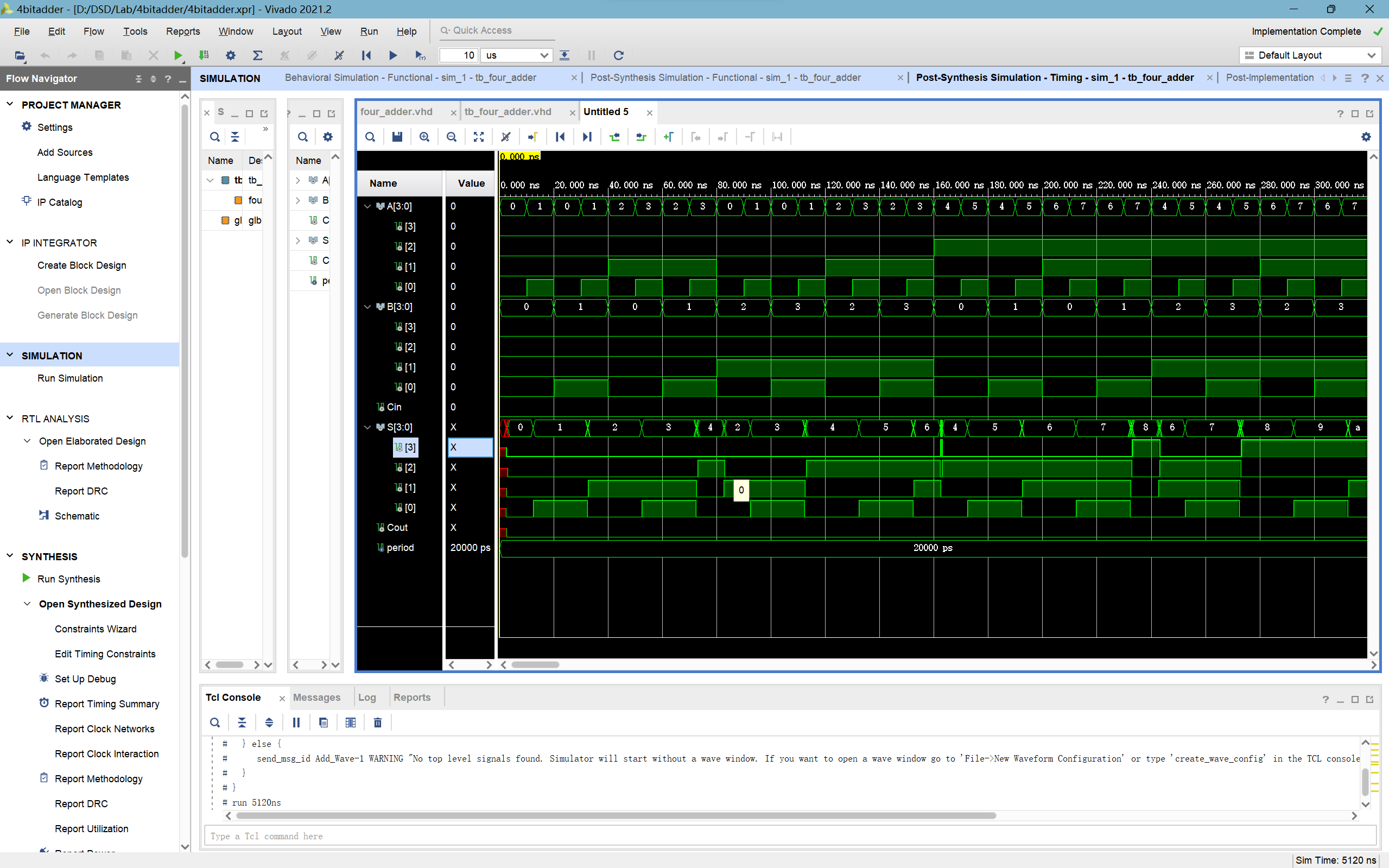
**仿真结果：**

1. 行为仿真：



1. 综合仿真：





1. 布线仿真：

