

Universidad del Valle de Guatemala

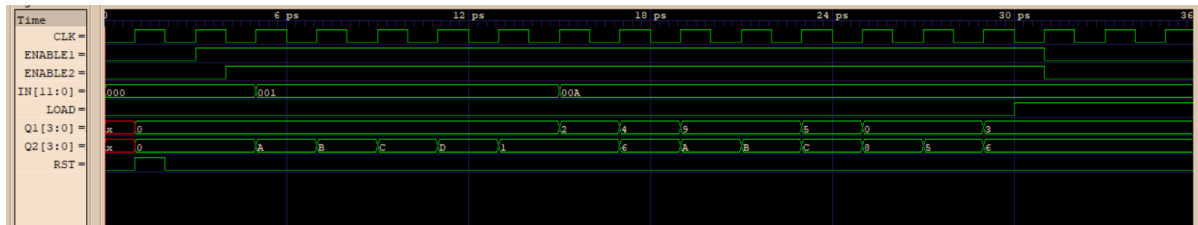
Digital 1

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Laboratorio #10

Link Repositorio: <https://github.com/gar19085/Digital-1-Garcia19085.git>

Ejercicio #01:

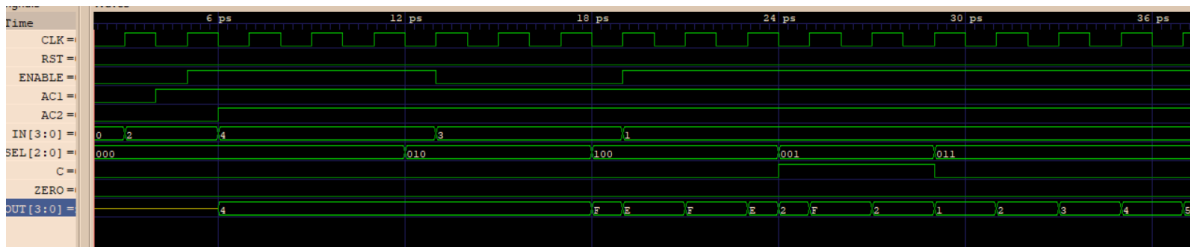


```
iverilog -o PRF_tb.out -D VCD_OUTPUT=PRF_tb C:/Users/rodri/.apio/packages/toolchain-yosys/share/yosys/ice40/c
vvp PRF_tb.out
WARNING: PRF.v:67: $readmemh(memory.list): Not enough words in the file for the requested range [0:4095].

EJERCICIO 01
CLK| RST | ENABLE1 | ENABLE2 | LOAD | IN | Q1 | Q2 | Q1Hex | Q2Hex |
VCD info: dumpfile PRF_tb.vcd opened for output.
0 | 0 | 0 | 0 | 0 | 000000000000 | xxxx | xxxx | x | x |
1 | 1 | 0 | 0 | 0 | 000000000000 | 0000 | 0000 | 0 | 0 |
0 | 0 | 0 | 0 | 0 | 000000000000 | 0000 | 0000 | 0 | 0 |
1 | 0 | 1 | 0 | 0 | 000000000000 | 0000 | 0000 | 0 | 0 |
0 | 0 | 1 | 1 | 0 | 000000000000 | 0000 | 0000 | 0 | 0 |
1 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1010 | 0 | a |
0 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1010 | 0 | a |
1 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1011 | 0 | b |
0 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1011 | 0 | b |
1 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1100 | 0 | c |
0 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1100 | 0 | c |
1 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1101 | 0 | d |
0 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 1101 | 0 | d |
1 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 0001 | 0 | 1 |
0 | 0 | 1 | 1 | 0 | 000000000001 | 0000 | 0001 | 0 | 1 |
1 | 0 | 1 | 1 | 0 | 000000001010 | 0010 | 0001 | 2 | 1 |
0 | 0 | 1 | 1 | 0 | 000000001010 | 0010 | 0001 | 2 | 1 |
1 | 0 | 1 | 1 | 0 | 000000001010 | 0100 | 0110 | 4 | 6 |
0 | 0 | 1 | 1 | 0 | 000000001010 | 0100 | 0110 | 4 | 6 |
1 | 0 | 1 | 1 | 0 | 000000001010 | 1001 | 1010 | 9 | a |
0 | 0 | 1 | 1 | 0 | 000000001010 | 1001 | 1010 | 9 | a |
1 | 0 | 1 | 1 | 0 | 000000001010 | 1001 | 1011 | 9 | b |
0 | 0 | 1 | 1 | 0 | 000000001010 | 1001 | 1011 | 9 | b |
1 | 0 | 1 | 1 | 0 | 000000001010 | 0101 | 1100 | 5 | c |
0 | 0 | 1 | 1 | 0 | 000000001010 | 0101 | 1100 | 5 | c |
1 | 0 | 1 | 1 | 0 | 000000001010 | 0000 | 1000 | 0 | 8 |
0 | 0 | 1 | 1 | 0 | 000000001010 | 0000 | 1000 | 0 | 8 |
1 | 0 | 1 | 1 | 0 | 000000001010 | 0000 | 0101 | 0 | 5 |
0 | 0 | 1 | 1 | 0 | 000000001010 | 0000 | 0101 | 0 | 5 |
1 | 0 | 1 | 1 | 0 | 000000001010 | 0011 | 0110 | 3 | 6 |
0 | 0 | 1 | 1 | 1 | 000000001010 | 0011 | 0110 | 3 | 6 |
1 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0011 | 0110 | 3 | 6 |
0 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0011 | 0110 | 3 | 6 |
1 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0011 | 0110 | 3 | 6 |
0 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0011 | 0110 | 3 | 6 |
1 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0011 | 0110 | 3 | 6 |
0 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0011 | 0110 | 3 | 6 |
1 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0101 | 1100 | 5 | c |
0 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0101 | 1100 | 5 | c |
1 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0101 | 1100 | 5 | c |
0 | 0 | 0 | 0 | 0 | 1 | 000000001010 | 0101 | 1100 | 5 | c |
0 | 0 | 1 | 1 | 1 | 1 | 000000001010 | 0101 | 1100 | 5 | c |
gtkwave PRF_tb.vcd PRF_tb.gtkw
```

El ejercicio 1 consistió en implementar un modulo principal en el cual se conectan los siguientes módulos: un Fetch que es un Flip Flop D, de 8 bits, un contador, y una memoria ROM de 4096x8.

Ejercicio #02:



```

vvp ACU_TB.OUT

EJERCICIO 02
CLK| RST | ENABLE | IN | AC1 | AC2 | SEL | C | ZERO | OUT|
VCD info: dumpfile ACU_TB.vcd opened for output.
0 | 0 | 0 | 0000 | 0 | 0 | 000 | 0 | 0 | ZZZZ |
1 | 1 | 0 | 0000 | 0 | 0 | 000 | 0 | 0 | ZZZZ |
0 | 0 | 0 | 0000 | 0 | 0 | 000 | 0 | 0 | ZZZZ |
1 | 0 | 0 | 0010 | 0 | 0 | 000 | 0 | 0 | ZZZZ |
0 | 0 | 0 | 0010 | 1 | 0 | 000 | 0 | 0 | ZZZZ |
1 | 0 | 1 | 0010 | 1 | 0 | 000 | 0 | 0 | ZZZZ |
0 | 0 | 1 | 0100 | 1 | 1 | 000 | 0 | 0 | 0100 |
1 | 0 | 1 | 0100 | 1 | 1 | 000 | 0 | 0 | 0100 |
0 | 0 | 1 | 0100 | 1 | 1 | 000 | 0 | 0 | 0100 |
1 | 0 | 1 | 0100 | 1 | 1 | 000 | 0 | 0 | 0100 |
0 | 0 | 1 | 0100 | 1 | 1 | 000 | 0 | 0 | 0100 |
1 | 0 | 1 | 0100 | 1 | 1 | 000 | 0 | 0 | 0100 |
0 | 0 | 1 | 0100 | 1 | 1 | 010 | 0 | 0 | 0100 |
1 | 0 | 0 | 0011 | 1 | 1 | 010 | 0 | 0 | 0100 |
0 | 0 | 0 | 0011 | 1 | 1 | 010 | 0 | 0 | 0100 |
1 | 0 | 0 | 0011 | 1 | 1 | 010 | 0 | 0 | 0100 |
0 | 0 | 0 | 0011 | 1 | 1 | 010 | 0 | 0 | 0100 |
1 | 0 | 0 | 0011 | 1 | 1 | 010 | 0 | 0 | 0100 |
0 | 0 | 0 | 0011 | 1 | 1 | 100 | 0 | 0 | 1111 |
1 | 0 | 1 | 0001 | 1 | 1 | 100 | 0 | 0 | 1110 |
0 | 0 | 1 | 0001 | 1 | 1 | 100 | 0 | 0 | 1110 |
1 | 0 | 1 | 0001 | 1 | 1 | 100 | 0 | 0 | 1111 |
0 | 0 | 1 | 0001 | 1 | 1 | 100 | 0 | 0 | 1111 |
1 | 0 | 1 | 0001 | 1 | 1 | 100 | 0 | 0 | 1110 |
0 | 0 | 1 | 0001 | 1 | 1 | 001 | 1 | 0 | 0010 |
1 | 0 | 1 | 0001 | 1 | 1 | 001 | 1 | 0 | 1111 |
0 | 0 | 1 | 0001 | 1 | 1 | 001 | 1 | 0 | 1111 |
1 | 0 | 1 | 0001 | 1 | 1 | 001 | 1 | 0 | 0010 |
0 | 0 | 1 | 0001 | 1 | 1 | 001 | 1 | 0 | 0010 |
1 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0001 |
0 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0001 |
1 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0010 |
0 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0010 |
1 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0011 |
0 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0011 |
1 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0100 |
0 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0100 |
1 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0101 |
0 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0101 |
1 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0110 |
0 | 0 | 1 | 0001 | 1 | 1 | 011 | 0 | 0 | 0110 |
gtkwave ACU_TB.vcd ACU_TB.gtkw

```

El ejercicio 2 consistió en implementar un modulo principal en el que se conectan los siguientes módulos: dos Bus Drivers que son buffers triestado, un Acumulador que es un Flip Flop D, de 4 bits, y por ultimo una ALU que realiza las operaciones necesarias para poder realizar las acciones de la tabla que se proporciona.