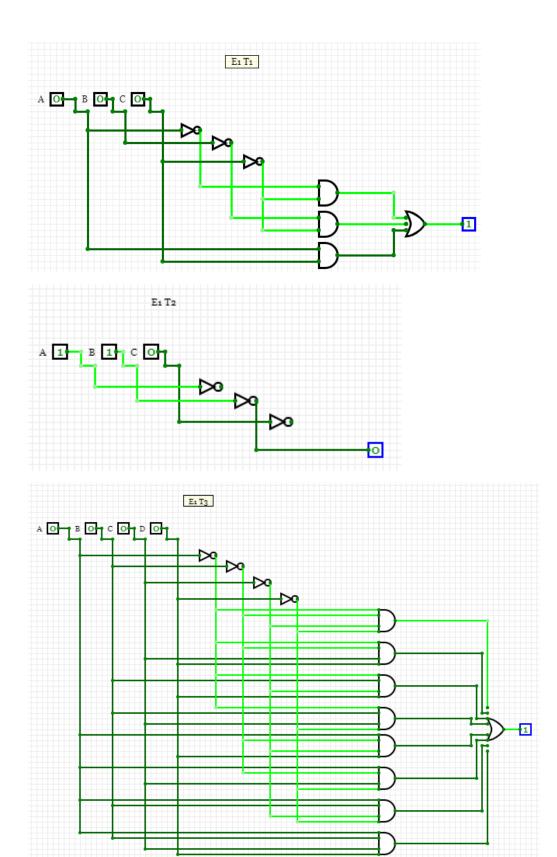
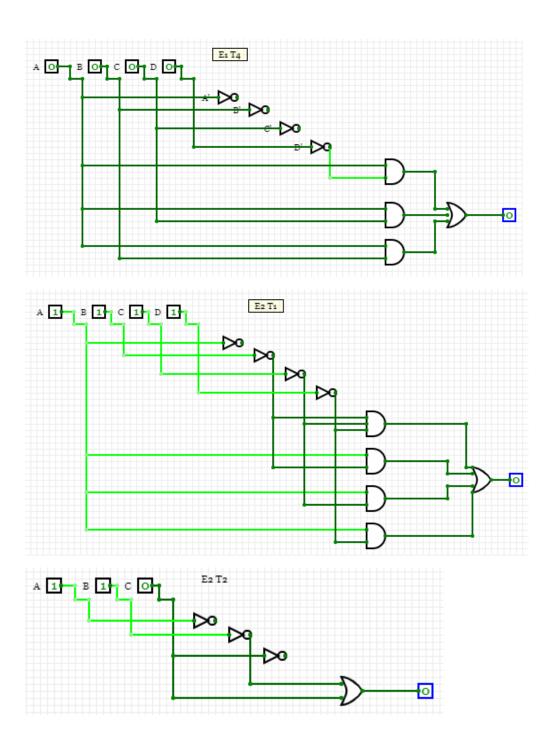


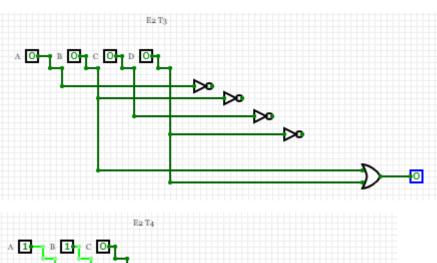
ejeso	010	7		12.	(H),	rd.	10	
1) Y = ABO			+(1	R +0.1	p)		, 3	Y
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	Y		00	01	11	20)	0
0000	1	00	11	0	12	119		
0001	0	01	0	0	(2)1	19		Y H
0010	0	12	0	0	0	9		
0011	0	20	0	101	(A)	(n)	00	(3)
0 100	0						T. D. C.	0
0101	0		A	B	C	D	1	P
0110	0		76	0.	0	0	2	
0111	0		1	70	75	0	9	
1000	1		1	7	0	2	2	
1001	1	r	2	0	2	α	2	
1010	1			00	00	0-0	00	/12 (2)
10'1	1			0		0		00
1100	1							00
1101	1							00
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								10
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				Int.		ta	36	01

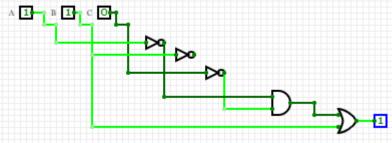
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10	1	1	1		X	0	90	2	0) 1	0
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10	1	1	1		A	B	0	Y			
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1	1	-	-	2	1.0	0	0		0	0	0
1	1	,	1 1	1		0	10		1	0	0
									0		0
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				£ 1), ·	-	A		0	0	1
				PI	0					0	1
				-					10	1	1
										-	









```
______
 module tablal_l(input wire A, B, C, output wire Y);
☐// Elementos
// reg A, B, C;
 wire w1,w2,w3,w4,w5,w6,w7;
 // compuertas
                              //A'
 not Ul (wl, A);
                              //B'
 not U2 (w2, B);
                              //C'
 not U3 (w3, C);
 not U4 (w4, D);
                              //D'
 and al (w5, w1, w3); //A'C'
and a2 (w6, w2, w3); //B'C'
and a3 (w7, A, C); //AC
or ol (Y, w5, w6, w7); //Salida
 endmodule
□// -----
// Ejercicio l Tabla 2/Gate Level Modelling
L// -----
 module tablal 2(input wire A, B, C, output wire Y);
☐// Elementos
L// reg A, B, C;
 wire w2;
 // compuertas
                              //B'=Salida
 not U2 (Y, B);
 endmodule
```

```
// -----
// Ejercicio 1 Tabla 3/Gate Level Modelling
// -----
module tablal_3(input wire A, B, C, D, output wire Y);
// Elementos
// reg A, B, C, D;
wire w1,w2,w3,w4,w5,w6,w7,w8,w9,w10,w11,w12;
// compuertas
                             //A'
not Ul (wl, A);
not U2 (w2, B);
                             //B'
not U3 (w3, C);
                             //C'
not U4 (w4, D);
                            //D'
and al (w5, w1, w2, w3, w4); //A'B'C'D'
and a2 (w6, w1, w2, C, D);
                           //A'B'CD
and a3 (w7, w1, B, w3, D);
                            //ABCD
and a4 (w8, w1, B, C ,w4);
                            //ABCD
and a5 (w9, A, B, w3, w4);
                            //ABCD
                            //ABCD
and a6 (w10, A, B, C, D);
and a7 (w11, A, w2, w3, D); //ABCD and a8 (w12, A, w2, C, w4); //ABCD
                            //ABCD
or ol (Y, w5,w6,w7,w8,w9,w10,w11,w12);
                                          //Salida
endmodule
// Ejercicio l Tabla 4/Gate Level Modelling
// -----
module tablal_4(input wire A, B, C, D, output wire J);
// Elementos
wire j1,j2,j3,j4;
// compuertas
not Ul (jl, D);
                             //D'
                             //AD'
and al (j2, A, j1);
                            //AC
and a2 (j3, A, C);
and a3 (j4, A, B);
                            //AB
or ol (J, j2, j3, j4);
                            //AD'+AC+AB
endmodule
```

```
// Ejercicio 2 Tabla 1/Operadores Logicos
// -----
module tabla2_1(input wire A,B,C,D, output wire Y);
assign Y = (\sim B\&\sim C\&\sim D) \mid (A\&\sim B) \mid (A\&\sim C) \mid (A\&\sim D);
endmodule
// Ejercicio 2 Tabla 2/Operadores Logicos
module tabla2_2(input wire A,B,C, output wire Y);
   assign Y = \sim B \mid C;
endmodule
// -----
// Ejercicio 2 Tabla 3/Operadores Logicos
module tabla2 3(input wire A,B,C,D, output wire Y);
   assign Y = B \mid D;
endmodule
// -----
// Ejercicio 2 Tabla 4/Operadores Logicos
// -----
module tabla2 4(input wire A,B,C, output wire Y);
   assign Y = \sim A\&\sim C \mid B;
endmodule
module testbench();
  reg Al, Bl, Cl,
                      //Entradas Ejercicio 1
     A2, B2, C2,
     A3, B3, C3, D3,
     A4, B4, C4, D4,
     pl, p2, p3, p4,
                     //Entradas Ejercicio 2
     p5, p6, p7,
     p8, p9, p10, p11,
     p12, p13, p14;
  wire Y1, Y2, Y3, Y4, //Salidas Ejercicio 1
      el, e2, e3, e4; //Salidas Ejercicio 2
//-----Modulos Ejercicio l------
  tablal_1 T1_1(A1, B1, C1, Y1);
  tabla1_2 T1_2(A2, B2, C2, Y2);
  tabla1_3 T1_3(A3, B3, C3, D3, Y3);
  tablal_4 Tl_4(A4, B4, C4, D4, Y4);
//-----Modulos Ejercicio 2-----
  tabla2_1 T2_1(p1,p2,p3,p4,e1);
  tabla2_2 T2_2(p5,p6,p7,e2);
  tabla2_3 T2_3(p8,p9,p10,p11,e3);
  tabla2_4 T2_4(p12,p13,p14,e4);
```

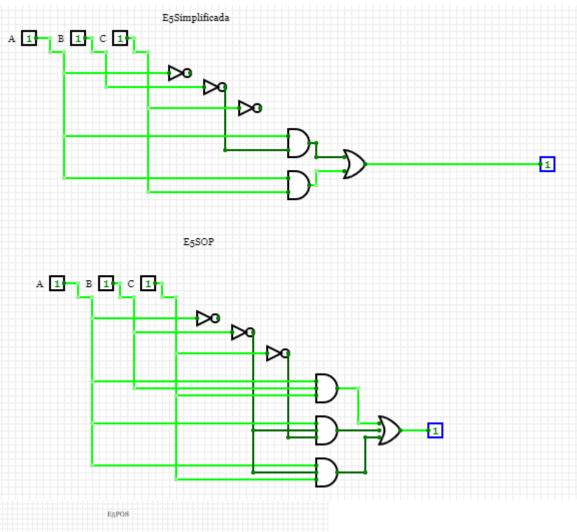
```
//Simulación Ejercicio 1
//----tabla 1-----
 initial begin
   $display("Ejercicio 1 Tabla 1");
   $display("A B C | Y ");
   $display("-----);
   $monitor("%b %b %b | %b", Al, Bl, Cl, Yl);
     A1 = 0; B1 = 0; C1 = 0;
   \#1 A1 = 0; B1 = 0; C1 = 1;
   \#1 A1 = 0; B1 = 1; C1 = 0;
   \#1 A1 = 0; B1 = 1; C1 = 1;
   \#1 A1 = 1; B1 = 0; C1 = 0;
   \#1 A1 = 1; B1 = 0; C1 = 1;
   \#1 A1 = 1; B1 = 1; C1 = 0;
   \#1 A1 = 1; B1 = 1; C1 = 1;
  end
//----tabla 2-----
 initial begin
   #20
   $display("Ejercicio 1 Tabla 2");
   $display("A B C | Y");
   $display("----|--");
   $monitor("%b %b %b | %b", A2, B2, C2, Y2);
     A2 = 0; B2 = 0; C2 = 0;
   \#1 A2 = 0; B2 = 0; C2 = 1;
   \#1 \ A2 = 0; \ B2 = 1; \ C2 = 0;
   \#1 A2 = 0; B2 = 1; C2 = 1;
   \#1 A2 = 1; B2 = 0; C2 = 0;
   \#1 A2 = 1; B2 = 0; C2 = 1;
   \#1 A2 = 1; B2 = 1; C2 = 0;
   \#1 A2 = 1; B2 = 1; C2 = 1;
  end
```

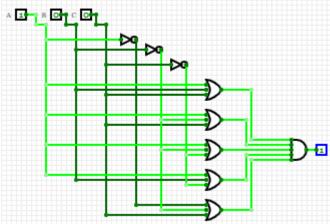
```
//----tabla 3-----
initial begin
    $display("Ejercicio 1 Tabla 3");
    $display("A B C D | Y ");
    $display("-----|---");
    $monitor("%b %b %b %b | %b", A3, B3, C3, D3, Y3);
     A3 = 0; B3 = 0; C3 = 0; D3 = 0;
    #1 A3 = 0; B3 = 0; C3 = 0; D3 = 1;
    #1 A3 = 0; B3 = 0; C3 = 1; D3 = 0;
    #1 A3 = 0; B3 = 0; C3 = 1; D3 = 1;
    #1 A3 = 0; B3 = 1; C3 = 0; D3 = 0;
    #1 A3 = 0; B3 = 1; C3 = 0; D3 = 1;
    #1 A3 = 0; B3 = 1; C3 = 1; D3 = 0;
    #1 A3 = 0; B3 = 1; C3 = 1; D3 = 1;
    #1 A3 = 1; B3 = 0; C3 = 0; D3 = 0;
    #1 A3 = 1; B3 = 0; C3 = 0; D3 = 1;
    #1 A3 = 1; B3 = 0; C3 = 1; D3 = 0;
    #1 A3 = 1; B3 = 0; C3 = 1; D3 = 1;
    #1 A3 = 1; B3 = 1; C3 = 0; D3 = 0;
    #1 A3 = 1; B3 = 1; C3 = 0; D3 = 1;
    #1 A3 = 1; B3 = 1; C3 = 1; D3 = 0;
    #1 A3 = 1; B3 = 1; C3 = 1; D3 = 1;
//----tabla 4-----
initial begin
    #50
    $display("Ejercicio 1 Tabla 4");
    $display("A B C D | Y");
    $display("-----|--");
    $monitor("%b %b %b %b | %b", A4, B4, C4, D4, Y4);
      A4 = 0; B4 = 0; C4 = 0; D4 = 0;
    #1 A4 = 0; B4 = 0; C4 = 0; D4 = 1;
    #1 A4 = 0; B4 = 0; C4 = 1; D4 = 0;
    #1 A4 = 0; B4 = 0; C4 = 1; D4 = 1;
    #1 A4 = 0; B4 = 1; C4 = 0; D4 = 0;
    #1 A4 = 0; B4 = 1; C4 = 0; D4 = 1;
    #1 A4 = 0; B4 = 1; C4 = 1; D4 = 0;
    #1 A4 = 0; B4 = 1; C4 = 1; D4 = 1;
    #1 A4 = 1; B4 = 0; C4 = 0; D4 = 0;
    #1 A4 = 1; B4 = 0; C4 = 0; D4 = 1;
    #1 A4 = 1; B4 = 0; C4 = 1; D4 = 0;
    #1 A4 = 1; B4 = 0; C4 = 1; D4 = 1;
    #1 A4 = 1; B4 = 1; C4 = 0; D4 = 0;
    #1 A4 = 1; B4 = 1; C4 = 0; D4 = 1;
    #1 A4 = 1; B4 = 1; C4 = 1; D4 = 0;
    #1 A4 = 1; B4 = 1; C4 = 1; D4 = 1;
```

```
//-----
//Simulación Ejercicio 2
//-----
-//----tabla 41-----
initial begin
   #70
    $display("Ejercicio 2 Tabla 1");
    $display("A B C D | Y ");
    $display("-----|---");
    $monitor("%b %b %b %b | %b", p1, p2, p3, p4,
     p1 = 0; p2 = 0; p3 = 0; p4 = 0;
    \#1 p1 = 0; p2 = 0; p3 = 0; p4 = 1;
    \#1 p1 = 0; p2 = 0; p3 = 1; p4 = 0;
    #1 p1 = 0; p2 = 0; p3 = 1; p4 = 1;
    \#1 p1 = 0; p2 = 1; p3 = 0; p4 = 0;
    \#1 p1 = 0; p2 = 1; p3 = 0; p4 = 1;
    \#1 p1 = 0; p2 = 1; p3 = 1; p4 = 0;
    \#1 p1 = 0; p2 = 1; p3 = 1; p4 = 1;
    \#1 p1 = 1; p2 = 0; p3 = 0; p4 = 0;
    #1 p1 = 1; p2 = 0; p3 = 0; p4 = 1;
    \#1 p1 = 1; p2 = 0; p3 = 1; p4 = 0;
    #1 p1 = 1; p2 = 0; p3 = 1; p4 = 1;
    \#1 p1 = 1; p2 = 1; p3 = 0; p4 = 0;
    #1 p1 = 1; p2 = 1; p3 = 0; p4 = 1;
    \#1 p1 = 1; p2 = 1; p3 = 1; p4 = 0;
    #1 p1 = 1; p2 = 1; p3 = 1; p4 = 1;
  end
//----tabla 2-----
initial begin
    $display("Ejercicio 2 Tabla 2");
    $display("A B C | Y");
    $display("-----|--");
    $monitor("%b %b %b | %b", p5, p6, p7, e2);
     p5 = 0; p6 = 0; p7 = 0;
    #1 p5 = 0; p6 = 0; p7 = 1;
    \#1 p5 = 0; p6 = 1; p7 = 0;
    \#1 p5 = 0; p6 = 1; p7 = 1;
    \#1 p5 = 1; p6 = 0; p7 = 0;
    \#1 p5 = 1; p6 = 0; p7 = 1;
    \#1 p5 = 1; p6 = 1; p7 = 0;
    #1 p5 = 1; p6 = 1; p7 = 1;
  end
```

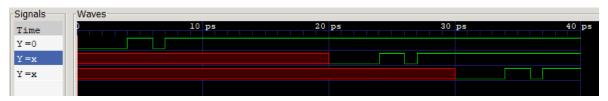
```
#100
    $display("Ejercicio 2 Tabla 3");
   $display("A B C D | Y ");
   $display("-----|---");
   $monitor("%b %b %b %b | %b", p8, p9, p10, p11, e2);
    p8 = 0; p9 = 0; p10 = 0; p11 = 0;
    #1 p8 = 0; p9 = 0; p10 = 0; p11 = 1;
   \#1 p8 = 0; p9 = 0; p10 = 1; p11 = 0;
   \#1 p8 = 0; p2 = 0; p10 = 1; p11 = 1;
   #1 p8 = 0; p9 = 1; p10 = 0; p11 = 0;
   \#1 p8 = 0; p9 = 1; p10 = 0; p11 = 1;
   #1 p8 = 0; p9 = 1; p10 = 1; p11 = 0;
   #1 p8 = 0; p9 = 1; p10 = 1; p11 = 1;
    #1 p8 = 1; p9 = 0; p10 = 0; p11 = 0;
   #1 p8 = 1; p9 = 0; p10 = 0; p11 = 1;
   \#1 p8 = 1; p9 = 0; p10 = 1; p11 = 0;
   #1 p8 = 1; p9 = 0; p10 = 1; p11 = 1;
   \#1 p8 = 1; p9 = 1; p10 = 0; p11 = 0;
   #1 p8 = 1; p9 = 1; p10 = 0; p11 = 1;
   \#1 p8 = 1; p9 = 1; p10 = 1; p11 = 0;
   #1 p8 = 1; p9 = 1; p10 = 1; p11 = 1;
//----tabla 4-----
 initial begin
   #120
   $display("Ejercicio 2 Tabla 4");
   $display("A B C | Y");
   $display("-----|--");
   $monitor("%b %b %b | %b", p12, p13, p14, e4);
    p12 = 0; p13 = 0; p14 = 0;
   #1 p12 = 0; p13 = 0; p14 = 1;
   \#1 p12 = 0; p13 = 1; p14 = 0;
   \#1 p12 = 0; p13 = 1; p14 = 1;
   \#1 p12 = 1; p13 = 0; p14 = 0;
   #1 p12 = 1; p13 = 0; p14 = 1;
   \#1 p12 = 1; p13 = 1; p14 = 0;
   #1 p12 = 1; p13 = 1; p14 = 1;
 initial
   #130 Sfinish;
//-----GTKWAVE-----
 initial begin
   $dumpfile("lap_tb.vcd");
   $dumpvars(0, testbench);
endmodule
```

Ejercicio S
Entradas: Sistema Alama armado (A), Sensor ventara / puerta (B) y sensor
movimien bo (E)
Soulidas: soñas alasma y encender luces (Y)
Cirios : was and a grant of a control to the
ABCY
00000000011110
001000001
0 1 0 0 0 1 0 0 1 121
0 1 1 0 8
1 0 0 0 5 Y= AB + AC
10115
1 10 08
1 1 1 1 5
501
ABC + ABC + ABC
P05
(ABB+0). (A+B+0). (A+B+0). (A+B+0). (A+B+0)





```
Tabla Simplificada
A B C | Y
VCD info: dumpfile ej5_tb.vcd opened for output.
000 | 0
001
      0
010
      0
011
      0
100
101
      1
110
     0
111 | 1
Tabla SOP
ABCI
000
      0
001
      0
010
      0
911
      0
100
101
      1
110
      0
111 | 1
Tabla POS
A B C | Y
000
001
      0
000
      0
001
      0
100
      1
101
      1
110
      0
1 1 1
```



```
// José Alejandro Garia Aguirre
 // Digital
 // lab4
 // -----
// Ejercicio 5 Simplificada /Gate Level Modelling
 module t5_S(input wire A, B, C, output wire Y);
 wire w1,w2,w3;
                         //B'
//AB'
//AC
 // compuertas
 not U1 (w1, B);
 and al (w2, A, w1);
 and a3 (w3, A, C);
 or ol (Y, w2,w3);
                              //Salida
3 // -----
// Ejercicio 5 SOP / Operadores Logicos
 module t5_SOP(input wire A,B,C, output wire Y);
 assign Y = (A & ~B & ~C) | (A & ~B & C ) | (A & B & C);
 endmodule
3 // -----
 // Ejercicio 5 POS / Operadores Logicos
 module t5_POS(input wire A,B,C, output wire Y);
assign Y = (A | B | C) & (A | B | ~C) & (A | ~B | C) & (~A | ~B | C) & (A | ~B | ~C);
endmodule
// José Alejandro Garia Aguirre
// Digital
// lab4
module testbench();
  reg Al, Bl, Cl,
                  //Entradas Ejercicio 5
     A2, B2, C2,
     A3, B3, C3;
  wire Y1, Y2, Y3;
                    //Salidas Ejercicio 5
 //-----Modulos Ejercicio 1-----
 t5_S tS(A1, B1, C1, Y1);
t5_SOP tSOP(A2, B2, C2, Y2);
 t5_POS tPOS(A3, B3, C3, Y3);
//Simulación Ejercicio 5
```

```
//----tabla 1-----
initial begin
    $display("Tabla Simplificada");
    $display("A B C | Y ");
    $display("-----);
    $monitor("%b %b %b | %b", A1, B1, C1, Y1);
     A1 = 0; B1 = 0; C1 = 0;
    #1 A1 = 0; B1 = 0; C1 = 1;
    #1 A1 = 0; B1 = 1; C1 = 0;
    #1 A1 = 0; B1 = 1; C1 = 1;
    #1 A1 = 1; B1 = 0; C1 = 0;
    #1 A1 = 1; B1 = 0; C1 = 1;
    #1 A1 = 1; B1 = 1; C1 = 0;
    #1 A1 = 1; B1 = 1; C1 = 1;
//----tabla 2-----
initial begin
    #20
    $display("Tabla SOP");
    $display("A B C | Y");
    $display("----|--");
    $monitor("%b %b %b | %b", A2, B2, C2, Y2);
    A2 = 0; B2 = 0; C2 = 0;
    #1 A2 = 0; B2 = 0; C2 = 1;
    #1 A2 = 0; B2 = 1; C2 = 0;
    #1 A2 = 0; B2 = 1; C2 = 1;
    #1 A2 = 1; B2 = 0; C2 = 0;
    #1 A2 = 1; B2 = 0; C2 = 1;
    #1 A2 = 1; B2 = 1; C2 = 0;
    #1 A2 = 1; B2 = 1; C2 = 1;
  end
//-----POS-----
  initial begin
   #30
    $display("Tabla POS");
   $display("A B C | Y ");
    $display("----");
  $monitor("%b %b %b | %b", A3, B3, C3, Y3);
    A3 = 0; B3 = 0; C3 = 0;
    #1 A3 = 0; B3 = 0; C3 = 1;
    #1 A3 = 0; B2 = 1; C3 = 0;
    #1 A3 = 0; B2 = 1; C3 = 1;
    #1 A3 = 1; B2 = 0; C3 = 0;
    #1 A3 = 1; B3 = 0; C3 = 1;
    #1 A3 = 1; B3 = 1; C3 = 0;
    #1 A3 = 1; B3 = 1; C3 = 1;
  end
  initial
   #40 $finish;
                ---GTKWAVE-----
  initial begin
   $dumpfile("ej5_tb.vcd");
    $dumpvars(0, testbench);
```