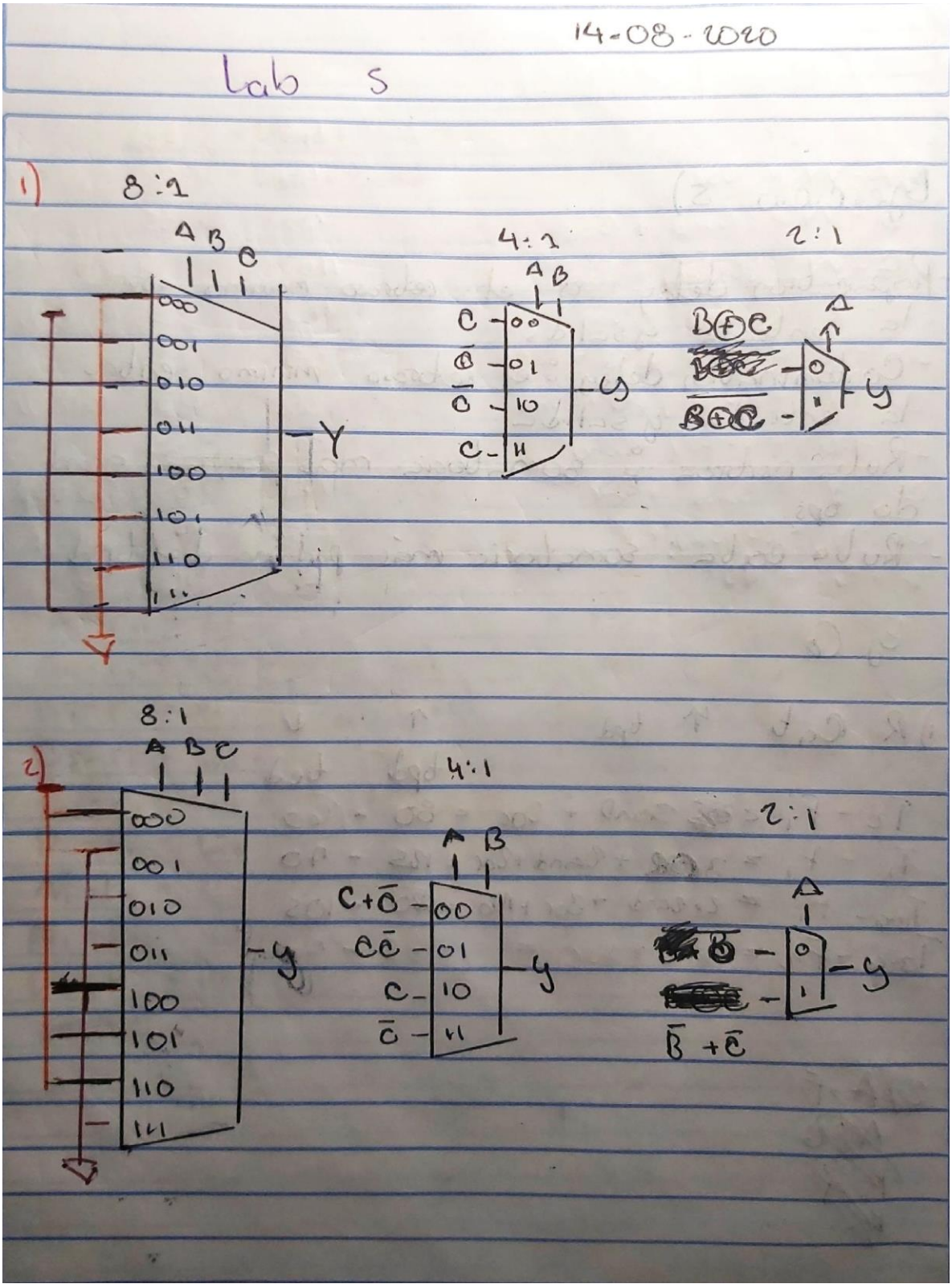
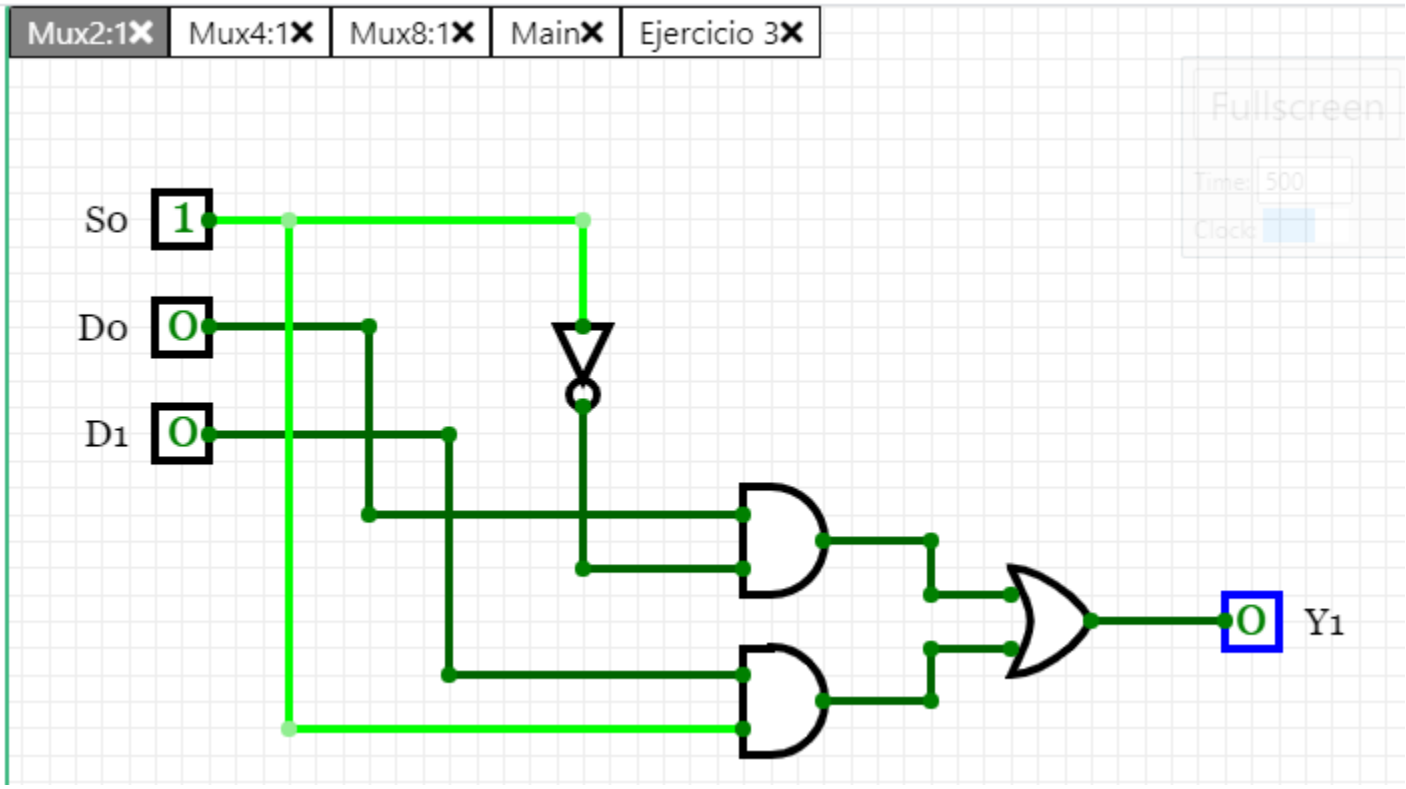
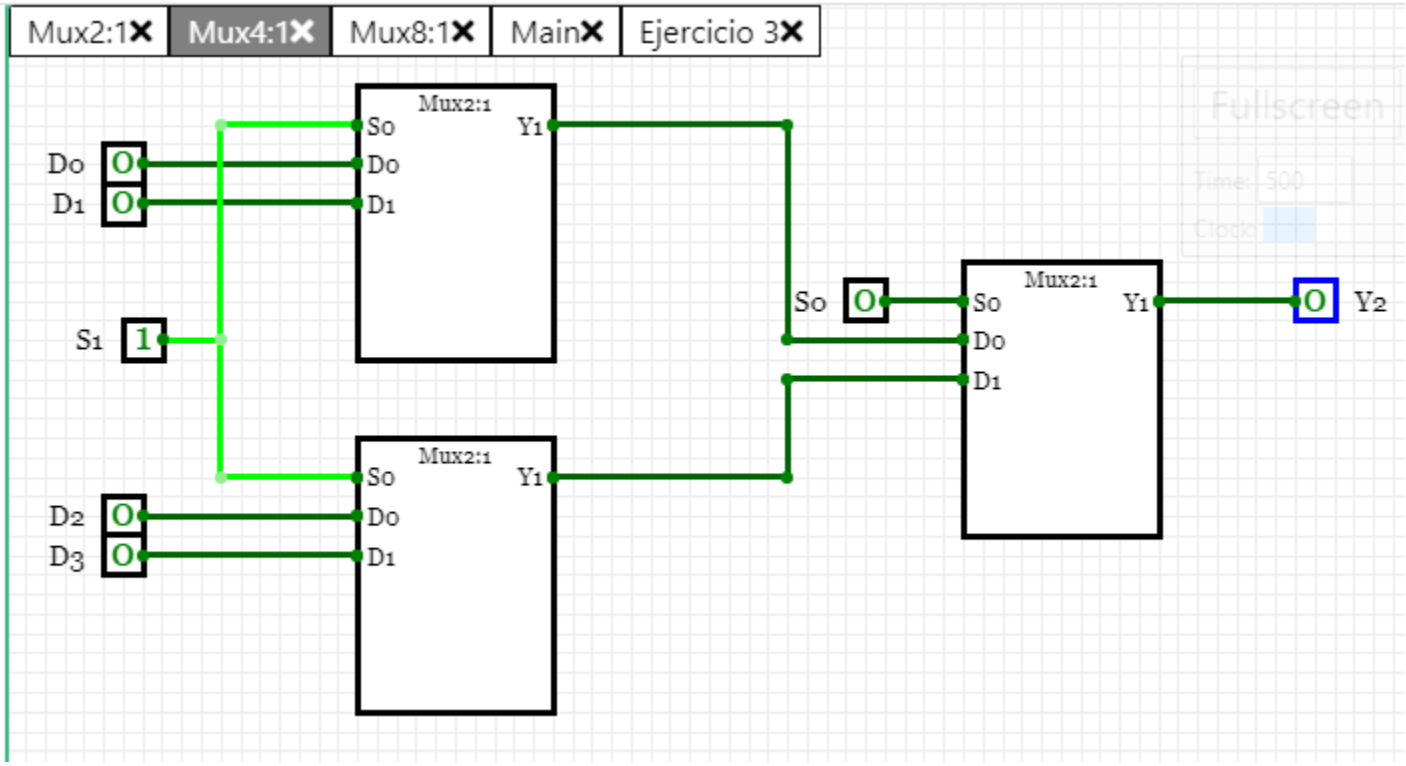
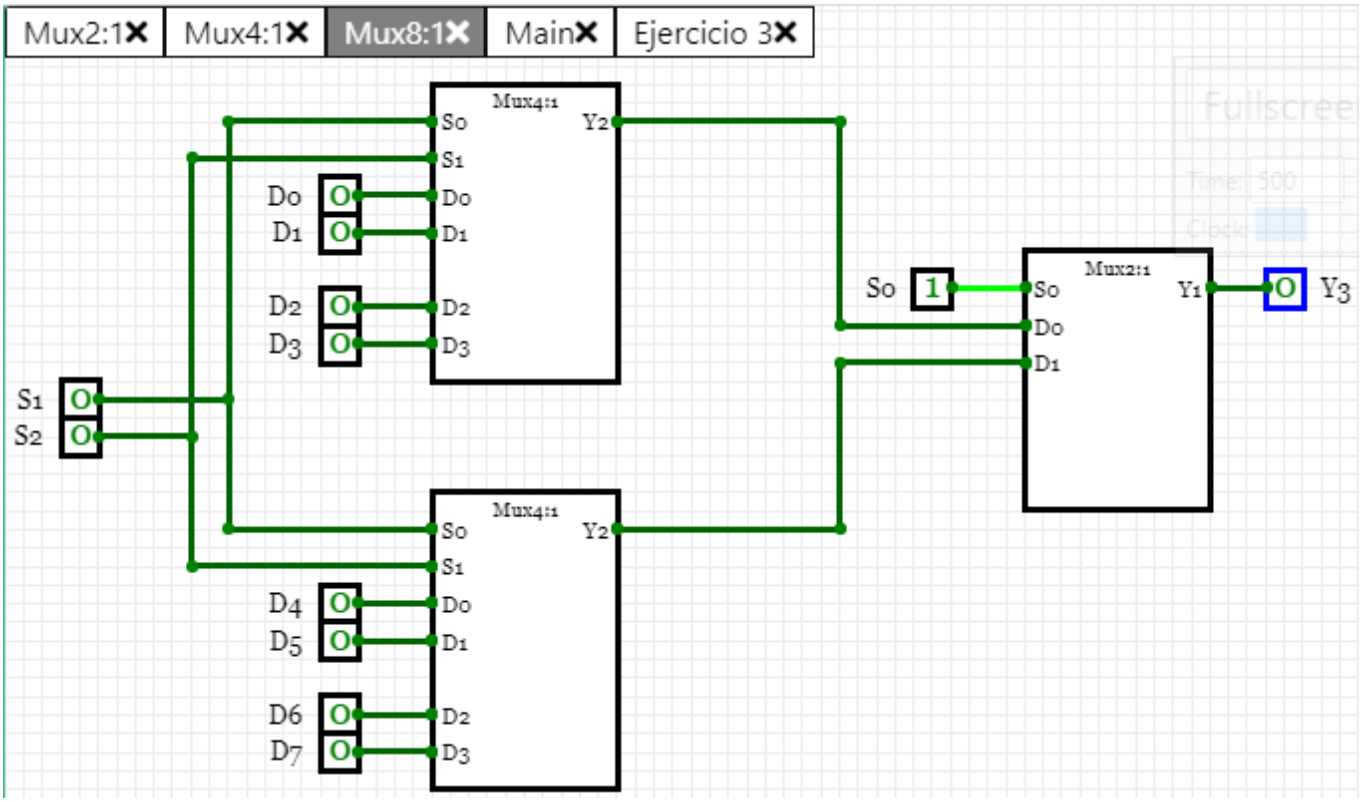

14-08-2020
Lab 5
1) 8:1
A B C
000
001
010
011
100
101
110
111
Y
4:1
A B
C
C̄
0
C
00
01
10
11
y
2:1
B⊕C
B⊕C
0
1
y
2) 8:1
A B C
000
001
010
011
100
101
110
111
y
4:1
A B
C+C̄
CC̄
C
C̄
00
01
10
11
y
2:1
B̄
B̄ +C̄
0
1
y

Ejercicio 1

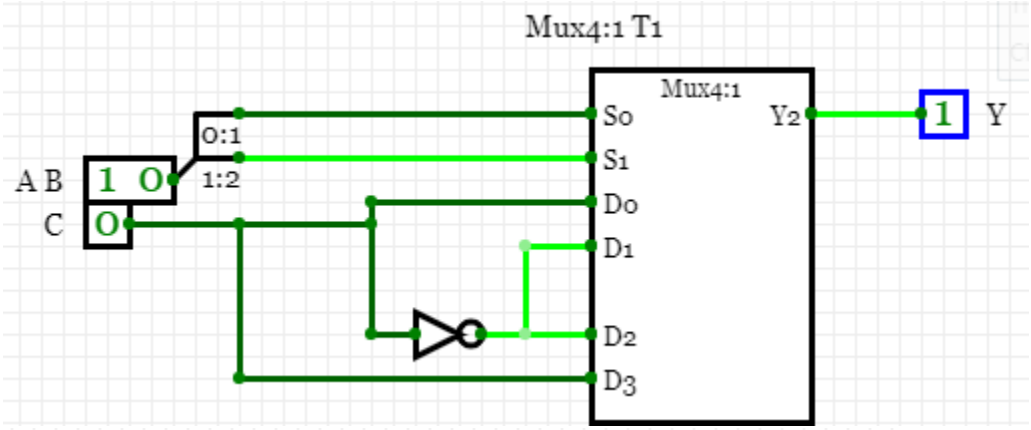
Ejercicio 2


Mux2:1
Mux4:1
Mux8:1
Main
Ejercicio 3
So
1
Do
0
D1
0
0
Y1

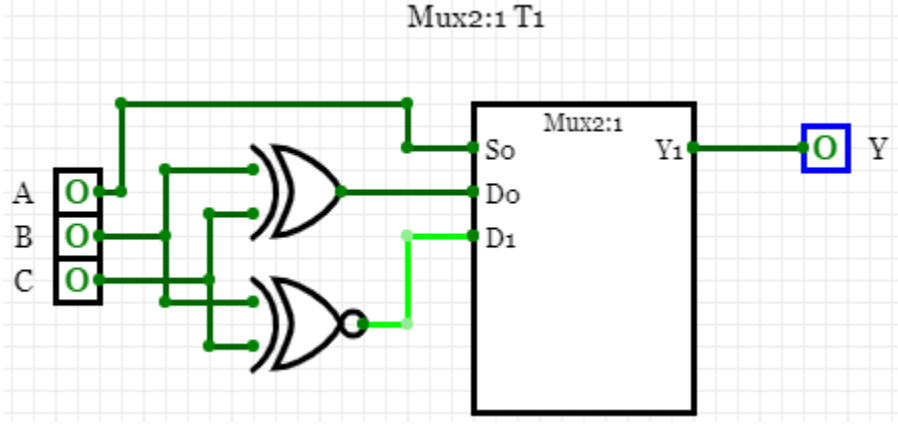

Mux2:1
Mux4:1
Mux8:1
Main
Ejercicio 3
Mux2:1
So
Y1
Do
D1
Do
0
D1
0
S1
1
D2
0
D3
0
So
0
Mux2:1
So
Y1
Do
D1
0
Y2

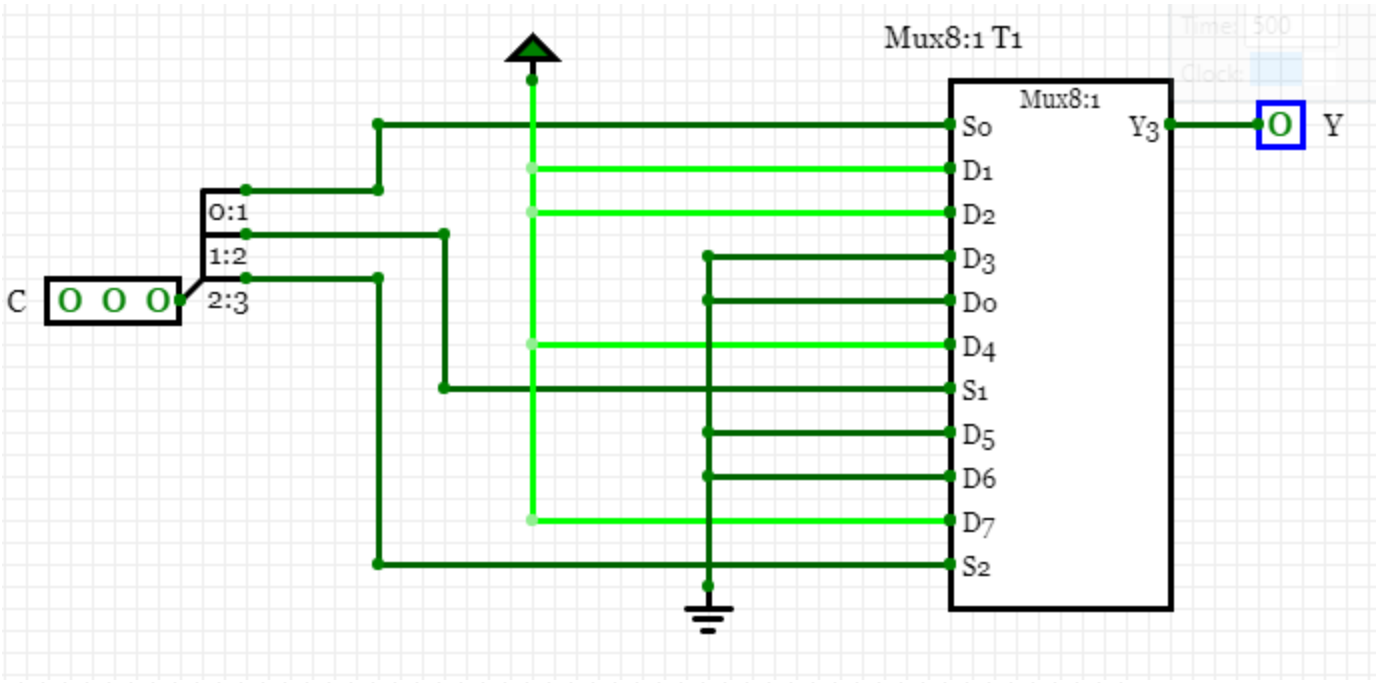


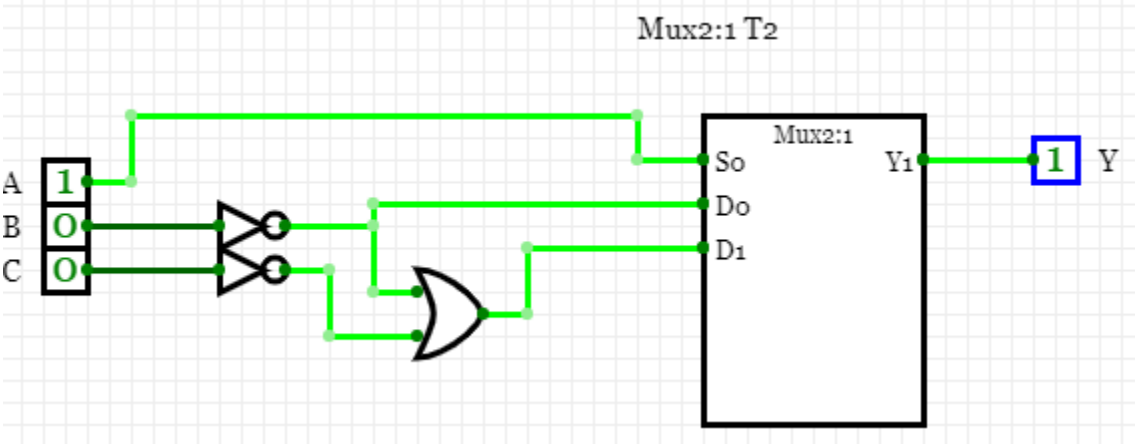
Mux4:1 T1

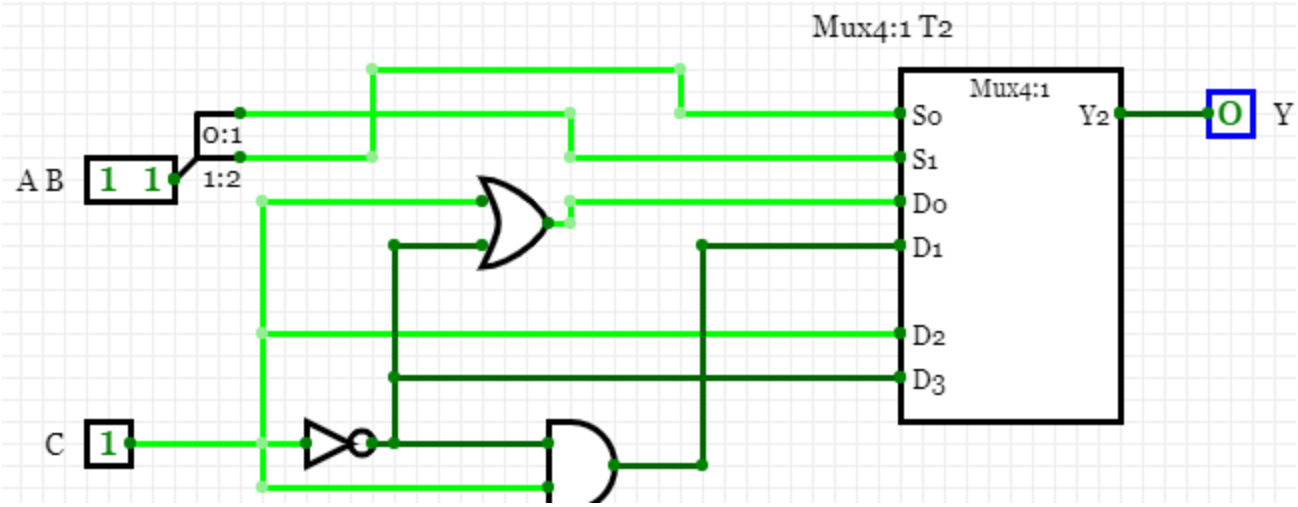


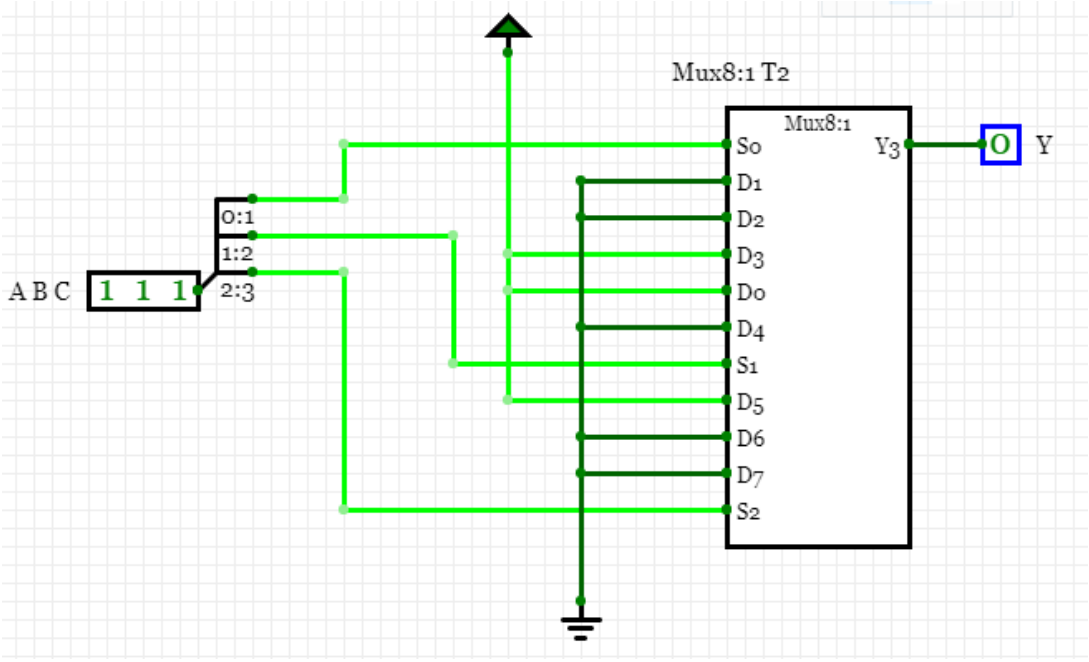
Mux2:1 T1



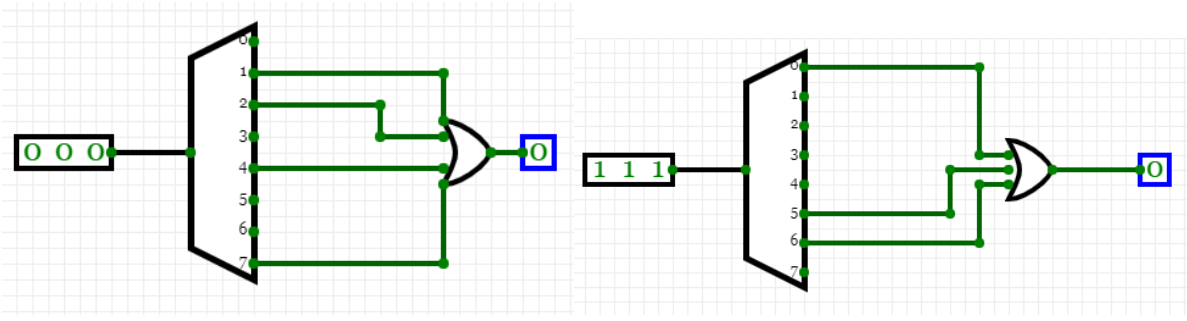

Mux8:1 T1
Mux8:1
So
Y3
O
Y
D1
D2
D3
Do
D4
S1
D5
D6
D7
S2
0:1
1:2
2:3
C
O O O


Mux2:1 T2
Mux2:1
So
Y1
1
Y
Do
D1
A
1
B
O
C
O





Ejercicio 3



Ejercicio 5-6

Ejercicio 5)

- Propagation delay: es el retraso maximo entre la entrada y salida
- Contamination delay: el retraso minimo entre la entrada y salida
- Ruta critica: sumatoria mas grande de tps
- Ruta corta: sumatoria más pequeña de tpd

Ej C6

1) R C1,6 ↑ tpd ↑ tpd ↓ tcd

T2 - F1 = 3and + 2or = 80 - 60 C0,6 F1

T1 - F1 = 3and + 2and + 2or = 145 - 70

T3-6 - F1 = 2·2and + 3or + 100 = 130 - 105 C1,6 F1

T3-6 - F2 = 2and + 3or = 85 - 70 F2

	tpd	tcd	
2) A - F₁ = N + 2Nand + 2and =	65	50	Cor F
- A - G = N + 2or + 2and =	85	65	
B - F = 2and + 2or =	100	80	Cot F
- B - G = 2 · 2and + 2or =	100	80	Cot G
A - F = N + 2or + 2and =	85	65	
- A - G = N + 2Nand + 2and =	65	50	
D - F = 2 · 2Nand + 2and =	70	55	
- D - G = 2Nand + 2and =	50	40	Cor G
A - F = N + 2Nand or + 2and =	85	65	
3) A₁ - F₁ = 2 · 2or =	80	80	Cor F₁
A₂ - F₁ = N + 2and + (2 · 2or) =	125	95	
B₁ - F₁ = N + 2and + (2or · 2) =	125	95	
B₂ - F₁ = 2and + 2or + 2or =	130	95	Cot F₁
C - F₁ = 2and + (2 · 2or) =	110	85	
D - F₁ = 2and + 2or =	100	70	
A₁ - F₂ = N + 2and + 2or =	85	65	Cot F₂
B₁ - F₂ = 2or + 2and =	70	55	
D₁ - F₂ = N + 2or =	55	40	Cot F₂

	tpd	tcd	
4) A - W = 2or	40	(30)	Cortoa W
B - W = 2and + 2or	70	55	
D - W = (2·2or) + 2and	(110)	85	Crit W
B - x = 2and + 2or	70	(55)	Cortb x
B - x = N + 2and + 2or	85	65	
CD - x = (2·2or) + N + 2and	(125)	95	Crit x
CD - x = (2·2or) + 2and	110	85	
CD - Y = 2and + 2or	70	(55)	Cortb Y
CD - Y = (2·2or) + N	(95)	70	Crit Y
D - Z = N	(15)	(10)	Z

```
// ------------------------------------
// José Alejandro García Aguirre
// Digital
// lab5
// ------------------------------------
// Ejercicio 2 Modulo mux2_1
// ------------------------------------
module m2(output wire Y, input wire d0,d1,s);

  assign Y=s ? d1: d0;

endmodule
// ------------------------------------
// Ejercicio 2 Modulo mux4_1
// ------------------------------------
module m4(output wire Y, input wire d0,d1,d2,d3,s0,s1);

  wire p0, p1;

  m2 x0(d0,d1,s0,p1);
  m2 x1(d2,d3,s1,p2);
  m2 x2(p0,p1,s1,Y);

endmodule

// ------------------------------------
// Ejercicio 2 Modulo mux8_1
// ------------------------------------
module m8(output wire y2, input wire d0,d1,d2,d3,d4,d5,d6,d7,s0,s1,s2);

  wire p2, p3;

  m4 x3(d0,d1,d2,d3,s0,s1,p1);
  m4 x4(d4,d5,d6,d7,s0,s1,p2);
  m2 x5(p2,p3,s2,y2);
endmodule

// ------------------------------------
// Tabla 1 Modulo mux2_1
// ------------------------------------
module t1m2(input wire A, B, C, output wire Y);

    m2 J1 (A, Y,(B~^C), (B^C));

endmodule
```

```
// Tabla 1 Modulo mux4_1
// ------------------------------------

module t1m4(input wire A, B, C, output wire Y);

    m4 J2(C, ~C, ~C, C, A, B, Y);

endmodule

// ------------------------------------
// Tabla 1 Modulo mux8_1
// ------------------------------------
module t1m8(input wire A, B, C, output wire Y);

    wire E, S;
    assign E = 1;
    assign S = 0;
    m8 J3(Sal, E, E, S, ENT, SAL, SAL, ENT, A, B, C, Y);

endmodule

// ------------------------------------
// Tabla 2 Modulo mux2_1
// ------------------------------------
module t2m2(input wire A, B, C, output wire Y);

    m2 U1(~(B|C), ~(B&C), A, Y);

endmodule

// ------------------------------------
// Tabla 2 Modulo mux4_1
// ------------------------------------
module t2m4(input wire A, B, C, output wire Y);

    m4 U2(~C, ~C&C, ~C|C, ~C, A, B, Y);

endmodule

// ------------------------------------
// Tabla 2 Modulo mux8_1
// ------------------------------------
module t2m8(input wire A, B, C, output wire Y);

    wire E, S;
    assign E = 1;
    assign S = 0;
    m8 U3(E, S, S, S, E, E, E, S, A, B, C, Y);

endmodule
```

```
// ------------------------------------
// José Alejandro García Aguirre
// Digital
// lab5 testbench
// ------------------------------------
module testbench();
// ------------------------------------
// Entradas
// ------------------------------------
  reg A21, B21, C21, A41, B41, C41, A81, B81, C81, A22, B22, C22, A42, B42, C42, A82, B82, C82;
  wire T1M2, T1M4, T1M8, T2M2, T2M4, T2M8;

    t1m2 t1_2(A21, B21, C21, T1M2);
    t1m4 t1_4(A41, B41, C41, T1M4);
    t1m8 t1_8(A81, B81, C81, T1M8);
    t2m2 t2_2(A22, B22, C22, T2M2);
    t2m4 t2_4(A42, B42, C42, T2M4);
    t2m8 t2_8(A82, B82, C82, T2M8);

// ------------------------------------
// Tabla 1 Modulo mux2_1
// ------------------------------------
  initial begin
    #5
    $display("Tabla 1 Mux2:1");
    $display("A B C | Y");
    $display("------|--");
    $monitor("%b %b %b | %b", A21, B21, C21, T1M2);
       A21 = 0; B21 = 0; C21 = 0;
    #1 A21 = 0; B21 = 0; C21 = 1;
    #1 A21 = 0; B21 = 1; C21 = 0;
    #1 A21 = 0; B21 = 1; C21 = 1;
    #1 A21 = 1; B21 = 0; C21 = 0;
    #1 A21 = 1; B21 = 0; C21 = 1;
    #1 A21 = 1; B21 = 1; C21 = 0;
    #1 A21 = 1; B21 = 1; C21 = 1;
  end
```

```
// ------------------------------------
// Tabla 1 Modulo mux4_1
// ------------------------------------
  initial begin
    #15
    $display("\n");
    $display("Tabla 1 Mux4:1");
    $display("A B C | Y");
    $display("------|--");
    $monitor("%b %b %b | %b", A41, B41, C41, T1M4);
       A41 = 0; B41 = 0; C41 = 0;
    #1 A41 = 0; B41 = 0; C41 = 1;
    #1 A41 = 0; B41 = 1; C41 = 0;
    #1 A41 = 0; B41 = 1; C41 = 1;
    #1 A41 = 1; B41 = 0; C41 = 0;
    #1 A41 = 1; B41 = 0; C41 = 1;
    #1 A41 = 1; B41 = 1; C41 = 0;
    #1 A41 = 1; B41 = 1; C41 = 1;
  end

// ------------------------------------
// Tabla 1 Modulo mux8_1
// ------------------------------------
  initial begin
    #25
    $display("\n");
    $display("Tabla 1 con Mux8:1");
    $display("A B C | Y");
    $display("------|--");
    $monitor("%b %b %b | %b", A81, B81, C81, T1M8);
       A81 = 0; B81 = 0; C81 = 0;
    #1 A81 = 0; B81 = 0; C81 = 1;
    #1 A81 = 0; B81 = 1; C81 = 0;
    #1 A81 = 0; B81 = 1; C81 = 1;
    #1 A81 = 1; B81 = 0; C81 = 0;
    #1 A81 = 1; B81 = 0; C81 = 1;
    #1 A81 = 1; B81 = 1; C81 = 0;
    #1 A81 = 1; B81 = 1; C81 = 1;
  end
```

```
// ------------------------------------
// Tabla 2 Modulo mux2_1
// ------------------------------------
  initial begin
    #30
    $display("\n");
    $display("Tabla 2 Mux2:1");
    $display("A B C | Y");
    $display("------|--");
    $monitor("%b %b %b | %b", A22, B22, C22, T2M2);
       A22 = 0; B22 = 0; C22 = 0;
    #1 A22 = 0; B22 = 0; C22 = 1;
    #1 A22 = 0; B22 = 1; C22 = 0;
    #1 A22 = 0; B22 = 1; C22 = 1;
    #1 A22 = 1; B22 = 0; C22 = 0;
    #1 A22 = 1; B22 = 0; C22 = 1;
    #1 A22 = 1; B22 = 1; C22 = 0;
    #1 A22 = 1; B22 = 1; C22 = 1;
  end

// ------------------------------------
// Tabla 2 Modulo mux4_1
// ------------------------------------
  initial begin
    #40
    $display("\n");
    $display("Tabla 2 Mux4:1");
    $display("A B C | Y");
    $display("------|--");
    $monitor("%b %b %b | %b", A42, B42, C42, T2M4);
       A42 = 0; B42 = 0; C42 = 0;
    #1 A42 = 0; B42 = 0; C42 = 1;
    #1 A42 = 0; B42 = 1; C42 = 0;
    #1 A42 = 0; B42 = 1; C42 = 1;
    #1 A42 = 1; B42 = 0; C42 = 0;
    #1 A42 = 1; B42 = 0; C42 = 1;
    #1 A42 = 1; B42 = 1; C42 = 0;
    #1 A42 = 1; B42 = 1; C42 = 1;
  end
```

```
// ------------------------------------
// Tabla 2 Modulo mux8_1
// ------------------------------------
  initial begin
    #50
    $display("\n");
    $display("Tabla 2 Mux8:1");
    $display("A B C | Y");
    $display("------|--");
    $monitor("%b %b %b | %b", A82, B82, C82, T2M8);
      A82 = 0; B82 = 0; C82 = 0;
    #1 A82 = 0; B82 = 0; C82 = 1;
    #1 A82 = 0; B82 = 1; C82 = 0;
    #1 A82 = 0; B82 = 1; C82 = 1;
    #1 A82 = 1; B82 = 0; C82 = 0;
    #1 A82 = 1; B82 = 0; C82 = 1;
    #1 A82 = 1; B82 = 1; C82 = 0;
    #1 A82 = 1; B82 = 1; C82 = 1;
  end


  initial
    #65 $finish;
// ------------------------------------
// GTKWAVE
// ------------------------------------
  initial begin
    $dumpfile("lab5_tb.vcd");
    $dumpvars(0, testbench);
  end

endmodule
```