Laboratorio #07
(octubre 2020)

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Máquinas de estados finitos:

- Links de tinkercad, diagramas y repositorio:

FSM #1: https://www.tinkercad.com/things/373YJyhUHPC

FSM #2: https://www.tinkercad.com/things/88klkoP0ube

FSM #3: https://www.tinkercad.com/things/56rxpMM0un5

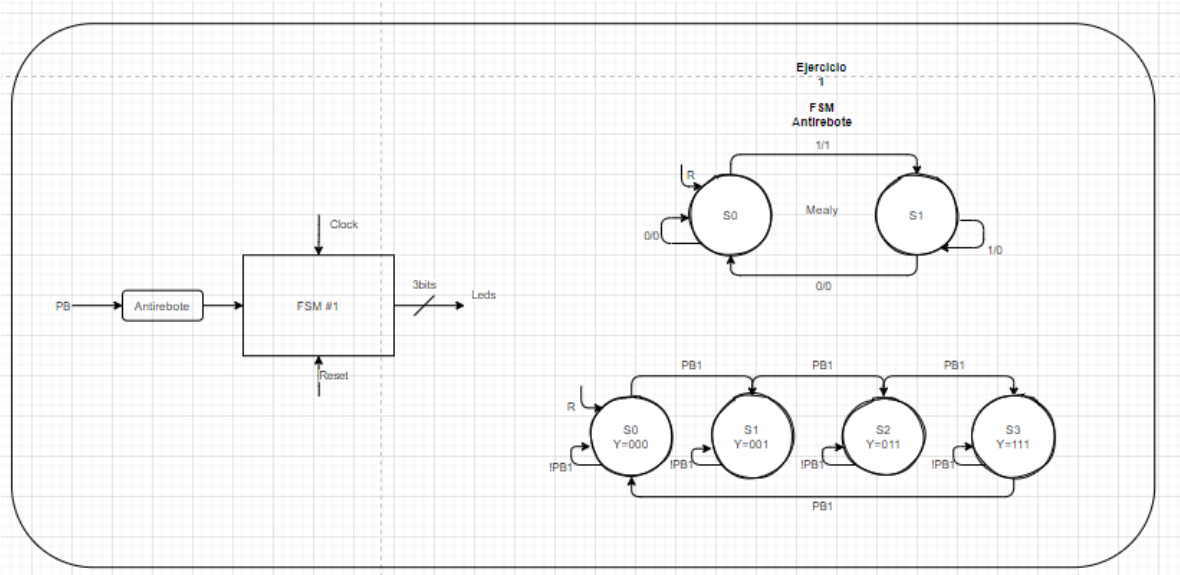
Diagramas en draw.io (ingresar con correo de la UVG):
https://drive.google.com/file/d/1guvn-Y80__vkAu_JfkAPlJuyDineNbXY/view?usp=sharing

Repositorio en github: https://github.com/gar19421/Lab-07-Digital.git

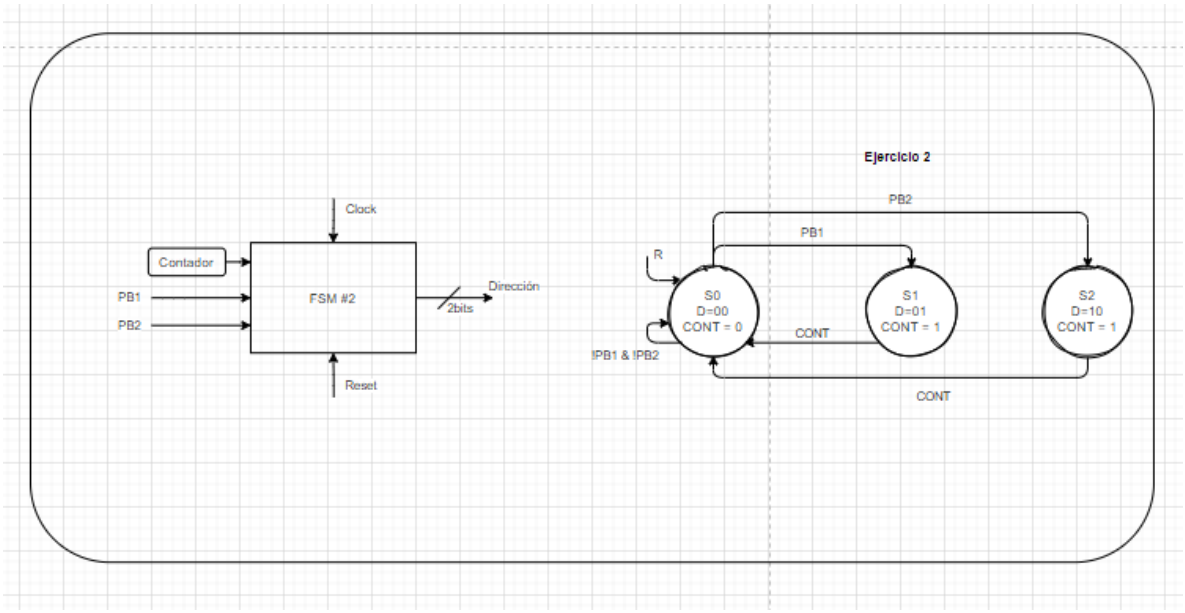
- Screenshots de evidencias:

Diagramas de transición y cajas negras:

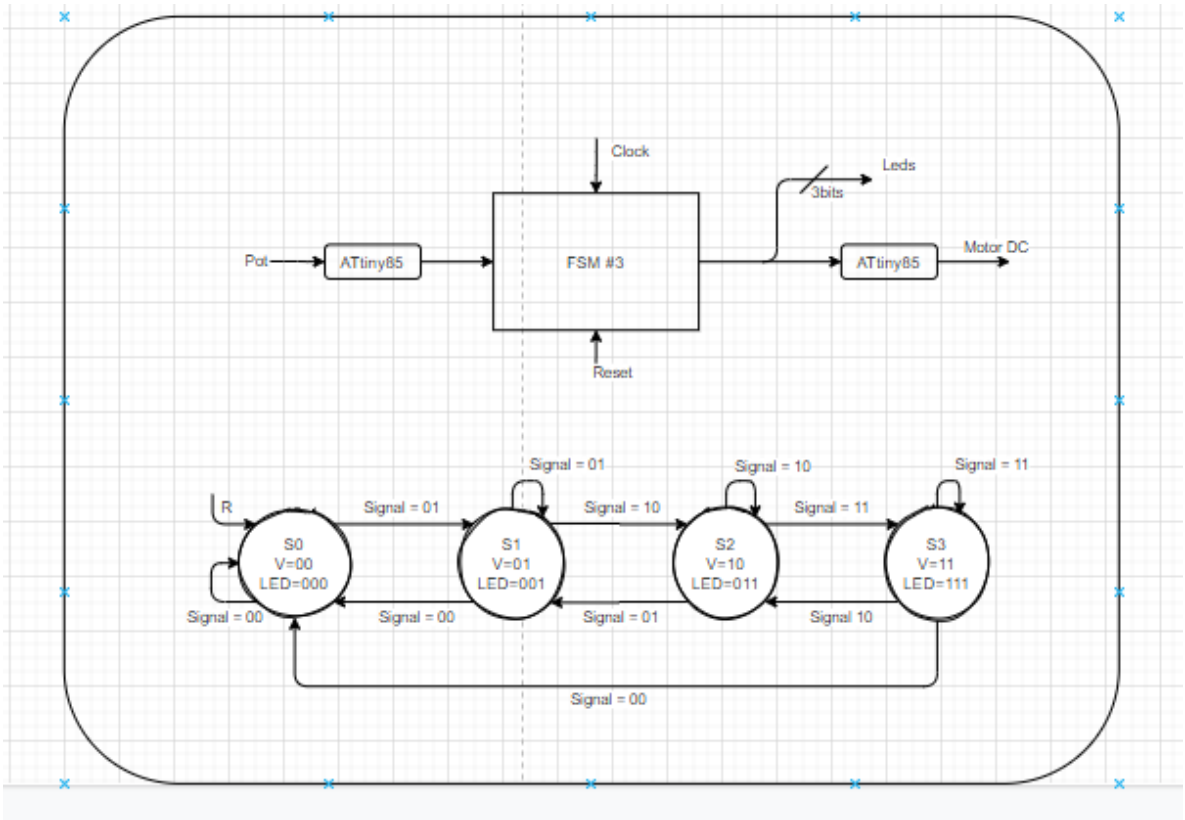
FSM #1:



FSM #2:


Ejercicio 2
Clock
Contador
PB1
PB2
FSM #2
Dirección
2bits
Reset
R
PB2
PB1
S0
D=00
CONT = 0
S1
D=01
CONT = 1
S2
D=10
CONT = 1
CONT
!PB1 & !PB2
CONT

FSM #3:


Clock
Leds
3bits
Pot
ATtiny85
FSM #3
ATtiny85
Motor DC
Reset
R
Signal = 01
Signal = 10
Signal = 11
S0
V=00
LED=000
S1
V=01
LED=001
S2
V=10
LED=011
S3
V=11
LED=111
Signal = 00
Signal = 00
Signal = 01
Signal 10
Signal = 00

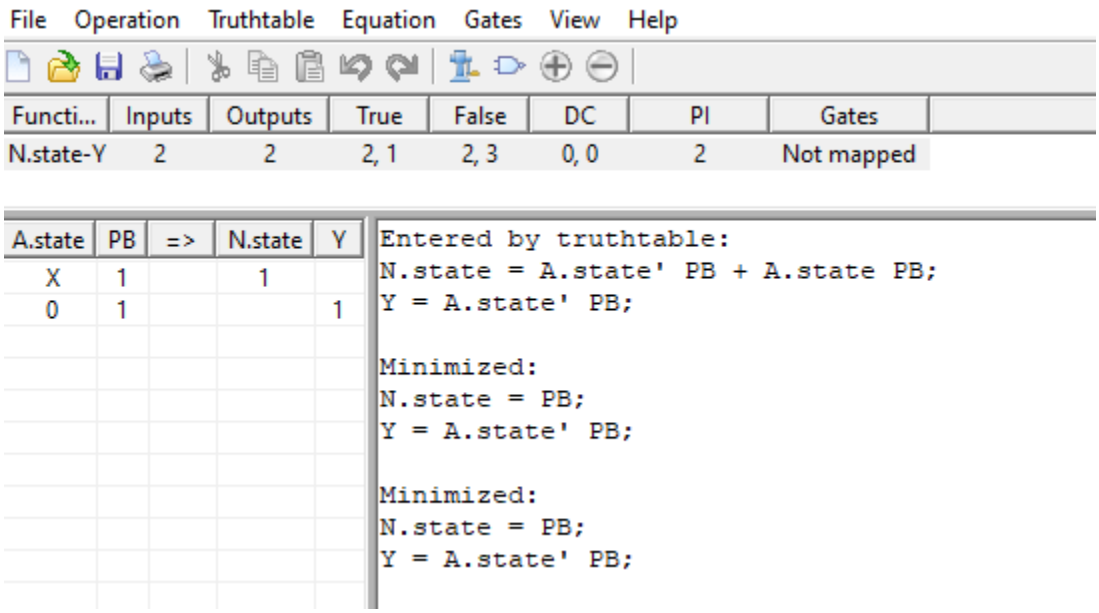
- FSM #1

Tablas de transición de anti-rebote:

Tabla de transición de estados y salidas (mealy)			
Current State	Input	Next State	Output
S0	0	S0	0
S0	1	S1	1
S1	0	S0	0
S1	1	S1	0

Tabla de transición de estados y salidas con codificación binaria			
Current State	Input	Next State	Output
0	0	0	0
0	1	1	1
1	0	0	0
1	1	1	0

Ecuaciones booleanas antirebote:



Tablas de transición de estado y salidas máquina principal:

TABLA DE TRANSICIÓN SC		
Current state	Input	Next state
S0	0	S0
S0	1	S1
S1	0	S1
S1	1	S2
S2	0	S2
S2	1	S3
S3	0	S3
S3	1	S0

TABLA DE TRANSICIÓN CC		
Current state	Input	Next state
00	0	00
00	1	01
01	0	01
01	1	10
10	0	10
10	1	11
11	0	11
11	1	00

TABLA DE SALIDAS SC	
S0	000
S1	001
S2	011
S3	111

TABLA DE SALIDAS CC	
00	000
01	001
10	011
11	111

Logic Friday:

Functi...	Inputs	Outputs	True	False	DC	PI	Gates
F1-F0	3	2	4, 4	4, 4	0, 0	5	Not mapped

S1	S0	PB	=>	F1	F0
X	0	1			1
X	1	0			1
0	1	1		1	
1	0	X		1	
1	X	0		1	

```
Entered by truthtable:
F1 = S1' S0 PB + S1 S0' PB' + S1 S0' PB + S1 S0
PB';
F0 = S1' S0' PB + S1' S0 PB' + S1 S0' PB + S1
S0 PB';

Minimized:
F1 = S1' S0 PB + S1 S0'  + S1 PB';
F0 = S0' PB + S0 PB';
```

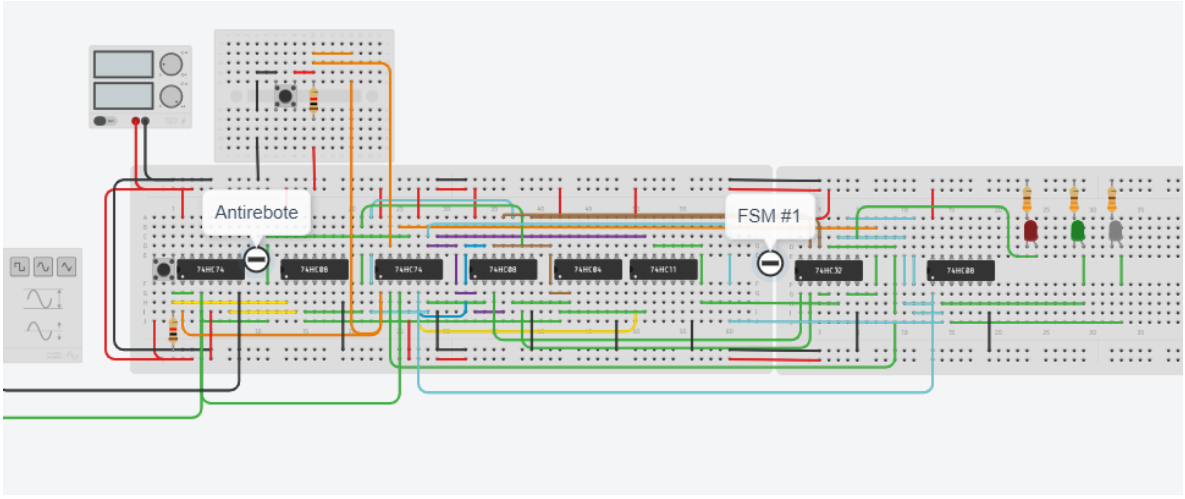
Functi...	Inputs	Outputs	True	False	DC	PI	Gates
LD3-LD1	2	3	1, 2, 3	3, 2, 1	0, 0, 0	3	Not mapped

S1	S0	=>	LD3	LD2	LD1
1	1		1		
X	1				1
1	X			1	1

```
Entered by truthtable:
LD3 = S1 S0;
LD2 = S1 S0' + S1 S0;
LD1 = S1' S0 + S1 S0' + S1 S0;

Minimized:
LD3 = S1 S0;
LD2 = S1 ;
LD1 = S0 + S1 ;
```

Circuito en tinkercad:



- FSM #2

Tabla de estados y salidas:

TABLA DE TRANSICIÓN SC				
Current state	PB1	PB2	CONT	Next state
S0	0	0	0	S0
S0	1	0	0	S1
S0	0	1	0	S2
S1	0	0	0	S1
S1	0	0	1	S0
S2	0	0	0	S2
S2	0	0	1	S0

TABLA DE TRANSICIÓN CC				
Current state	PB1	PB2	CONT	Next state
00	0	0	0	00
00	1	0	0	01
00	0	1	0	10
01	0	0	0	01
01	0	0	1	00
10	0	0	0	10
10	0	0	1	00

TABLA DE SALIDAS SC		
State	DIRECCION	CONT
S0	00	0
S1	01	1
S2	10	1

TABLA DE SALIDAS CC		
State	DIRECCION	CONT
00	00	0
01	01	1
10	10	1

Logic Friday:

Functi...	Inputs	Outputs	True	False	DC	PI	Gates
D1-CO...	2	3	1, 1, 2	2, 2, 1	1, 1, 1	2	Not mapped

S1	S0	=>	D1	D0	CONT
X	1			1	1
1	X		1		1

```
Entered by truthtable:
D1 = S1 S0';
D0 = S1' S0;
CONT = S1' S0 + S1 S0';

Minimized:
D1 = S1 ;
D0 = S0;
CONT = S0 + S1 ;
```

File Operation Truthtable Equation Gates View Help

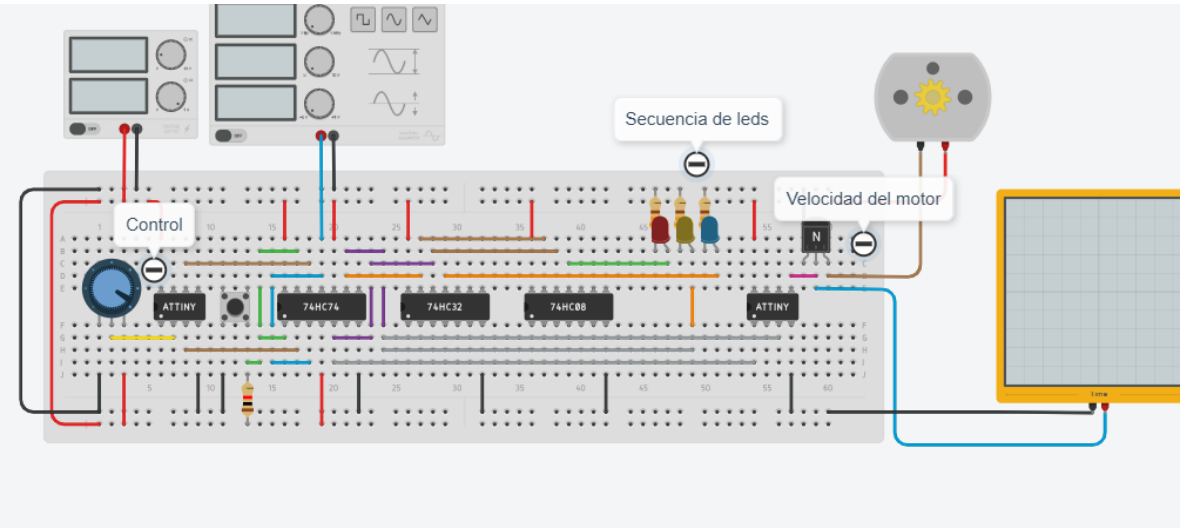
Functi...	Inputs	Outputs	True	False	DC	PI	Gates
F1-F0	5	2	2, 2	22, 22	8, 8	4	Not mapped

S1	S0	PB2	PB1	CONT	=>	F1	F0
X	1	0	0	0			1
1	X	0	0	0		1	
0	0	0	1	0			1
0	0	1	0	0		1	

```
Entered by truthtable:
F1 = S1' S0' PB2 PB1' CONT' + S1 S0'
PB2' PB1' CONT';
F0 = S1' S0' PB2' PB1 CONT' + S1' S0
PB2' PB1' CONT';

Minimized:
F1 = S1 PB2' PB1' CONT' + S1' S0' PB2
PB1' CONT';
F0 = S0 PB2' PB1' CONT' + S1' S0'
PB2' PB1 CONT';
```

Circuito:



- FSM #3:

Tablas de transición de estados y salidas:

TABLA DE TRANSICIÓN SC		
Current state	Input	Next state
S0	00	S0
S0	10	S1
S1	00	S0
S1	01	S1
S1	10	S2
S2	01	S1
S2	10	S2
S2	11	S3
S3	11	S3
S3	10	S2
S3	00	S0

TABLA DE TRANSICIÓN CC		
Current state	Input	Next state
00	00	00
00	10	01
01	00	00
01	01	01
01	10	10
10	01	01
10	10	10
10	11	11
11	11	11
11	10	10
11	00	00

TABLA DE SALIDAS SC		
State	Leds	Velocidad
S0	000	00
S1	001	00
S2	011	10
S3	111	11

TABLA DE SALIDAS CC		
State	Leds	Velocidad
00	000	00
01	001	00
10	011	10
11	111	11

Logic Friday:

Functi...	Inputs	Outputs	True	False	DC	PI	Gates
F1-F0	4	2	5, 5	11, 11	0, 0	6	Not mapped

S1	S0	AT1	AT0	=>	F1	F0
0	1	0	1			1
0	0	1	0			1
X	1	1	0		1	
1	0	X	1			1
1	X	1	1			1
1	X	1	X		1	

```
Entered by truthtable:
F1 = S1' S0 AT1 AT0' + S1 S0' AT1 AT0' + S1
S0' AT1 AT0 + S1 S0 AT1 AT0' + S1 S0 AT1
AT0;
F0 = S1' S0' AT1 AT0' + S1' S0 AT1' AT0 +
S1 S0' AT1' AT0 + S1 S0' AT1 AT0 + S1 S0
AT1 AT0;

Minimized:
F1 = S0 AT1 AT0' + S1 AT1 ;
F0 = S1' S0 AT1' AT0 + S1' S0' AT1 AT0' +
S1 S0' AT0 + S1 AT1 AT0;
```

Functi...	Inputs	Outputs	True	False	DC	PI	Gates
LD3-V0	2	5	1, 2, ...	3, 2, ...	0, 0, ...	3	Not mapped

S1	S0	=>	LD3	LD2	LD1	V1	V0
1	1		1				1
X	1				1		
1	X			1	1	1	

```
Entered by truthtable:
LD3 = S1 S0;
LD2 = S1 S0' + S1 S0;
LD1 = S1' S0 + S1 S0' + S1 S0;
V1 = S1 S0' + S1 S0;
V0 = S1 S0;

Minimized:
LD3 = S1 S0;
LD2 = S1 ;
LD1 = S0 + S1 ;
V1 = S1 ;
V0 = S1 S0;
```

Circuito: