Design of a Compact Complementary Metal-Oxide Semiconductor Imager

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***Abstract*— This project presents the schematic design, simulation, and integrated circuit layout of an active pixel sensor (APS) array using Complementary Metal-Oxide Semiconductor (CMOS) technology on a compact 2.5 mm × 2.5 mm chip. The objective was to develop a scalable imager-on-a-chip in the Cadence design environment with the highest pixel density and sensitivity. We began by designing and validating the functionality of a single 3-transistor APS pixel. The layout of each individual pixel maximizes the photodiode area within to enhance light sensitivity. We then combined the pixel with shift registers to create a 4×4 pixel array. Following successful validation of the 4x4 array, we expanded the design to a 248×248 pixel array, efficiently utilizing the entire chip area. We also implemented methods to reduce fixed pattern noise. This project demonstrates the feasibility of high-resolution CMOS imaging within strict area constraints and opens the door towards future hardware implementation and testing.**

***Index Terms* — CMOS, APS (Active Pixel Sensor), Photosensors, Imager-o-a-chip, Semiconductors, IC Chip Design**

I. Introduction

The metal-oxide semiconductor image sensor was first developed in the 1960s but was initially overshadowed by the charge-coupled device (CCD) image sensor [1]. The rapid advancement of complementary metal-oxide semiconductor (CMOS) technology in the 1990s [1] laid the foundation for its widespread adoption during the surge in demand for mobile imaging in cell phones and video cameras in the 21st century [2]. By integrating sensing and processing on a single chip, thus consuming less power, offering a lower cost, and enabling faster imaging than the CCD sensor [3], CMOS image sensors have become the dominant technology in modern day consumer electronics such as smartphones and digital cameras.

The first CMOS image sensors used passive pixel sensors (PPS). However, advancements in active pixel sensor (APS) technology, which differs from PPS by its inclusion of transistors within the pixel for direct photodiode signal amplification, enabled the APS to have significantly improved performance in low-light conditions and a higher signal-to-noise ratio [4]. As a result, despite its greater structural complexity, the APS is now the preferred choice for CMOS image sensors.

This project explores the circuit design, transient simulations, and integrated circuit (IC) layout of a CMOS-based APS array contained within a compact 2.5 mm × 2.5 mm chip using the Cadence design environment.

The primary goal was to maximize the photodiode area within each 10μm x 10μm APS pixel, improving light sensitivity, and to maximize the number of pixels that can be placed on a single chip, enhancing image resolution. The result is a highly compact imager-on-a-chip with a high pixel density and sensitivity to light, thus improving its optical performance.

The CMOS imager was developed in stages, with each component being individually designed and validated before being joined together to create the full imager-on-a-chip system. We first designed the circuit schematic and IC layout for a single 3-transistor active pixel sensor (3T-APS) pixel in Cadence, with an emphasis on maximizing the photodiode area to enhance light sensitivity. The pixel's performance was verified through transient simulations and waveform analysis. Alongside the main pixel, we also designed a custom shift register circuit to generate control signals for reset, row select, and column select, as well as a buffer circuit to amplify column readout. These components were then combined into a functional 4×4 pixel array complete with scanning control logic. Simulations of the 4x4 array confirmed correct signal propagation, accurate pixel responses to varying light intensity, and consistent readout behavior for each column. After successfully verifying the functionality of the 4x4, the design was scaled up a 248x248 pixel array. We also designed a correlated double sampling circuit to reduce fixed pattern noise.

This imager-on-a-chip system demonstrates the technological capacity for compact, high-resolution CMOS imagers, providing the foundation for future hardware fabrication and integration into electronic devices.

II. 3-Transistor Active Pixel Sensor

A. Schematic

The circuit schematic for the individual 3T-APS pixel was constructed in Cadence, following the design outlined by [5], and shown in Fig. 1(a). Each transistor performs a crucial function for the pixel. The source follower transistor is always on and buffers the photodiode voltage to the readout line. The reset and row select transistors act as a switches. When activated, the reset transistor charges the photodiode to a known reference voltage, establishing a consistent starting point for image capture. The row select transistor controls the connection of the source follower's output to the column readout bus, ensuring that only one row of pixels is read at a time. The complete pixel circuit was wrapped in a symbol in Cadence for easier testing and further implementation.

Fig. 1(b) shows the testbench circuit used to verify the functionality of the 3T-APS pixel. The reset and row select signals are driven by voltage sources. To replicate the behavior of a photodiode, a current mirror biased to generate 1 pA is

connected to the pixel's input node, along with a capacitor to ground. This configuration produces a decaying voltage signal that reaches its maximum value when the reset signal is turned to high, effectively mimicking the discharge behavior of a photodiode in response to light. A second current mirror is used to sense the output of the pixel for analysis.

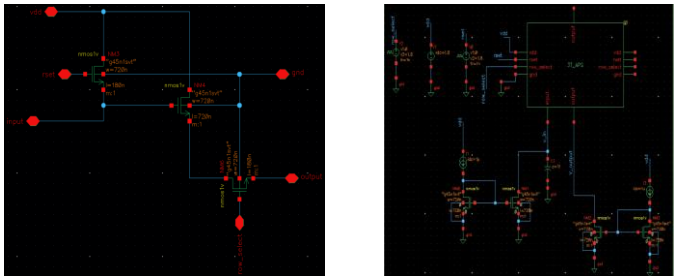
B. Simulation

The transient simulation pictured in Fig. 2 confirms that the 3T-APS functions as expected. When the row select signal is high, indicating that pixels in the selected row are being read, the output of the 3T-APS accurately follows the emulated input signal, demonstrating successful readout. When the row select signal is low, the output drops to zero, indicating correctly that the pixel is not actively being accessed.

C. Layout

After validating the 3T-APS pixel circuit, we used the schematic to design the layout of a single pixel, shown in Fig. 3. Each pixel was constrained to a 10µm x 10µm area. To maximize photodiode size, thereby improving low-light performance, the transistors were concentrated in the upper right corner of the layout, strategically leaving the majority of the area available for the photodiode. We additionally had wires running the full vertical and horizontal lengths so that it would allow our 3T-APS to be tile able for when we created our 4x4 layout.

As specified in the guidelines, the source follower transistor was 720 nm x 720 nm and the switching transistors were 720 nm x 180 nm. These transistors were strategically placed to minimize the area spanned and enable compact routing. The various rails were placed on the edges of the pixel layout to be both easily accessible by the transistors as well as being space efficient for the photodiode. This also enabled sharing across the components, reduced electrical noise, and supported seamless integration into larger arrays. When placing metal layers, we took special care to minimize crossover and keep interconnection lengths short, reducing parasitic capacitance and resistive delays. Through continuously refining the layout after running design rule checks (DRC) and layout-versus-schematic (LVS) verification, the resulting final layout has a fill factor of 90.36% while adhering to CMOS IC layout standards.



(a) (b)

Fig. 1. 3T-APS circuit schematic (a) and 3T-APS testbench (b) in Cadence.

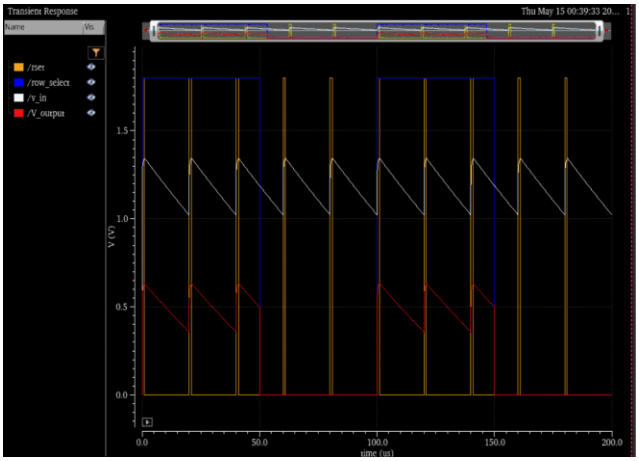


Fig. 2. 3T-APS testbench simulation in Cadence

III. 4X4 ACTIVE PIXEL SENSOR ARRAY

A. Schematic

Scaling up, 16 APS pixels were arranged in a 4x4 array. Pixels in the same row share reset and row select lines, while pixels in each column share a common output line for selected pixels to transmit their signals. To evaluate the functionality of this array, a comprehensive testbench was created, as shown in Fig. 4.

Custom-designed CMOS D flip flops, shown in Fig. 5(a), are connected to create shift registers responsible for controlling the reset, row select, and column select signals. To ensure accurate and reliable readout, we chose to connect each column output to a custom-designed CMOS buffer, as shown in Fig. 5(b). These buffers amplify the pixel output signal and minimize signal degradation caused by the loading effect of additional pixels connected to the same column line.

Together, this system facilitates independent and accurate readout of all 16 pixels, demonstrating its potential for scalability into larger CMOS image sensor arrays.

B. Simulation

To simulate varying light intensities across the pixel array, each column of pixels was connected to a current mirror that controlled the input current, like described in Section II. The input current increased in 10 nA increments from pixel to pixel, starting at 10 nA and from top to bottom, left to right, increasing up to a maximum of 160 nA.

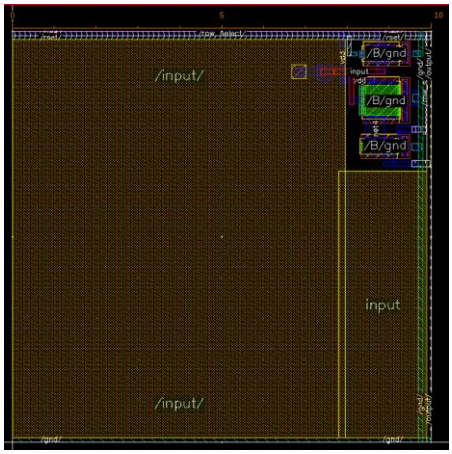


Fig. 3. 3T-APS Layout with a fill factor of 90.36%

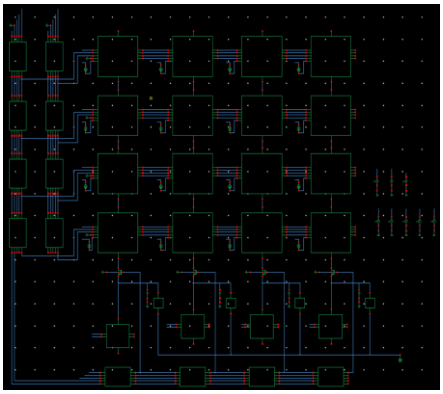
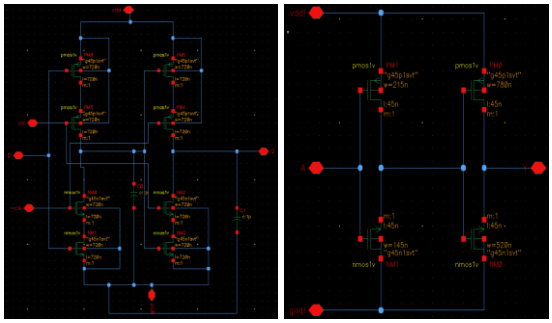


Fig. 4. 4x4 APS Pixel Array testbench circuit



(a) (b)

Fig. 5. Circuit schematic for a D flip flop (a) and one buffer (b).

The simulation results confirm the correct functionality of the 4x4 APS array. As depicted in Fig. 6(a), after all 4 rows have been reset, when a specific row is activated, four corresponding column select signals are enabled in order, allowing the outputs of the four pixels in that specific row to be read one by one. A pixel's output is only read when both its row and column are selected. After all 16 pixels have been read, the sensor is reset: the reset signal follows the same pattern as the reading where it goes through and individually resets the pixels for all four rows, reinitializing the pixel voltages for the next readout cycle. The shift registers that control the reset, row-select are driven by one clock, and the column-select signals are driven by another, enabling the control lines to activate sequentially, one at a time, for each row and column.

Furthermore, Fig. 6(b) shows each pixel producing a distinct output matching the applied input current, confirming both the intended pixel behavior and that the scanning system is successfully reading the outputs from all 16 individual pixels.

C. Layout

The previously designed 10µm x 10µm pixels were placed in a 4x4 formation which did not require any wiring between the pixels as they were designed to be connected in an array. The D flip flops, shown in Fig. 7(a), were also strategically designed so that they would not require any wiring between them and the PMOS and NMOS transistors were placed to minimize layout area while ensuring efficient routing of shared connections and signal integrity. We used 720 nm x 720 nm transistors, and the design passed DRC and LVS.

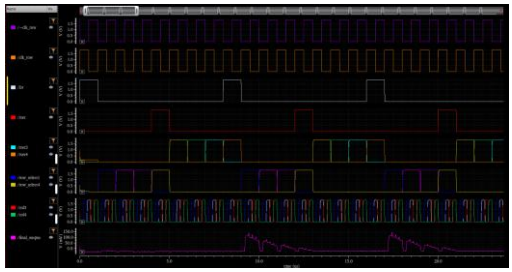
Twelve D flip flops were combined to create the three shift registers, and the completed 4x4 APS pixel layout and scanning system, passing DRC and LVS, is shown in Fig. 7(b).

IV. Complete 2.5mm x 2.5mm Imager

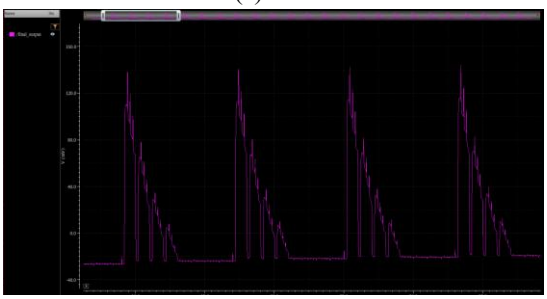
After verifying the functionality of the 4x4 APS pixel array, the design was expanded by adding additional rows and columns of pixels until the entire 2.5 mm x 2.5 mm chip area was utilized. The final implementation features a 248 x 248 pixel array, more than 61 thousand individual pixels. The layout of this chip is shown in Fig. 8. The complete design meets all space constraints and passes DRC.

V. Extra Credit: Correlated Double Sampling

To reduce fixed pattern noise (FPN) caused by pixel-to-pixel variations in the CMOS read-out path, we added a correlated double sampling (CDS) circuit [7], shown in Fig. 9(a), to each column. This circuit samples each pixel twice: once immediately after reset and once at charge integration. The differential amplifier in Fig. 9(b) subtracts the reset-level sample from the signal-level sample, cancelling the offset component of FPN and improving image uniformity. The overall schematic shown in Fig. 10 produced a less noisy output when compared to Fig. 6a.

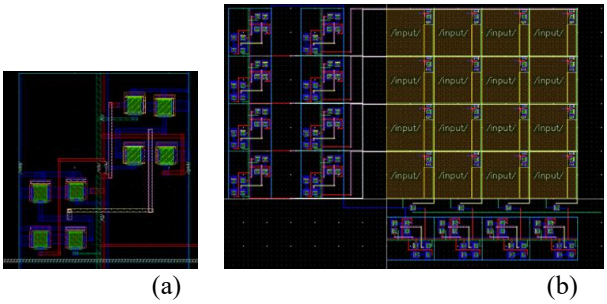


(a)



(b)

Fig. 6. Full simulation for the 4x4 APS array (a) and just the output signal (b)



(a) (b)

Fig. 7. Layout of a D flip flop (a) and the 4x4 APS pixel array with scanning system (b)

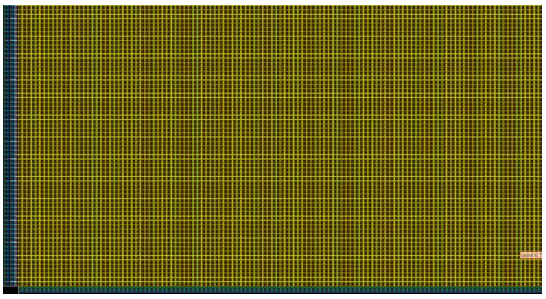
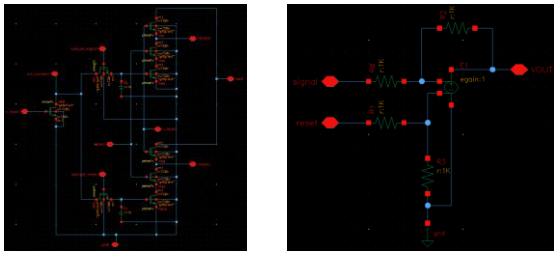


Fig. 8. Snapshot of 248x248 pixel chip layout (entire file too large to view)



(a) (b)

Fig. 9. Correlated double sampling circuit (a) and differential amplifier (b)

Another way to further improve signal-to-noise ratio and reduce FPN was to implement an inverting amplifier with a capacitive differencing circuit for each column. This circuit also samples each pixel output twice, once after reset and once after integration, and amplifies the difference, where the gain is set by the ratio of the two capacitors, as described in [8].

VI. Results and Conclusions

The final 248x248 pixel array fits within a 2.5mm x 2.5mm chip area and has both high pixel density and sensitivity to light. These results emphasize the effectiveness of our design approach and confirm that high-resolution CMOS image sensors can be successfully implemented within strict area constraints, laying the groundwork for future fabrication.

VII. Global Impacts of IC Design

Advancements in microprocessor design continue to prioritize maximizing computing power and efficiency through innovations such as multi-core systems, pipelining, parallel processing, and specialized hardware accelerators [6]. At the same time, continuing reductions in transistor size, combined with advancements in IC fabrication technologies, allow for more transistors than ever to be packed on a single chip, enabling faster processing speeds and improved energy efficiency.

However, these technological breakthroughs come at the expense of our environment. IC fabrication is highly resource-intensive, demanding significant quantities of energy, water, and hazardous chemicals, and contributing significant greenhouse gas emissions. Additionally, improper disposal of electronic devices introduces non-biodegradable materials, such as the silicon from integrated circuits, into the environment, while toxic metals like mercury can leach into the soil and waterways.

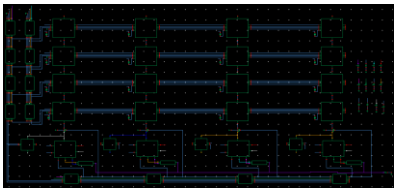


Fig. 10. Correlated double sampling ciruit implemented into schematic

VIII. Engineering Ethics

Throughout this project, we strived to adhere to the IEEE Code of Ethics by prioritizing honesty, transparency, and responsibility in all aspects of our design and presentations. For each deliverable, we presented only results we had directly achieved and remained open and honest about limitations in our design to avoid misrepresenting our progress. All team members collaborated closely and contributed equally (33% each) to all parts. We would like to give special recognition to Rocia for addressing key issues in the 4x4 schematic, Lucas for troubleshooting the layout, and Caroline for finalizing the presentation material. We also received valuable guidance from our mentors, whose support is acknowledged below.

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