HGCAL ELink Mapping Rules And Schema - Update

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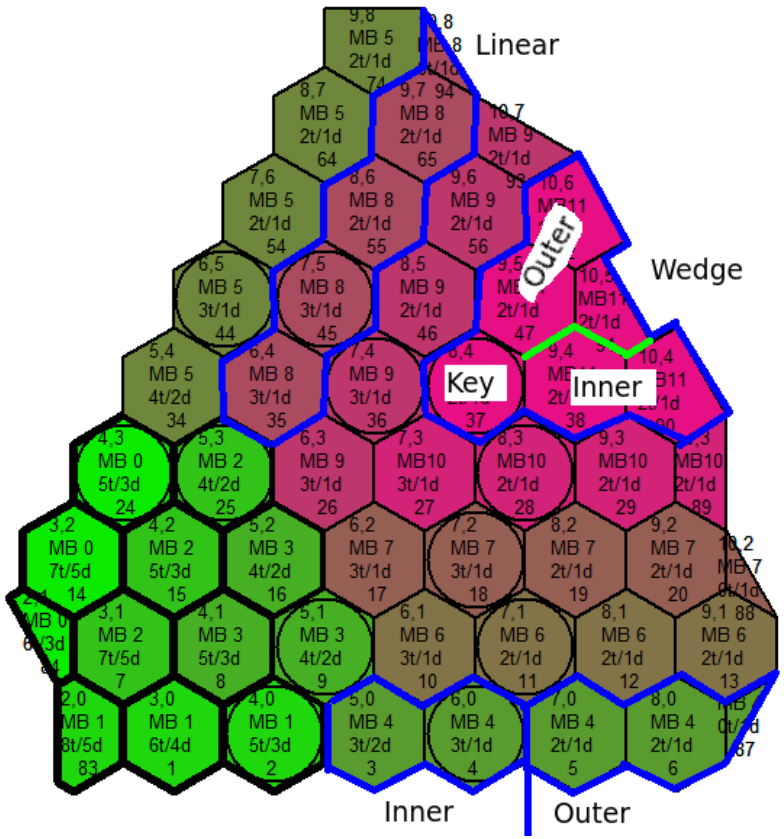
18^{th} February 2020

Allocation Algorithm

LD-MotherBoards

- The allocation was done by Paul R.
  - the LD-WagonBoard branches are termed "Inner" and "Outer" based on the radius
- "Linear" Type MotherBoard Organisations:
  - The LD-HexModules are ordered by increasing radius
  - triangles are considered part of the adjacent "FO" module
  - the position of the HD-EngineBoard is then swept through all positions
  - link counts for each side of the LD-EngineBoard are summed
  - no flexibility in the LD-Engine is assumed
    - elinks cannot be switched from one side to the other
  - a valid split is then one that respects the number of DAQ and Trigger inputs
  - then the differences between valid splits are calculated
    - smallest one chosen (best BW balance between inner and outer branches)
    - if there are two equivalient placements, the one closest to the centre is chosen
- "Wedge" Type MotherBoard Organisation:
  - The LD-HexModules are ordered counter-clockwise
  - The inner-most LD-HexModule (the "key") is selected as the split
  - The "Bottom" branch is chosen as "Outer" and "Upper" branch as "Inner"
  - the LD-EngineBoard is placed either side of the Key and configuration checked

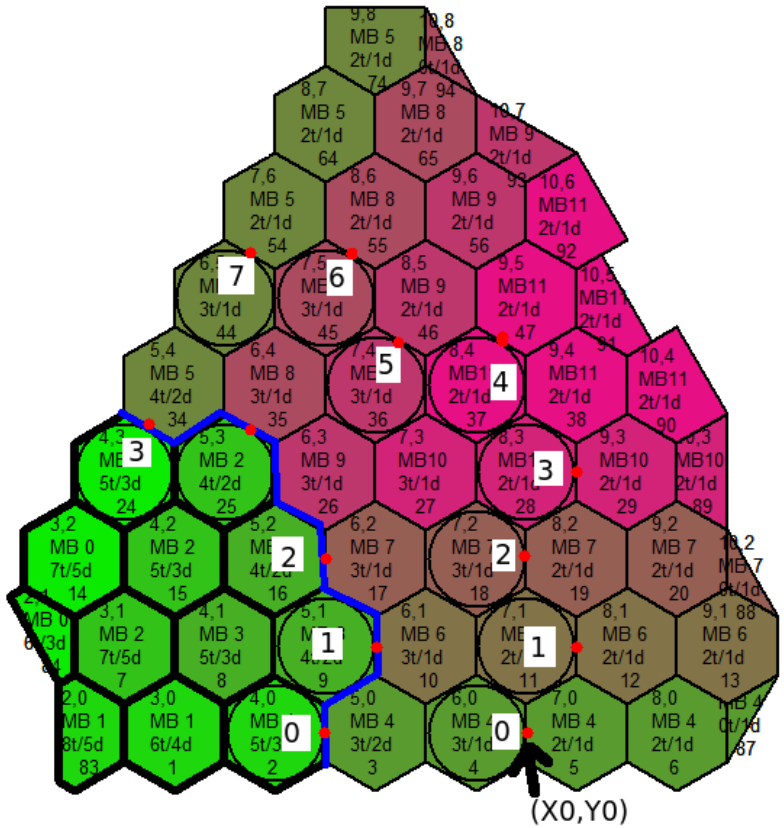


HD-MotherBoards

- The allocation was done by Paul R.
  - LD-HexModules assigned to HD-MotherBoards are converted to HD-HexModules
  - See Spec Doc for counts
- "Linear" Type MotherBoard Organisations:
  - The HD-HexModules are ordered by increasing radius
- "Wedge" Type MotherBoard Organisation:
  - The HD-HexModules are ordered counter-clockwise
- All HD-HexModules are considered as "Inner"

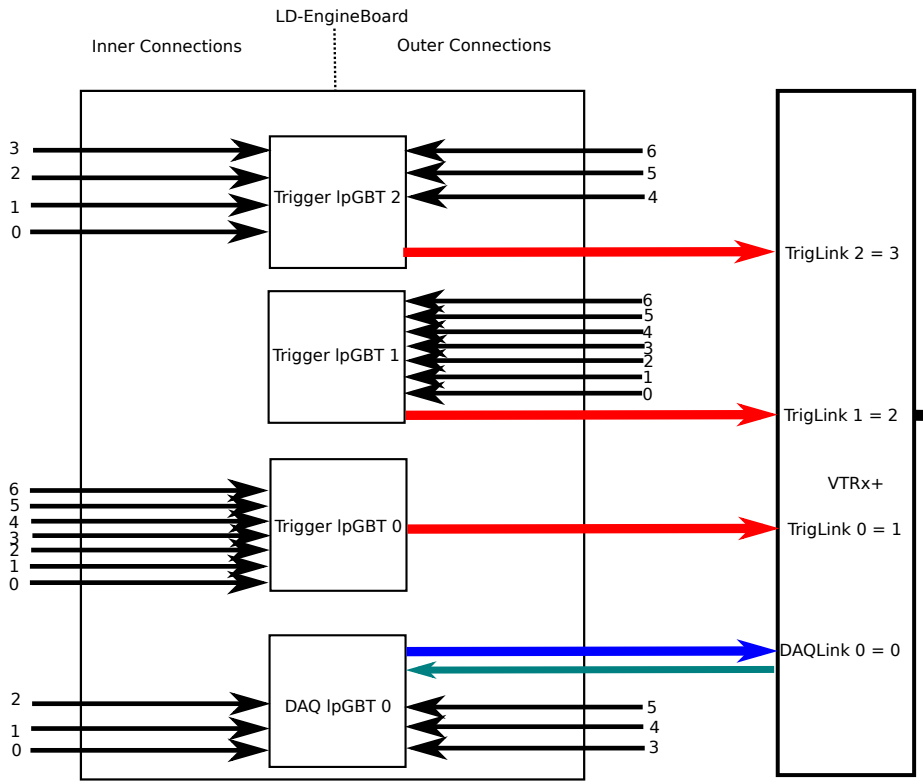
MotherBoard Labeling/Numbering Scheme

- Scaleable for entire detecctor
  - EndCap: Z+/Z-
  - Layer: 1-50
  - Cassette: 0-5
  - MB Index: Counter clockwise increment from cassette "bottom" edge
  - Type: HD = high density ; LD = Low Density
    - HD.1 = 1 VTRx+ fitted; HD.2 = 2 VTRx+ fitted
    - LD.1 is the only option
  - Organisation: L = Linear ; W = Wedge
  - Approximate (X,Y) position calculated
    - Nearest HexModule centre displaced by "Flat-To-Flat/2" outwards
    - centre of the next outer flat edge at the appropriate angle
    - Red dots show this
  - Example:
    - Z-,1,0,3,HD.2,L,(460.46 507.52)



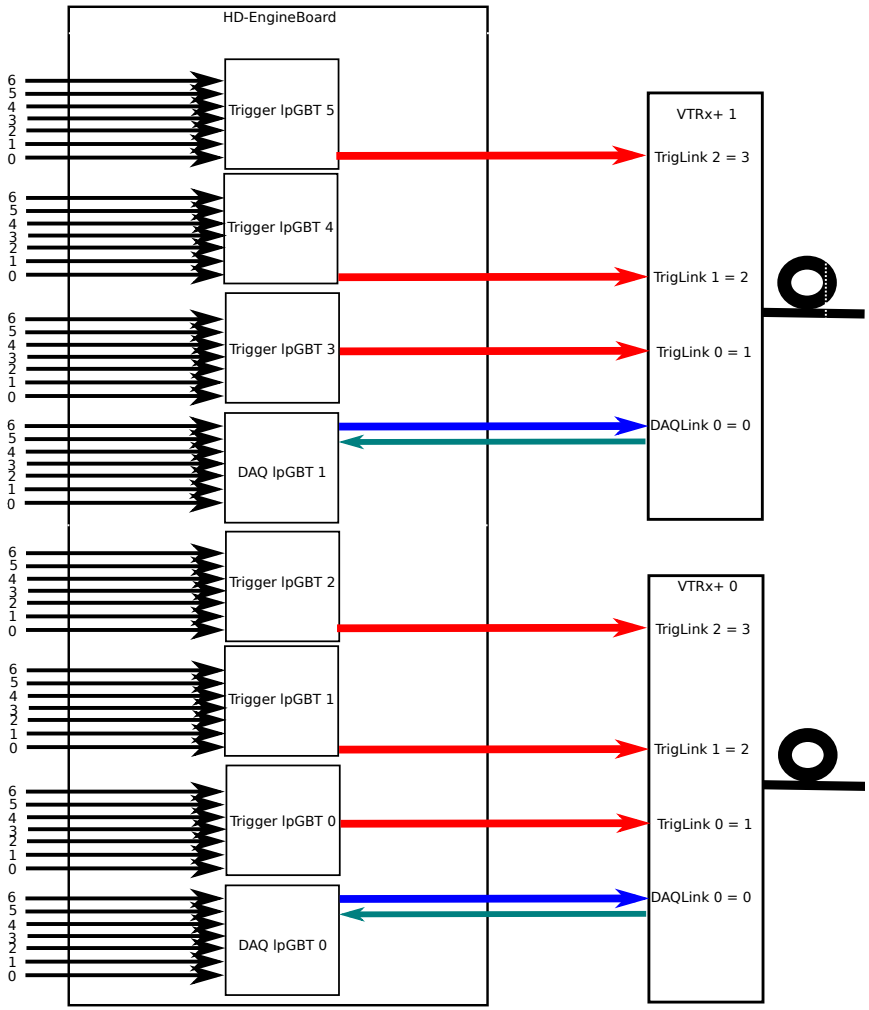
LD EngineBoard Architecture and Link Ordering

- Assumed no flexibility to select which elinks go to which side
- 6 available DAQ elinks allocated 3 per side
  - Inner: 0,1,2
  - Outer: 3,4,5
- 7 available trigger links available per Trig lpGBT
  - Trig lpGBT 0 : Inner elinks 0-6
  - Trig lpGBT 1 : Outer elinks 0-6
  - Trig lpGBT 2 :
    - Inner elinks 0,1,2,3
    - Outer elinks 5,6,7
- Allocation to LD-HexModules: DAQ
  - Starting at inner-most:
    - allocate number required for each HexModule lowest index first
- Allocation to LD-HexModules: Trigger
  - Inner: allocate from TriglpGBT0 first, when full, allocate from TriglpGBT2 elinks 0,1,2,3
  - Outer: allocate from TriglpGBT1 first, when full, allocate from TriglpGBT2 elinks 4,5,6
- VTRx+ fibre allocations:
  - DAQ link 0 $\rightarrow$ fibre 0
  - Trig link 0 $\rightarrow$ fibre 1
  - Trig link 1 $\rightarrow$ fibre 2
  - Trig link 2 $\rightarrow$ fibre 3



HD EngineBoard Architecture and Link Ordering

- assumed that VTRx+1 (2nd one) will only be fitted where necessary
- Allocation: DAQ
  - inner-most HD-HexModule assigned to lowest elink in DAQlpGBT0
  - moving out, the links are allocated in increasing index
  - when complete, VTRx+1 is assumed to be fitted and elinks from DAQlpGBT1 are allocated
- Allocation: Trigger
  - inner-most HD-HexModule assigned to lowest elink
  - moving out, the links are allocated in increasing index:
    - TriglpGBT0 elink 0,1,..6 ; then TriglpGBT1 elink 0,1,..6 ; etc
  - when VTRx+ complete, VTRx+1 is assumed to be fitted
- VTRx+ fibre allocations:
  - DAQ link 0 → VTRX+0 fibre 0
  - Trig link 0 → VTRX+0 fibre 1
  - Trig link 1 → VTRX+0 fibre 2
  - Trig link 2 → VTRX+0 fibre 3
  - DAQ link 1 → VTRX+1 fibre 0
  - Trig link 0 → VTRX+1 fibre 1
  - Trig link 1 → VTRX+1 fibre 2
  - Trig link 2 → VTRX+1 fibre 3



Overview

- output of mapping software is a text file with some punctuation for ease of reading
- each motherboard mapping fits on a single line
  - There are some long lines in the file
- 3 main fields:
  - MB description field
  - Inner WagonBoard description field
  - Outer Wagonboard description field
- for the HD cases, there is no Outer WagonBoard field.
- structure of inner and outer WagonBoard fields is the same
- main fields are separated with a pipe character "|"

EngineBoard Field

- there are 7 comma separated variables:
  1. EndCap: either Z- or Z+ (only Z- exists at the moment)
  2. Layer: 1 - 50 inclusive
  3. Cassette: 0 - 5, but currently only 0 qand 1 exist
  4. MotherBoard Index integer: incrementing with Engine azimuth
     - see slide 5
  5. MB type: HD.1, HD.2, LD.1
     - the number indicates how many VTRx+ are fitted
  6. MotherBoard "Organisation": L for Linear, and W for Wedge shaped.
  7. the motherboard approximate origin as (X0 Y0) [2 floats]
- some examples are opposite

```
|Z-,1,0,3,HD.2,L,(460.46 507.52) |
|Z-,1,0,0,HD.2,L,(753.48 0.00) |
|Z-,1,0,2,HD.2,L,(627.90 507.52) |
|Z-,1,0,1,HD.1,W,(837.20 145.01) |
|Z-,1,0,0,LD.1,L,(1088.36 0.00) |
|Z-,1,0,7,LD.1,L,(627.90 797.54) |
|Z-,1,0,1,LD.1,L,(1172.09 145.01)|
|Z-,1,0,2,LD.1,L,(1088.36 290.02)|
|Z-,1,0,6,LD.1,L,(795.34 797.54) |
|Z-,1,0,5,LD.1,L,(879.06 652.53) |
|Z-,1,0,3,LD.1,L,(1172.09 435.02)|
|Z-,1,0,4,LD.1,W,(1423.25 580.03)|
|Z-,2,0,0,HD.2,L,(753.48 0.00) |
|Z-,2,0,3,HD.2,L,(460.46 507.52) |
```

WagonBoard Field

- a designator at the start indicates inner (I:) or outer (O:)
  - there is no O: for HD
- A list of HexModules and connections is then enclosed in square braces
- The HexModule ID is followed by an arrow and then curly braces, which enclose the list of connections
  - I:[(HM desc) -> {D:(DAQ list) T:(TRIG list)}; (HM)->{D:(DAQ list) T:(TRIG list)}]
- DAQ connections start with a D: and Trigger with a T:
  - the lists are comma separated and enclosed in parentheses

I:[(FM.0.5.4) -> D:(0.0.0.0, 0.0.0.1) T:(0.1.0.0, 0.1.0.1, 0.1.0.2, 0.1.0.3);(FM.0.6.5) -> D:(0.0.0.2) T:(0.1.0.4, 0.1.0.5, 0.1.0.6)]
I:[(FM.0.6.1) -> D:(0.0.0.0) T:(0.1.0.0, 0.1.0.1, 0.1.0.2);(FM.0.7.1) -> D:(0.0.0.1) T:(0.1.0.3, 0.1.0.4)]
I:[(FM.0.6.2) -> D:(0.0.0.0) T:(0.1.0.0, 0.1.0.1, 0.1.0.2);(FM.0.7.2) -> D:(0.0.0.1) T:(0.1.0.3, 0.1.0.4, 0.1.0.5)]
I:[(FM.0.6.4) -> D:(0.0.0.0) T:(0.1.0.0, 0.1.0.1, 0.1.0.2);(FM.0.7.5) -> D:(0.0.0.1) T:(0.1.0.3, 0.1.0.4, 0.1.0.5)]
I:[(FM.0.6.3) -> D:(0.0.0.0) T:(0.1.0.0, 0.1.0.1, 0.1.0.2);(FM.0.7.4) -> D:(0.0.0.1) T:(0.1.0.3, 0.1.0.4, 0.1.0.5)]

HexModule Descriptor Field

- The HexModules are specified by a string with 4 fields separated by a "."
  1. the module descrption string (FI,FM,a,...)
  2. rotation index 0-5
     - note that these are currently all 0 $\rightarrow$ awaiting confirmation from Paul R.
  3. Module u coordinate
  4. Module v coordinate
- (FM.0.6.1)
  - designates a full LD-HexModule in position (u,v) = (6,1)

Connection Descriptor Fields

- The connection list is a comma separated list of strings with 4 numbers
- each string has 4 fields separated by a "."
- each connection contains:
  1. VTRx+ index
     - always 0 for LD, 0 or 1 for HD
  2. VTRX+ Fibre index
     - 0 for LD DAQ link
     - 1,2,3 for trigger link
  3. lpGBT:
     - 0 for LD DAQ ; 0 or 1 for HD DAQ
     - 0,1,2 for LD trigger link; 0,1,2,3,4,5 for HD trigger links
  4. eLink index
     - DAQ (see opposite)
     - Trigger (see opposite)

- DAQ eLink Indices:
  - 0,1,2 for Inner LD case, 3,4,5 for outer LD case
  - 0 - 6 for HD DAQ case
- Trigger eLink Indices
  - 0,1,2 for Inner LD case, 3,4,5 for outer LD case
  - 0 - 6 for HD DAQ case

Example:

(HexModule) -> {D:(0.0.0.1) T:(0.1.0.3, 0.1.0.4, 0.1.0.5)}

Notes and Special Cases

- Even layers have no trigger connectivity
  - Even layers have no trigger connectivity
  - this is an empty list: e.g. (FI.0.5.3) -> {D:(0.0.0.0, 0.0.0.1) T:()};
- c0 modules (triangles) have no connectivity
  - this is assumed to be passed through the neighbouring FO module
  - e.g. (cO.0.10.3) -> {D:()}

Comments: Jim Hirschauer

- Add rates and occupancies to the mapping file
  - this is possible and relatively easy
- VTRX+ Fibre index: index within the pigtail bundle
  - always 0 for DAQ, 1,2, or 3 for TRIG
- ModMap.xlsx file: 18th December 2019
  - I will add this to the collection of files
  - differences in counts between this and 8th November to be ivestigated
- The numers on slide 12
  - These are maximum possible ranges, not what occurs in the mapping file

Comments: Paul Dauncey

- Format typo on slide 5 $\rightarrow$ fixed in this file
- Are all elinks used for any active lpGBT?
  - I haven't had time to understand this question
- My allocation rules give cases where the data are unnecessarily split over multiple lpGBTs
  - I will refine the allocation rules and come back with another one

Comments: Danny Noonan

- Empty Outer LD-WagonBoard in layer 34
  - origin is an incorrect allocation in Paul R's original mapping file (a "clicko")
  - to be revised
- Made his parser available
  - https://cernbox.cern.ch/index.php/s/e5IR3WQ1SIAMnk0

Outlook

- Thank you for all the quick and detailed feedback!
- Files can be downloaded here:
  - https://cernbox.cern.ch/index.php/s/qn3LGuhTCZP6QIb
  - (including Modmap and this file)
- I will come back to this next week.
  - Please feel free to look and comment