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SPECIFICATION

HGCAL SILICON MODULE DAQ AND TRG ARCHITECTURE SPECIFICATION

ABSTRACT:

DOCUMENT PREPARED BY:	DOCUMENT TO BE CHECKED BY:	DOCUMENT TO BE APPROVED BY:
Paul ASPELL(CERN) Philippe BLOCH(Imperial College) Jim HIRSCHAUER(FNAL) Matthew NOY(CERN) Paul M. RUBINOV(FNAL)	Dave BARNEY(CERN) Karl GILL(CERN) André DAVID(CERN) Matthew NOY(CERN)	

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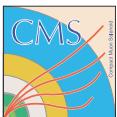
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REV. NO.	DATE	PAGES	DESCRIPTIONS OF THE CHANGES
0.1	2019-12-10	6	Working Snapshot
0.2	2020-02-28	6	Read-Through
0.3	2020-04-05	6	Post Read-Through Release
0.4	2020-04-21	6	Release with PR's comments



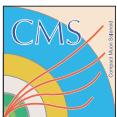
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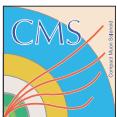
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1 Introduction

1.1 Scope

The scope of the system baseline task force is defined as a series of prioritised tasks. These are detailed in table 1. The completion of task force activities is limited to items with a designated priority of 1 or 2.

Order	Description	Assignment
1	Detail for 1 or 2 layers <ul style="list-style-type: none"> - Counts and types of Engines and Wagons - Schematic (inter-connectivity) - Detail of the e-links allocation for the TPG "Threshold" option. - Placement of ECONs, SCAs, IpGBTs - DCDC placement and associated connector/mechanical aspects 	PR,MN
1	Small 3 pcb stack mockup <ul style="list-style-type: none"> All layers - Engine / wagon drawing for all layers - Number of types of Engine and Wagons. - Number of components 	PR
2	CAD model to prepare for cassette mechanical mockup	PR,MN
3	Detailed mockup of cassette from CAD model	PR
3	Common Altium repository for each layer <ul style="list-style-type: none"> Based on power estimate of all components 	PR
3	<ul style="list-style-type: none"> - Define cabling (with PWG) - Define grounding Scheme (with PWG) 	PR,MN,PWG
3	Optical link definition, patch panels, and fan-outs	AS
3	Unit costs and counts required to calculate total on-detector electronics cost	PR,MN

Table 1: System Baseline Task Force Scope and Priorities

1.2 Time Line

The Task Force activities were originally scheduled to run from mid-August 2019 to the end of October 2019. At the end of this period, some time was given to document the progress and design decisions taken, and also put in place the working structures necessary to carry the project forwards.

1.3 Review Process

At present, there is no external formal review of the document in place to judge the process. However, throughout the duration of the task force activities, a continuous process of meetings ensured that there was constant contact between internal members of the process.

2 Data Rates

The determination of data (both DAQ and Trigger) rates requires two main ingredients:

- the multiplicities of cells (or of trigger cells above threshold) in an event
- the data format, to translate the multiplicity into a number of bits.

The multiplicities are obtained from full simulations in CMSSW. The (preliminary) data formats have been proposed as part of the task force by the FNAL group.

2.1 Trigger Data Rates

Trigger multiplicities have been obtained by Jean-Baptiste Sauvan using full CMSSW simulations based on the V10 geometry of the HGCAL. A neutrino gun sample with 200 pileup events has been used.

The generation includes previous bunch crossings, to take into account out-of-time pileup. The pulse shape is tuned to obtain 20% of the charge in the following bunch crossing. Trigger cells are sums of 4 or 9 sensor cells, for low density and high density modules respectively, in order to provide the same area for all trigger cells across the detector. Before the summation of sensor cells the ToT values are re-scaled to a LSB of about 0.1 fC, corresponding to the LSB of the ADC values. After summation, the trigger cell charges are compressed on a floating point format with 4 bits of exponent and 3 bits of mantissa.

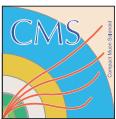
The multiplicities in each module are obtained by applying a threshold of $1.35 \text{ MIP}/\sin(\theta)$ on the trigger cells. The average values of these multiplicities in each module are computed, taking into account the 60 degree and forward-backward symmetries of the detector. The digitisation of the Front-End corresponds to **beginning-of-life** conditions, with a charge collection efficiency of 1. However, since the applied threshold is rather high and the noise of the 4(9) summed cells is assumed to be incoherent, the impact of the increased noise at end-of life should be small.

The CMSSW V10 geometry does not include the corner-centred geometry in CE-H, and therefore the positions of the modules are not the final ones. To correct for this, the trigger cells multiplicity of full modules obtained with V10 has been parameterised in each layer as a function of the radial position of the module centre, allowing us to correct for the position of the modules in the Tiling Geometry. In the case of the partials, the multiplicity is re-scaled to take into account the reduced area of the partial.

The data format used to translate multiplicity into bits is the one presented by Jim Hirschauer on August 13th (<https://indico.cern.ch/event/840129/>). Rates are obtained by multiplying the number of bits by the crossing rate of 40 MHz.

The number of e-links required to transmit the trigger data of the module is computed using the following procedure:

- the data rate is multiplied by 1.3, to take into account possible fluctuations. A check is done that this rate is not greater than the data rate corresponding to a "full" module with 48 trigger cells above threshold.
- the number of e-links is the number of 1.28 Gb/s links required to transmit this increased rate.
- the number of e-links should always be greater than or equal to 2, except for Halves and Semis where the minimum is 1 e-link
- the small triangles (Threes) are not included in the trigger (0 e-link).



2.2 DAQ Data Rates

DAQ multiplicities in the silicon sensors have been obtained by Pedro Silva using full simulations based on CMSSW-V11. The V11 geometry is very close to the geometry currently proposed for the sensors tiling [EDMS...]. In particular, it includes the corner-centred geometry for the CE-H cassettes. The only difference concerns the partials on the periphery.

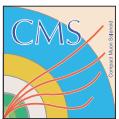
To be representative of L1 trigger events, $t\bar{t}$ events have been generated (over the whole phase space) with 200 pileup events. The generation includes previous bunch crossings, to take into account out-of-time pileup. The HGCROC front-end amplifier pulse shape is tuned to obtain 20% of the charge in the following bunch crossing. The digitisation of the Front-End corresponds to **end-of-life conditions** (3000 fb^{-1}) with the corresponding charge collection efficiency (CCE) and noise. At end-of-life, the noise is dominated by the shot noise due to leakage current in the cell, and the leakage current has been computed using a parameterisation of the 1-MeV-neutron-equivalent fluence as a function of radius, based on the FLUKA BRIL model 3.7.15.9. The MIP is re-calibrated to take into account the reduced CCE. The gain of the HGCROC has been selected to have the MIP as close as possible to the target of 10 ADC channels per MIP.

A threshold of 0.5 MIP has been applied to all cells. The output of the simulation is a file giving the average (50% quantile) number of cells in each module (multiplicity). In the case of the partials, the multiplicity is re-scaled to take into account the difference between the numbers of cells in CMSSW and in the Tiling Geometry.

The data format used to translate multiplicity into bits is the one presented by Jim Hirschauer on September 10th (<https://indico.cern.ch/event/846568/>). Since then, small modifications of the header section have been proposed for a better handling of errors, but the impact should be small. Data rates are obtained by multiplying the number of bits by the maximal average L1 trigger rate of 750 kHz.

The number of e-links required to transmit the module data is computed using the following procedure:

- the data rate is multiplied by 1.3, to take into account possible (Poisson) fluctuations. A check is done that this data rate is not greater than the data rate corresponding to a full module.
- the number of e-links is the number of 1.28 Gb/s links required to transmit this increased rate.



3 Trigger Algorithms

3.1 Threshold

3.1.1 Description

3.1.2 Link Count Implications

3.2 Best Choice

3.2.1 Description

3.2.2 Link Count Implications

3.3 Selection Criteria and Choice

4 Baseline Silicon Architecture Description

The architecture of the readout system for the silicon modules required a solution permitting the following constraints to be satisfied:

- a mixture of High-Density and Low-Density modules in a plane;
- irregular boundaries;
- large physical extent;
- congested services routing;
- fine pitch packaging for the IGBT;
- the radiation environment; and
- the large variation in data rates within a given layer.

This led to the design of an Engine-Wagon architecture. The basic principle relies on the design of a small "Engine" card, of which there are 4 variants, providing the interconnectivity required between the I/Os of the VTRx+ and those of the concentrator chips. The connections between the Engine board and the Hex Modules are made by Wagon PCBs. These are simple, low layer count PCBs, with very relaxed requirements on pitch and signal speed, that can be inexpensively manufactured in any shape necessary to provide the required connections. A given Engine/Wagon combination connects only to High-Density or Low-Density modules: no mixing of module types is possible. This constraint has caused some of the LD-HexModules on the boundaries between the HD and LD regions to be changed for HD-HexModules. Counts are included in section 4.12.9.

4.1 Low Density Interconnectivity

An overview of the LD connections is shown in figure 1.

The LD stack-up is shown in figure 2. There are multiple connectors shown in this figure, each of which is tailored to the use case. The connector shown for the VTRx+ is the standard one in the 2mm stack height. The VTRx+ PCB is 500 μ m thick, giving a total nominal height envelope of 2.5mm (note that tolerances are not included in this). The bPOL12V-based DCDC converters mounted on the LD-EngineBoard are shown as a fully integrated solution, however a mezzanine-style solution is also a possibility.

Table 2 summarises the signals between the (single) LD-EngineBoard and the LD-WagonBoards. Note that there will be a pair of such connectors per LD-WagonBoard: one for the InnerWagon and one for the OuterWagon.

Provision for 4 connections to LD-HexModules was initially included to cater for the "cO" (triangular) modules at the outer periphery. As these will be an integral part of the neighbouring "FO" module (called "F+cO"), control and data acquisition will be done through the standard connectors to the LD-WagonBoard and the concentrator mezzanine card, this has been reduced to 3 such connections per LD-WagonBoard and the signal counts in the connectors between the LD-HexModule and the LD-WagonBoard adapted accordingly.

The signals connecting the LD-HexModule to the LD-WagonBoard are listed in table 3. The connector selected for this is currently an 80 pin DF12 in a 3.5mm stack height variant.

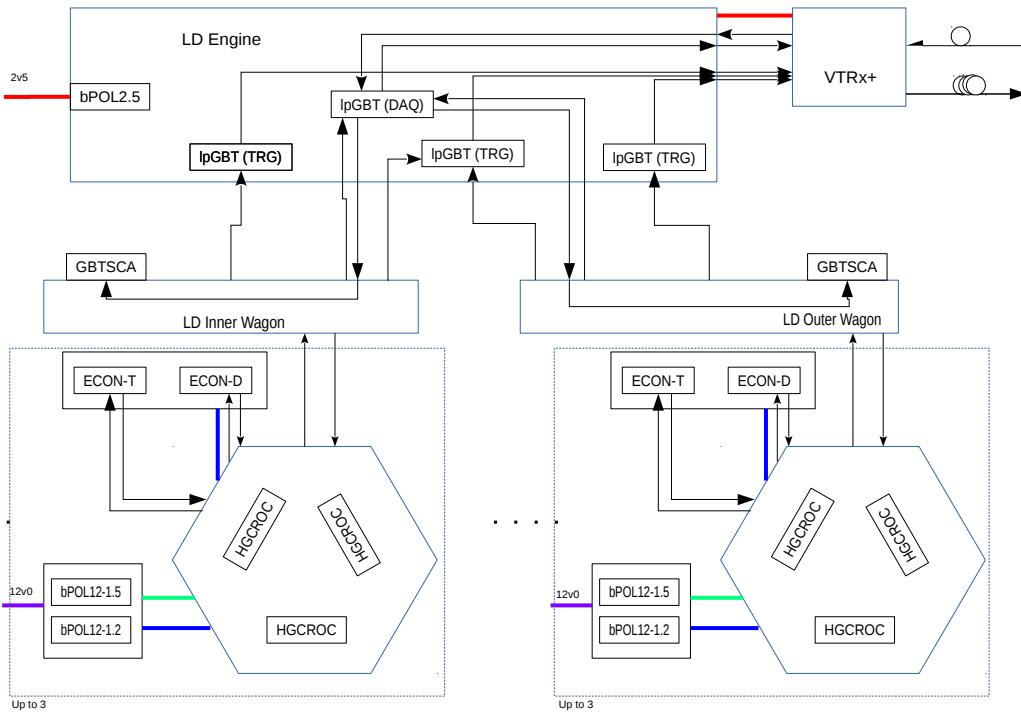


Figure 1: An overview of the connections between LD-HexModules, LD-WagonBoards, LD-EngineBoard and VTRx+ in the Low-Density regions.



Figure 2: The Low-Density PCB Stack-up. Only one LD-WagonBoard is shown for simplicity.

4.2 LD-EngineBoard

In the LD region, an LD-EngineBoard connects to 2 LD-WagonBoards, referred to as the Inner- and Outer LD-WagonBoards due to the radial nature of the envisaged tiling. Signals are relayed to and from the counting room via optical links connected to the VTRx+. There are 4 IpGBTs operated in 2 different modes: a single DAQ IpGBT, operated as a (FEC5) transceiver, for the DAQ data and both the slow and fast control subsystems, and up to 3 Trigger IpGBTs, operating in (FEC5) Simplex TX mode. A reduced-functionality prototype version of this card has been designed at Minnesota and is under test at the time of writing. It is foreseen to operate the DAQ IpGBT in self-reference mode in which the clock generator block derives its 40MHz reference clock from incoming data stream. The Trigger IpGBTs will each be allocated one of the clocks from the 29 available clock outputs.

4.2.1 LD Fast Control

The Fast Control is distributed through the down-link (direction: control room → detector) to the DAQ IpGBT running at approximately 2.5Gb/s. The VTRx+ has a single optical input to permit this

Eng ↔ WB	connector 0	connector 1	type	Padding GSSG	103 of 120	103 of 120	notes
CLK320	4	4	pairs	1.5	12	12	HGCROC clk; 1/HGCROC
FST_CMD_E2C	4	4	pairs	1.5	12	12	4 pairs; 1/HGCROC
SCA_EC_IN	2	2	pairs	1.5	6	6	HDLC Format
SCA_EC_OUT	2	2	pairs	1.5	6	6	HDLC Format
SCA_CLK	2	2	pairs	1.5	6	6	
SCA_RSTB	2	2	se	1	2	2	active low reset
PROBE_DC1	1	1	ana	1	1	1	Wagon power monitoring
PROBE_DC2	1	1	ana	1	1	1	
SCA_GPIO	1	1	se	1	1	1	GPIO signal
GLB_ERR	1	1	se	1	1	1	spare error path
DAQ_ELNK	3	3	pairs	1.5	9	9	1.28Gb/s DAQ
TRIG_ELNK	9	9	pairs	1.5	27	27	1.28Gb/s TRIG
VDDD_SCA_1v2	4	4	pwr	2	8	8	80mA
VDDA_SCA_1v5	1	1	pwr	1	1	1	3mA
DAC	2	2	ana	1	2	2	Scintillator test LED biasing
I2C_SDA_eFUSE	1	1	se	1	1	1	IpGBT setup during production
I2C_SCL_eFUSE	1	1	se	1	1	1	Production only.
IpGBT_Reset	1	1	se	1	1	1	Used for production only.
efuse_power	1	1	pwr	1	1	1	
GPIO_TEST_RST_EN	2	2	se	1	2	2	Scintillator production tests

Table 2: LD-EngineBoard to LD-WagonBoard connector signals.

connection. The DAQ IpGBT has 16 down-link output pairs. These are organised into 4 groups of 4 outputs and share the bandwidth available. The clock and fast control links to the Concentrator ASICs (ECON-D and ECON-T) and HGCROCs run at 320MHz and 320Mb/s respectively¹. Operated at this speed, there are 4 independent outputs. These can be mirrored permitting 4 possible partitions each with 4 possible separate output drivers. It isn't yet clear whether this level of partitioning will be used in the detector. The maximum number of outputs required is linked to the number of LD-HexModules connected to a LD-WagonBoard. The clock-320 and fast-control are to be fanned out by the ECON-D, thus these signals pass from the DAQ IpGBT through the LD-WagonBoards to the LD-HexModule, through the Concentrator Mezzanine connector to the ECON-D. The ECON-D is being designed with a 1:6 fan-out (see section 4.6.4) module in it and thus will duplicate both the clock-320 and the fast-command signals permitting their subsequent point-to-point distribution to the HGCROCs through the connector, and the ECON-T when fitted to the mezzanine card for the layers participating in the trigger.

The HGCROC derives the phase of the 40MHz clock from the encoding of the fast command signal. This scheme is detailed in figure 3.

4.2.2 LD Slow Control and Monitoring

Slow control and slow monitoring is foreseen via the IpGBT and GBTSCA chipsets through the External Control link. This is an 80Mb/s full-duplex data stream intended for use as a dedicated slow control and monitoring pathway. As it isn't possible to gang GBTSCA chips together and one is required on each of the Inner and Outer LD-WagonBoards, one of the e-port downstream channels not in use for the fast-control interface will be divided down off detector by 1:4 bit-duplication (to give 80Mb/s) and one of the 7 upstream e-link ports operating at 1.28Gb/s will be used to recuperate the data sent via the

¹The actual speed is a multiple of 8 of the LHC clock.

Signal WB ↔ HB	51		GSS(G)	67 /80	Comments
CLK320	1	pairs	x1.5	3	
FST_CMD_E2C	1	pairs	x1.5	3	
DAQ_ELNK	2	pairs	x1.5	6	2 DAQ links: PR Confirms
TRIG_ELNK	4	pairs	x1.5	12	there should be 4 elinks for TRIG outputs
RESETB_HGCROC	1	se	x1	1	HGCROC Hard Reset: broadcast
RESETB_ECONT	1	se	x1	1	ECONT-T Hard Reset
RESETB_ECOND	1	se	x1	1	ECOND-D Hard Reset
HGCROC_ERR	4	OC	x1	4	HGCROC Error Signal
ECONT_ERR	1	OC	x1	1	ECONT-T Error Signal
ECOND_ERR	1	OC	x1	1	ECOND-D Error Signal
PWR_EN_DCDC	1	se	x1	1	Power Enable for DCDC
PG_DCDC	1	se	x1	1	Power Good for DCDC
PWR_EN_LDO	1	se	x1	1	Power Enable for the LDO
PG_LDO	1	se	x1	1	Power Good LDO
LDO_P50MV	1	se	x1	1	LDO output trim:+50mV
LDO_M50MV	1	se	x1	1	LDO output trim:-50mV
I2C_SDA	6	se	x1	6	ECONT; ECOND; HGCROCs(x4)
I2C_SCL	6	se	x1	6	ECONT; ECOND; HGCROCs(x4)
I2C_RST	2	se	x1	2	I2C Reset for ECONT+ECOND; I2C Reset for HGCROCs
PROBE_DC_I	4	ana	x1	4	probe connections to HGCROCs
PROBE_DC_V	4	ana	x1	4	probe connections to HGCROCs
MGND	1	ana	x1	1	SCA ADC GND reference
RTD	1	ana	x1	1	temperature measurement
RTD_REF	1	ana	x1	1	reference for temperature measurement
VMON_LVS	1	ana	x1	1	voltage monitor for LDO
VMON_DCDC	2	ana	x1	2	Monitor voltage for DCDC modules

Table 3: List of signals between the LD-HexModule and the LD-WagonBoard

return path. This represents a 16-fold oversampling of the EC serial stream, which shall be handled by the off-detector electronics. Each GBTSCA requires a source synchronous clock operating at 40MHz, which are to be provided by the clock outputs of the IGBT.

Note that the connector on each side of the LD-EngineBoard currently has 2 such sets of connections. This second set (per connector) is to provide connections for scintillator testing.

There are two GPIO connections for test and reset purposes per connector. Additionally, 2 analogue pins have been allocated through which voltages can be driven to permit bias tuning of the test LED.

The list of values to be monitored from the LD-HexModule is presented in table 3. Currently there are 17 such digital control and status signals listed. The GBTSCA has a total of 32 GPIO pins available: a maximum of 3 LD-HexModules per LD-WagonBoard means that 10 such signals are available per LD-HexModule. A scheme to common these together is currently under investigation to support the functionality required within the available resources. For now the signals to be monitored are represented as a black arrow in figure 4. The I2C connections are shown in purple. The I2C_SCL and I2C_SDA are enumerated separately as these connect to the dedicated interface of the GBTSCA. The analogue values to be measured are also shown in table 3: these currently number 14 individual signals per LD-HexModule. As the GBTSCA has 31 ADC inputs, giving 10 per LD-HexModule, a similar scheme to connect these

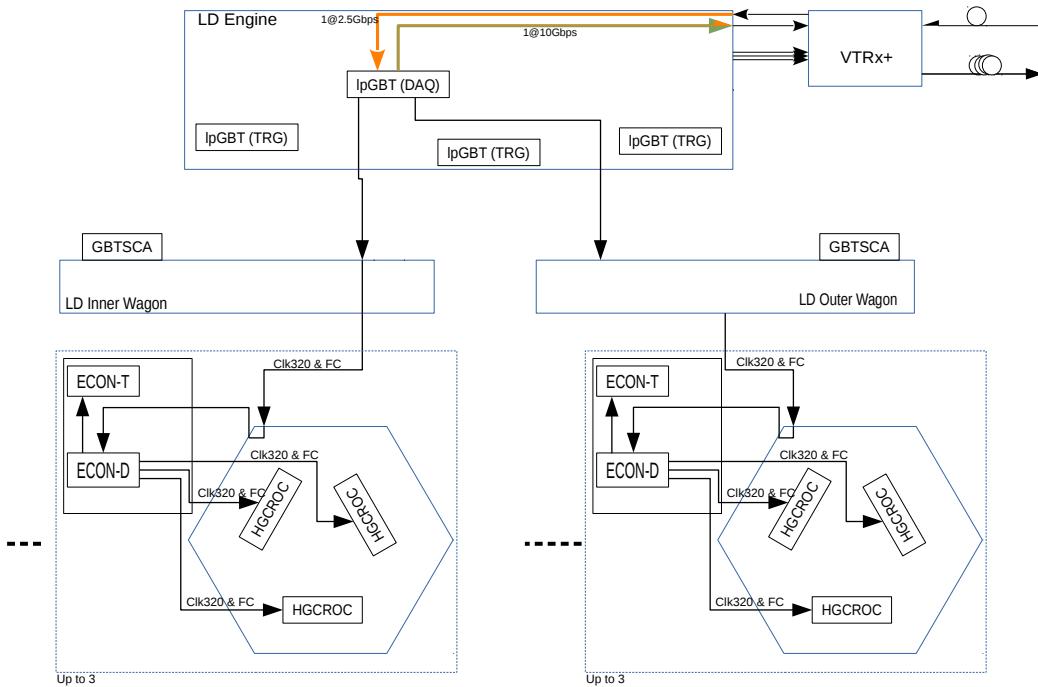


Figure 3: An overview of the Fast control connections from the VTRx+ through to the LD-HexModule for the Low-Density case.

signals together will be devised.

For the configuration of the HGCROC and ECON-D/T registers, I2C is foreseen. The GBTSCA has 16 independent I2C master interfaces. Dividing these equally by up to 3 LD-HexModules gives 5 each. The ECON-D/Ts and the HGCROCs both have 4 slave address select pins and thus up to 16 can be operated from a single I2C bus. However, both ECONs and LD-HexModules will be connected independently to allow configuration to proceed in parallel. The minority case where there are 4 HGCROCs on the LD-HexModule (thus there are 6 I2C targets on the LD-HexModule assembly) can be dealt with by connecting the extra HGCROC configuration interface to its neighbour. Even if the baseline is to configure these chips separately, a different I2C address for each of the chips in the LD-HexModule assembly is advised in case the project constraints evolve requiring I2C buses to be connected together.

4.3 Concentrator Mezzanine Card

In order to decouple the schedule of the Concentrator ASICs from that of the HGCROC and LD-HexModules, the Concentrator ASICs will be placed on a separate mezzanine card that is to be mounted on the LD-HexModule via two 80 pin FX11 connectors with a mated height of 2mm. The signals required are detailed in table 4. Note that the direction quoted is as seen from the Concentrator Mezzanine perspective. The mating height has been chosen to permit the Mezzanine card to fit underneath the LD-WagonBoard, providing that the packaged ECON chip(s) are fitted on the connector side of the Mezzanine card (see the schematic in figure 2).

The power for this mezzanine card is taken from the VDDD plane of the LD-HexModule, thus the power and ground signals are also passed through these connectors.

The Mezzanine card will exist in two variants for the full LD-HexModules: those destined for the CE-H and for the layers of the CE-E that contribute to the L1 Trigger decision will be fitted with both

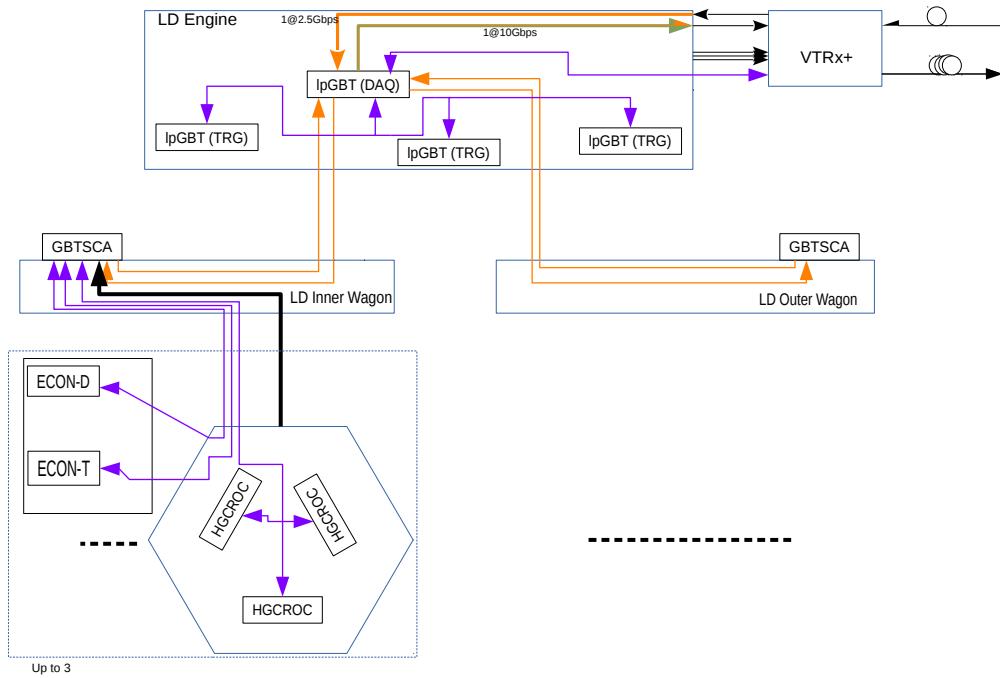


Figure 4: An overview of the slow-control and monitoring connections from the VTRx+ through to the LD-HexModule for the Low-Density case.

an ECON-D and an ECON-T ; those for the non-TPG layers of the CE-E will only be fitted with the ECON-D. Should space constraints prove to be too restrictive, the size of the PCB can be optimised by wire bonding the ECON-T to the mezzanine card. The device yield can then be transparently absorbed by selecting non-working ASICs for the non-trigger layers of the CE-E . The ECON-D will be packaged, thus only working chips will be fitted. An alternative solution to ease the space constraints would be to adopt a BGA package. The additional cost, design time, and testing complexity will need to be carefully evaluated before such a solution can be chosen.

Some of the partial modules have space requirements that still require study and may imply a different design of the mezzanine card. This is currently under study by the Mechanical CAD and Mock-Up effort.

As one of the the DAQ IpGBT uplinks is required for the upstream path of the second GBTSCA EC port, only $6 \times 1.28\text{Gb/s}$ e-links are available for the data streams from both the inner and outer LD-WagonBoards (see section 4.2.2). Equal allocation implies one such link per LD-HexModule, however the current expectation is that a small fraction of LD-HexModules, will require two. The current proposition is judicious pairing of the LD-HexModules in question through careful placement of the LD-EngineBoard and appropriate allocation of the e-links. An alternative would be to adjust the rate at the LD-HexModule by trimming the zero suppression threshold. Note that for uniformity and simplicity of the the LD-EngineBoard, the current e-link allocation scheme under investigation assume equal allocation of 3 e-links to the inner LD-WagonBoard and 3 to the outer LD-WagonBoard.

The Trigger IpGBTs have no GBTSCA connected, thus all 7 e-link inputs at 1.28Gbps are available, giving a total of 21 e-links to be divided between the LD-HexModules. Some of the LD-HexModules require more than 3 e-links, and again it is foreseen to manage the bandwidth by careful allocation of the links and, if necessary, trimming the trigger thresholds.

This e-link allocation is currently under study. As the counting rules assume an optimal bandwidth

Signals HexModule↔Mezz	58		GSGSG	160 /160	I/O (Mezz)	Comments
CLK320	1	pairs	x2	4	in	IpGBT→ECON-D
FST_CMD_E2C	1	pairs	x2	4	in	IpGBT→ECON-D
CLK320_C2R	4	pairs	x2	16	out	ECON-D→HGCROCs:4th for triangle
FST_CMD_C2R	3	pairs	x2	12	out	ECON-D→HGCROCs:multiplex triangle
DAQ	7	pairs	x2	28	in	ECON-D inputs: 7th for triangle
TRIG	12	pairs	x2	48	in	ECON-T inputs: no TPG from triangle
DAQ_ELNK	2	pairs	x2	4	out	ECON-D outputs → IpGBT (DAQ)
TRIG_ELNK	4	pairs	x2	16	out	ECON-T outputs → IpGBT(TRIG)
RESETB_I2C	1	se	x1	1	in	I2C reset for ECON-D and ECON-T
I2C_ECON_T_SDA	1	se	x1	1	bi	
I2C_ECON_T_SCL	1	se	x1	1	bi	
I2C_ECON_D_SDA	1	se	x1	1	bi	
I2C_ECON_D_SCL	1	se	x1	1	bi	
RESETB_ECON_D	1	se	x1	1	in	Hard Reset for ECON-D
RESETB_ECON_T	1	se	x1	1	in	Hard Reset for ECON-T
ECONT_ERR	1	se	x1	1	od	Open drain ECON error signals
ECOND_ERR	1	se	x1	1	od	Open drain ECON error signals
PWR_ECON	15		x1	15	POWER	VDDD(=1.2V) plane for ECONs

Table 4: The list of signals required between the LD-HexModule and the Concentrator Mezzanine Card

allocation everywhere, it could be that once realistic constraints are imposed, the component counts shown in section 4.12 increase.

4.4 LD Powering Scheme

	Full-Size-DCDC	Half-Size-DCDC
Signal	Pin count per connector	pin count per connector
GND	20	24
VDDA1.5	14	24
VDDD1.2	14	0
EN	1	1
PG	1	1

Table 5: The list of signals required between the LD-HexModule and the DCDC converters. This assumes a Hirose DF40 connector with 50 pins.

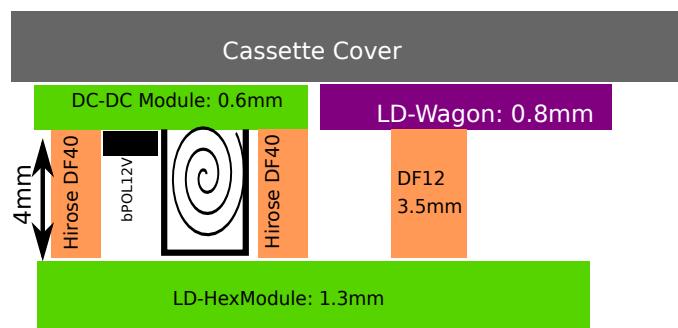


Figure 5: A zoom of the vertical space available for the Low Density DCDC Module.

are shown in table 5. This configuration was chosen to optimise the space available for the coil and minimise the constraints that the DCDC modules impose on component placement on the LD-HexModule. Two connectors are used to match the current requirements, ease the placement constraints on the LD-HexModule, and provide a robust mechanical interface.

Each bPOL12V module on the dual DCDC converter could be independently enabled and issue an independent PGood signal (indicating power-good), however, the baseline design is to connect these together and have a single enable and single active-low PGood indicator, formed from the wire-OR of the PGood outputs from the bPOL12V devices. If the DCDC module PCB is 0.8mm thick, the remaining vertical space into which the coil and shield must be fitted is approximately 4mm.

The VDDD will also be used to power the Concentrator Mezzanine via the connectors detailed in figure 1 and table 4.

The GBTSCA requires a 1.5V supply for the analogue components to operate correctly. It is envisaged to regulate this from the LD-EngineBoard. The LD-EngineBoard and LD-WagonBoards to which it connects will share a common 1.2V digital supply voltage.

The cooling loops are situated in the absorbers below the silicon sensor, which would be on the bottom of the LD-HexModule in figure 5. A thermal compliance layer will be placed where necessary between the DCDC modules and the LD-HexModule, although this is not shown in the diagram.

Each LD-HexModule has a DCDC converter mounted on it. This module is derived from the bPOL12V chip-set and exists in two variants: a Full-Size-DCDC and a Half-Size-DCDC. The Full-Size-DCDC has two bPOL12V chips (and inductors, sets of decoupling capacitors, trimming resistors, etc.), with each one independently regulating the 8-10V rail: one to VDDD = 1.2V for the digital components on the LD-HexModule and the Concentrator Mezzanine Card; and the other regulating it to VDDA = 1.5V for the analogue requirements on the LD-HexModule. The 1.5V rail is further regulated to 1.2V via the LDO, which is fitted directly to the LD-HexModule.

The Half-Size-DCDC regulates the 8-10V rail down to VDD = 1.5V. This variant is to accommodate LD-HexModule partials that are too small to have a Full-Size-DCDC fitted. To preserve adequate supply separation between the analogue and digital domains, these partial types will be fitted with multiple LDOs to regulate to VDDA (1.2V) and VDDD (1.2V). The input to this DCDC converter will be a Hirose DF61 connected to 22-gauge wire in both Full-Size and Half-Size cases. These bring in the power (8-10V) and return from and to PP0. Note that this is not currently shown in figure 5.

The connector foreseen for this application is the Hirose DF40 in a 50 pin, 4mm total mated height configuration. The envisaged pin allocations

4.5 High Density

An overview of the HD connections is shown in figure 6. This diagram shows the worst case² of 3 Full HD-HexModules and 1 Partial HD-HexModule.

The PCB stack-up is shown in figure 7.

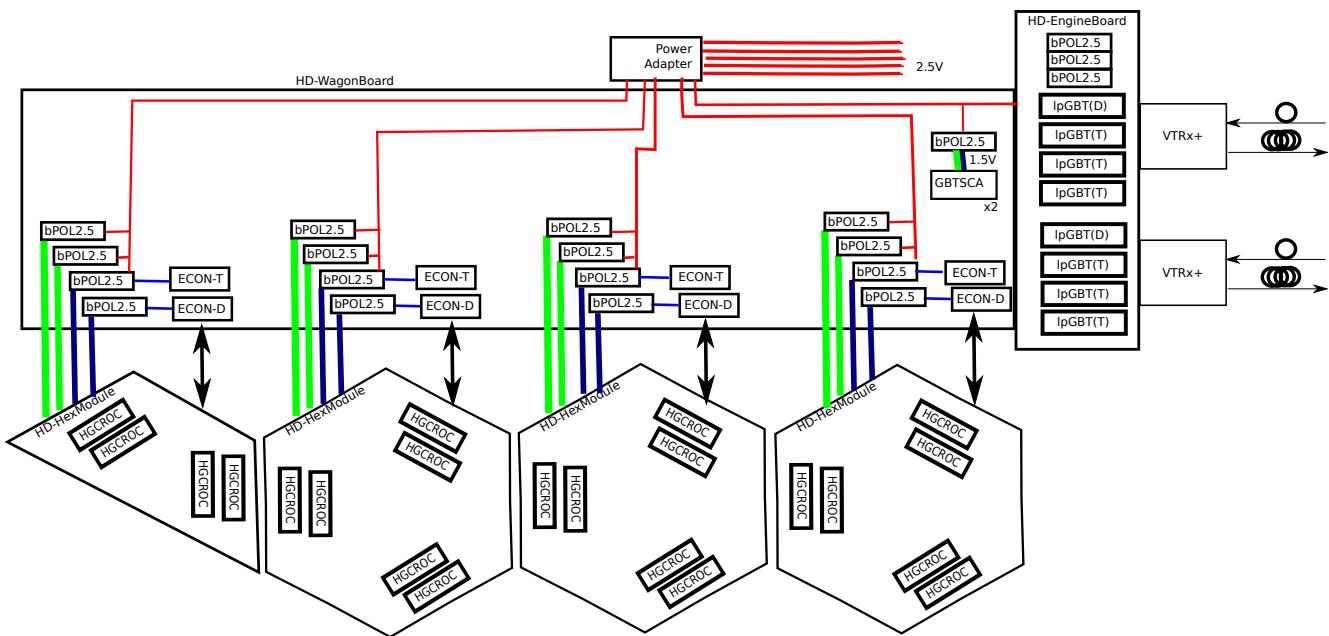


Figure 6: An overview of the connections between HD-HexModules, HD-WagonBoard, HD-EngineBoard and VTRx+ for the High-Density worst case with 3 Full HD-HexModules and a Partial HD-HexModule.

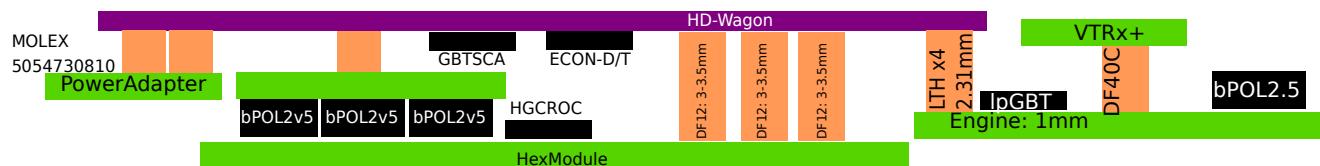


Figure 7: The PCB stack-up for the High Density case: note that component and connector counts in this diagram are illustrative.

The signals connecting the HD-HexModule to the HD-WagonBoard are listed in table 7. The connectors selected for this interface are 3 x 80 pin DF12 in a 3mm or 3.5mm stack height variant from Hirose. This connector was selected because it has appropriate height options and locating pins.

4.6 HD-EngineBoard

The HD-EngineBoard is similar to the LD-EngineBoard in concept, but with a maximum of 2 VTRx+ optical modules, 2 DAQ IpGBTs and 6 Trigger IpGBTs. It connects to the HD-WagonBoard through a set of 4 x 60 pin LTH connectors, the required connections of which are detailed in table 6. Unlike the LD-EngineBoard, these are situated along one edge, as there is only 1 inner HD-WagonBoard. The

²The number of HGCROCs are required for each partial HD-HexModule is not yet concretely defined - see table 39 for initial estimates.

Signal Eng ↔ MB	Signal Count		GSSG	237 /240	Comments
CLK320	8	pairs	1.5	24	$\leq 8 \times$ elink clocks:1/ECON-D & 1/ECON-T
FC	8	pairs	1.5	24	$\leq 8 \times$ elink FC:1/ECON-D & 1/ECON-T
SCA_EC_IN	2	pairs	1.5	6	HDLC format
SCA_EC_OUT	2	pairs	1.5	6	HDLC format
SCA_CLK	2	pairs	1.5	6	
SCA_RST	2	se	1	2	
SCA_ERR	2	se	1	2	Wagon SCA error signal to IpGBT spare error path
GLB_ERR	2	se	1	2	
I2C_SDA_eFUSE	1	se	1	1	
I2C_SCL_eFUSE	1	se	1	1	
I2C_SDA_eFUSE	1	se	1	1	2 VTRx+:so two master IpGBTs.
I2C_SCL_eFUSE	1	se	1	1	efuse programmed through IpGBT/I2C
IpGBT_Reset	1	se	1	1	
efuse_power	2	pwr	1	2	
PROBE_DC1	1	ana	1	1	Wagon power monitoring
PROBE_DC2	1	ana	1	1	
DAQ_ELNK	14	pairs	1.5	42	DAQ lines at 1.28Gb/s to ECON-D
TRIG_ELNK	28	pairs	1.5	84	Trig lines at 1.28Gb/s top ECON-T
GND	15	pwr	1	15	Power to bPOL2V5. May not be needed
PWR_2V5	15	pwr	1	15	

Table 6: HD-WagonBoard to HD-EngineBoard signals.

bandwidth requirements have been used to determine the number of components to be mounted in each case and are presented in section 4.12.14. To satisfy the monitoring and DAQ bandwidth requirements two GBTSCAs are needed on the HD-WagonBoard, which in turn requires that there are always 2 VTRx+ modules and 2 DAQ IpGBTs - making this design choice preserves the bandwidth available by allowing all 7 of the 1.28Gb/s e-link inputs to the IpGBT to be available for data transmission. The counting rules have been updated and additional tables generated to reflect this change in the architecture as well as to estimate the number of Trigger IpGBTs required to homogenise the production: these are also shown in section 4.12.14.

nnn

HD Wagon ↔ HB	163		GSS(G)	228/ 240	Comments
CLK320	6	pairs	1.5	18	1xCLK320 per HGCROC from ECON-D fan-out
FST_CMD_E2C	6	pairs	1.5	18	1xFc per HGCROC from ECON-D fan-out
DAQ_ELNK	12	pairs	1.5	36	2xDAQ O/P per HGCROC
TRIG_ELNK	12	pairs	1.5	36	2xTRIGGER O/P per HGCROC (Sum-9 Mode)
I2C_SDA	2	se	1	2	I2C for each HGCROC triplet
I2C_SCL	2	se	1	2	I2C for each HGCROC triplet
I2C_RST	2	se	1	2	I2C Reset for each HGCROC triplet
RESETB_HGCROC	2	se	1	2	Active low hard reset for each HGCROC triplet
HGCROC_ERR	2	se	1	2	wire-or of 3xHGCROCs
PWR_EN_LDO	2	se	1	2	Enable for each LDO
LDO_P50MV	2	se	1	2	LDO Trim: adds 50mV to LDO output
LDO_M50MV	2	se	1	2	LDO Trim: subtracts 50mV from LDO output
PG_LDO	2	se	1	2	PG from each LDO
VDD	50	pwr	1	50	300mA/pin: 7W → 3.95mV drop
GND	50	pwr	1	50	
MGND	1	ana	1	1	Monitor ground: reference for the SCA ADC
RTD	1	ana	1	1	temperature measurement
RTD_REF	1	ana	1	1	reference for temperature measurement
VMON_LDO	2	ana	1	2	voltage monitor for LDO
PROBE_DC_I	2	ana	1	2	probe connections to HGCROC triplets
PROBE_DC_V	2	ana	1	2	probe connections to HGCROC triplets

Table 7: List of signals between the HD-HexModule and the HD-WagonBoard

4.6.1 HD-WagonBoard

The HD-WagonBoard connects to up to 4 HD-HexModules. In these cases, the inner-most HD-HexModule is a partial (a, d- or g-: see table 12). The data concentrators are mounted directly on the HD-WagonBoard and connections to the HD-EngineBoard are to be made in a way that effectively shares the bandwidth. The scheme for this is under investigation at the time of writing.

4.6.2 HD Powering Scheme

The powering scheme in the HD region relies on 2.5V being brought into the central regions of the detector, where it connects directly to the HD-WagonBoard which performs the power distribution to the HD-HexModules, the HD-EngineBoard and, through the HD-EngineBoard, the VTRx+ modules connected to it.

Signal	Domain	Connector 1:power	Connector 2: power	Signal
GND	0,1,2,3,4	2	2	0
VDDD2.5	0	1	0	0
VDDD2.5	1	1	0	0
VDDD2.5	2	0	1	0
VDDD2.5	3	0	1	0
VDDD2.5V	4	0	0	4+4

Table 8: The list of signals required between the HD-WagonBoard and power adaptor card.

For the 5th power domain required in the case where 4 HD-HexModules are connected to the HD-WagonBoard, the signal contacts, of which there are 4 per connector, may be used, each supporting 0.5A to give a total of 4A.

The connection between the power and grounding cables will be made via a Power Adapter card. This is a small passive PCB that will have solder pads for the cables on one side and the connectors on the other. An alternative solution could be to use a mezzanine card for the bPOL2.5 modules and connect the cables to this via a board-to-cable connector.

The 2.5V power plane will be used to power the HD-HexModules, with VDDA (1.5V) and VDDD (1.2V) being regulated independently from separate bPOL2.5 modules for each HD-HexModule. The concentrator chips, requiring only a digital supply at 1.2V, will use the same power plane as the HD-HexModule to which they connect.

4.6.3 HD-HexModule Power Partitions

A common ground plane throughout a given HD-MotherBoard and HD-HexModule assembly is envisaged. Note that analogue the power requirements of the HGCROCs necessitate two bPOL2.5V regulators for each HD-HexModule, and the combined digital requirements of the HGCROCs and the ECON-D and ECON-T, when present, also necessitate two bPOL2.5V regulators. This naturally gives two power partitions of 3 HGCROCs each - this also fits in with the LDO current capacity. Due to the number of control and monitoring signals available on the GBTSCA and the number of pins available on the DF12 connectors, some of the control and status signals must be combined, and this is possible due to them having been designed as open-collectors or having a high-impedance setting. However, these combinations should not be made across the two different power partitions if the ability to switch off one such partition in the event of malfunction is required. Thus the control and status/monitoring signals listed in table 7 show

The power dissipation is thus expected to be relatively high, and provision for a current of approximately 18A must be budgeted for in the worst case. To allow effective transfer of power from the cables to the HD-WagonBoard, a slimstack, board-to-board battery connector has been chosen (Molex 5054730810). The series resistance of a single power contact is sufficiently low to allow one contact per power domain. This requires that two such connectors be used in parallel. For

the numbers required for these triplets. Note that the presented power architecture places the ECON-D and ECON-T in different power partitions, which defeats the scheme. Some alternative would be required here.

4.6.4 HD Fast Control and Fan Out

The ECON-D is currently foreseen to include a component that will serve as two 1:6 fan-outs: one for the differential CLK320 signal from the IpGBT and the second for the differential fast control (FC) signal at 320Mb/s. The exact specifications of this functionality are beyond the scope of this report and, as the design of the fan-out circuitry is currently under consideration, it remains to be decided if the CLK320 and/or FC data streams are to be registered in the ECON-D or not. Figure 8 shows an overview of these clock and fast control fan-outs. The ECON-D and the ECON-T will be driven by separate clock and fast command outputs from the IpGBT. The 6 output copies of these signals from the ECON-D will subsequently drive the 6 HGCROCs on the HD-HexModule. This implies a single logical fast command partition per ECON-D/HD-HexModule. Note that the same assumption has been made for the low density case.

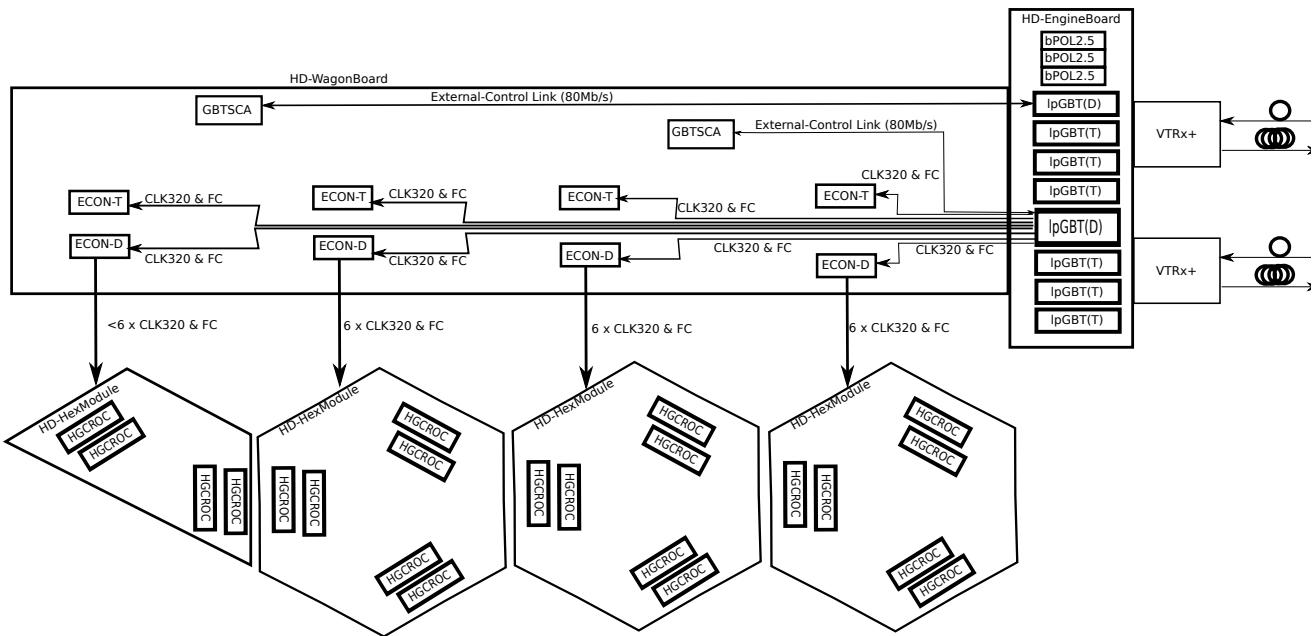


Figure 8: An overview of the clock and fast control connections between HD-HexModules, HD-WagonBoard, HD-EngineBoard for the High-Density.

4.6.5 HD Slow Control and Monitoring

Slow control and monitoring in the HD region are orchestrated via the GBTSCA ASIC. There are 2 fitted to the HD-WagonBoard and controlled through the EC port of the DAQ IpGBTs. Both the HGCROCs and the ECON-T/D chips possess I²C slave interfaces through which the configuration parameters are controlled, and status information can be read back. The HD-HexModules have up to 6 HGCROCs on them and provision has been made in the FX11 pin allocations for a separate connection to each, and whilst this might be desirable from a performance perspective, it places a large requirement on the number of independent I²C masters required: possibly up to 22 in the case where 4 HD-HexModules are connected to a single HD-WagonBoard. The HGCROC and the ECON-T/D are equipped with a 4-bit slave address,

Signal Name	Number/ HD-HexModule	Group	Type	GBTSCA Direction	Notes
DCDC_EN	4	2	DIG	OUT	Match pwr partitions
DCDC_PG	4	2	OC	IN	Open Collector
VDDD_VMON	2	1	ANA	IN	
VDDA_VMON	2	1	ANA	IN	
ECONT_RSTB	1	1	DIG	OUT	
ECONT_I2C_RSTB	1	1	DIG	OUT	
ECONT_ERRB	1	1	OC	IN	
ECOND_RSTB	1	1	DIG	OUT	
ECOND_I2C_RSTB	1	1	DIG	OUT	
ECOND_ERRB	1	1	OC	IN	

Table 9: HD-WagonBoard Control and Monitoring Requirements.

allowing up to 16 to co-exist on the same I²C bus. Each GBTSCA contains 16 independent I²C master interfaces to be shared between up to 4 HD-HexModules, allowing for 8 each: a homogeneous distribution would allow one bus per ECON-T/ECON-D and 1 bus per HGCROC. The available pin count on the connectors do not permit the HGCROCs to have such an independent connection, however. Thus it is proposed to group these connections with the HD-HexModule power partitions.

Each GBTSCA has 32 GPIO pins, giving a total of 64 available on the HD-WagonBoard and meaning that up to 16 are available for each HD-HexModule and associated components. Table 7 lists the signals required between the HD-HexModule and the HD-WagonBoard. Here it can be seen that presently a total of 14 digital control and status pins have been allocated: 2 each of I2C_RST, RESETB_HGCROC, HGCROC_ERR, PWR_EN_LDO, LDO_P50MV, LDO_M50MV, and PG_LDO. The additional requirements per HD-HexModule on the HD-WagonBoard are listed in table 9 (note that the I2C_SCL and I2C_SDA requirements are counted separately). A total of 14 signals are listed, which brings the total number of digital signals to be controlled and monitored to 28. A scheme to match these requirements to the 16 available GPIO/HD-HexModule is currently under investigation. An additional 8 digital outputs (no interrupt or input/high impedance functionality is available) per GBTSCA are available through appropriate configuration of the otherwise unused SPI master interface, which allows transparent control of the *SS*. Note that this functionality should be verified before it is assumed. If adopted, an additional 16 output signals become available: thus up to 4 per HD-HexModule.

Each GBTSCA has 31 analogue inputs, giving a total of 62. A homogeneous allocation thus gives 15 available for each HD-HexModule and associated components. The HD-HexModule currently requires 9 analogue inputs to the GBTSCA: these are 1xMGND, 1xRTD, 1xRTD_REF, 2xVMON_LDO, 2xPROBE_DC_I, 2xPROBE_DC_V. Additionally, voltage monitoring requirements on the HD-WagonBoard amount to 4 ADC channels/HD-HexModule. The total is thus 13, which fits within the GBTSCA ADC channel count.

4.7 HD and LD Sensor Bias Connections

Each sensor is expected to require a maximum bias of 1000V and, in the worst case, draw a maximum of 20mA. The sensor bias is to be provided to each sensor through a BHT connector from JST. This is a 2-contact, shrouded, crimped, connector rated to up to 1500V and 1A. The PCB side is surface mount and available in reels for automated assembly. The connector footprint requires approximately 10mm x 12mm on the PCB and has a full height of 2.8mm. It supports crimping to wires from 28-gauge to 24-gauge. Choosing the smallest, would give a worst case voltage drop across the wire of about 5mV and an additional 20mΩ from the maximum contact resistance would incur a further 0.4mV.



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Each bias wire will be routed to the periphery to be connected to the PP0 feed-through. The details of this are under discussion at present.

4.8 HD and LD Peripheral Power Regulation

A series of DCDC converters is required at the periphery to regulate the 2.5V supply required for the HD region. This requirement shall be fulfilled by banks of bPOL12V converter modules situated at the periphery of the cassette. Each bPOL12V is capable of providing a maximum continuous current of 4A, so a worst case of 4+1 (the 5th being for the HD-EngineBoard and VTRx+) such chips will be required to provide the maximum 18A budgeted for per HD-MotherBoard, HD-WagonBoard and associated HD-HexModules with a small margin. Note that the bPOL12V control circuitry operates in voltage regulation mode, thus ganging the outputs of multiple bPOL12Vs is not possible. This implies that a cable for each bPOL12V output must be used to connect it to the corresponding part of the HD circuit it drives. Up to 5 bPOL12Vs per peripheral power board were chosen as this matches the maximum number of HD-HexModules connected to a single HD-WagonBoard, plus a channel for the HD-EngineBoard. A schematic diagram of the power distribution is shown in 9.

Additionally, the LD-EngineBoard requires a 2.5V input (see Figure 1), thus a separate bPOL2.5 regulator is foreseen for each of these. The same 5-module bPOL12V board is a possibility, thus the LD case counts 0.2 PCBs and 1 x bPOL12V per LD-EngineBoard. This number is then rounded to the nearest integer for the PCB counting, but not to the nearest multiple of 5 for the module counting. The required quantities for these components are detailed in section 4.12.2 in tables 16 and 17 for the CE-E and CE-H respectively.

Note that these requirements are counted separately from the DCDC modules fitted to LD-HexModules inside the detector: see tables 14, 15 for these counts.

Transfer of 2.5V from the periphery to the readout is to be done through sets of 15-gauge or 16-gauge cables. These permit a maximum current of 4.7A/3.7A respectively to be transferred, representing about the thinnest conductors that satisfy the current constraints. At room temperature, an I-R drop of between 4.5mV/6mV respectively can be expected for a 1.5m cable carrying 3A (n.b. this must be doubled to include the return cable if the same type is used).

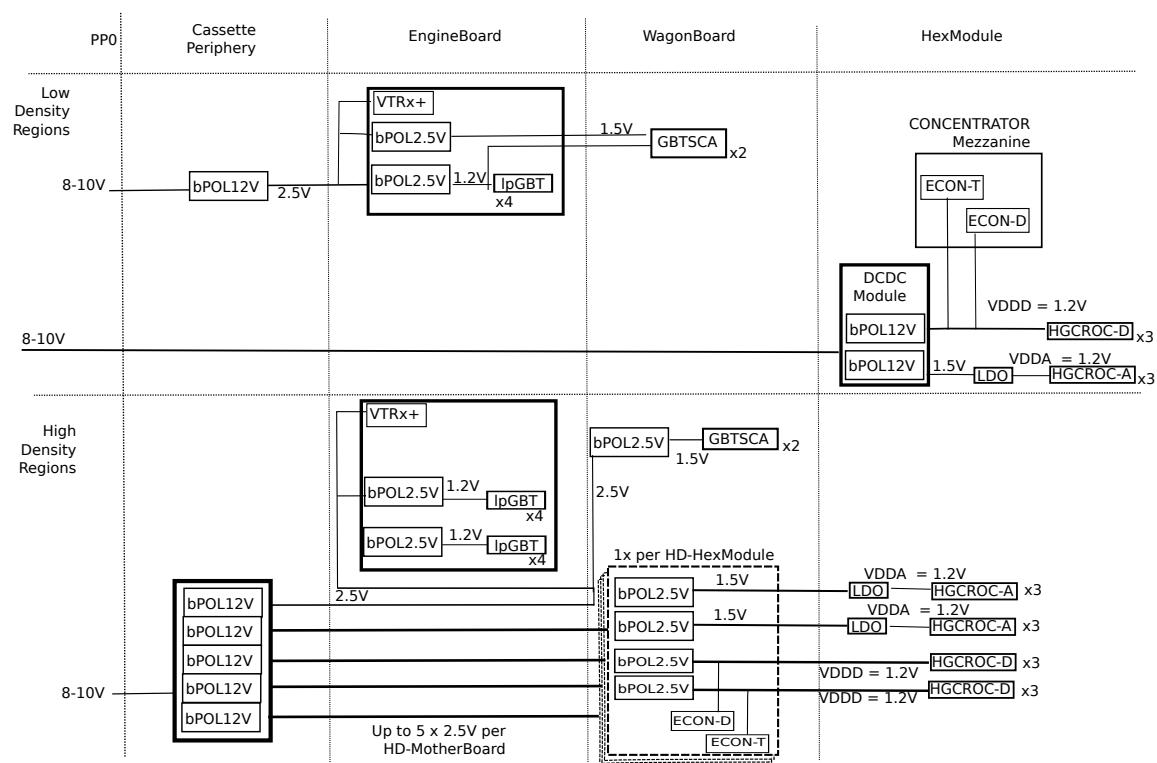


Figure 9: An overview of the cassette power distribution.

4.9 Identical and Similar Layers

The inhomogeneous nature of the detector means that there are relatively few identical layers. Some layers have the same shape but differ in the number of HD/LD modules and others have small differences in the outer periphery. These could potentially be changed to facilitate production and are enumerated in tables 10 and 11 for the CE-E and CE-H respectively.

In the CE-E there are no layers that differ only in the number and/or placement of LD-HexModules/HD-HexModules. The last column of table 10 shows layers that could be matched by making small changes in the outer periphery. The criteria are relatively loose, but the key idea is to change the type, or remove, only LD-HexModules at the outer border. The CE-H contains no such possibilities and thus this column is not shown.

Layer	Identical Layers	Outer Periphery
1	3,5,7	
2		
4	6	8
8		
9	11	13
10		12
12		14
13		15
14		16
15	17	19
16	18	20
20	22	24
21	23	25
24		
25		27
26		28
28		

Table 10: List of identical and near identical layers for the CE-E .

Note that in the CE-H case there are differences between the even and odd cassettes, which comes from an effective 60° rotation of the full plane. These are denoted in the table by "e↔o". Table 10 also shows layers for which there is a difference only in the sensor thickness (M/O corresponding to $200\mu m$ and $300\mu m$ respectively). There are no such cases in the CE-E.

Layer	Identical Layers	HD/LD Differences	$200\mu m \leftrightarrow 300\mu m$
29			
30		31(e↔o)	31(e↔o)
31			
32			33(e↔o)
33			
34			
35			
36			
37	39		
38		40	
39			
40			
41			
42			
43		45	
44		46	
45			
46			
47		49	
48	49(e↔o),		50
50			

Table 11: List of identical and near identical layers for the CE-H .

4.10 Full Layer Detail

The complete, high level, baseline tiling scheme for CE-E and CE-H layers is shown in Appendix A. The component counts for this layout are detailed in section 4.12. Note that for all CE-E layers (1-28 inclusive), diagrams and tables are based on a 6-fold symmetry: a 60° cassette that is assumed identical within a given plane. Whereas for the CE-H (layers 29-50 inclusive), a pair of adjacent cassettes is taken, corresponding to a 120° slice and a 3-fold symmetry.

Figure 10 shows the LD-HexModule and HD-HexModules tiled to form a cassette in layer 1, including connector positions and rotations. There are currently no MotherBoard assemblies or other services shown. Work to delimit the space required and envelopes available for all the components required in the stackup is underway in collaboration with the mechanical design team.

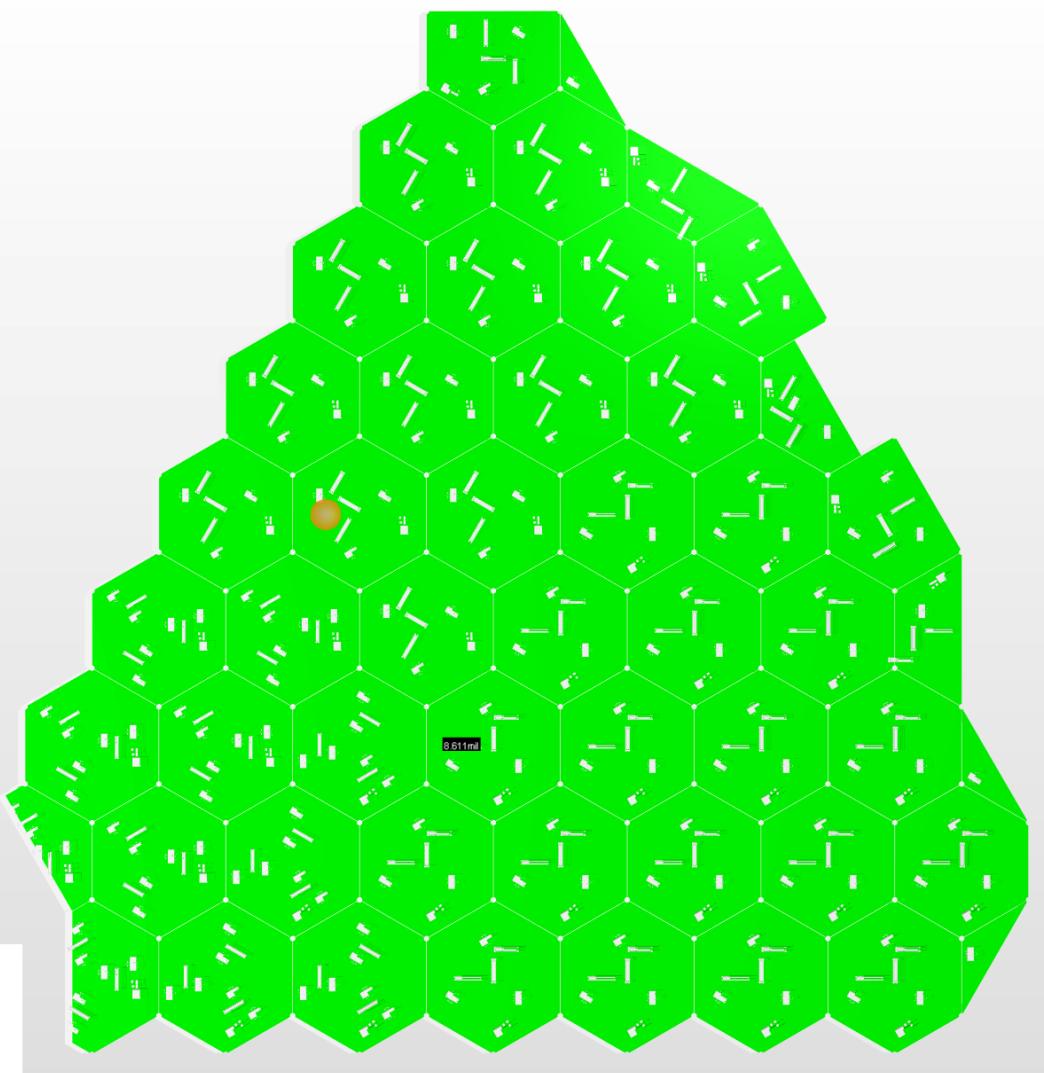


Figure 10: CAD Layout of the HexModules in Layer 1 showing connector positions.

4.11 HexModule Naming and Identification

Table 12 shows the HexModule types, their designators and the sensor full depletion thickness. Note that a distinction is made between cO being the shape and thickness of the silicon sensor, and F+cO being the assembled module with the triangle and the adjacent FO sensors both mounted on the F+cO PCB. The sensitive thickness of the sensor is given by codes I, M, and O corresponding to $120\mu m$, $200\mu m$, and $300\mu m$ respectively

Module Type	Designator	Cell Size	Sensor Thickness
	FI	HD	$120\mu m$
	aI	HD	$120\mu m$
	bI	HD	$120\mu m$
	dI	HD	$120\mu m$
	gI	HD	$120\mu m$
	FO	LD	$300\mu m$
	aO	LD	$300\mu m$
	bO	LD	$300\mu m$
	cO	LD	$300\mu m$
	F+cO	LD	$300\mu m$
	dO	LD	$300\mu m$
	FM	LD	$200\mu m$
	aM	LD	$200\mu m$
	bM	LD	$200\mu m$

Table 12: HexModule Naming and Identification

4.12 Component Counts

In the following sections, the tables output by the component counting software are detailed. The counts are broken down by layer, and given separately for CE-E and CE-H . For each quantity the counts follow rotational symmetries in the respective sections: 60° for the CE-E and 120° for the CE-H , but the value per plane is also given ($\times 6$ for the CE-E and $\times 3$ for the CE-H). The penultimate row in each table shows

the totals for a full wedge, meaning the values summed over layers 1-28 for 1 cassette in the CE-E and over layers 29-50 for 1 even and 1 odd cassette for the CE-H . The last row shows the totals for the whole detector: sum over all cassettes for each layer, all layers, and both end-caps.

At the end there is a summary table that gives the CE-E and CE-H totals as well as the detector totals for each quantity counted.

These numbers are for the final installed detector, and as such there are several things absent from these lists that should be borne in mind:

- an accuracy of about 10% can be assumed;
- no prototyping is included;
- there are no spares included;
- only the data-driven, baseline trigger algorithms are currently considered;
- a minimalistic/reductionist approach is adopted implying that unused components are assumed not to be soldered/fitted or counted; and
- that the numbers given here do not include the scintillator section.

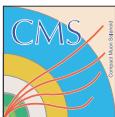
For the last point, a second document is under preparation detailing the architecture, from which similar counts will be extracted.

4.12.1 Module bPOL Counts

Tables 14 and 15 show the numbers of bPOL2v5 and bPOL12 ASICs necessary for the powering schemes in the CE-E and CE-H sections respectively for the local regulation on the LD-HexModules and the HD-WagonBoards. These numbers are based on the numbers and types of Engines, Wagons, and HexModules and DCDC converters: see table 13. Please refer to the relevant sections for a deeper explanation of where these come from. Note that the peripheral powering scheme is not included here - refer to section 4.12.2 for these bPOL12V counts.

Case	bPOL2.5	bPOL12
HD-EngineBoard	3	0
HD-WagonBoard	4 per HD-HexModule + 1	0
HD-HexModule	0	0
LD-EngineBoard	1	0
Dual DCDC Converter	0	2
Single DCDC Converter	0	1

Table 13: Counting rules for bPOL modules used on the EngineBoards, WagonBoards, HexModules.



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plane	bPOL2v5/60°	bPOL2v5/plane	bPOL12/60°	bPOL12/plane	
1	80	480	69	414	
2	80	480	60	360	
3	80	480	69	414	
4	80	480	63	378	
5	80	480	69	414	
6	80	480	63	378	
7	80	480	69	414	
8	80	480	65	390	
9	80	480	74	444	
10	80	480	66	396	
11	84	504	72	432	
12	84	504	68	408	
13	84	504	73	438	
14	84	504	69	414	
15	86	516	73	438	
16	84	504	73	438	
17	86	516	73	438	
18	86	516	73	438	
19	86	516	74	444	
20	86	516	73	438	
21	86	516	77	462	
22	86	516	73	438	
23	86	516	77	462	
24	86	516	74	444	
25	86	516	79	474	
26	86	516	77	462	
27	86	516	80	480	
28	86	516	80	480	
Column Totals	2338	14028	2005	12030	
Detector Totals	-	28056	-	24060	

Table 14: CE-E bPOL Count



plane	bPOL2v5/120°	bPOL2v5/plane	bPOL12/120°	bPOL12/plane
29	148	444	170	510
30	150	450	175	525
31	166	498	177	531
32	150	450	185	555
33	154	462	187	561
34	160	480	203	609
35	164	492	231	693
36	162	486	256	768
37	84	252	170	510
38	50	150	180	540
39	52	156	180	540
40	52	156	180	540
41	30	90	135	405
42	30	90	135	405
43	24	72	98	294
44	26	78	98	294
45	22	66	98	294
46	22	66	98	294
47	20	60	68	204
48	20	60	68	204
49	20	60	68	204
50	22	66	68	204
Column Totals	1728	5184	3228	9684
Detector Totals	-	10368	-	19368

Table 15: CE-H bPOL Count

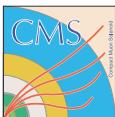


4.12.2 Peripheral Powering Module and bPOL12v Counts

Tables 16 and 17 show the HD and LD peripheral power regulation PCB counts and the associated bPOL12V counts per layer for the CE-E and CE-H layers respectively. The counts are obtained by assuming 1 x bPOL12V per HD-HexModule and 1 x bPOL12V per HD-EngineBoard in the HD regions and 1 x bPOL12V per LD-EngineBoard in the LD regions.

05.04.20 14:50:53	1586098253							
plane	HD PCB/ 60°	HD bPOL12/ 60°	HD PCB/ plane	HD bPOL12/ plane	LD PCB/ 60°	LD bPOL12/ 60°	LD PCB/ plane	LD bPOL12/ plane
1	4	16	24	96	2	8	12	48
2	4	16	24	96	2	8	12	48
3	4	16	24	96	2	8	12	48
4	4	16	24	96	2	8	12	48
5	4	16	24	96	2	8	12	48
6	4	16	24	96	2	8	12	48
7	4	16	24	96	2	8	12	48
8	4	16	24	96	2	8	12	48
9	4	16	24	96	2	8	12	48
10	4	16	24	96	2	8	12	48
11	4	17	24	102	2	8	12	48
12	4	17	24	102	2	8	12	48
13	4	17	24	102	2	8	12	48
14	4	17	24	102	2	8	12	48
15	4	17	24	102	2	9	12	54
16	4	17	24	102	2	8	12	48
17	4	17	24	102	2	9	12	54
18	4	17	24	102	2	9	12	54
19	4	17	24	102	2	9	12	54
20	4	17	24	102	2	9	12	54
21	4	17	24	102	2	9	12	54
22	4	17	24	102	2	9	12	54
23	4	17	24	102	2	9	12	54
24	4	17	24	102	2	9	12	54
25	4	17	24	102	2	9	12	54
26	4	17	24	102	2	9	12	54
27	4	17	24	102	2	9	12	54
28	4	17	24	102	2	9	12	54
Column Totals	112	466	672	2796	56	237	336	1422
Detector Totals	-	-	1344	5592	-	-	672	2844

Table 16: CE-E Peripheral Regulation Count

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plane	HD PCB/ 120°	HD bPOL12/ 120°	HD PCB/ plane	HD bPOL12/ plane	LD PCB/ 120°	LD bPOL12/ 120°	LD PCB/ plane	LD bPOL12/ plane
29	7	28	21	84	4	18	12	54
30	7	28	21	84	4	19	12	57
31	8	32	24	96	4	19	12	57
32	7	28	21	84	4	19	12	57
33	7	28	21	84	5	21	15	63
34	7	28	21	84	5	24	15	72
35	7	28	21	84	6	26	18	78
36	6	26	18	78	6	29	18	87
37	2	8	6	24	6	26	18	78
38	0	0	0	0	6	25	18	75
39	0	0	0	0	6	26	18	78
40	0	0	0	0	6	26	18	78
41	0	0	0	0	4	15	12	45
42	0	0	0	0	4	15	12	45
43	0	0	0	0	3	12	9	36
44	0	0	0	0	3	13	9	39
45	0	0	0	0	3	11	9	33
46	0	0	0	0	3	11	9	33
47	0	0	0	0	2	10	6	30
48	0	0	0	0	2	10	6	30
49	0	0	0	0	2	10	6	30
50	0	0	0	0	3	11	9	33
Column Totals	58	234	174	702	91	396	273	1188
Detector Totals	-	-	348	1404	-	-	546	2376

Table 17: CE-H Peripheral Regulation Count



4.12.3 Concentrator Mezzanine Connector Counts

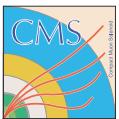
Tables 18 and 19 list the numbers of FX11 (80 pin, 2mm mated height) connectors required for the connections between the LD-HexModule variants and the Concentrator Mezzanine Card. Two per LD-HexModule are assumed. Note that the numbers refer to the mated pairs. If purchased separately, the price of the pair must be used.

05.04.20 14:50:53		1586098253
plane	LD/60°	LD/plane
1	72	432
2	62	372
3	72	432
4	68	408
5	72	432
6	68	408
7	72	432
8	72	432
9	78	468
10	72	432
11	76	456
12	72	432
13	76	456
14	72	432
15	76	456
16	76	456
17	76	456
18	76	456
19	76	456
20	76	456
21	78	468
22	76	456
23	78	468
24	76	456
25	82	492
26	78	468
27	84	504
28	84	504
Column Totals	2096	12576
Detector Totals	-	25152

Table 18: CE-E HexModule to Concentrator Connector Count

05.04.20 14:50:53		1586098253	
plane	LD/120°	LD/plane	
29	174	522	
30	184	552	
31	186	558	
32	192	576	
33	196	588	
34	210	630	
35	238	714	
36	264	792	
37	178	534	
38	190	570	
39	190	570	
40	190	570	
41	144	432	
42	144	432	
43	104	312	
44	104	312	
45	104	312	
46	104	312	
47	74	222	
48	74	222	
49	74	222	
50	74	222	
Column Totals		3392	10176
Detector Totals		-	20352

Table 19: CE-H HexModule to Concentrator Connector Count



4.12.4 Data and Trigger Concentrator Mezzanine Card Count

Tables 21 and 22 list the numbers of concentrator mezzanine cards required for the LD regions of the CE-E and CE-H respectively. The counts differentiate between cards populated with both the ECON-T and ECON-D (dual) for the TPG layers and those populated only with the ECON-D (single) used only in the even layers of the CE-E . The counting rules are shown in table 20. Note that there are no connectors counted for the triangles (cO) as these are read out through the adjacent Full LD-HexModule.

Region	Counting Rule
LD CE-E Odd Layers	1 dual-populated module per LD-HexModule
LD CE-E Even Layers	1 single-populated module per LD-HexModule
LD CE-H All Layers	1 dual-populated module per LD-HexModule
LD CE-H All Layers	0 single-populated module per LD-HexModule
HD CE-E	0
HD CE-H	0

Table 20: Concentrator Mezzanine Card Counting Rules.



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plane	Single/60°	Single/plane	Dual/60°	Dual/plane
1	0	0	36	216
2	31	186	0	0
3	0	0	36	216
4	34	204	0	0
5	0	0	36	216
6	34	204	0	0
7	0	0	36	216
8	36	216	0	0
9	0	0	39	234
10	36	216	0	0
11	0	0	38	228
12	36	216	0	0
13	0	0	38	228
14	36	216	0	0
15	0	0	38	228
16	38	228	0	0
17	0	0	38	228
18	38	228	0	0
19	0	0	38	228
20	38	228	0	0
21	0	0	39	234
22	38	228	0	0
23	0	0	39	234
24	38	228	0	0
25	0	0	41	246
26	39	234	0	0
27	0	0	42	252
28	42	252	0	0
Column Totals	514	3084	534	3204
Detector Totals	-	6168	-	6408

Table 21: CE-E Concentrator Mezzanine Count

05.04.20 14:50:53		1586098253			
plane		Single/120°	Single/plane	Dual/120°	Dual/plane
29		0	0	87	261
30		0	0	92	276
31		0	0	93	279
32		0	0	96	288
33		0	0	98	294
34		0	0	105	315
35		0	0	119	357
36		0	0	132	396
37		0	0	89	267
38		0	0	95	285
39		0	0	95	285
40		0	0	95	285
41		0	0	72	216
42		0	0	72	216
43		0	0	52	156
44		0	0	52	156
45		0	0	52	156
46		0	0	52	156
47		0	0	37	111
48		0	0	37	111
49		0	0	37	111
50		0	0	37	111
Column Totals		0	0	1696	5088
Detector Totals		-	0	-	10176

Table 22: CE-H Concentrator Mezzanine Count

4.12.5 DCDC Module Count

Power to the LD-HexModule and Concentrator Mezzanine passes through the DCDC converter, which exists in two flavours: a Full-Size-DCDC module and a Half-Size-DCDC module. The Full-Size-DCDC module regulates the input power supply at 8-10V to provide the VDDD at 1.2V, and the VDDA at 1.5V (subsequently regulated to 1.2V using the LDO) using two separate bPOL12Vs. The single module, regulates in 12V input rail, providing a single 1.5V supply for small ("a" and "d" = half and semi modules), which is further regulated to separate VDDD=1.2V and VDDA=1.2V using separate LDO regulators on these HexModules.

As the current design concept of the HD region places the local regulation on the HD-WagonBoard, there are currently no DCDC modules there.

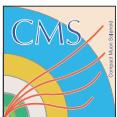
Note that it is assumed that the Triangle ("c") will be powered from the double DCDC converter mounted on the neighbouring "FO" HexModule.

Tables 24 and 25 show the Full-Size-DCDC and Half-Size-DCDC module counts per layer for the CE-E and CE-H respectively. The counts come from the counting rules shown in table 23.

Refer to table 12 in section 4.11 for a deeper explanation of the module types.

Region	HD					LD							
	(f) Full	(a) Half	(b) Five	(d) Semi(-)	(g) Choptwo(-)	(f) Full	(a) Half	(b) Five	(c) Three	(d) Semi	(f) Full	(a) Half	(b) Five
Module Type	Fl	al	bl	dl	gl	FO	aO	bO	cO	dO	FM	aM	bM
Double Count	0	0	0	0	0	1	0	1	0	0	1	0	1
Single Count	0	0	0	0	0	0	1	0	0	1	0	1	0

Table 23: Counting rules for the DCDC modules.



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plane	Single/60°	Single/plane	Double/60°	Double/plane
1	3	18	33	198
2	2	12	29	174
3	3	18	33	198
4	5	30	29	174
5	3	18	33	198
6	5	30	29	174
7	3	18	33	198
8	7	42	29	174
9	4	24	35	210
10	6	36	30	180
11	4	24	34	204
12	4	24	32	192
13	3	18	35	210
14	3	18	33	198
15	3	18	35	210
16	3	18	35	210
17	3	18	35	210
18	3	18	35	210
19	2	12	36	216
20	3	18	35	210
21	1	6	38	228
22	3	18	35	210
23	1	6	38	228
24	2	12	36	216
25	3	18	38	228
26	1	6	38	228
27	4	24	38	228
28	4	24	38	228
Column Totals	91	546	957	5742
Detector Totals	-	1092	-	11484

Table 24: CE-E DCDC Module Count

05.04.20 14:50:53		1586098253			
plane		Single/120°	Single/plane	Double/120°	Double/plane
29		4	12	83	249
30		9	27	83	249
31		9	27	84	252
32		7	21	89	267
33		9	27	89	267
34		7	21	98	294
35		7	21	112	336
36		8	24	124	372
37		8	24	81	243
38		10	30	85	255
39		10	30	85	255
40		10	30	85	255
41		9	27	63	189
42		9	27	63	189
43		6	18	46	138
44		6	18	46	138
45		6	18	46	138
46		6	18	46	138
47		6	18	31	93
48		6	18	31	93
49		6	18	31	93
50		6	18	31	93
Column Totals		164	492	1532	4596
Detector Totals		-	984	-	9192

Table 25: CE-H DCDC Module Count

4.12.6 ECON-D and ECON-T Counts

Tables 27 and 28 show the layer-by-layer ECON-D and ECON-T counts for the CE-E and CE-H respectively. These counts consider only TPG layers where appropriate (no ECON-Ts counted for even CE-E layers). One ECON-[DT] is counted per HD-HexModule in the HD regions and one ECON-[DT] per mezzanine card (and hence per LD-HexModule) in the LD regions. These are detailed for clarity in table 26. Note that cells from the cO sensors never contribute to the TPG regardless of the layer.

Case	ECON-D	ECON-T
LD CE-E Odd Layers	1 per LD-HexModule	1 per LD-HexModule
LD CE-E Even Layers	1 per LD-HexModule	0
HD CE-E Odd Layers	1 per HD-HexModule	1 per HD-HexModule
HD CE-E Even Layers	1 per HD-HexModule	0
LD CE-H All Layers	1 per LD-HexModule	1 per LD-HexModule
HD CE-H All Layers	1 per HD-HexModule	1 per HD-HexModule

Table 26: ECON-D/T Counting Rules.



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plane	ECON-D/60°	ECON-D/plane	ECON-T/60°	ECON-T/plane
1	51	306	51	306
2	46	276	0	0
3	51	306	51	306
4	48	288	0	0
5	51	306	51	306
6	48	288	0	0
7	51	306	51	306
8	48	288	0	0
9	51	306	51	306
10	48	288	0	0
11	51	306	51	306
12	49	294	0	0
13	51	306	51	306
14	51	306	0	0
15	53	318	53	318
16	51	306	0	0
17	53	318	53	318
18	51	306	0	0
19	54	324	54	324
20	51	306	0	0
21	55	330	55	330
22	51	306	0	0
23	55	330	55	330
24	54	324	0	0
25	59	354	59	354
26	57	342	0	0
27	59	354	59	354
28	57	342	0	0
Column Totals	1455	8730	745	4470
Detector Totals	-	17460	-	8940

Table 27: "CE-E ECON-T/D Count"



plane	ECON-D/120°	ECON-D/plane	ECON-T/120°	ECON-T/plane
29	115	345	115	345
30	119	357	119	357
31	123	369	123	369
32	125	375	125	375
33	125	375	125	375
34	128	384	128	384
35	144	432	144	432
36	160	480	160	480
37	100	300	100	300
38	99	297	99	297
39	100	300	100	300
40	100	300	100	300
41	76	228	76	228
42	76	228	76	228
43	56	168	56	168
44	56	168	56	168
45	56	168	56	168
46	56	168	56	168
47	40	120	40	120
48	40	120	40	120
49	40	120	40	120
50	40	120	40	120
Column Totals	1974	5922	1974	5922
Detector Totals	-	11844	-	11844

Table 28: "CE-H ECON-T/D Count"

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4.12.7 Engine-Wagon Connector Count

Tables 29 and 30 show the numbers of connectors between the LD/HD-EngineBoard and LD/HD-WagonBoard(s). The numbers are based on 2 per each side of the LD-EngineBoard and 4 for the HD-EngineBoard.

05.04.20 14:50:53		1586098253		
plane	HD/60°	HD/plane	LD/60°	LD/plane
1	16	96	32	192
2	16	96	32	192
3	16	96	32	192
4	16	96	32	192
5	16	96	32	192
6	16	96	32	192
7	16	96	32	192
8	16	96	32	192
9	16	96	32	192
10	16	96	32	192
11	16	96	32	192
12	16	96	32	192
13	16	96	32	192
14	16	96	32	192
15	16	96	36	216
16	16	96	32	192
17	16	96	36	216
18	16	96	36	216
19	16	96	36	216
20	16	96	36	216
21	16	96	36	216
22	16	96	36	216
23	16	96	36	216
24	16	96	36	216
25	16	96	36	216
26	16	96	36	216
27	16	96	36	216
28	16	96	36	216
Column Totals		448	2688	948
Detector Totals		-	5376	11376

Table 29: CE-E Engine-Wagon Connector Count



05.04.20 14:50:53	1586098253			
plane	HD/120°	HD/Plane	LD/120°	LD/Plane
29	28	84	72	216
30	28	84	76	228
31	32	96	76	228
32	28	84	76	228
33	28	84	84	252
34	28	84	96	288
35	28	84	104	312
36	24	72	116	348
37	8	24	104	312
38	0	0	100	300
39	0	0	104	312
40	0	0	104	312
41	0	0	60	180
42	0	0	60	180
43	0	0	48	144
44	0	0	52	156
45	0	0	44	132
46	0	0	44	132
47	0	0	40	120
48	0	0	40	120
49	0	0	40	120
50	0	0	44	132
Column Totals	232	696	1584	4752
Detector Totals	-	1392	-	9504

Table 30: CE-H Engine-Wagon Connector Count

4.12.8 GBTSCA Count

Tables 31 and 32 show the numbers of GBTSCA chips required for the CE-E and CE-H respectively. The numbers are based on 1 GBTSCA per LD-WagonBoard (\rightarrow one each for the inner and outer LD-WagonBoard) and 2 GBTSCAs per HD-WagonBoard.

05.04.20 14:50:53	1586098253	
plane	GBTSCA/60°	GBTSCA/plane
1	24	144
2	24	144
3	24	144
4	24	144
5	24	144
6	24	144
7	24	144
8	24	144
9	24	144
10	24	144
11	24	144
12	24	144
13	24	144
14	24	144
15	26	156
16	24	144
17	26	156
18	26	156
19	26	156
20	26	156
21	26	156
22	26	156
23	26	156
24	26	156
25	26	156
26	26	156
27	26	156
28	26	156
Column Totals	698	4188
Detector Totals	-	8376

Table 31: CE-E GBTSCA Count

05.04.20 14:50:53	1586098253	
plane	GBTSCA/120°	GBTSCA/plane
29	50	150
30	52	156
31	54	162
32	52	156
33	56	168
34	62	186
35	66	198
36	70	210
37	56	168
38	50	150
39	52	156
40	52	156
41	30	90
42	30	90
43	24	72
44	26	78
45	22	66
46	22	66
47	20	60
48	20	60
49	20	60
50	22	66
Column Totals	908	2724
Detector Totals	-	5448

Table 32: CE-H GBTSCA Count

4.12.9 LD-HexModule To HD-HexModule Conversion

With the current mapping it was necessary to connect some Full LD-HexModules to motherboards reading out Full HD-HexModules at the boundary between the LD and HD regions. Due to the differences in architecture, the LD-HexModules are currently automatically converted to HD-HexModules. The counts of these conversions per layer for the CE-E and CE-H regions are shown in tables 33 and 34.

05.04.20 14:50:53		1586098253	
plane	Count/60°	Count/Plane	
1	1	6	
2	1	6	
3	1	6	
4	1	6	
5	1	6	
6	1	6	
7	1	6	
8	1	6	
9	1	6	
10	1	6	
11	0	0	
12	0	0	
13	0	0	
14	0	0	
15	0	0	
16	0	0	
17	0	0	
18	0	0	
19	0	0	
20	0	0	
21	0	0	
22	0	0	
23	0	0	
24	0	0	
25	2	12	
26	2	12	
27	2	12	
28	2	12	
Column Totals	18	108	
Detector Totals	-	216	

Table 33: CE-E LD To HD Conversion Count

05.04.20 14:50:53		1586098253
plane	Count/120°	Count/Plane
29	2	6
30	4	12
31	10	30
32	7	21
33	9	27
34	11	33
35	11	33
36	12	36
37	4	12
38	0	0
39	0	0
40	0	0
41	0	0
42	0	0
43	0	0
44	0	0
45	0	0
46	0	0
47	0	0
48	0	0
49	0	0
50	0	0
Column Totals	70	210
Detector Totals	-	420

Table 34: CE-H LD To HD Conversion Count



4.12.10 HexModule Count

Tables 35 and 36 list the total numbers of HexModules summed over all module types for the CE-E and CE-H sections respectively (see section 4.11 for a list of the types). These tables are included as a way of making quick estimates and are perhaps superseded by tables 37 and 38. The "cO" sensors are counted as part of the "F+cO" module.

05.04.20 14:50:53	1586098253			
plane	HD/60°	HD/plane	LD/60°	LD/plane
1	12	72	36	216
2	12	72	31	186
3	12	72	36	216
4	12	72	34	204
5	12	72	36	216
6	12	72	34	204
7	12	72	36	216
8	12	72	36	216
9	12	72	39	234
10	12	72	36	216
11	13	78	38	228
12	13	78	36	216
13	13	78	38	228
14	13	78	36	216
15	13	78	38	228
16	13	78	38	228
17	13	78	38	228
18	13	78	38	228
19	13	78	38	228
20	13	78	38	228
21	13	78	39	234
22	13	78	38	228
23	13	78	39	234
24	13	78	38	228
25	13	78	41	246
26	13	78	39	234
27	13	78	42	252
28	13	78	42	252
Column Totals	354	2124	1048	6288
Detector Totals	-	4248	-	12576

Table 35: CE-E HexModule Count

05.04.20 14:50:53	1586098253			
plane	HD/120°	HD/plane	LD/120°	LD/plane
29	21	63	87	261
30	21	63	92	276
31	24	72	93	279
32	21	63	96	288
33	21	63	98	294
34	21	63	105	315
35	21	63	119	357
36	20	60	132	396
37	6	18	89	267
38	0	0	95	285
39	0	0	95	285
40	0	0	95	285
41	0	0	72	216
42	0	0	72	216
43	0	0	52	156
44	0	0	52	156
45	0	0	52	156
46	0	0	52	156
47	0	0	37	111
48	0	0	37	111
49	0	0	37	111
50	0	0	37	111
Column Totals	176	528	1696	5088
Detector Totals	-	1056	-	10176

Table 36: CE-H HexModule Count

4.12.11 HexModule Histogram

Tables 37 and 38 show the layer by layer HexModule counts by module type, for the CE-E and CE-H respectively. Note that the counting rules consider the triangle module ("cO") to include the adjacent LD full module ("FO") as being part of the same module. The partial type sensor codes are illustrated in figure 11. The sensitive thickness of the sensor is given by codes I, M, and O corresponding to $120\ \mu m$, $200\ \mu m$, and $300\ \mu m$ respectively. For completeness, figure 13 shows the partial sensor rotations and the indexing scheme used in the geometry description. Note that the counts include the modules converted from LD to HD to fit the current tiling and mixing rules (see section 4.12.9) as HD-HexModules. The LD-HexModule and HD-HexModule types map to the sensor type, however a distinction must be made for the triangles ("cO") as these sensors are to be mounted on the same "partial" as the neighbouring "FO" sensor. This implies a dedicated LD-HexModule design, that has been named "F+cO" and is shown in figure 12. Note that HexModule reflections are not counted separately.

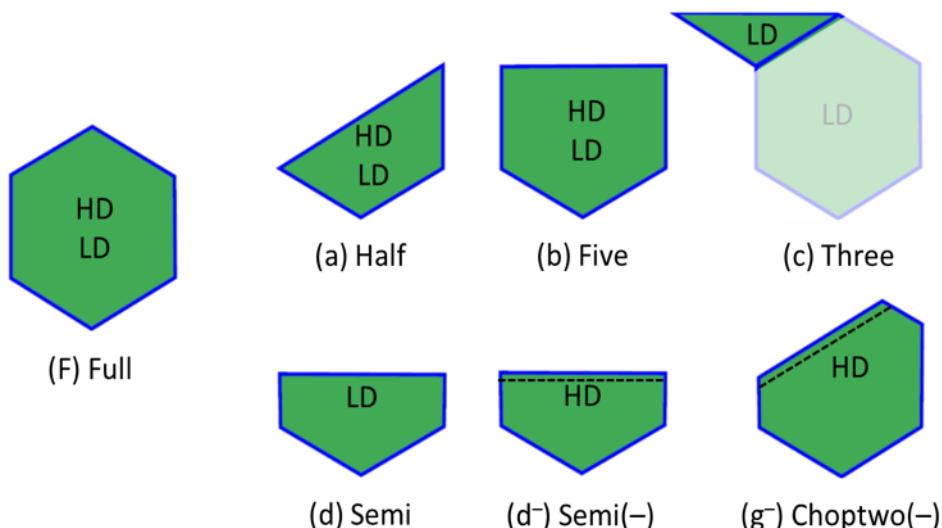


Figure 11: Silicon sensor types and their corresponding codes.

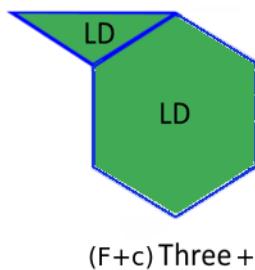


Figure 12: The "F+cO" LD-HexModule.

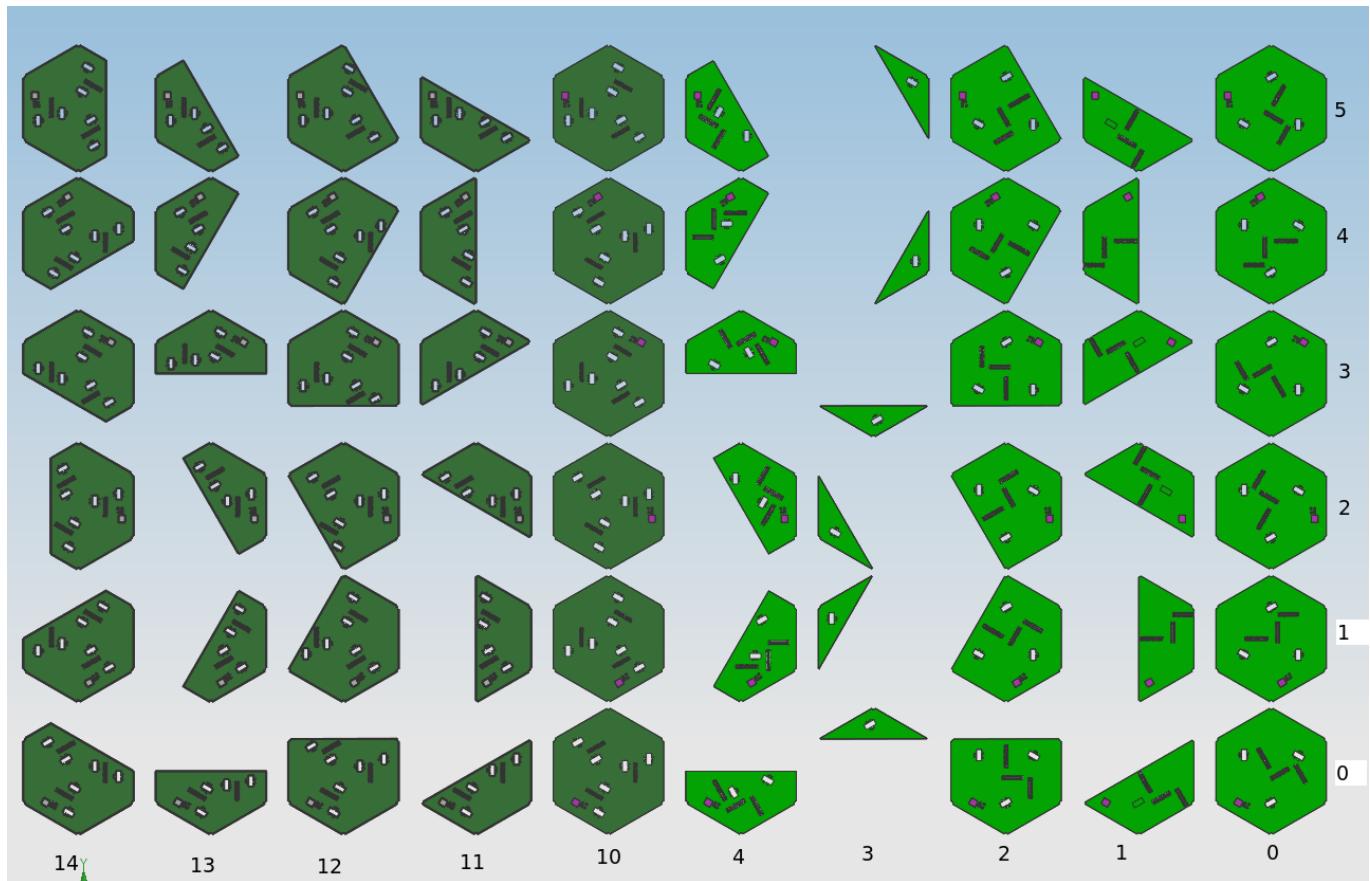
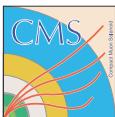


Figure 13: Silicon sensor types, rotations, and their corresponding indices. Note that connector positions are illustrative.



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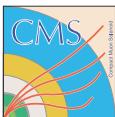
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07.04.20 13:18:57	1586265537														
Plane	Fl	aI	bI	dI	gI	FO	aO	bO	cO	F+cO	dO	FM	aM	bM	
1	10	0	0	1	1	7	2	3	0	3	1	20	0	0	
2	10	0	0	1	1	4	2	2	0	3	0	20	0	0	
3	10	0	0	1	1	7	2	3	0	3	1	20	0	0	
4	10	0	0	1	1	7	2	0	0	2	3	20	0	0	
5	10	0	0	1	1	7	2	3	0	3	1	20	0	0	
6	10	0	0	1	1	7	2	0	0	2	3	20	0	0	
7	10	0	0	1	1	7	2	3	0	3	1	20	0	0	
8	10	0	0	1	1	9	2	0	0	0	5	20	0	0	
9	10	0	0	1	1	13	3	2	0	0	1	20	0	0	
10	10	0	0	1	1	9	1	2	0	0	5	19	0	0	
11	11	0	0	1	1	13	3	2	0	0	1	19	0	0	
12	11	0	0	1	1	9	3	4	0	0	1	19	0	0	
13	11	0	0	1	1	13	3	3	0	0	0	19	0	0	
14	11	0	0	1	1	9	1	3	0	2	2	19	0	0	
15	11	0	0	1	1	13	3	1	0	2	0	19	0	0	
16	11	0	0	1	1	11	3	5	0	0	0	19	0	0	
17	11	0	0	1	1	13	3	1	0	2	0	19	0	0	
18	11	0	0	1	1	11	3	5	0	0	0	19	0	0	
19	11	0	0	1	1	12	2	2	0	3	0	19	0	0	
20	11	0	0	1	1	13	3	3	0	0	0	19	0	0	
21	11	0	0	1	1	12	1	4	0	3	0	19	0	0	
22	11	0	0	1	1	13	3	3	0	0	0	19	0	0	
23	11	0	0	1	1	12	1	4	0	3	0	19	0	0	
24	11	0	0	1	1	12	2	2	0	3	0	19	0	0	
25	11	0	0	1	1	13	1	1	0	5	2	19	0	0	
26	11	0	0	1	1	11	1	3	0	5	0	19	0	0	
27	11	0	0	1	1	15	2	0	0	4	2	19	0	0	
28	11	0	0	1	1	17	2	2	0	2	2	17	0	0	
Column Totals	298	0	0	28	28	299	60	66	0	53	31	539	0	0	
Detector Totals	3576	0	0	336	336	3588	720	792	0	636	372	6468	0	0	

Table 37: CE-E HexModule Counts By Type for 60° Sector



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Plane	Fl	al	bl	dl	gl	FO	aO	bO	cO	F+cO	dO	FM	aM	bM	
29	18	2	1	0	0	37	4	4	0	7	0	35	0	0	
30	18	2	1	0	0	44	6	0	0	6	3	33	0	0	
31	21	2	1	0	0	50	4	2	0	6	5	26	0	0	
32	18	2	1	0	0	54	6	2	0	8	1	25	0	0	
33	18	2	1	0	0	59	6	2	0	6	3	22	0	0	
34	18	2	1	0	0	73	5	5	0	2	2	18	0	0	
35	18	2	1	0	0	86	5	6	0	4	2	16	0	0	
36	17	2	1	0	0	98	8	4	0	8	0	14	0	0	
37	4	2	0	0	0	53	4	2	0	5	4	20	0	1	
38	0	0	0	0	0	54	4	2	0	4	4	24	2	1	
39	0	0	0	0	0	57	4	2	0	5	4	20	2	1	
40	0	0	0	0	0	59	4	2	0	5	4	18	2	1	
41	0	0	0	0	0	44	4	2	0	4	3	11	2	2	
42	0	0	0	0	0	46	4	2	0	4	3	9	2	2	
43	0	0	0	0	0	27	4	4	0	4	0	9	2	2	
44	0	0	0	0	0	27	4	4	0	4	0	9	2	2	
45	0	0	0	0	0	29	4	4	0	4	0	7	2	2	
46	0	0	0	0	0	32	4	4	0	4	0	4	2	2	
47	0	0	0	0	0	19	4	3	0	3	0	4	2	2	
48	0	0	0	0	0	19	4	3	0	3	0	4	2	2	
49	0	0	0	0	0	21	4	3	0	3	0	2	2	2	
50	0	0	0	0	0	23	6	3	0	3	0	0	0	2	
Column Totals	150	18	8	0	0	1011	102	65	0	102	38	330	24	24	
Detector Totals	900	108	48	0	0	6066	612	390	0	612	228	1980	144	144	

Table 38: CE-H HexModule Counts By Type for 120° Sector

4.12.12 HGCROC Count

Tables 40 and 41 show the counts by layer for the HGCROCs for the CE-E and CE-H respectively. These are based on the numbers in table 39. The triangles are assumed to contribute an extra chip (so 4 on the adjacent FO module) of which only one side is used.

Note that the component counts here are based on an estimate of number required based on the surface area of the partial relative to the full module.

Region	HD					LD							
	(f) Full	(a) Half	(b) Five	(d) Semi(-)	(g) Choptwo(-)	(f) Full	(a) Half	(b) Five	(c) Three	(d) Semi	(f) Full	(a) Half	(b) Five
Variant	Fl	al	bl	dl	gl	FO	aO	bO	cO	dO	FM	aM	bM
HGCROCs/HM	6	3	4	3	4	3	2	2	1	2	3	2	2

Table 39: HGCROC Counts for each HexModule variant



05.04.20 14:50:53	1586098253	
plane	HGCROC/60°	HGCROC/plane
1	172	1032
2	159	954
3	172	1032
4	166	996
5	172	1032
6	166	996
7	172	1032
8	168	1008
9	178	1068
10	167	1002
11	181	1086
12	173	1038
13	181	1086
14	177	1062
15	185	1110
16	179	1074
17	185	1110
18	179	1074
19	186	1116
20	181	1086
21	188	1128
22	181	1086
23	188	1128
24	186	1116
25	197	1182
26	191	1146
27	199	1194
28	195	1170
Column Totals	5024	30144
Detector Totals	-	60288

Table 40: CE-E HGCROC Count



05.04.20 14:50:53	1586098253	
plane	HGCROC/120°	HGCROC/plane
29	378	1134
30	391	1173
31	410	1230
32	405	1215
33	407	1221
34	423	1269
35	466	1398
36	504	1512
37	291	873
38	276	828
39	277	831
40	277	831
41	207	621
42	207	621
43	148	444
44	148	444
45	148	444
46	148	444
47	103	309
48	103	309
49	103	309
50	103	309
Column Totals	5923	17769
Detector Totals	-	35538

Table 41: CE-H HGCROC Count

4.12.13 LDO Count

Tables 43 and 44 show the number of LDO regulators required for the HexModules. The counting is done in accordance with LDO/HexModule list shown in table 42.

	 (f) Full	 (a) Half	 (b) Five	 (d') Semi(-)	 (g*) Choptwo(-)	 (f) Full	 (a) Half	 (b) Five	 (c) Three	 (d) Semi	 (f) Full	 (a) Half	 (b) Five	
Variant	Fl	al	bl	dl	gl	FO	aO	bO	cO	dO	FM	aM	bM	
LDOs/HM	3	2	2	2	2	1	2	1	1	2	1	2	1	1

Table 42: Breakdown of LDO usage on each HexModule variant



05.04.20 14:50:53	1586098253	
plane	LDO/60°	LDO/plane
1	76	456
2	70	420
3	76	456
4	75	450
5	76	456
6	75	450
7	76	456
8	77	462
9	77	462
10	76	456
11	79	474
12	77	462
13	78	468
14	78	468
15	80	480
16	78	468
17	80	480
18	78	468
19	80	480
20	78	468
21	80	480
22	78	468
23	80	480
24	80	480
25	86	516
26	82	492
27	87	522
28	85	510
Column Totals	2198	13188
Detector Totals	-	26376

Table 43: CE-E LDO Count

05.04.20 14:50:53	1586098253	
plane	LDO/120°	LDO/plane
29	158	474
30	167	501
31	177	531
32	171	513
33	173	519
34	174	522
35	190	570
36	205	615
37	118	354
38	109	327
39	110	330
40	110	330
41	85	255
42	85	255
43	62	186
44	62	186
45	62	186
46	62	186
47	46	138
48	46	138
49	46	138
50	46	138
Column Totals	2464	7392
Detector Totals	-	14784

Table 44: CE-H LDO Count

4.12.14 LPGBT Counts

Tables 45 and 46 show the numbers of IpGBTs required per layer, separated by DAQ and Trigger functionality for the CE-E and CE-H respectively. These numbers are based on the data rates and how they aggregate as a result of the MotherBoard tiling.

Note that:

- it is assumed that unused IpGBTs will not be fitted to the EngineBoards;
- 6 e-links/IpGBT are available for DAQ data in the LD regions; and
- 7 e-links/IpGBT are available for DAQ data in the HD regions.

Tables 47 and 48 also show the numbers of IpGBTs required per layer but for the case where the HD-WagonBoard is fitted with 2 GBTSCAs implying that both DAQ IpGBTs be fitted to the HD-EngineBoard. Note that the Trigger IpGBTs have been fixed to the maximum currently required by the mapping (4 per HD-MotherBoard) throughout. This is to illustrate the numbers required to completely homogenise the production of the HD-EngineBoard.

05.04.20 14:50:53	1586098253			
plane	DAQ/60°	DAQ/plane	TRIG/60°	TRIG/plane
1	15	90	27	162
2	15	90	0	0
3	16	96	34	204
4	16	96	0	0
5	16	96	33	198
6	16	96	0	0
7	16	96	31	186
8	16	96	0	0
9	16	96	29	174
10	15	90	0	0
11	15	90	27	162
12	15	90	0	0
13	15	90	26	156
14	15	90	0	0
15	16	96	24	144
16	15	90	0	0
17	16	96	23	138
18	16	96	0	0
19	16	96	23	138
20	16	96	0	0
21	16	96	23	138
22	16	96	0	0
23	16	96	22	132
24	16	96	0	0
25	15	90	22	132
26	15	90	0	0
27	16	96	22	132
28	16	96	0	0
Column Totals	438	2628	366	2196
Detector Totals	-	5256	-	4392

Table 45: CE-E IpGBT Count



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05.04.20 14:50:53		1586098253		
plane		DAQ/120°	DAQ/plane	TRIG/120°
29		29	87	41
30		29	87	42
31		27	81	43
32		27	81	42
33		28	84	43
34		31	93	44
35		33	99	50
36		35	105	53
37		28	84	34
38		25	75	35
39		26	78	36
40		26	78	36
41		15	45	27
42		15	45	27
43		12	36	22
44		13	39	22
45		11	33	22
46		11	33	22
47		10	30	11
48		10	30	11
49		10	30	11
50		11	33	11
Column Totals		462	1386	685
Detector Totals		-	2772	2055

Table 46: CE-H IpGBT Count

05.04.20 14:50:53		1586098253			
plane		DAQ/60°	DAQ/plane	TRIG/60°	TRIG/plane
1		16	96	32	192
2		16	96	0	0
3		18	108	35	210
4		17	102	0	0
5		18	108	34	204
6		17	102	0	0
7		18	108	33	198
8		16	96	0	0
9		16	96	32	192
10		16	96	0	0
11		17	102	32	192
12		17	102	0	0
13		17	102	32	192
14		17	102	0	0
15		18	108	32	192
16		17	102	0	0
17		18	108	32	192
18		18	108	0	0
19		18	108	32	192
20		18	108	0	0
21		18	108	32	192
22		18	108	0	0
23		18	108	32	192
24		18	108	0	0
25		17	102	32	192
26		17	102	0	0
27		17	102	32	192
28		17	102	0	0
Column Totals		483	2898	454	2724
Detector Totals		-	5796	-	5448

Table 47: CE-E IpGBT Count with 2 HD DAQ IpGBTs

05.04.20 14:50:53		1586098253			
plane		DAQ/120°	DAQ/plane	TRIG/120°	TRIG/plane
29		32	96	62	186
30		33	99	63	189
31		35	105	67	201
32		34	102	63	189
33		35	105	64	192
34		39	117	65	195
35		43	129	71	213
36		45	135	71	213
37		30	90	40	120
38		25	75	35	105
39		27	81	36	108
40		26	78	36	108
41		16	48	27	81
42		15	45	27	81
43		12	36	22	66
44		13	39	22	66
45		12	36	22	66
46		12	36	22	66
47		10	30	11	33
48		10	30	11	33
49		10	30	11	33
50		11	33	11	33
Column Totals		525	1575	859	2577
Detector Totals		-	3150	-	5154

Table 48: CE-H IpGBT Count with 2 HD DAQ IpGBTs

4.12.15 WagonBoard to HexModule Connector Count

Tables 50 and 51 show the connector counts required by type and by plane for the CE-E and CE-H regions respectively. These counts are based on the numbers of connections per HexModule shown in table 49. Note that the mated pair is counted. If these are purchased separately, then the cost of each will need to be added together for the system cost.

For a deeper description of the HexModule types, please refer to table 12 in section 4.11.

Region	HD					LD							
	(f) Full	(a) Half	(b) Five	(d) Semil(-)	(g) Choptwo(-)	(f) Full	(a) Half	(b) Five	(f+c) Three +	(d) Semi	(f) Full	(a) Half	(b) Five
Variant	Fl	al	bl	dl	gl	FO	aO	bO	F+cO	dO	FM	aM	bM
FX11/HM	3	2	3	2	3	1	1	1	1	1	1	1	1

Table 49: FX11 Connector Pairs by HexModule variant

05.04.20 14:50:53	1586098253			
plane	HD/60°	HD/plane	LD/60°	LD/plane
1	35	210	36	216
2	35	210	31	186
3	35	210	36	216
4	35	210	34	204
5	35	210	36	216
6	35	210	34	204
7	35	210	36	216
8	35	210	36	216
9	35	210	39	234
10	35	210	36	216
11	38	228	38	228
12	38	228	36	216
13	38	228	38	228
14	38	228	36	216
15	38	228	38	228
16	38	228	38	228
17	38	228	38	228
18	38	228	38	228
19	38	228	38	228
20	38	228	38	228
21	38	228	39	234
22	38	228	38	228
23	38	228	39	234
24	38	228	38	228
25	38	228	41	246
26	38	228	39	234
27	38	228	42	252
28	38	228	42	252
Column Totals	1048	6288	1034	6204
Detector Totals	-	12576	-	12408

Table 50: CE-E WagonBoard to HexModule Connector Count

plane	HD/120°	HD/plane	LD/120°	LD/plane
29	61	183	87	261
30	61	183	92	276
31	70	210	93	279
32	61	183	96	288
33	61	183	98	294
34	61	183	105	315
35	61	183	119	357
36	58	174	132	396
37	16	48	89	267
38	0	0	95	285
39	0	0	95	285
40	0	0	95	285
41	0	0	72	216
42	0	0	72	216
43	0	0	52	156
44	0	0	52	156
45	0	0	52	156
46	0	0	52	156
47	0	0	37	111
48	0	0	37	111
49	0	0	37	111
50	0	0	37	111
Column Totals	1696	5088	510	1530
Detector Totals	-	10176	-	3060

Table 51: CE-H WagonBoard to HexModule Connector Count

4.12.16 MotherBoard Count

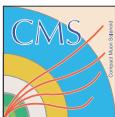
Tables 52 and 53 show the numbers of MotherBoards by plane for the CE-E and CE-H regions respectively. Note that the HD-MotherBoard comprises one HD-EngineBoard and one HD-WagonBoard and the LD-MotherBoard comprises one LD-EngineBoard and two LD-WagonBoards. The latter is explicitly enumerated in the right-most column of each table.

05.04.20 14:50:53	1586098253				
plane	HD/60°	HD/plane	LD/60°	LD/plane	LD-Wagons/plane
1	4	24	8	48	96
2	4	24	8	48	96
3	4	24	8	48	96
4	4	24	8	48	96
5	4	24	8	48	96
6	4	24	8	48	96
7	4	24	8	48	96
8	4	24	8	48	96
9	4	24	8	48	96
10	4	24	8	48	96
11	4	24	8	48	96
12	4	24	8	48	96
13	4	24	8	48	96
14	4	24	8	48	96
15	4	24	9	54	108
16	4	24	8	48	96
17	4	24	9	54	108
18	4	24	9	54	108
19	4	24	9	54	108
20	4	24	9	54	108
21	4	24	9	54	108
22	4	24	9	54	108
23	4	24	9	54	108
24	4	24	9	54	108
25	4	24	9	54	108
26	4	24	9	54	108
27	4	24	9	54	108
28	4	24	9	54	108
Column Totals	112	672	237	1422	2844
Detector Totals	-	1344	-	2844	5688

Table 52: CE-E MotherBoard Count

plane	HD/120°	HD/plane	LD/120°	LD/plane	LD-Wagons/plane
29	7	21	18	54	108
30	7	21	19	57	114
31	8	24	19	57	114
32	7	21	19	57	114
33	7	21	21	63	126
34	7	21	24	72	144
35	7	21	26	78	156
36	6	18	29	87	174
37	2	6	26	78	156
38	0	0	25	75	150
39	0	0	26	78	156
40	0	0	26	78	156
41	0	0	15	45	90
42	0	0	15	45	90
43	0	0	12	36	72
44	0	0	13	39	78
45	0	0	11	33	66
46	0	0	11	33	66
47	0	0	10	30	60
48	0	0	10	30	60
49	0	0	10	30	60
50	0	0	11	33	66
Column Totals	58	174	396	1188	2376
Detector Totals	-	348	-	2376	4752

Table 53: CE-H MotherBoard Count



4.12.17 Power Connector

Tables 54 and 55 show the power connectors required for the HD and LD cases, by plane, for the CE-E and CE-H respectively. These numbers are based on a single connection to each LD-HexModule and two connectors to each HD-WagonBoard, through the power connector adapter card. The counts here represent the connector pairs.

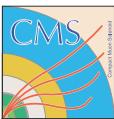
05.04.20 14:50:53	1586098253			
plane	HD/60°	HD/plane	LD/60°	LD/plane
1	8	48	39	234
2	8	48	34	204
3	8	48	39	234
4	8	48	36	216
5	8	48	39	234
6	8	48	36	216
7	8	48	39	234
8	8	48	36	216
9	8	48	39	234
10	8	48	36	216
11	8	48	38	228
12	8	48	36	216
13	8	48	38	228
14	8	48	38	228
15	8	48	40	240
16	8	48	38	228
17	8	48	40	240
18	8	48	38	228
19	8	48	41	246
20	8	48	38	228
21	8	48	42	252
22	8	48	38	228
23	8	48	42	252
24	8	48	41	246
25	8	48	46	276
26	8	48	44	264
27	8	48	46	276
28	8	48	44	264
Column Totals	224	1344	1101	6606
Detector Totals	-	2688	-	13212

Table 54: CE-E Power Connector Count



05.04.20 14:50:53	1586098253			
plane	HD/120°	HD/Plane	LD/120°	LD/Plane
29	14	42	94	282
30	14	42	98	294
31	16	48	99	297
32	14	42	104	312
33	14	42	104	312
34	14	42	107	321
35	14	42	123	369
36	12	36	140	420
37	4	12	94	282
38	0	0	99	297
39	0	0	100	300
40	0	0	100	300
41	0	0	76	228
42	0	0	76	228
43	0	0	56	168
44	0	0	56	168
45	0	0	56	168
46	0	0	56	168
47	0	0	40	120
48	0	0	40	120
49	0	0	40	120
50	0	0	40	120
Column Totals	116	348	1798	5394
Detector Totals	-	696	-	10788

Table 55: CE-H Power Connector Count



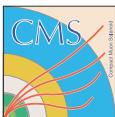
4.12.18 VTRX+ Counts

Tables 56 and 57 show the VTRX+ counts by plane and cassette/cassette pair for the CE-E and CE-H respectively when counted using the reductionist approach of not mounting VTRX+ components when the bandwidth requirements permit it. This counting proceeds by assuming that the LD-EngineBoard will only ever be fitted with a single VTRX+ module, and the HD-EngineBoard will be fitted with either 1 or 2 VTRX+ modules, with the lowest value permitted by the number of 10gb/s DAQ links, and the sum of the number of 10gb/s DAQ and trigger links. This requirement is used to facilitate the uniformity of the firmware in the off-detector region. See the IGBT section (4.12.14) for a description of the 10gb/s counting rules in use.

Tables 58 and 59 show the VTRX+ counts by plane and cassette/cassette pair for the CE-E and CE-H respectively when counted using the requirement that the HD-EngineBoard always be fitted with 2 VTRX+ modules to permit access to the control and monitoring functionality provided by the second GBTSCA on the HD-WagonBoard.

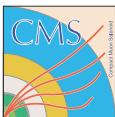
05.04.20 14:50:53		1586098253			
plane	10gbps link count/60°	10gbps link count/plane	VTRX+/60°	VTRX+/plane	
1	42	252	15	90	
2	15	90	15	90	
3	50	300	16	96	
4	16	96	16	96	
5	49	294	16	96	
6	16	96	16	96	
7	47	282	16	96	
8	16	96	16	96	
9	45	270	16	96	
10	15	90	15	90	
11	42	252	15	90	
12	15	90	15	90	
13	41	246	15	90	
14	15	90	15	90	
15	40	240	16	96	
16	15	90	15	90	
17	39	234	16	96	
18	16	96	16	96	
19	39	234	16	96	
20	16	96	16	96	
21	39	234	16	96	
22	16	96	16	96	
23	38	228	16	96	
24	16	96	16	96	
25	37	222	15	90	
26	15	90	15	90	
27	38	228	16	96	
28	16	96	16	96	
Column Totals	804	4824	438	2628	
Detector Totals	-	9648	-	5256	

Table 56: CE-E VTRX+ Count



05.04.20 14:50:53	1586098253			
plane	10gbps link count/120°	10gbps link count/plane	VTRX+/120°	VTRX+/plane
29	70	210	29	87
30	71	213	29	87
31	70	210	27	81
32	69	207	27	81
33	71	213	28	84
34	75	225	31	93
35	83	249	33	99
36	88	264	35	105
37	62	186	28	84
38	60	180	25	75
39	62	186	26	78
40	62	186	26	78
41	42	126	15	45
42	42	126	15	45
43	34	102	12	36
44	35	105	13	39
45	33	99	11	33
46	33	99	11	33
47	21	63	10	30
48	21	63	10	30
49	21	63	10	30
50	22	66	11	33
Column Totals	1147	3441	462	1386
Detector Totals	-	6882	-	2772

Table 57: CE-H VTRX+ Count



05.04.20 14:50:53	1586098253					
plane	10gbps link count/60°	10gbps link count/plane	VTRX+/60°	VTRX+/plane	Simple Counts/60°	Simple Counts/plane
1	48	288	16	96	16	96
2	32	192	16	96	16	96
3	53	318	16	96	16	96
4	33	198	16	96	16	96
5	52	312	16	96	16	96
6	33	198	16	96	16	96
7	51	306	16	96	16	96
8	32	192	16	96	16	96
9	48	288	16	96	16	96
10	32	192	16	96	16	96
11	49	294	16	96	16	96
12	33	198	16	96	16	96
13	49	294	16	96	16	96
14	33	198	16	96	16	96
15	50	300	17	102	17	102
16	33	198	16	96	16	96
17	50	300	17	102	17	102
18	34	204	17	102	17	102
19	50	300	17	102	17	102
20	34	204	17	102	17	102
21	50	300	17	102	17	102
22	34	204	17	102	17	102
23	50	300	17	102	17	102
24	34	204	17	102	17	102
25	49	294	17	102	17	102
26	33	198	17	102	17	102
27	49	294	17	102	17	102
28	33	198	17	102	17	102
Column Totals	1161	6966	461	2766	461	2766
Detector Totals	-	13932	-	5532	-	5532

Table 58: Simple CE-E VTRX+ Count



05.04.20 14:50:53	1586098253					
plane	10gbps link count/120°	10gbps link count/plane	VTRX+/120°	VTRX+/plane	Simple Counts/60°	Simple Counts/plane
29	94	282	32	96	32	96
30	96	288	33	99	33	99
31	102	306	35	105	35	105
32	97	291	33	99	33	99
33	99	297	35	105	35	105
34	104	312	38	114	38	114
35	114	342	40	120	40	120
36	116	348	41	123	41	123
37	70	210	30	90	30	90
38	60	180	25	75	25	75
39	63	189	26	78	26	78
40	62	186	26	78	26	78
41	43	129	15	45	15	45
42	42	126	15	45	15	45
43	34	102	12	36	12	36
44	35	105	13	39	13	39
45	34	102	11	33	11	33
46	34	102	11	33	11	33
47	21	63	10	30	10	30
48	21	63	10	30	10	30
49	21	63	10	30	10	30
50	22	66	11	33	11	33
Column Totals	1384	4152	512	1536	512	1536
Detector Totals	-	8304	-	3072	-	3072

Table 59: Simple CE-H VTRX+ Count



4.12.19 VTRX+ Multiplicity Histograms

Tables 60, 61, 62, 63 show the counts of the number of VTRx+ modules required by each plane

Plane	0	1	2	3	4	5
1	0	0	24	0	0	0
2	0	0	24	0	0	0
3	0	0	24	0	0	0
4	0	0	24	0	0	0
5	0	0	24	0	0	0
6	0	0	24	0	0	0
7	0	0	24	0	0	0
8	0	0	24	0	0	0
9	0	0	24	0	0	0
10	0	0	24	0	0	0
11	0	0	24	0	0	0
12	0	0	24	0	0	0
13	0	0	24	0	0	0
14	0	0	24	0	0	0
15	0	0	24	0	0	0
16	0	0	24	0	0	0
17	0	0	24	0	0	0
18	0	0	24	0	0	0
19	0	0	24	0	0	0
20	0	0	24	0	0	0
21	0	0	24	0	0	0
22	0	0	24	0	0	0
23	0	0	24	0	0	0
24	0	0	24	0	0	0
25	0	0	24	0	0	0
26	0	0	24	0	0	0
27	0	0	24	0	0	0
28	0	0	24	0	0	0
Totals	0	0	672	0	0	0
Detector Totals	0	0	1344	0	0	0

Table 60: CE-E VTRX+ HD Multiplicity Count



05.04.20 14:50:53	1586098253					
Plane	0	1	2	3	4	5
29	0	0	21	0	0	0
30	0	0	21	0	0	0
31	0	0	24	0	0	0
32	0	0	21	0	0	0
33	0	0	21	0	0	0
34	0	0	21	0	0	0
35	0	0	21	0	0	0
36	0	0	18	0	0	0
37	0	0	6	0	0	0
38	0	0	0	0	0	0
39	0	0	0	0	0	0
40	0	0	0	0	0	0
41	0	0	0	0	0	0
42	0	0	0	0	0	0
43	0	0	0	0	0	0
44	0	0	0	0	0	0
45	0	0	0	0	0	0
46	0	0	0	0	0	0
47	0	0	0	0	0	0
48	0	0	0	0	0	0
49	0	0	0	0	0	0
50	0	0	0	0	0	0
Totals	0	0	174	0	0	0
Detector Totals	0	0	348	0	0	0

Table 61: CE-H VTRX+ HD Multiplicity Count



05.04.20 14:50:53		1586098253						
Plane		0	1	2	3	4	5	
1		0	48	0	0	0	0	0
2		0	48	0	0	0	0	0
3		0	48	0	0	0	0	0
4		0	48	0	0	0	0	0
5		0	48	0	0	0	0	0
6		0	48	0	0	0	0	0
7		0	48	0	0	0	0	0
8		0	48	0	0	0	0	0
9		0	48	0	0	0	0	0
10		0	48	0	0	0	0	0
11		0	48	0	0	0	0	0
12		0	48	0	0	0	0	0
13		0	48	0	0	0	0	0
14		0	48	0	0	0	0	0
15		0	54	0	0	0	0	0
16		0	48	0	0	0	0	0
17		0	54	0	0	0	0	0
18		0	54	0	0	0	0	0
19		0	54	0	0	0	0	0
20		0	54	0	0	0	0	0
21		0	54	0	0	0	0	0
22		0	54	0	0	0	0	0
23		0	54	0	0	0	0	0
24		0	54	0	0	0	0	0
25		0	54	0	0	0	0	0
26		0	54	0	0	0	0	0
27		0	54	0	0	0	0	0
28		0	54	0	0	0	0	0
Totals		0	1422	0	0	0	0	0
Detector Totals		0	2844	0	0	0	0	0

Table 62: CE-E VTRX+ LD Multiplicity Count



05.04.20 14:50:53	1586098253					
Plane	0	1	2	3	4	5
29	0	54	0	0	0	0
30	0	57	0	0	0	0
31	0	57	0	0	0	0
32	0	57	0	0	0	0
33	0	63	0	0	0	0
34	0	72	0	0	0	0
35	0	78	0	0	0	0
36	0	87	0	0	0	0
37	0	78	0	0	0	0
38	0	75	0	0	0	0
39	0	78	0	0	0	0
40	0	78	0	0	0	0
41	0	45	0	0	0	0
42	0	45	0	0	0	0
43	0	36	0	0	0	0
44	0	39	0	0	0	0
45	0	33	0	0	0	0
46	0	33	0	0	0	0
47	0	30	0	0	0	0
48	0	30	0	0	0	0
49	0	30	0	0	0	0
50	0	33	0	0	0	0
Totals	0	1188	0	0	0	0
Detector Totals	0	2376	0	0	0	0

Table 63: CE-H VTRX+ LD Multiplicity Count

4.12.20 WagonBoard Zoo

Tables 65 and 66, and show the types and counts for the CE-E and CE-H HD-WagonBoards, and the CE-E and CE-H LD-WagonBoards respectively.

The types and numbers are counted from the outputs of the eLink allocation algorithm. Currently no effort to minimise these has been invested, so some reduction in the number of different LD types is possible by judicious LD-EngineBoard placement. The "F+cO" modules are counted separately from the "F" modules. These two types could possibly be combined. Note that peripheral rotations are not yet considered, which could further increase the number of variants. The WagonBoard "Type" descriptor comprises "dash" separated characters. The explanation of these fields is shown in table 64.

Field	Valid Values	Meaning	Explanation
1	[L,W]	Linear,Wedge	WagonBoard shape
2	[HD,LDO,LDI]	High Density,LowDensity-Outer/LowDensity-Inner	
3-4,5..	[a,b,c,d,F,g]	HexModule shape	See table 12

Table 64: WagonBoard Type Descriptors

Index	WagonBoard Type	Count
1	L-HD-d-F-F	120
2	L-HD-g-F-F	336
3	L-HD-F-F-F	456
4	W-HD-F-F-F	408
5	L-HD-d-F-F-F	216
6	L-HD-a-F-F	96
7	L-HD-b-F-F	48
8	L-HD-a-F-F-F	12
	Detector Total	1692

Table 65: CE-E-and-CE-H HD-Wagonboard Types and Full Detector Counts

Inner/Outer	Index	WagonBoard Type	Count
I	1	L-LDI-F-F	3444
I	2	W-LDI-F-F-b	108
I	3	W-LDI-F-F	156
I	4	W-LDI-F-F-a	18
I	5	W-LDI-F-F-d	126
I	6	W-LDI-F-F-F	78
I	7	W-LDI-F-F-c	114
I	8	L-LDI-F	360
I	9	W-LDI-F-b	36
I	10	L-LDI-F-F-F	420
I	11	W-LDI-F-b-c	6
I	12	W-LDI-F-d	36
I	13	W-LDI-F-b-d	6
I	14	W-LDI-F-a	6
I	15	W-LDI-F-F-F-c	6
I	16	L-LDI-b	24
I	17	L-LDI-a	36
I	18	L-LDI-a-F-F	24
I	19	L-LDI-b-F-F	24
I	20	L-LDI-a-F	96
I	21	L-LDI-b-F	96
Detector Total			5220
O	1	L-LDO-F-F-c	570
O	2	L-LDO-F-F-b	372
O	3	L-LDO-F-F	1098
O	4	L-LDO-F-F-a	930
O	5	L-LDO-F-a	348
O	6	W-LDO-F-d-b	60
O	7	L-LDO-F-b	312
O	8	L-LDO-F-c	228
O	9	W-LDO-F-c	84
O	10	W-LDO-F-d-d	66
O	11	L-LDO-F-d	54
O	12	L-LDO-F-d	108
O	13	L-LDO-F-F	468
O	14	W-LDO-F-d-F	24
O	15	W-LDO-F-b-F	12
O	16	W-LDO-F-b-b	60
O	17	W-LDO-b	126
O	18	W-LDO-F-c-c	60
O	19	W-LDO-b-c	6
O	20	W-LDO-F-c-F	6
O	21	W-LDO-F-d	18
O	22	W-LDO-d	24
O	23	L-LDO-F-F-F-c	30
O	24	W-LDO-F-b	6
O	25	W-LDO-F	78
O	26	L-LDO-b	6
O	27	W-LDO-	6
O	28	W-LDO-F-d-F-c	6
O	29	W-LDO-b-d	6
O	30	W-LDO-a	6
O	31	W-LDO-F-F	6
O	32	W-LDO-a-c	6
O	33	W-LDO-F-a-F-c-c	6
O	34	W-LDO-F-F-F-c-c	18
O	35	W-LDO-F-F-F-c-c-c	6
Detector Total			5220

Table 66: CE-E-and-CE-H LD-Wagonboard Types and Full Detector Counts

4.12.21 Summary Table

Table 67 shows a summary of the key components counted for both end-caps of the detector, shown the the CE-E and CE-H separately. This table is effectively the last row in those tables detailed in the preceding subsections. Please refer to each section for a description of the counting method employed.

05.04.20 14:50:53	1586098253			
Component	Usage	CE-E	CE-H	Total
Concentrator Mezz	single populated	6168	0	6168
Concentrator Mezz	dual populated	6408	10176	16584
FX11(100-pin;3mm)	LD Wagon-HexMod	12576	10176	22752
FX11(100-pin;3mm)	HD Wagon-HexMod	12408	3060	15468
FX11(80-pin;2mm)	LD HexMod-Concentrator	25152	20352	45504
Molex 5054730810	LD HexMod Pwr Connector	13212	10788	24000
Molex 5054730810	HD Wagon Pwr Connector	2688	696	3384
LTH-030-01-G-D	LD Engine-Wagon Connector	11376	9504	20880
LTH-030-01-G-D	HD Engine-Wagon Connector	5376	1392	6768
Single Engine + 2 Wagons	LD	2844	2376	5220
Double Engine + 1 Wagon	HD	1344	348	1692
DCDC Converter	Single Module	1092	984	2076
DCDC Converter	Dual Module	11484	9192	20676
LDO	VDDA on HexMod	26376	14784	41160
bPOL2v5	Power regulation:HD region	28056	10368	38424
bPOL12	Power regulation:LD region	24060	19368	43428
PPWRMOD	Peripheral Regulation:HD	1344	348	1692
PPWRMOD	Peripheral Regulation:LD	672	546	1218
bPOL12V	Peripheral Regulation:HD	5592	1404	6996
bPOL12V	Peripheral Regulation:LD	2844	2376	5220
GBTSCA	LD and HD Ctrl & monitoring	8376	5448	13824
HGCROC	LD and HD regions	60288	35538	95826
lpGBT	Data	5256	2772	8028
lpGBT	Trigger	4392	4110	8502
lpGBT	Data:2nd rule set	5796	3150	8946
lpGBT	Trigger:2nd rule set	5448	5154	10602
ECON-D	LD and HD regions	17460	11844	29304
ECON-T	LD and HD regions	8940	11844	20784
VTRx+	LD and HD Regions	5256	2772	8028

Table 67: Total Component Counts



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5 Conclusions



A Tiling Scheme For All Layers

At the time the MotherBoard tiling was done, there was a bug in the code that calculates the UV indices for the CE-H region. This resulted in the indices needing to be incremented by 1 (in both directions).



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A.0.1 CE-E

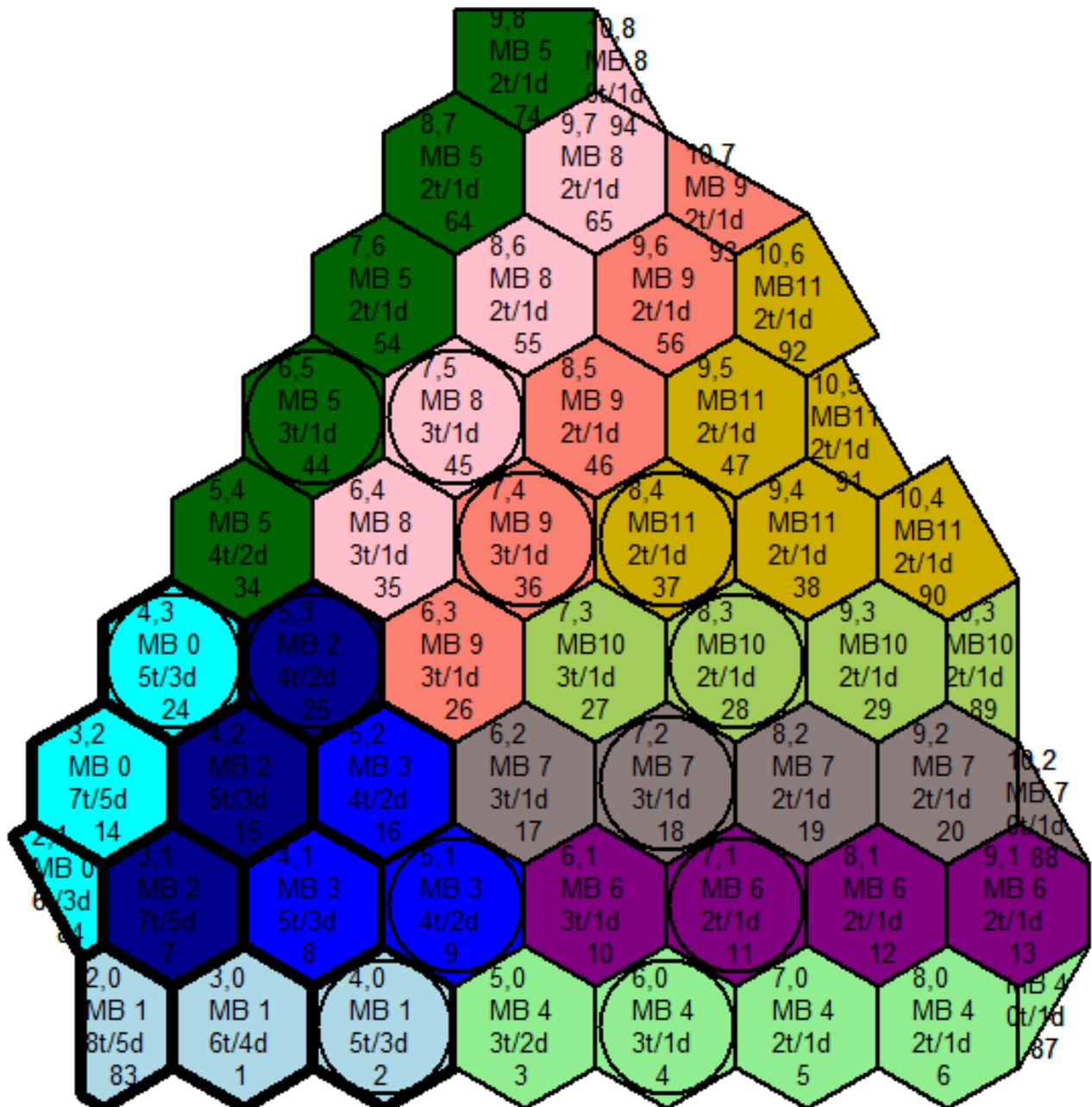


Figure 14: Tiling assignment for CE-E Cassette 0, Layer 1

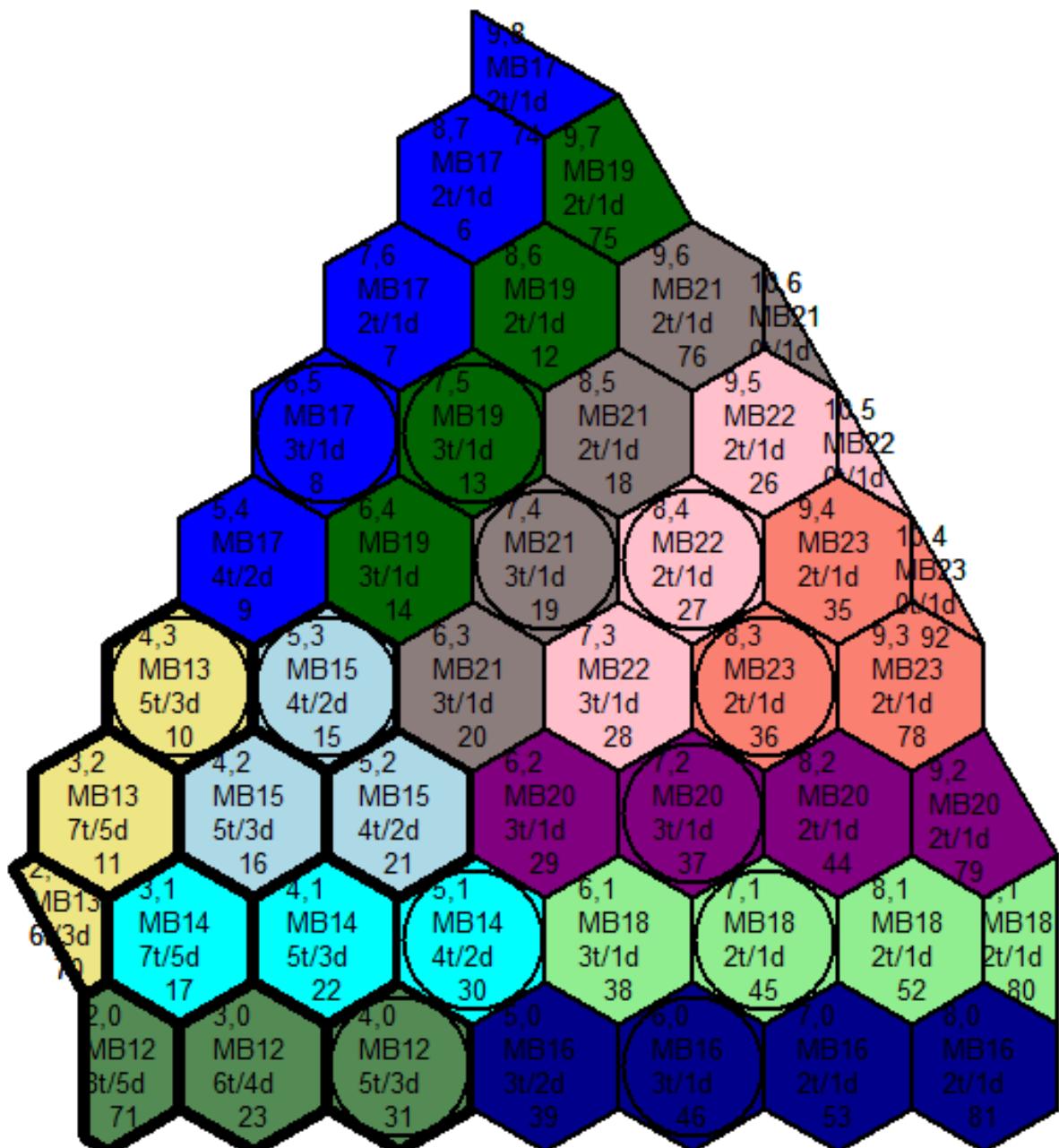


Figure 15: Tiling assignment for CE-E Cassette 0, Layer 2

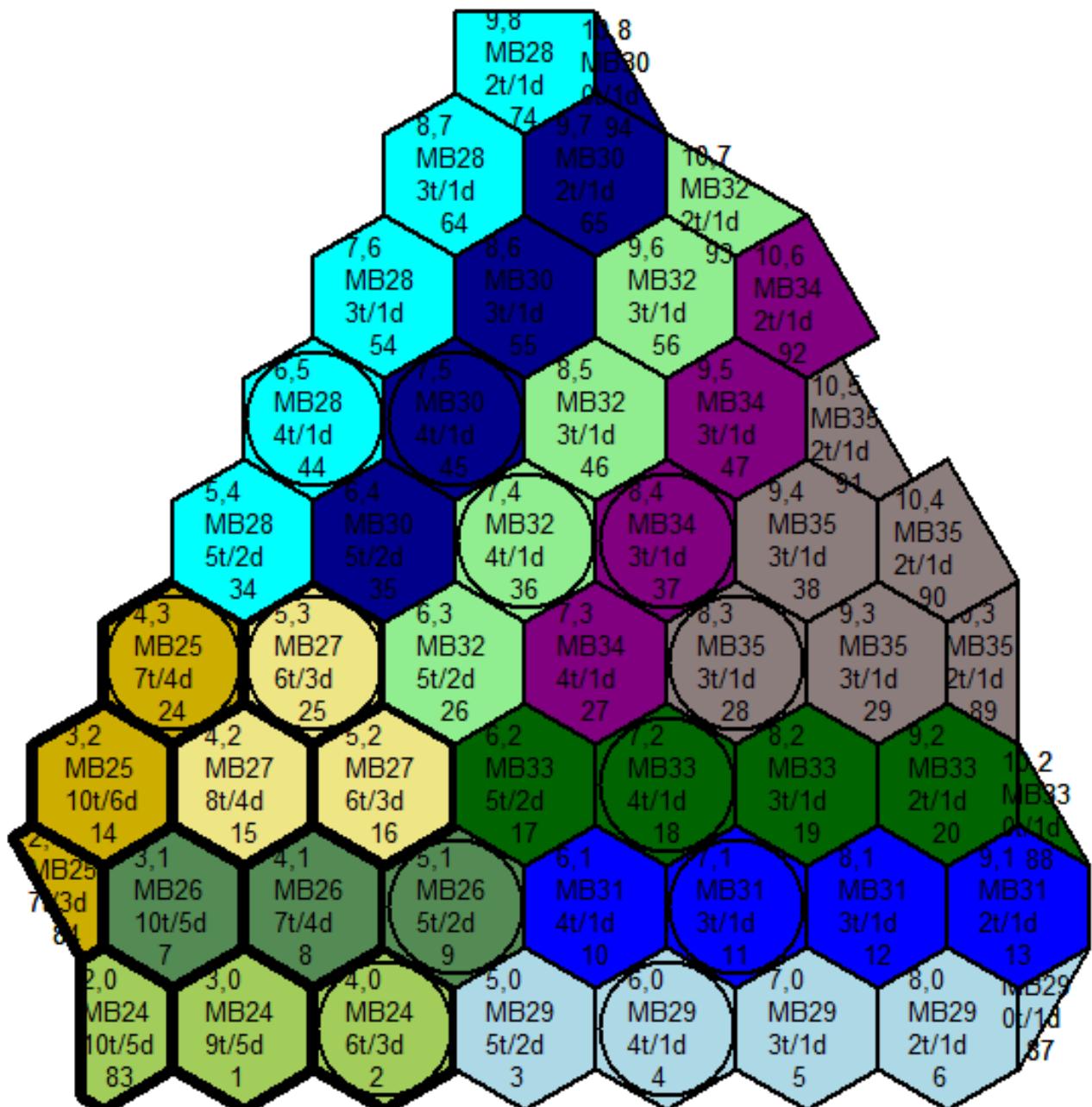


Figure 16: Tiling assignment for CE-E Cassette 0, Layer 3

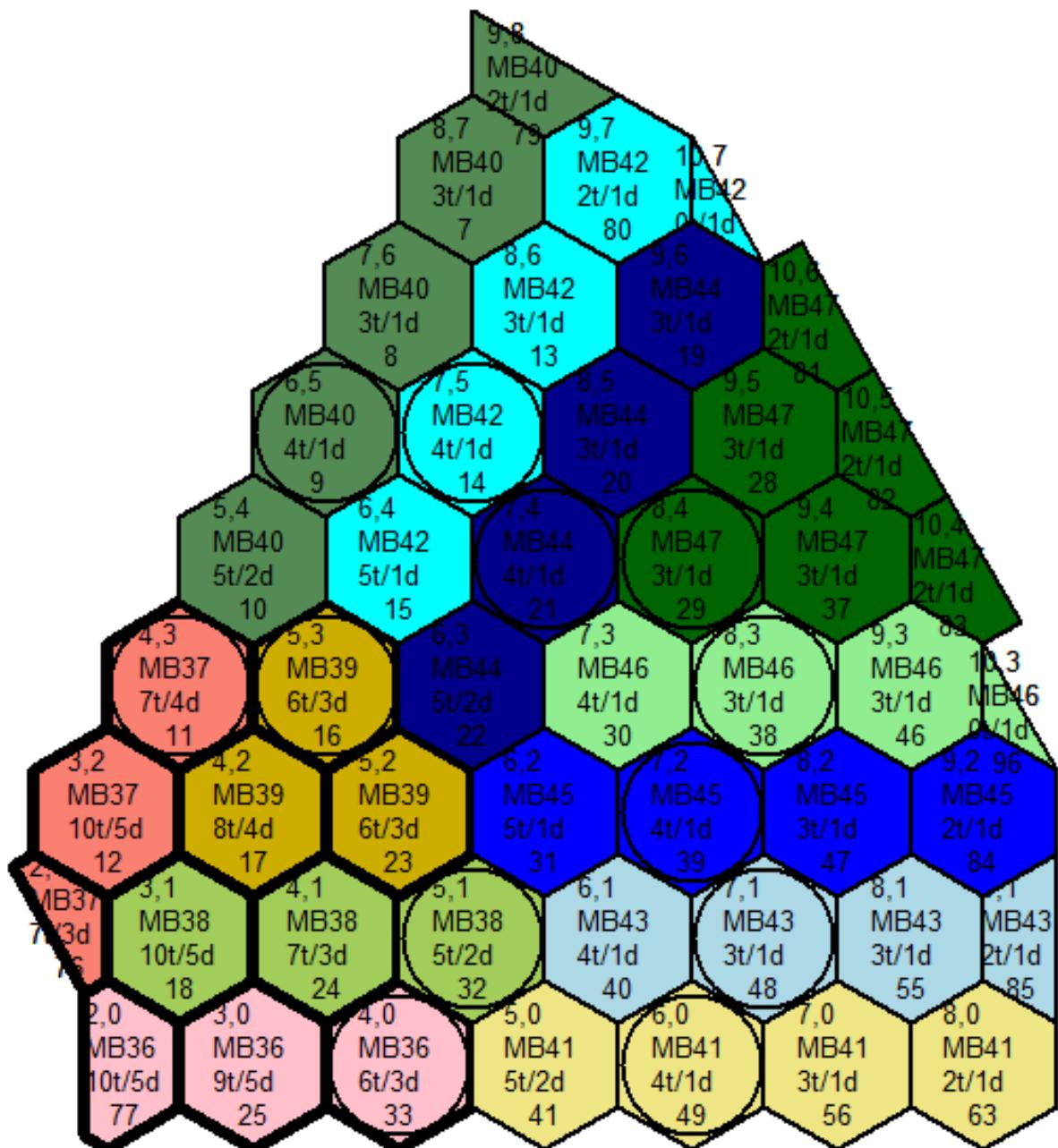


Figure 17: Tiling assignment for CE-E Cassette 0, Layer 4

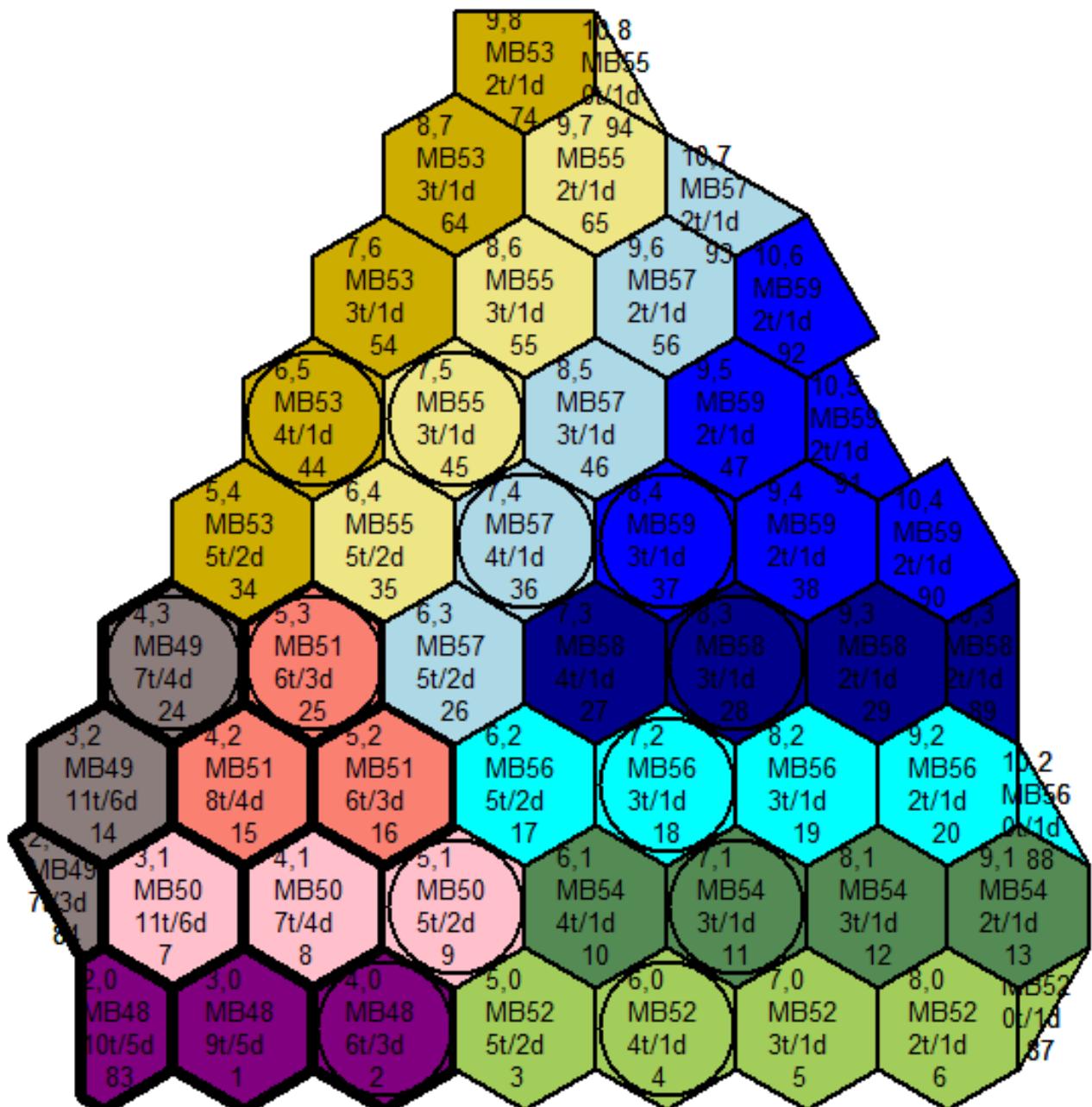


Figure 18: Tiling assignment for CE-E Cassette 0, Layer 5

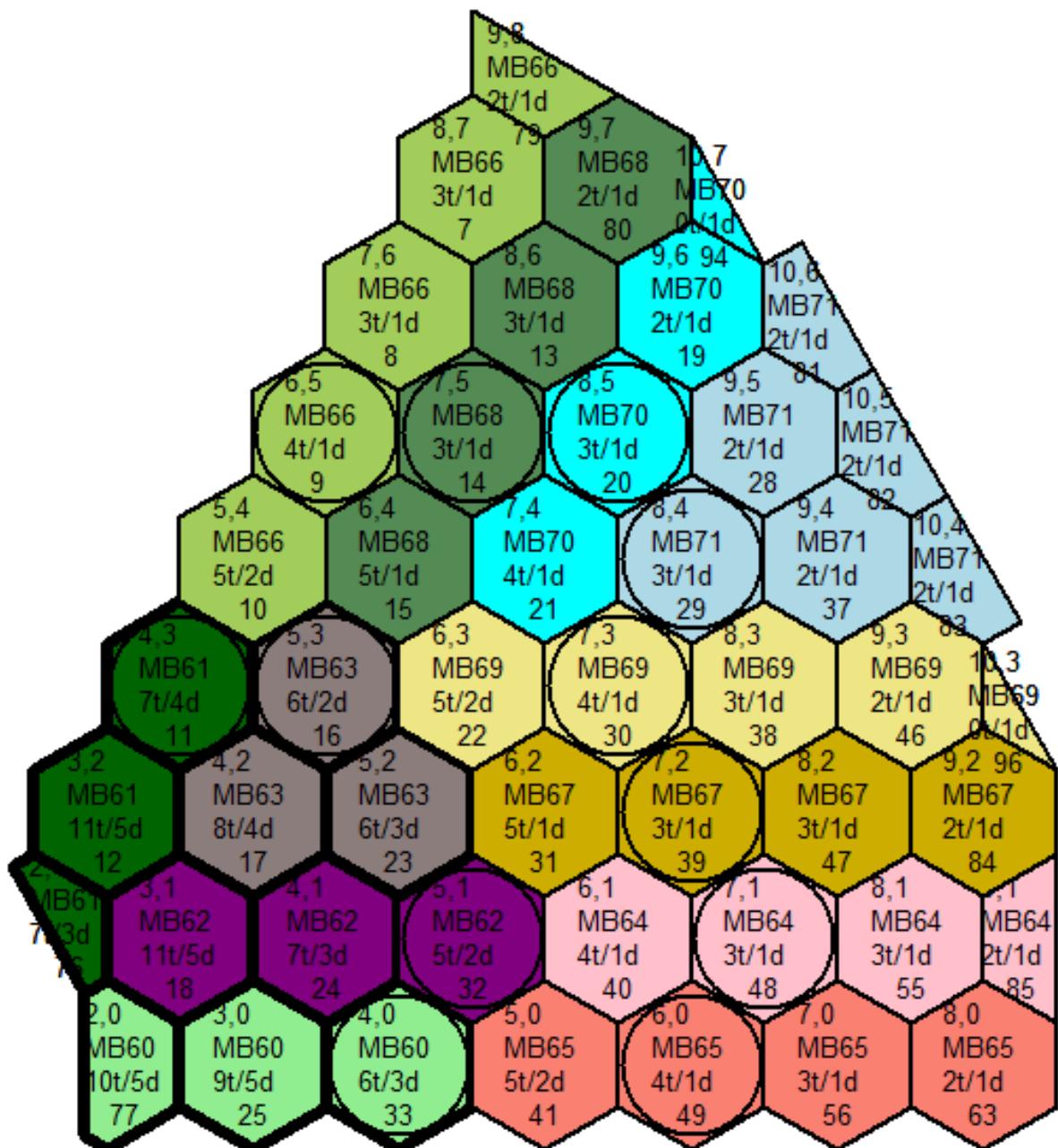


Figure 19: Tiling assignment for CE-E Cassette 0, Layer 6

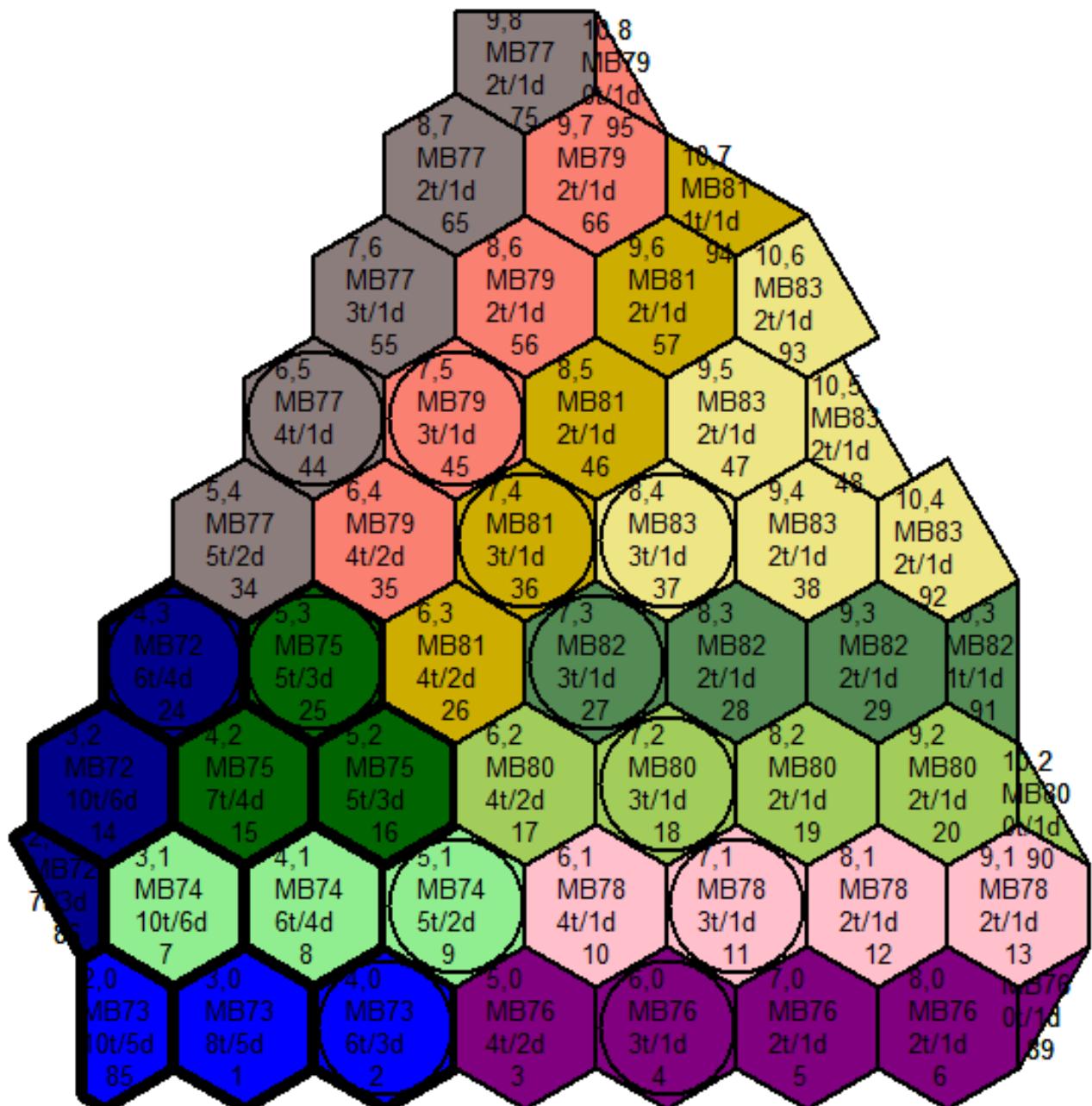


Figure 20: Tiling assignment for CE-E Cassette 0, Layer 7

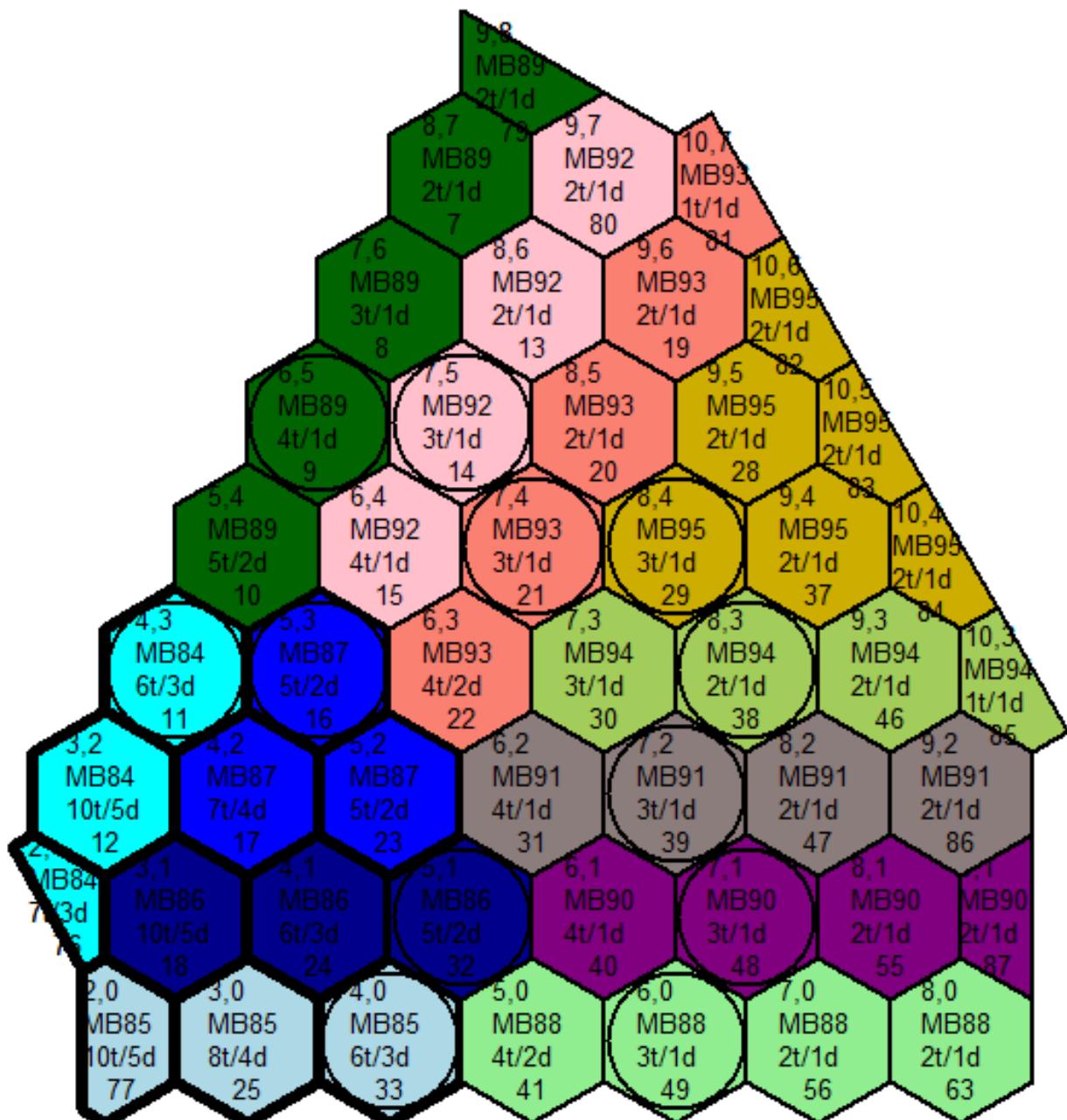


Figure 21: Tiling assignment for CE-E Cassette 0, Layer 8

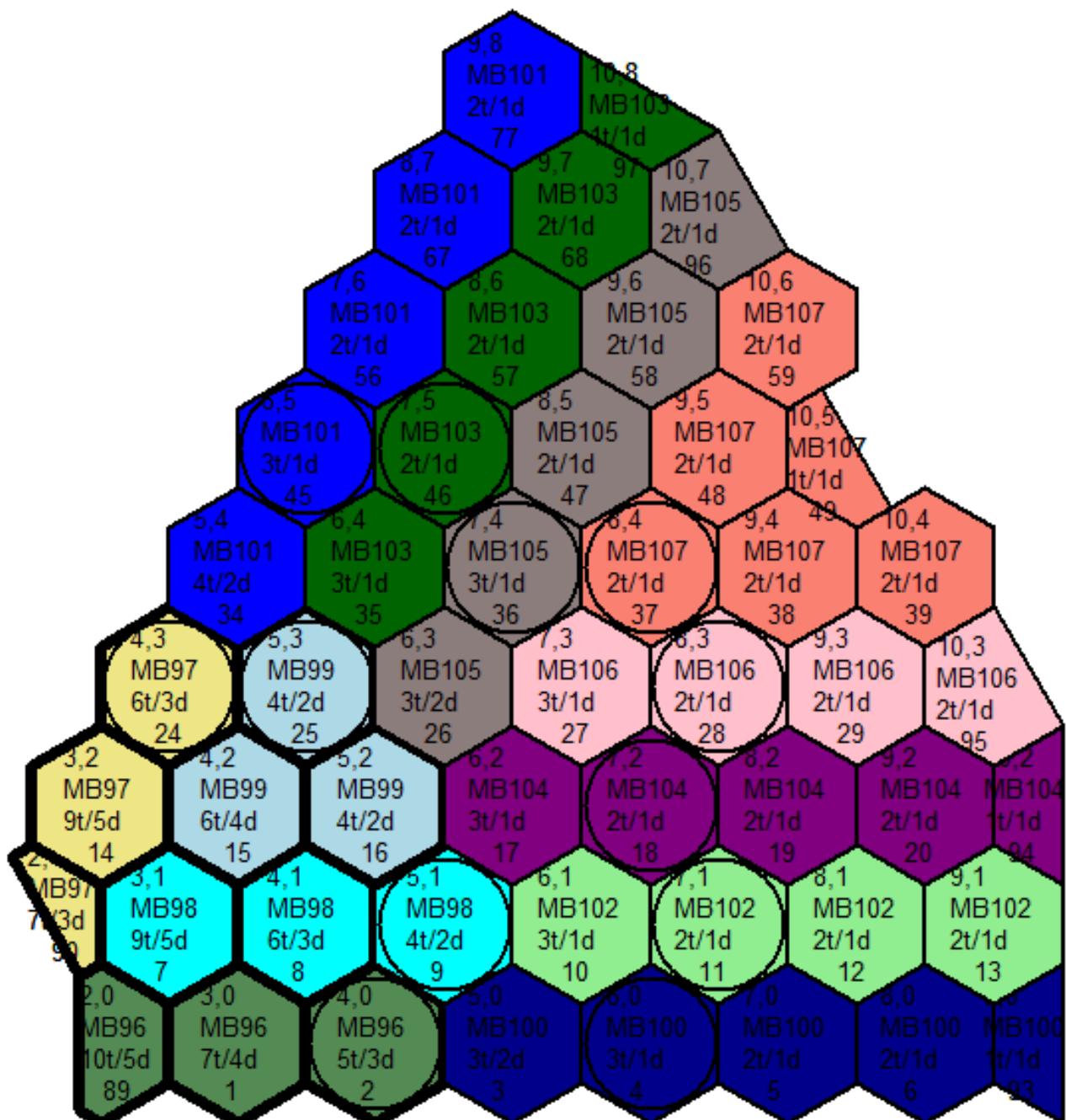


Figure 22: Tiling assignment for CE-E Cassette 0, Layer 9

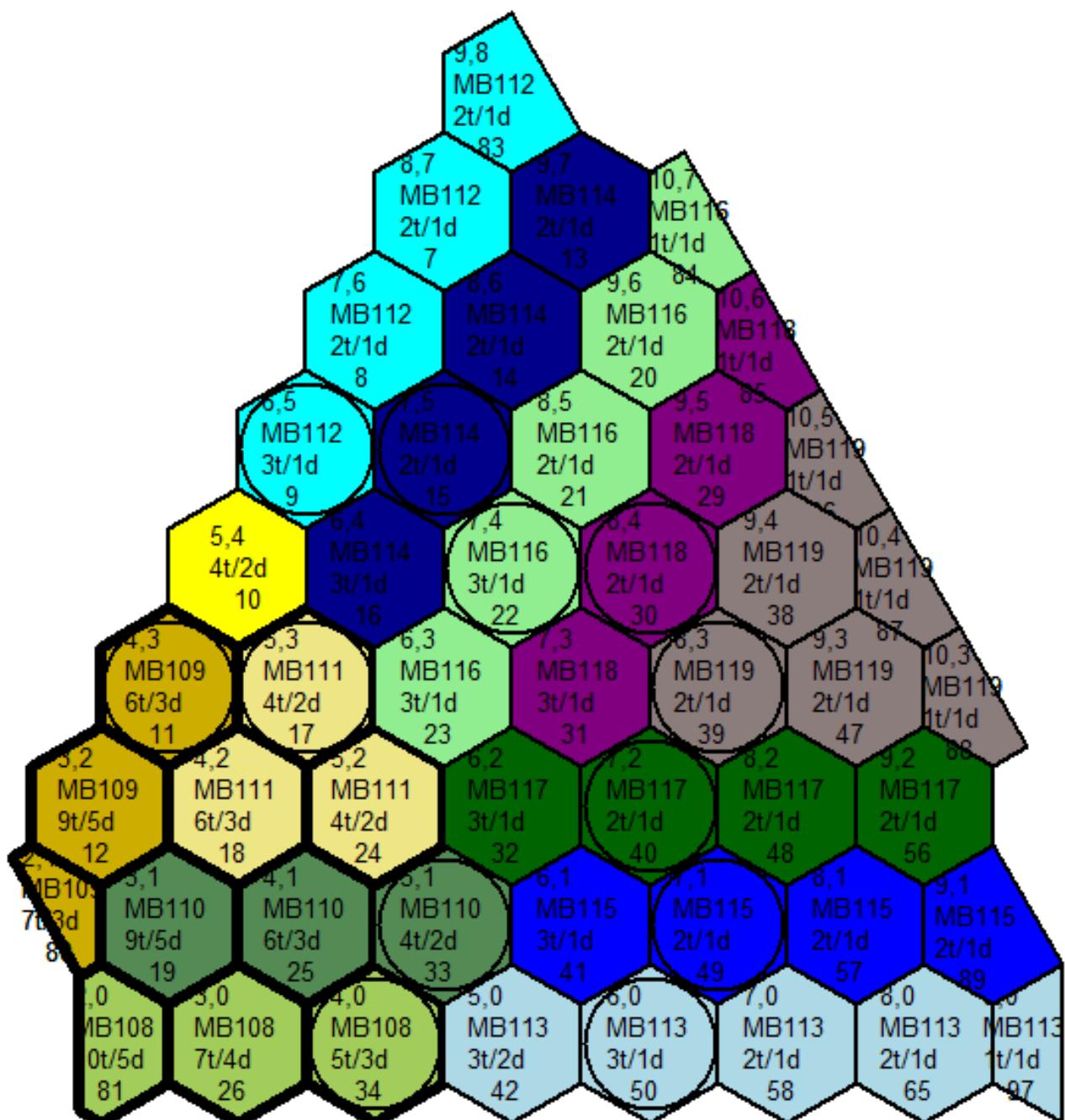


Figure 23: Tiling assignment for CE-E Cassette 0, Layer 10

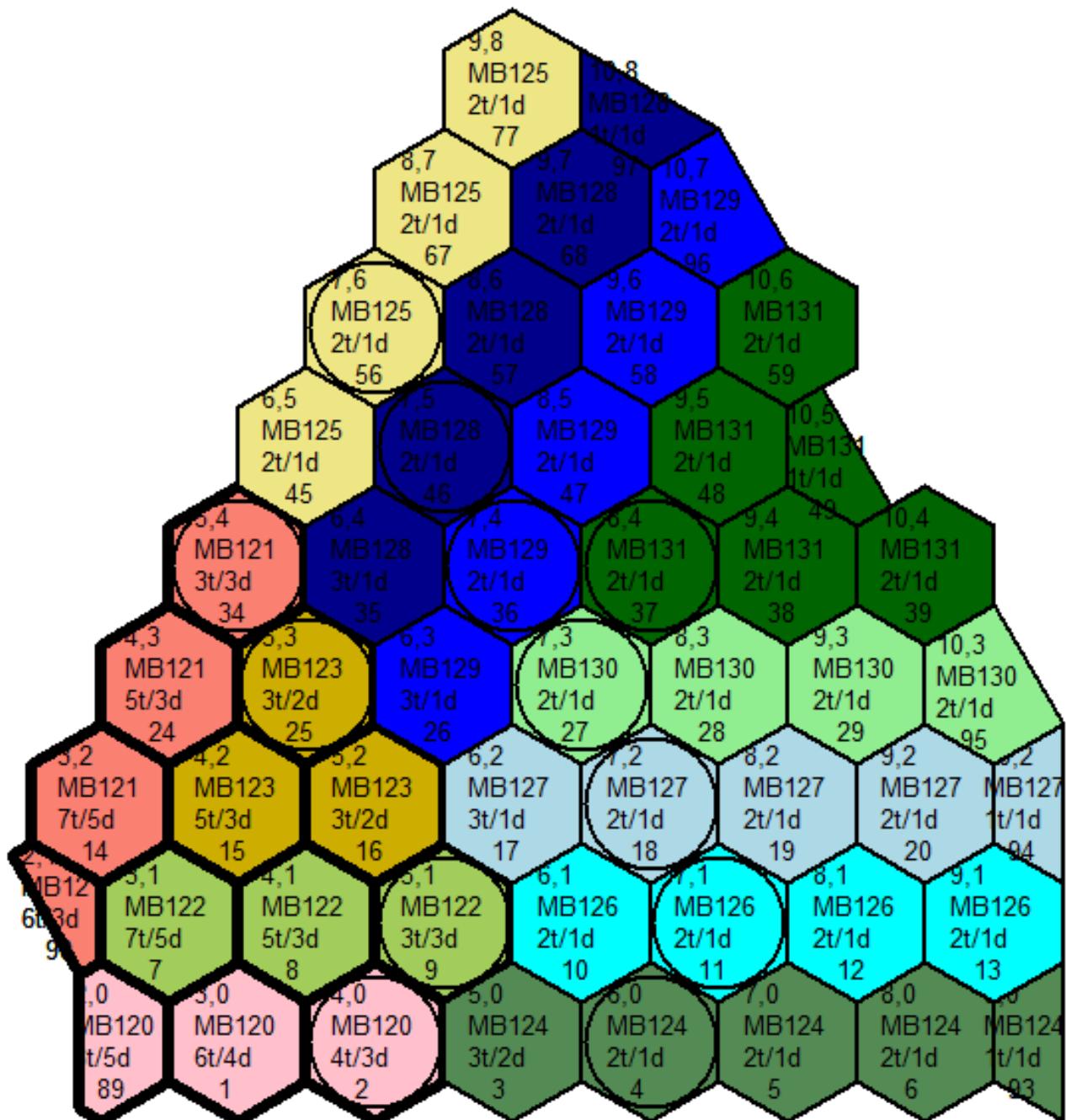


Figure 24: Tiling assignment for CE-E Cassette 0, Layer 11

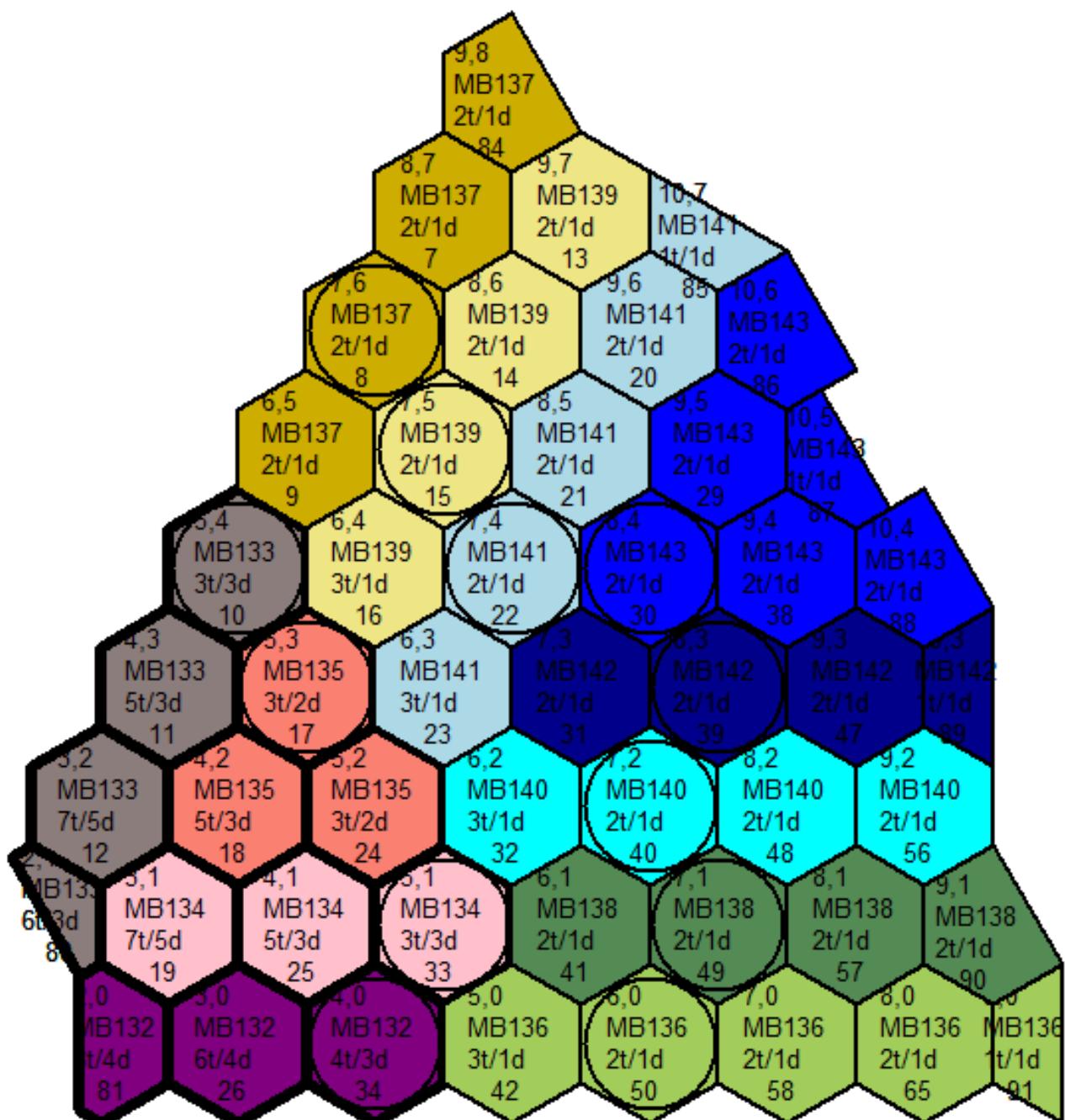


Figure 25: Tiling assignment for CE-E Cassette 0, Layer 12

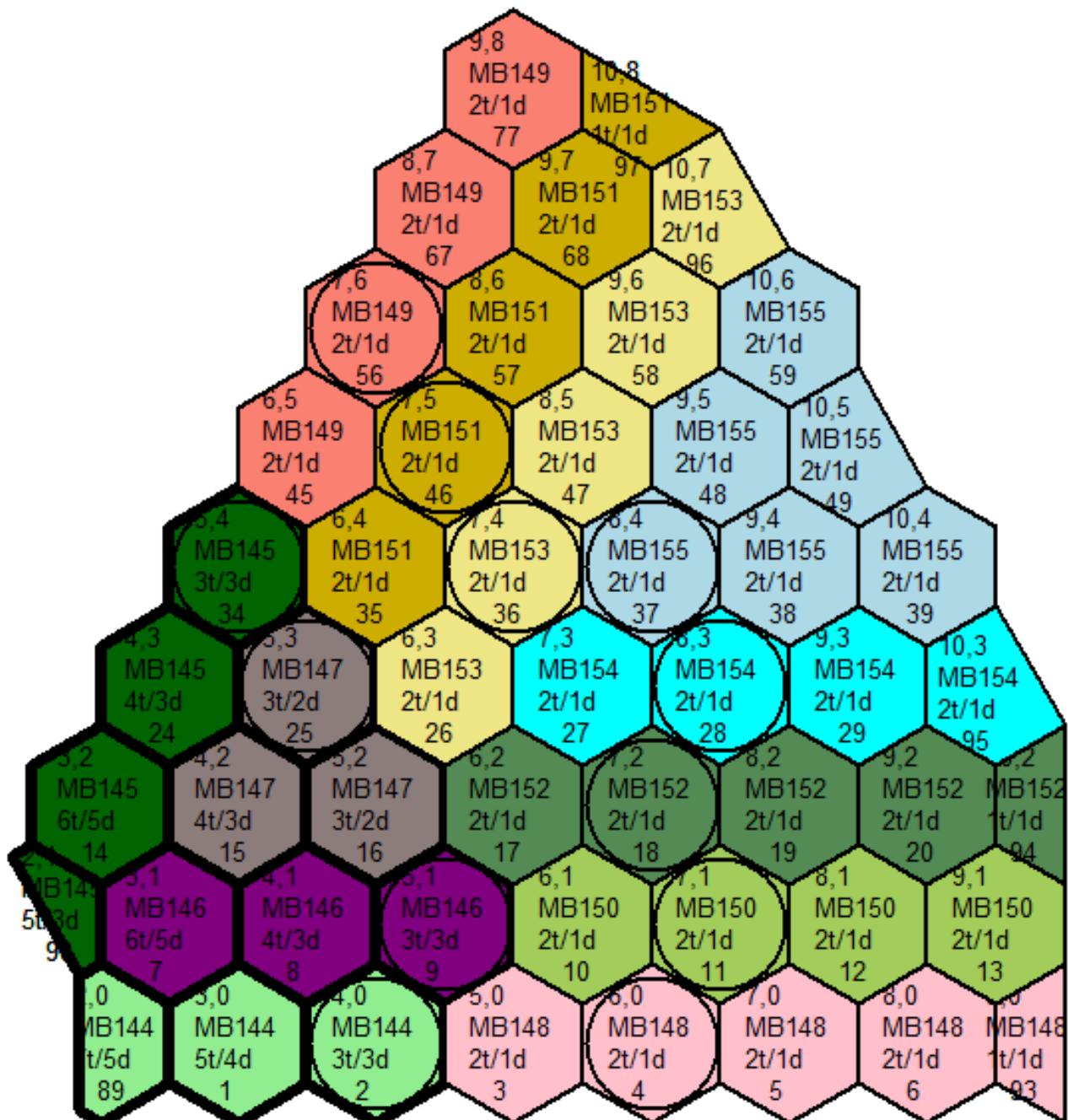


Figure 26: Tiling assignment for CE-E Cassette 0, Layer 13

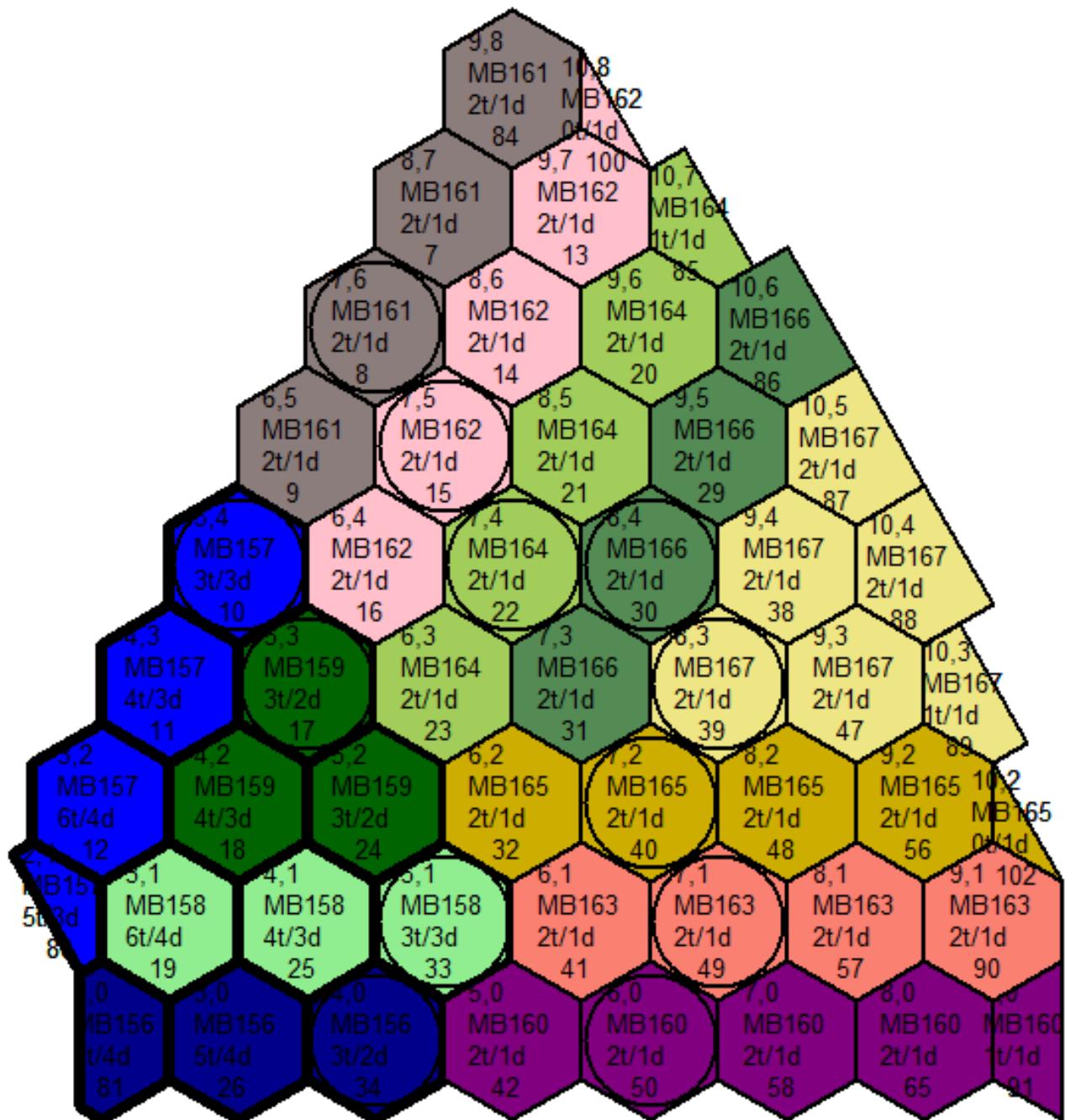


Figure 27: Tiling assignment for CE-E Cassette 0, Layer 14

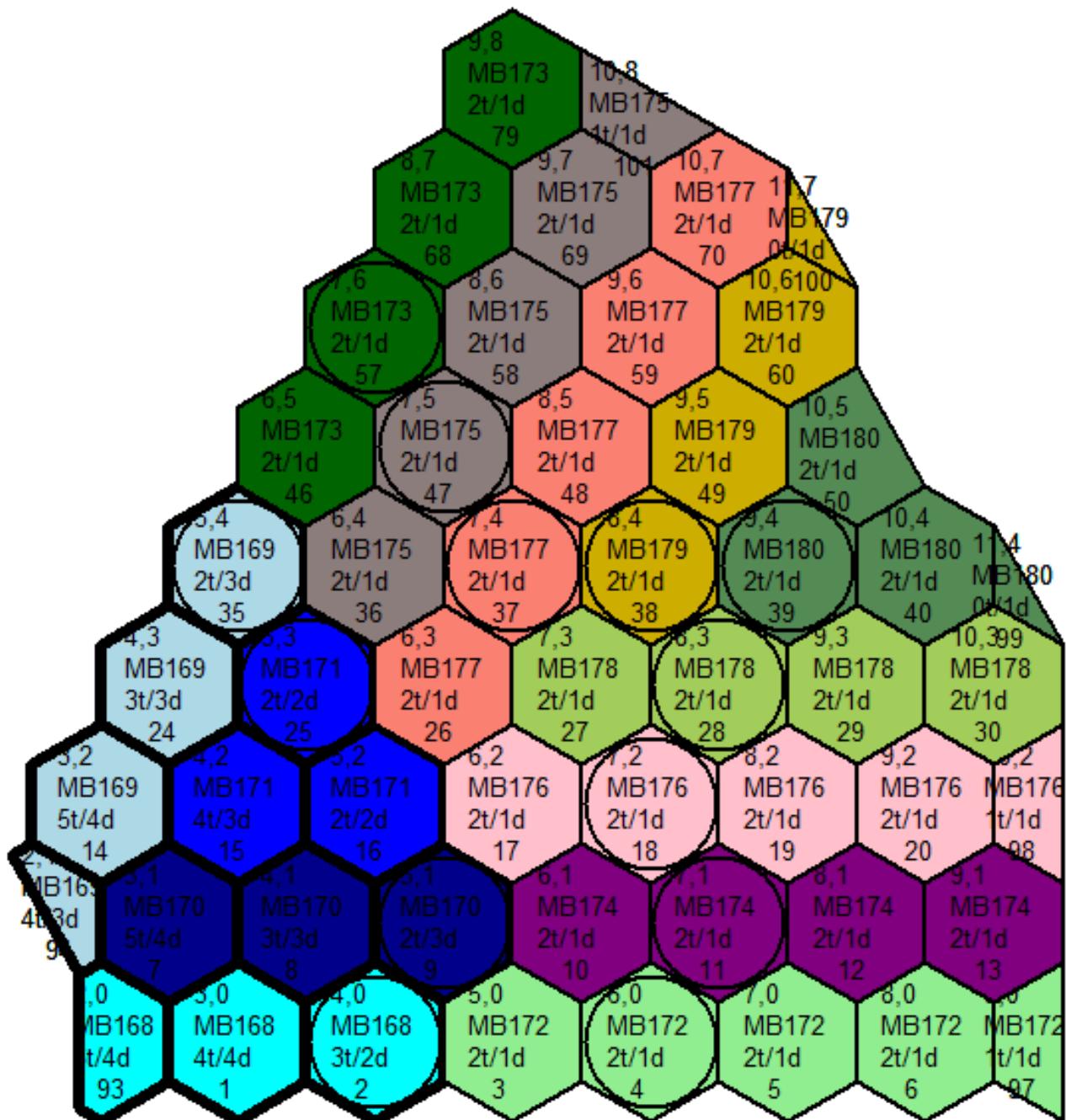


Figure 28: Tiling assignment for CE-E Cassette 0, Layer 15

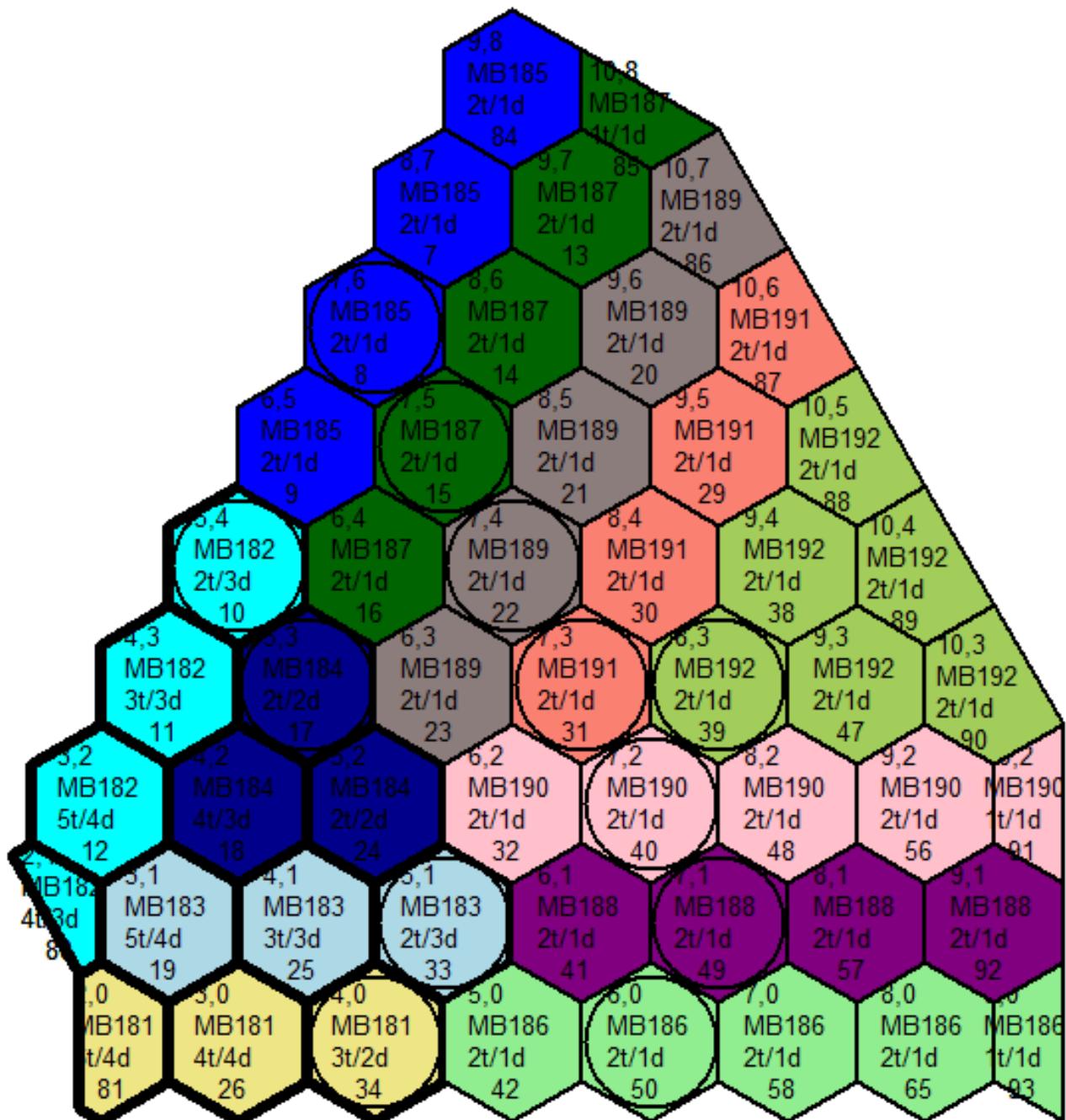


Figure 29: Tiling assignment for CE-E Cassette 0, Layer 16

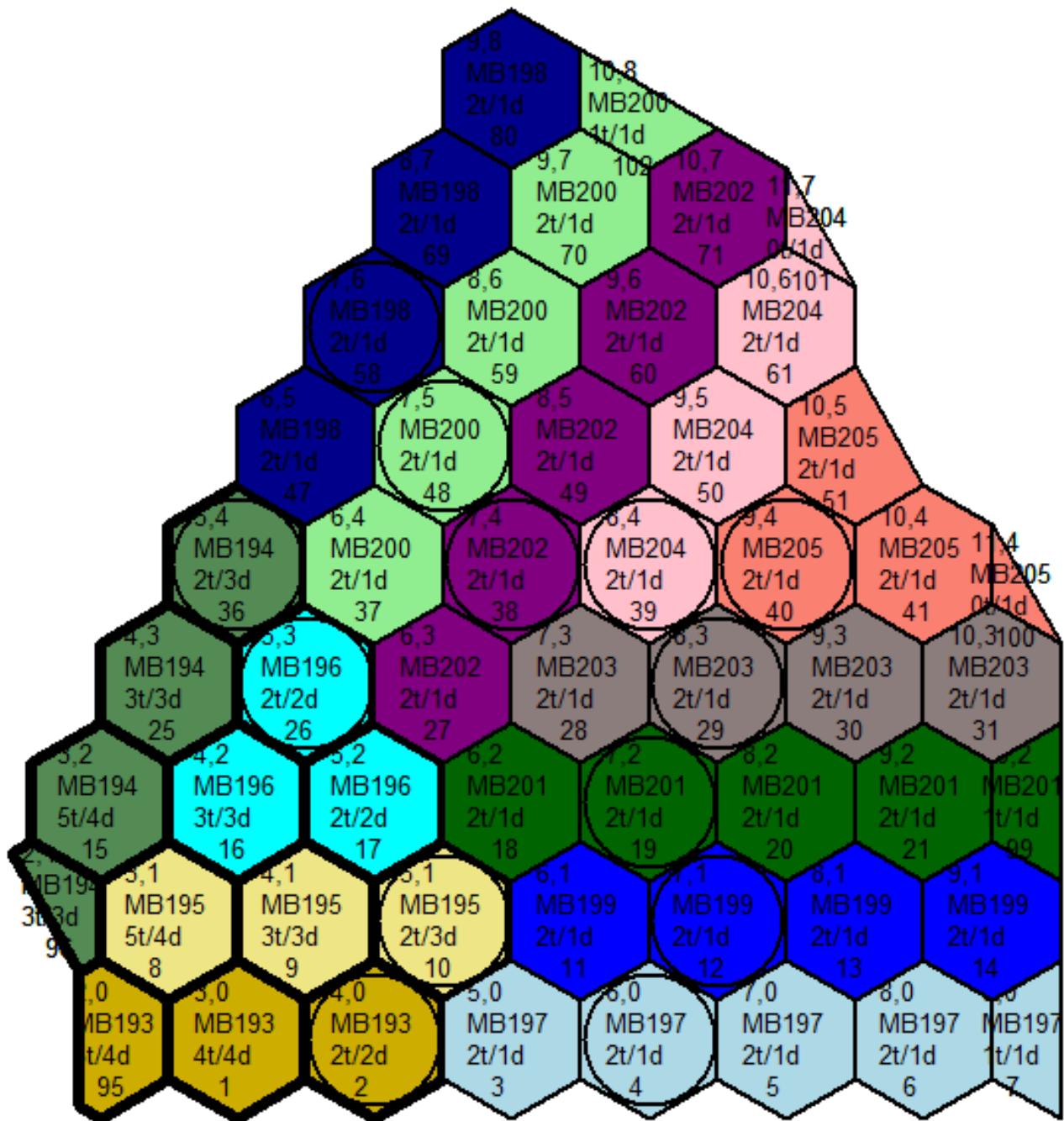


Figure 30: Tiling assignment for CE-E Cassette 0, Layer 17

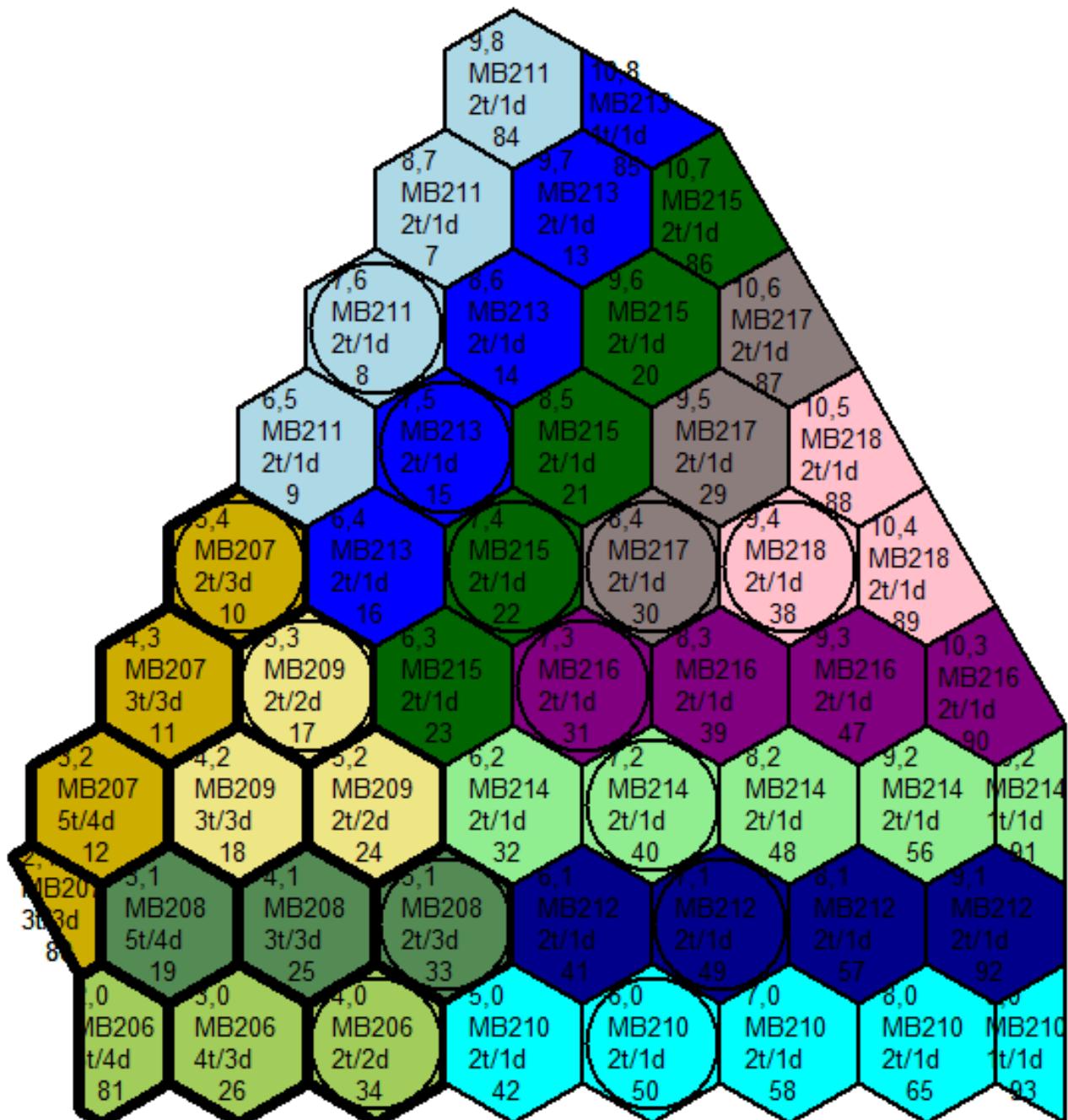


Figure 31: Tiling assignment for CE-E Cassette 0, Layer 18

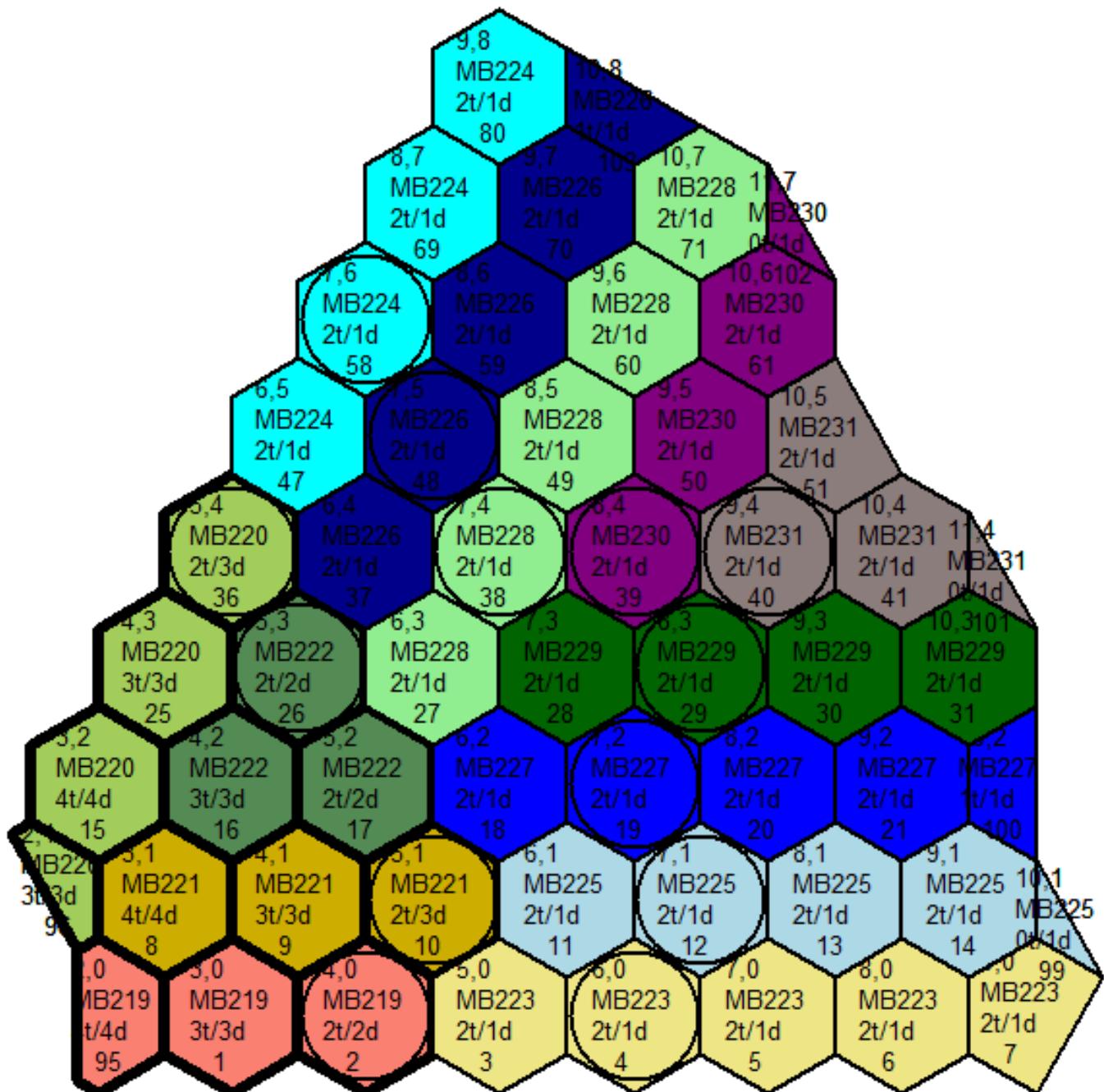


Figure 32: Tiling assignment for CE-E Cassette 0, Layer 19

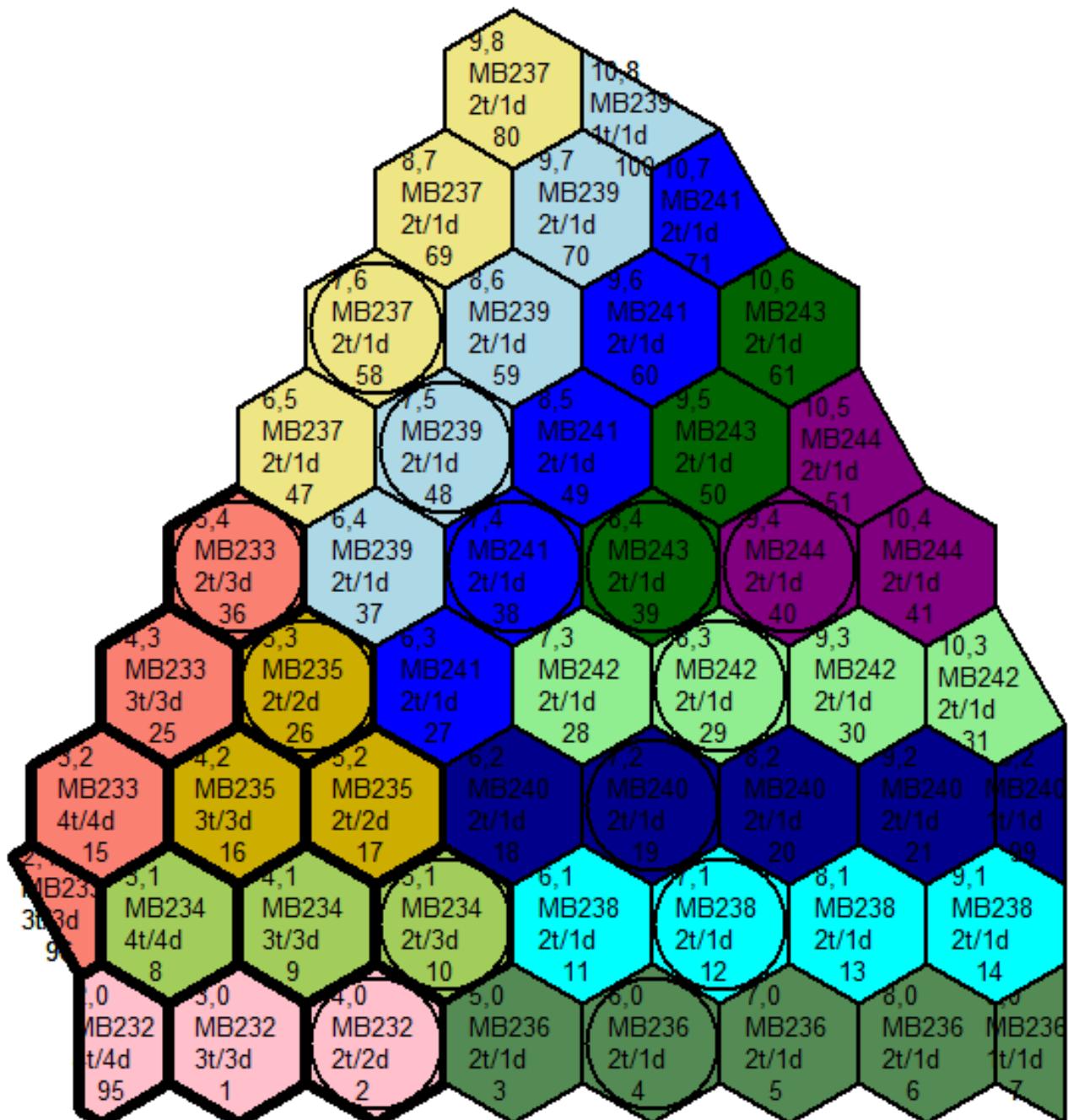


Figure 33: Tiling assignment for CE-E Cassette 0, Layer 20

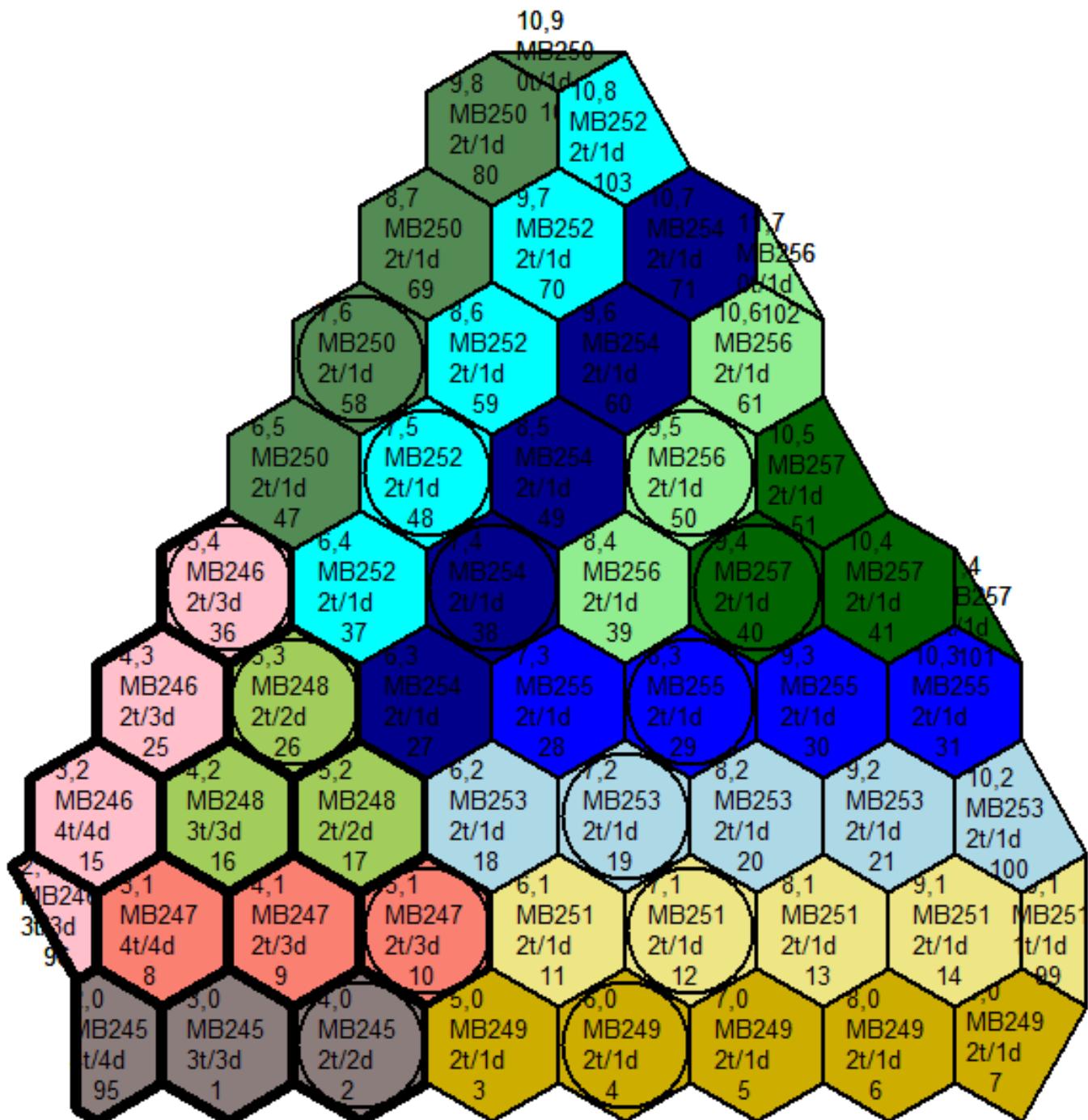


Figure 34: Tiling assignment for CE-E Cassette 0, Layer 21

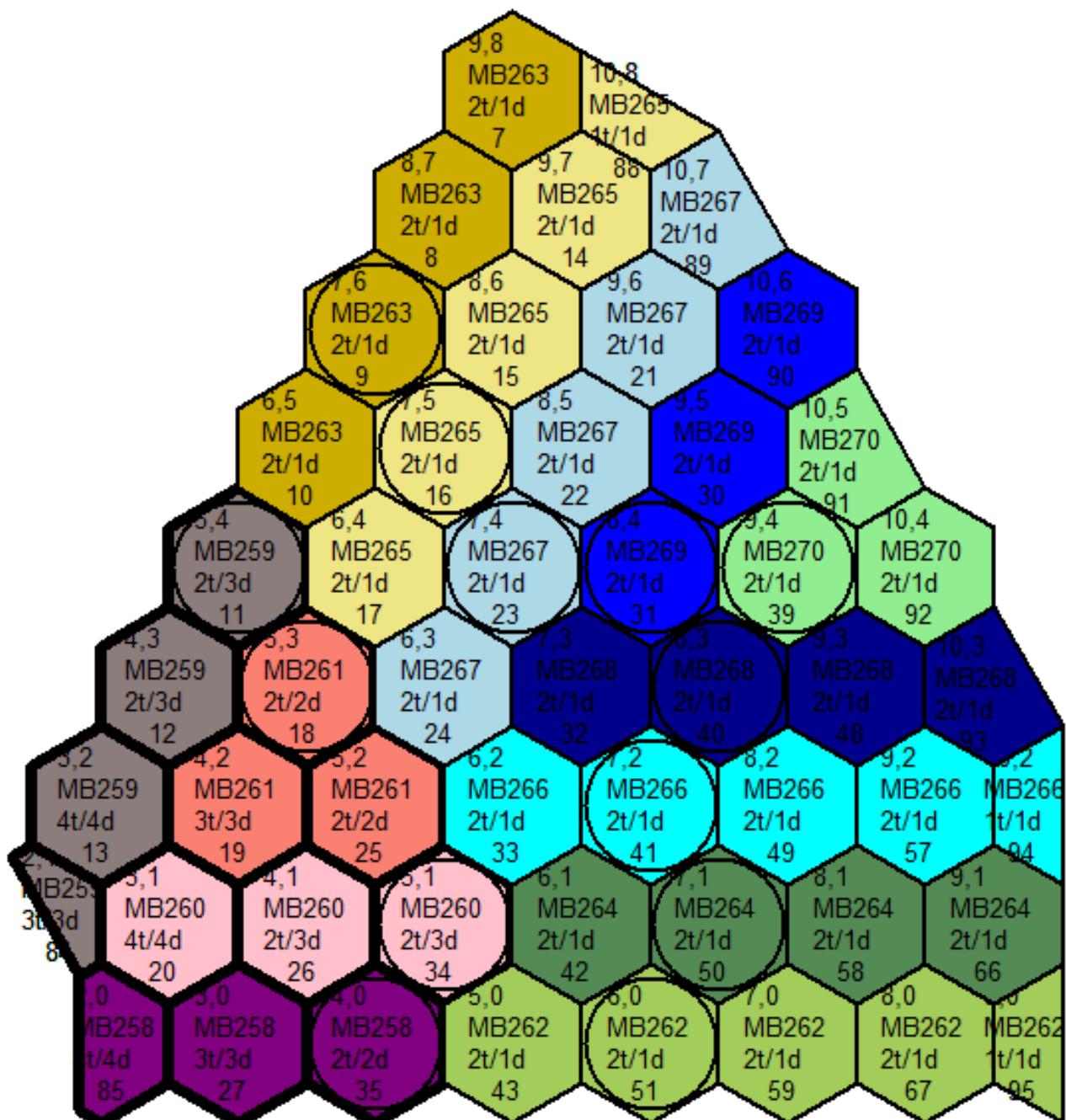


Figure 35: Tiling assignment for CE-E Cassette 0, Layer 22

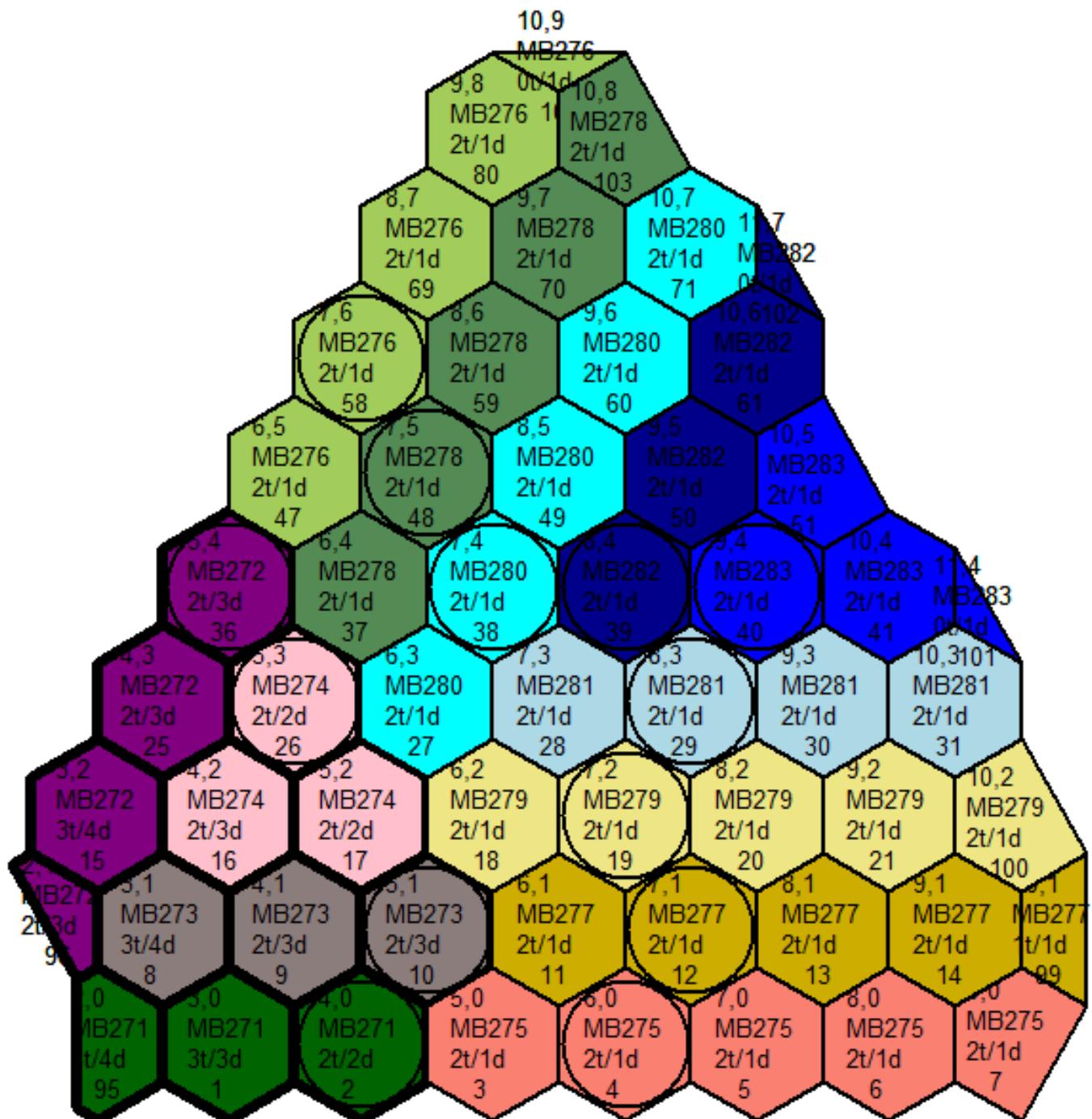


Figure 36: Tiling assignment for CE-E Cassette 0, Layer 23

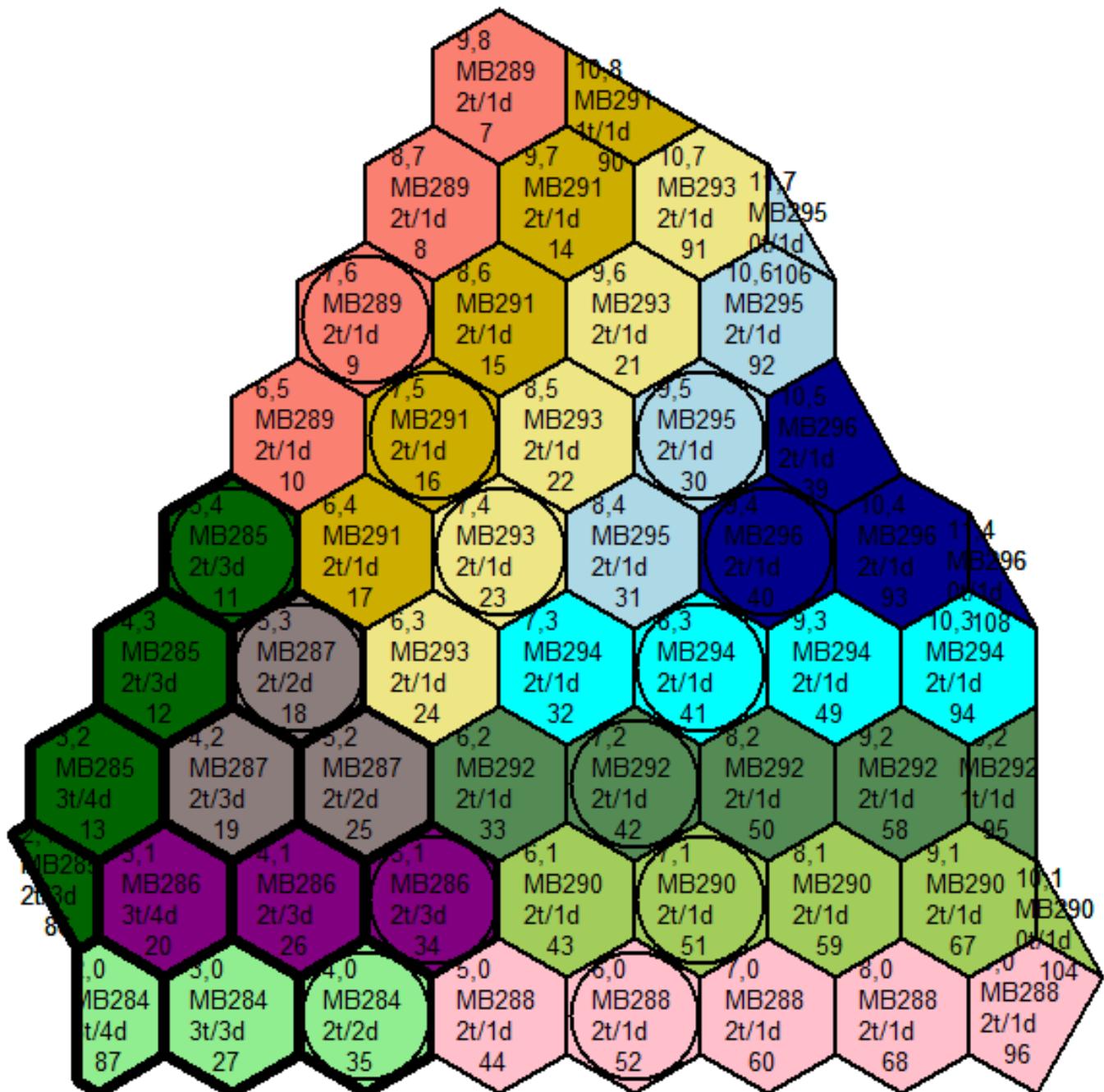


Figure 37: Tiling assignment for CE-E Cassette 0, Layer 24

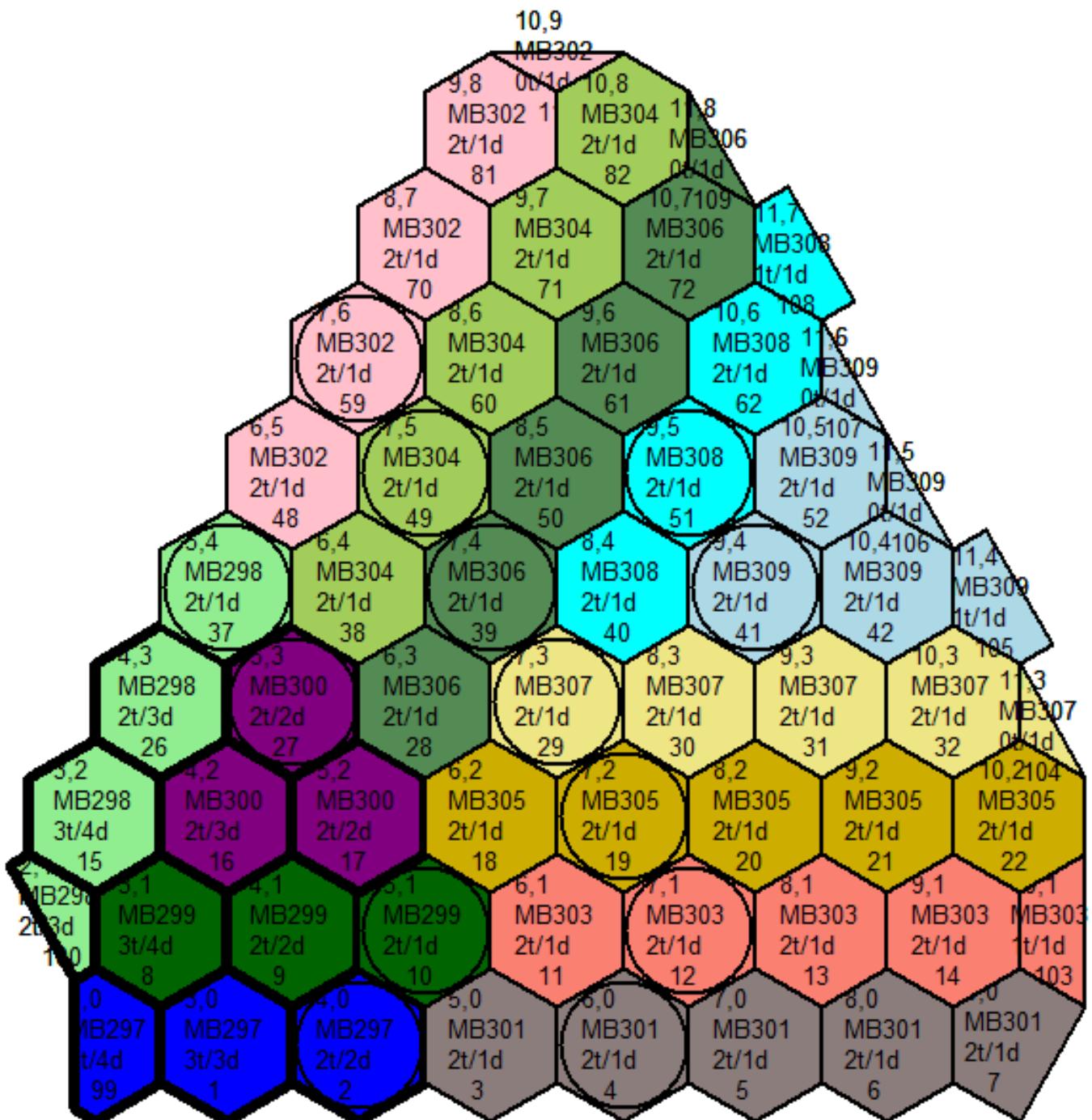


Figure 38: Tiling assignment for CE-E Cassette 0, Layer 25

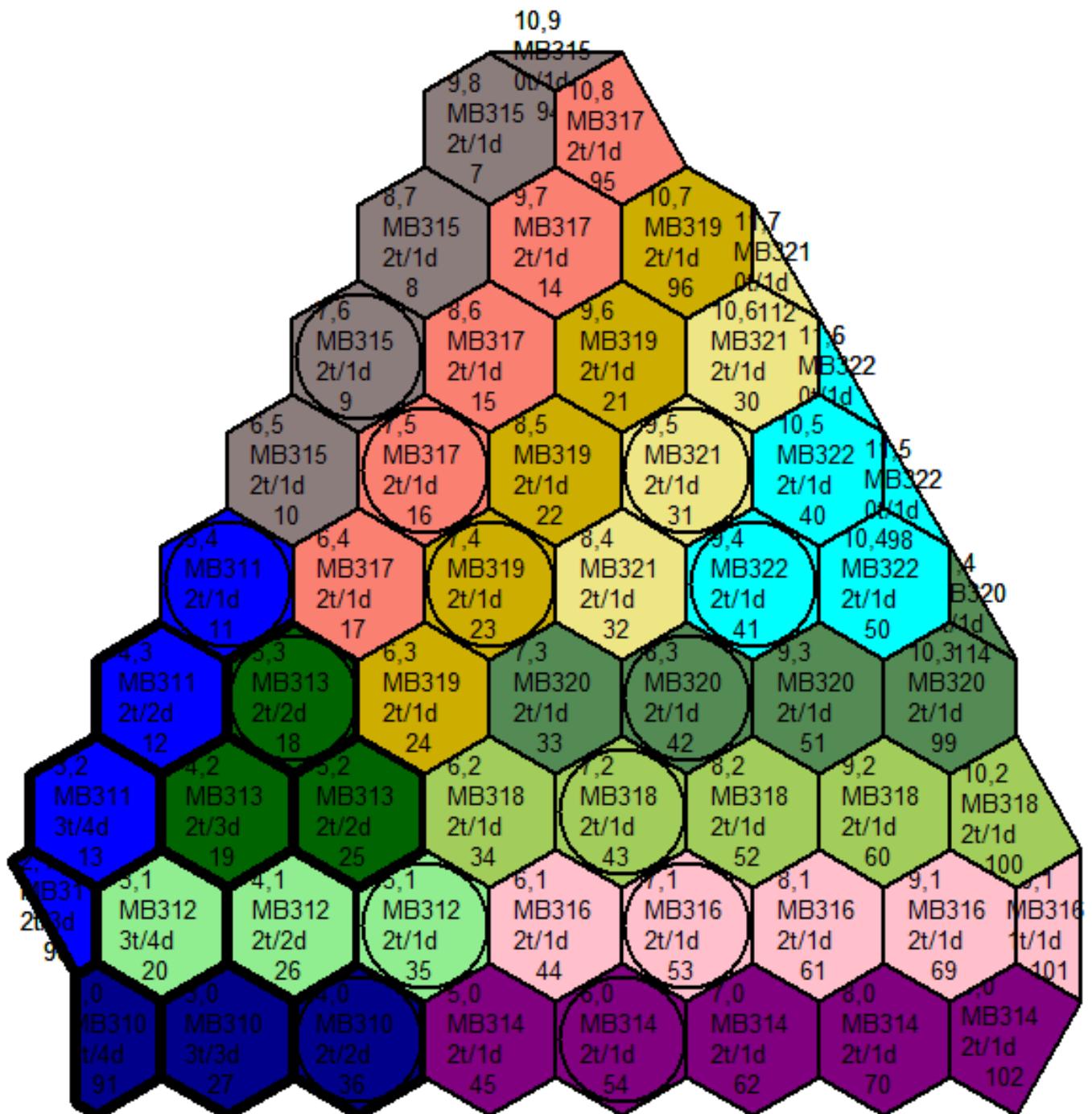


Figure 39: Tiling assignment for CE-E Cassette 0, Layer 26

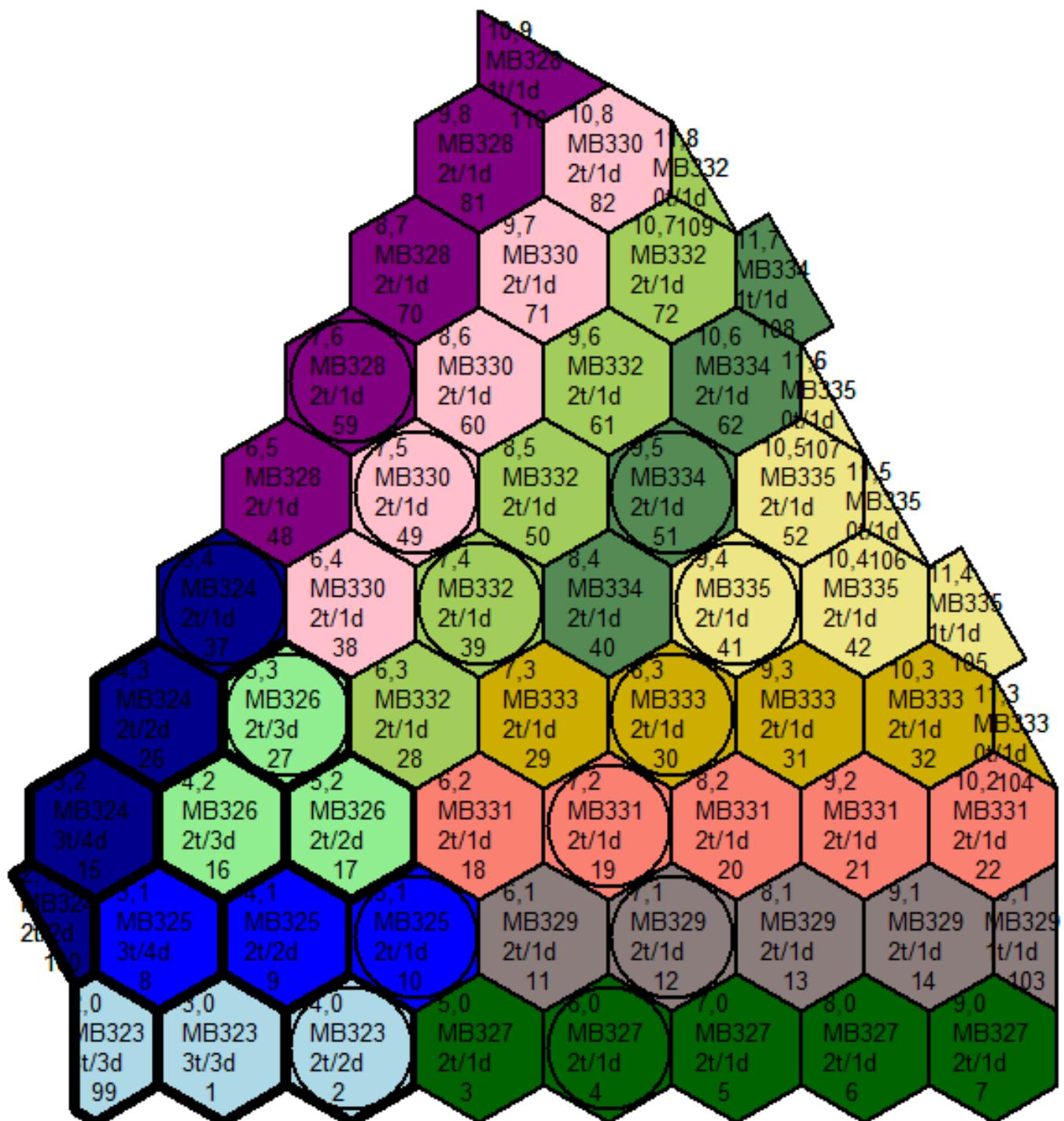


Figure 40: Tiling assignment for CE-E Cassette 0, Layer 27

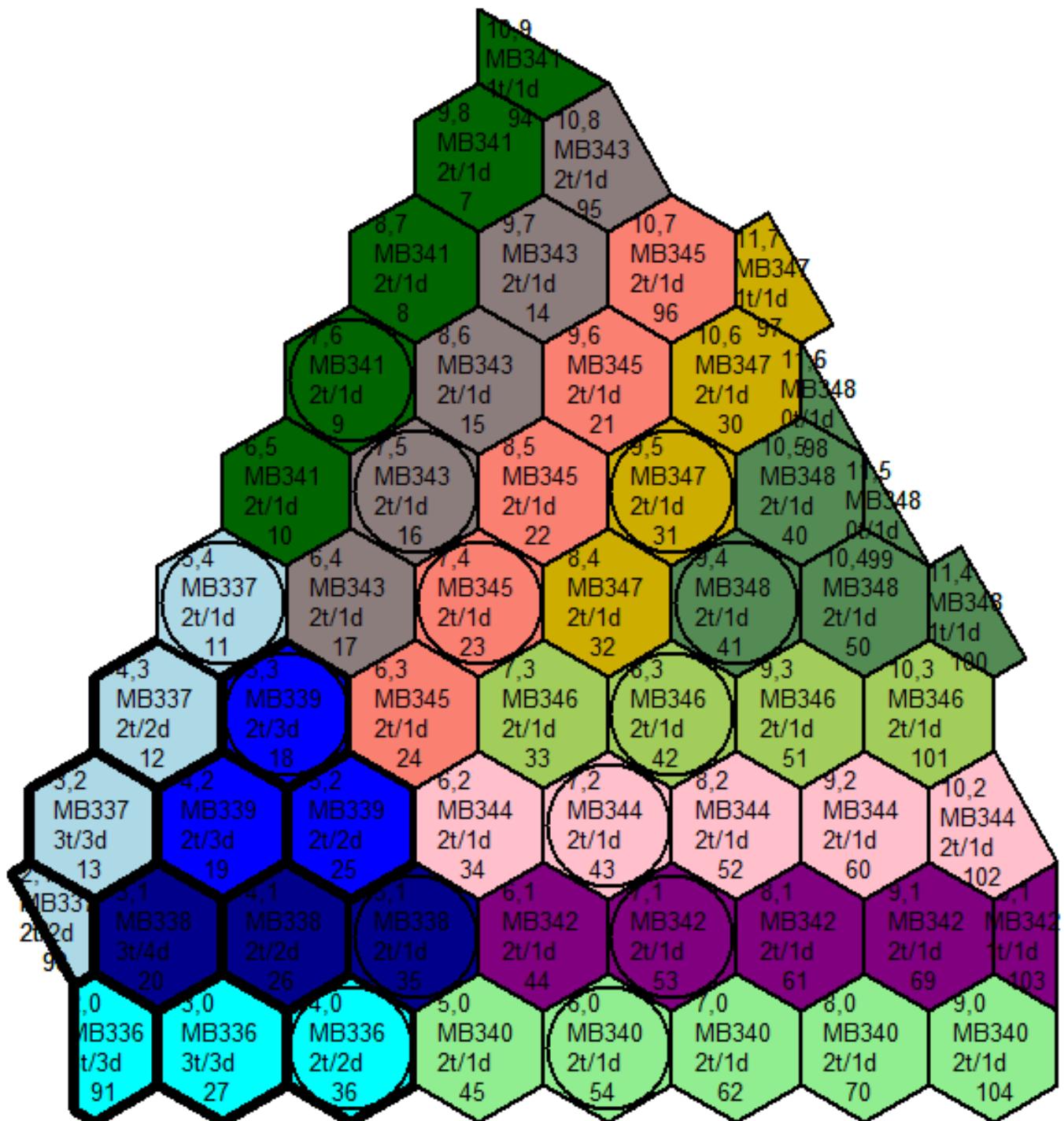


Figure 41: Tiling assignment for CE-E Cassette 0, Layer 28

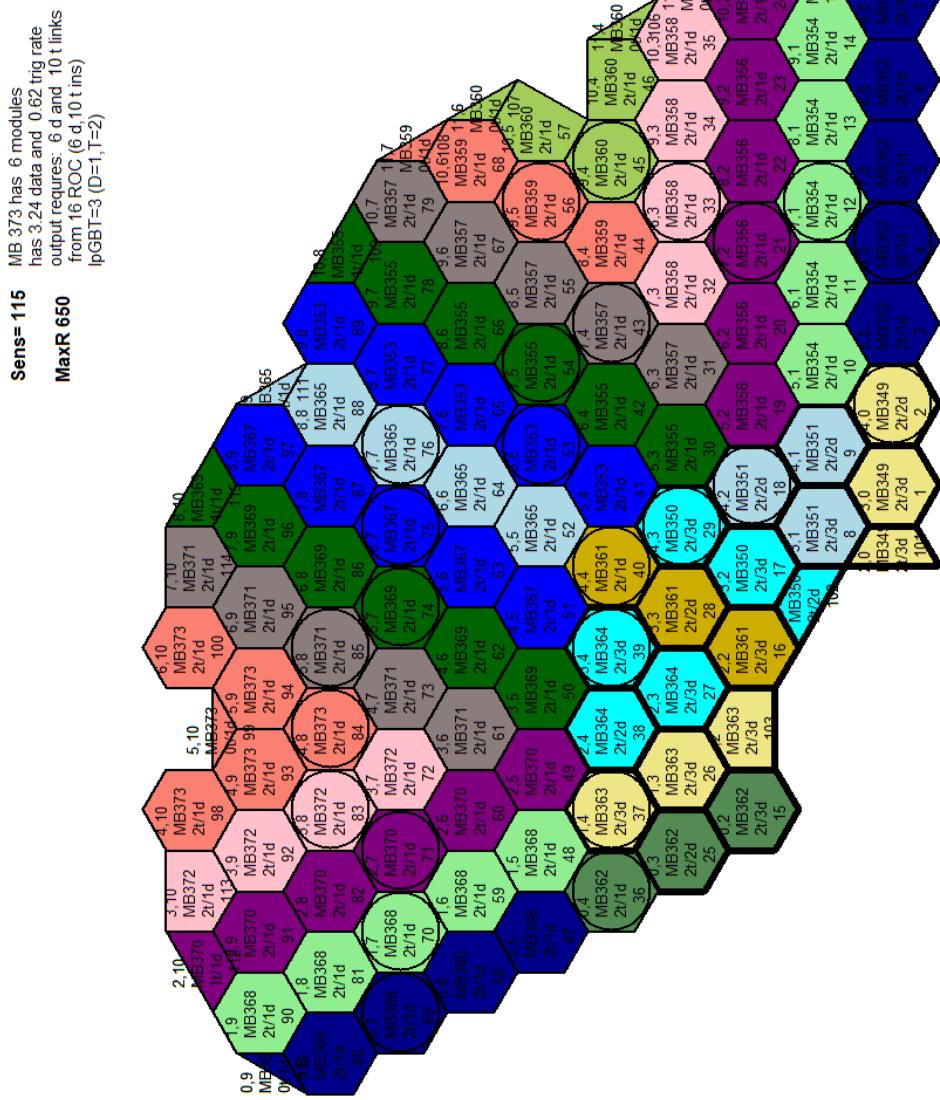
A.0.2 CE-H


Figure 42: Tiling assignment for CE-H Cassette 0 and 1, Layer 29

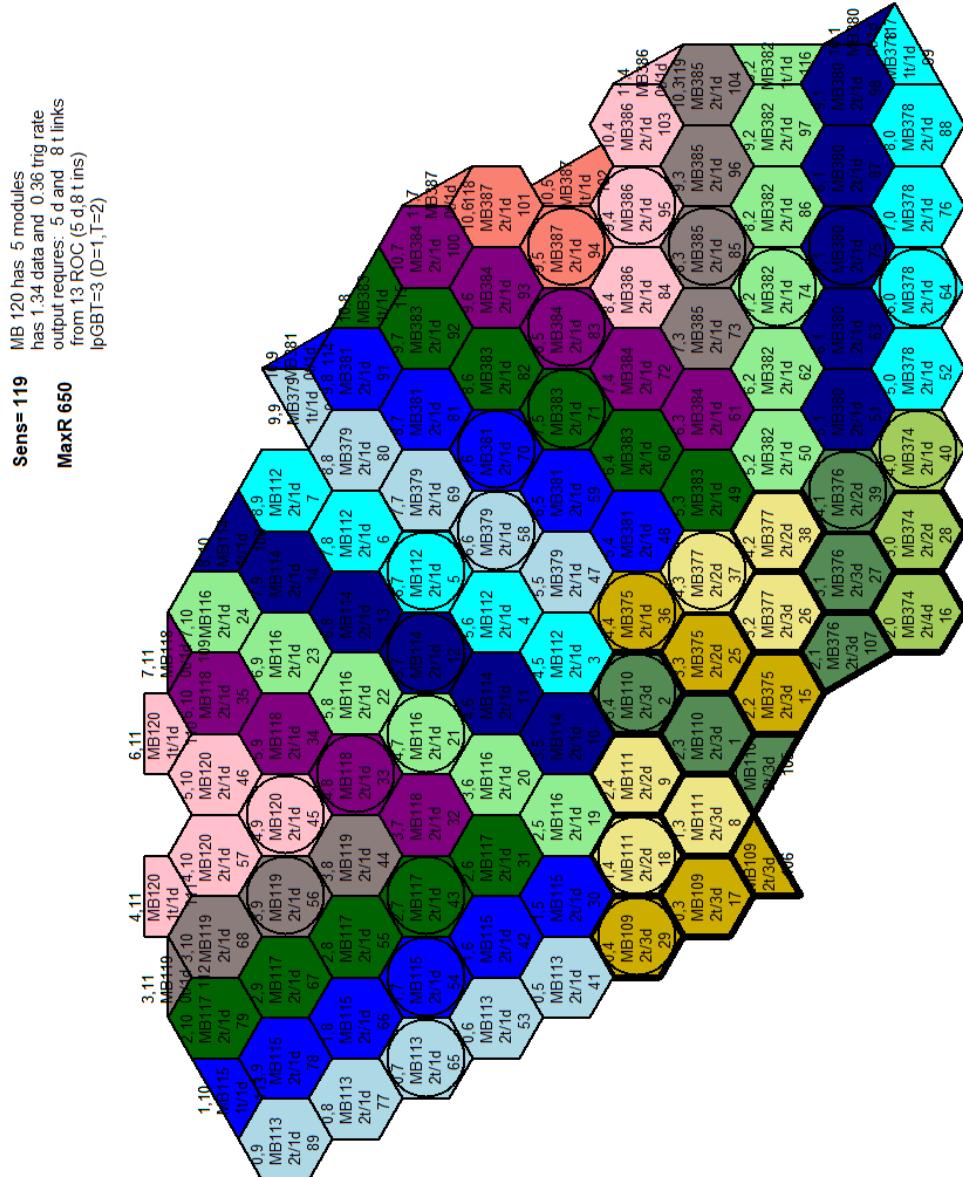


Figure 43: Tiling assignment for CE-H Cassettes 0 and 1, Layer 30

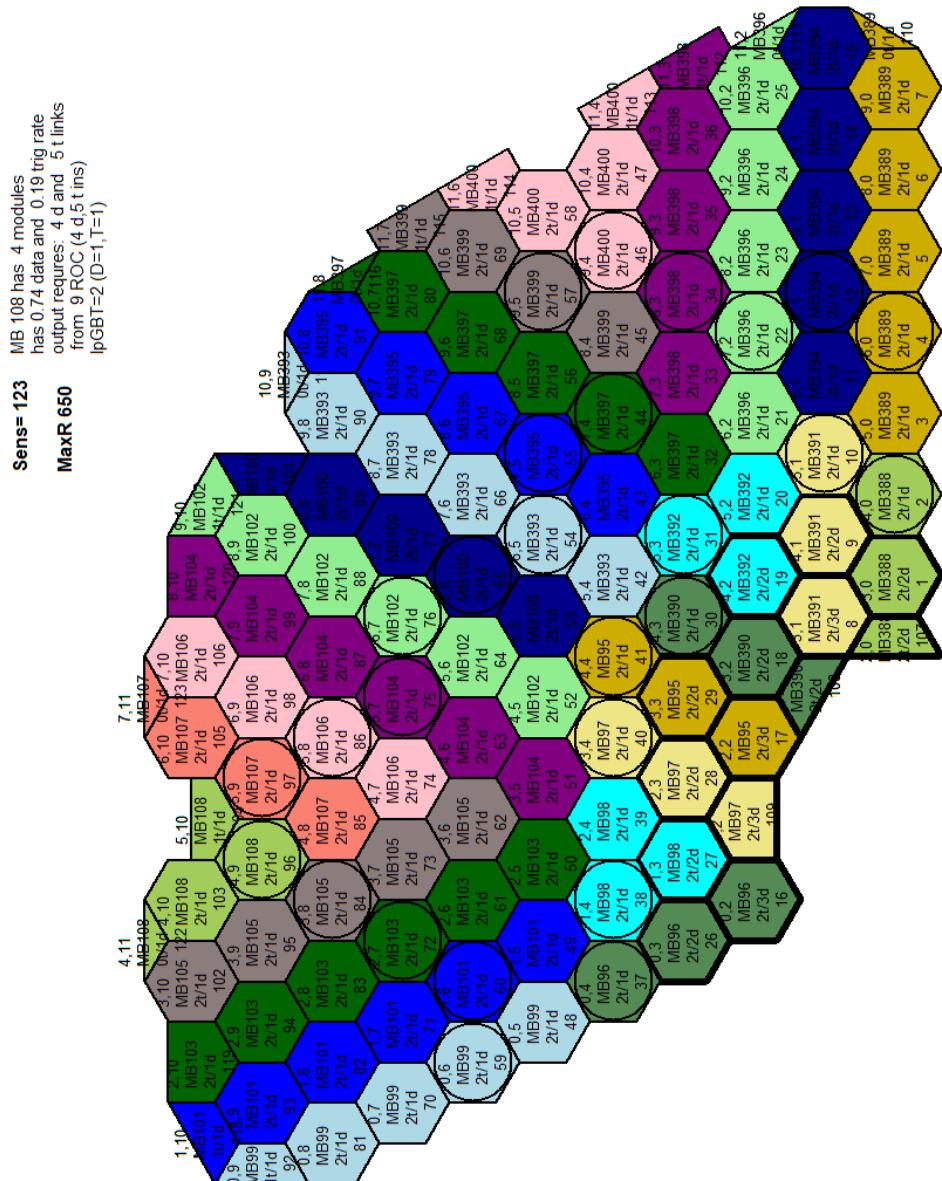


Figure 44: Tiling assignment for CE-H Cassette 0 and 1, Layer 31

Sens= 125 MB 94 has 5 modules
has 1.09 data and 0.26 trig rate
output requires: 5 d and 10 t links
from 15 ROC (5 d,10 tins)
lpGBT=3 (D=1,T=2)

MaxR 650

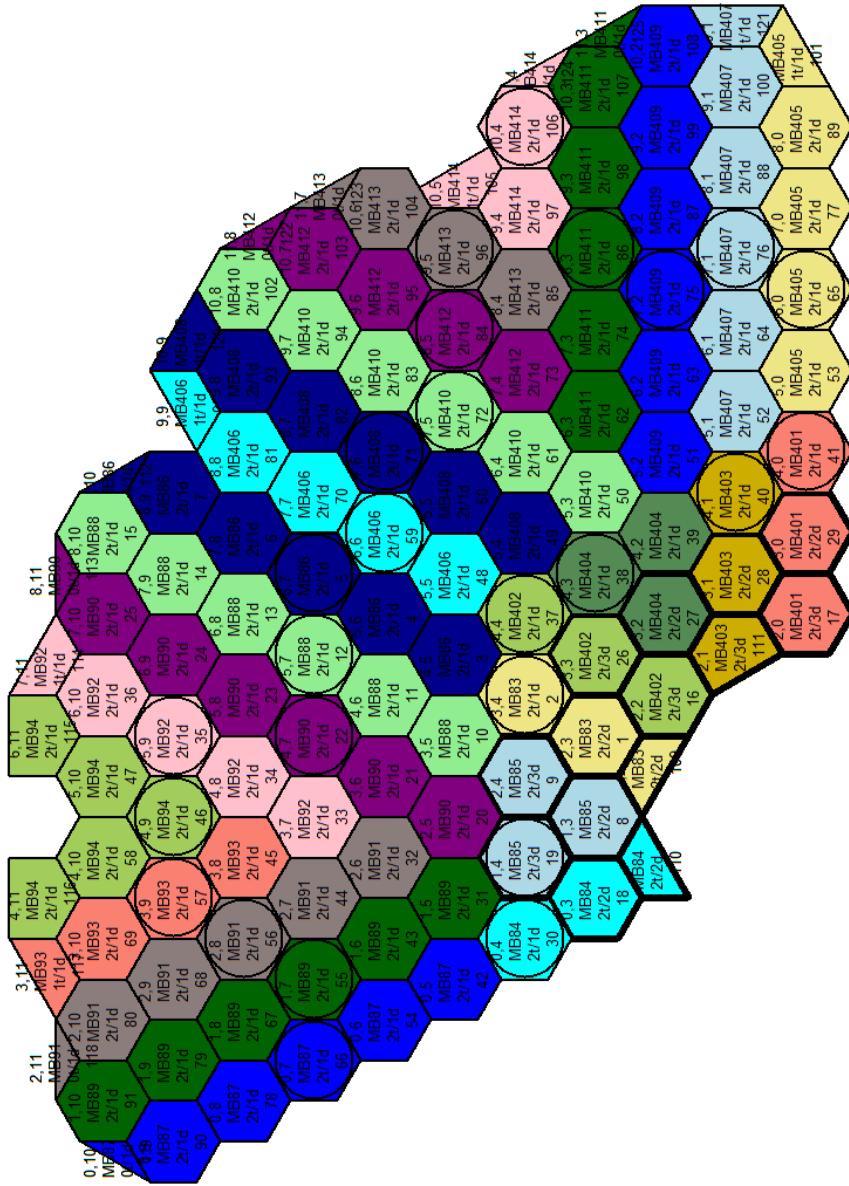


Figure 45: Tiling assignment for CE-H Cassettes 0 and 1, Layer 32

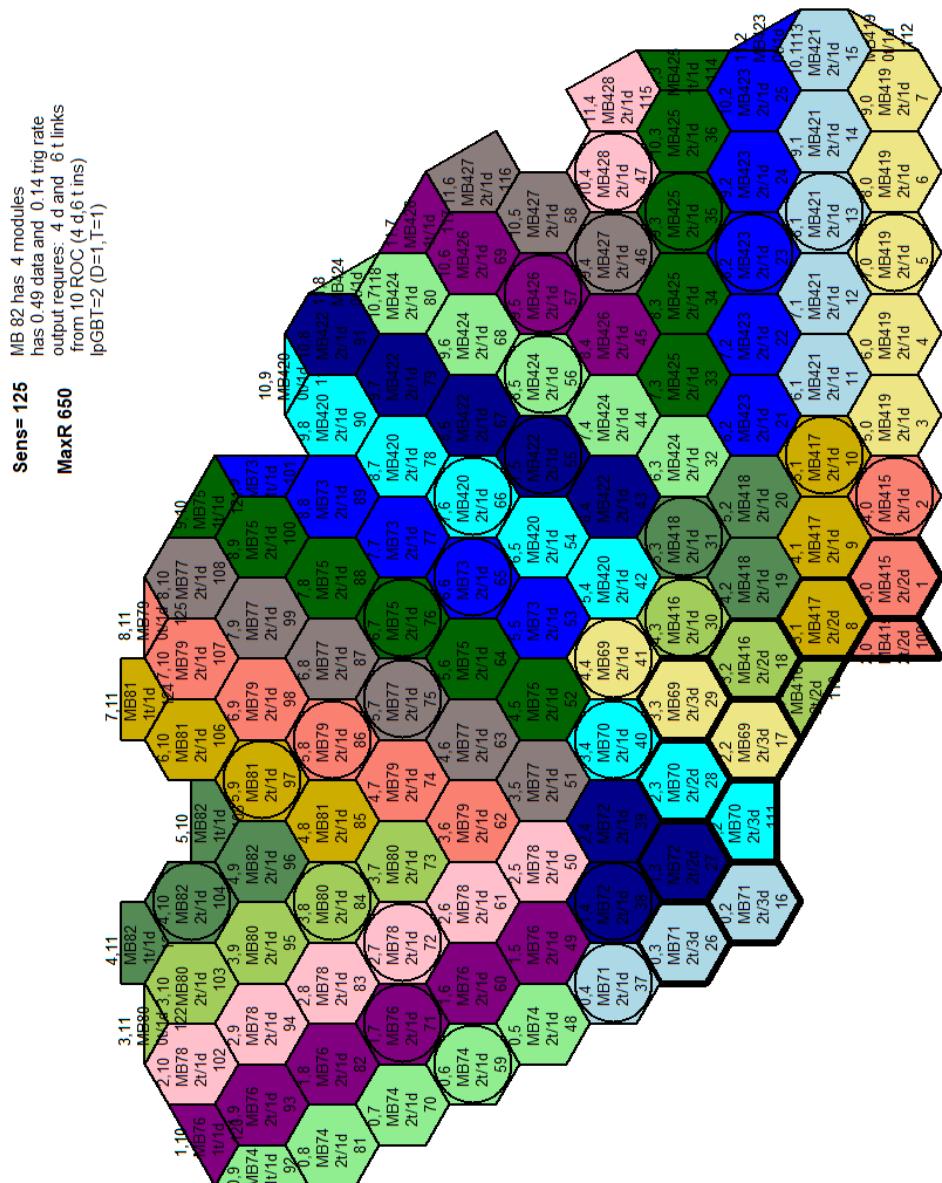


Figure 46: Tiling assignment for CE-H Cassette 0 and 1, Layer 33

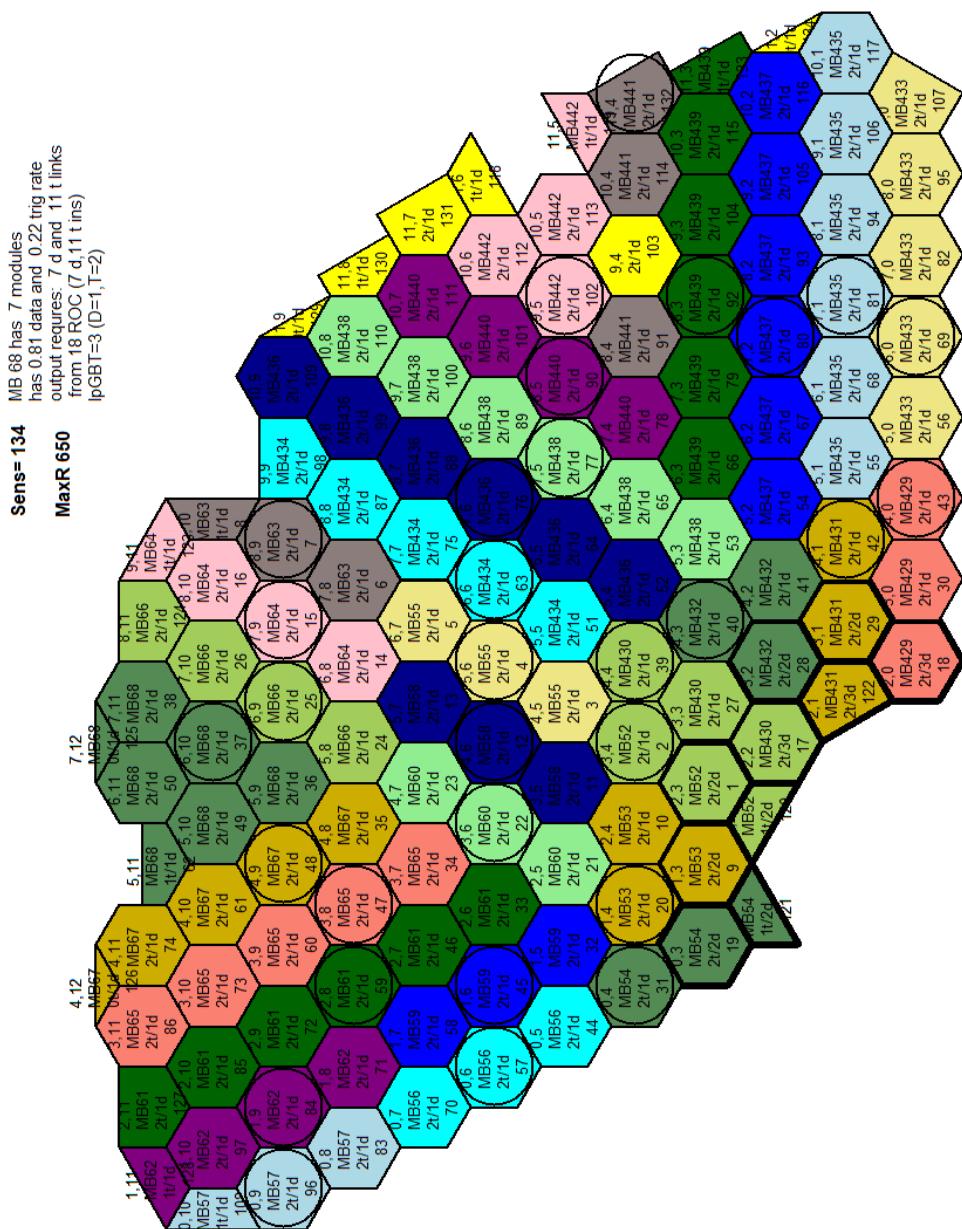


Figure 47: Tiling assignment for CE-H Cassettes 0 and 1, Layer 34

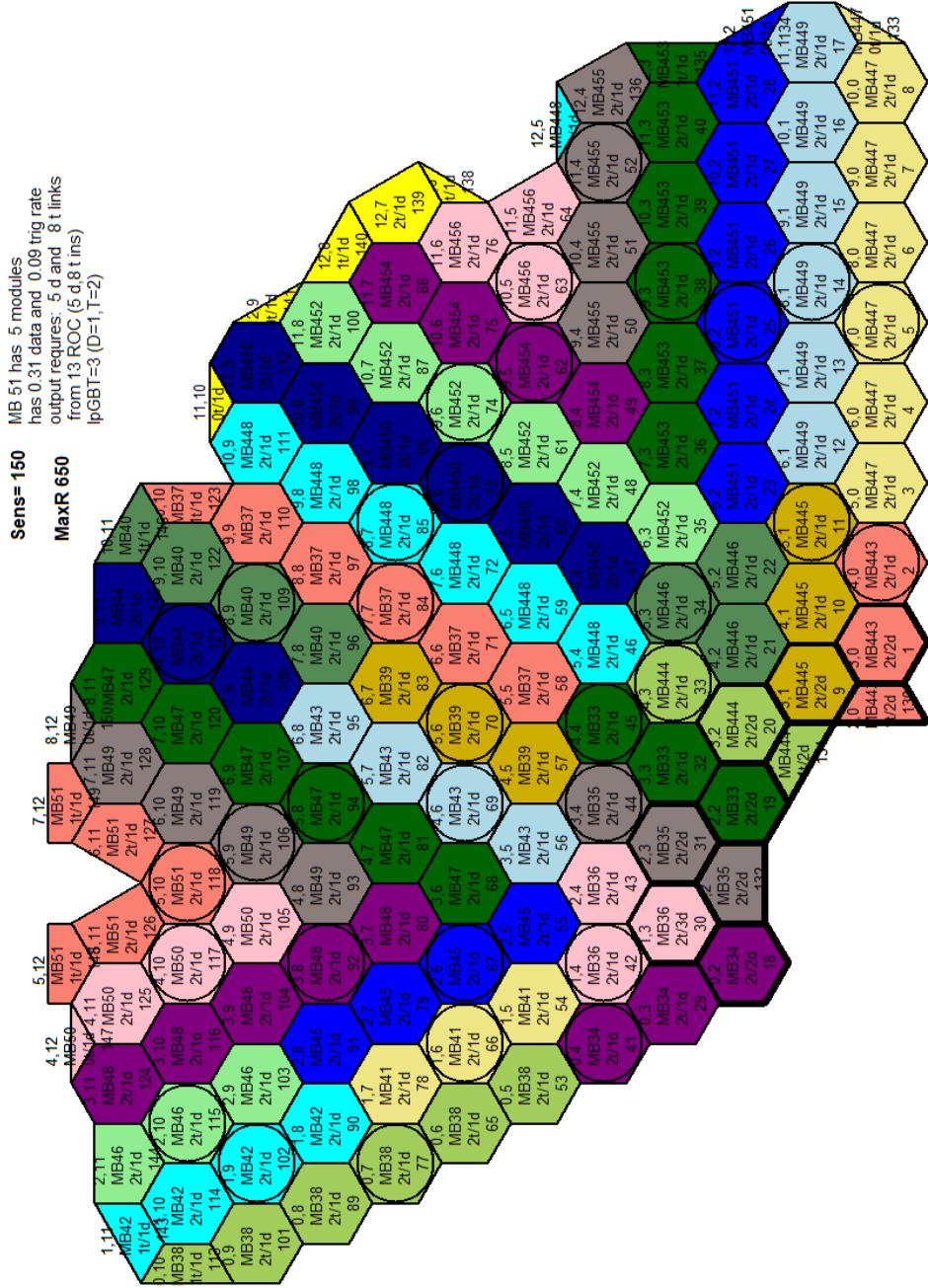


Figure 48: Tiling assignment for CE-H Cassettes 0 and 1, Layer 35

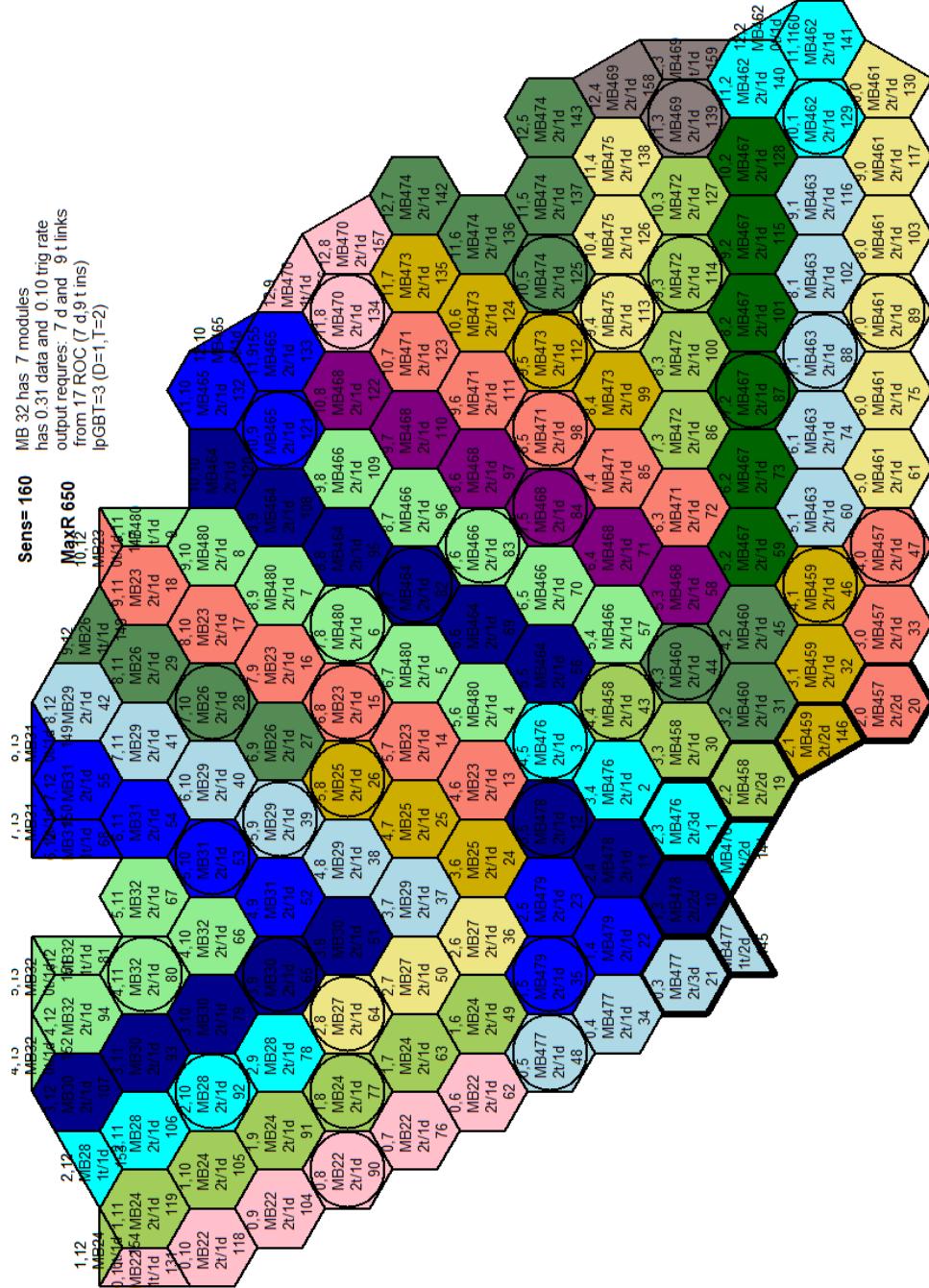


Figure 49: Tiling assignment for CE-H Cassettes 0 and 1, Layer 36

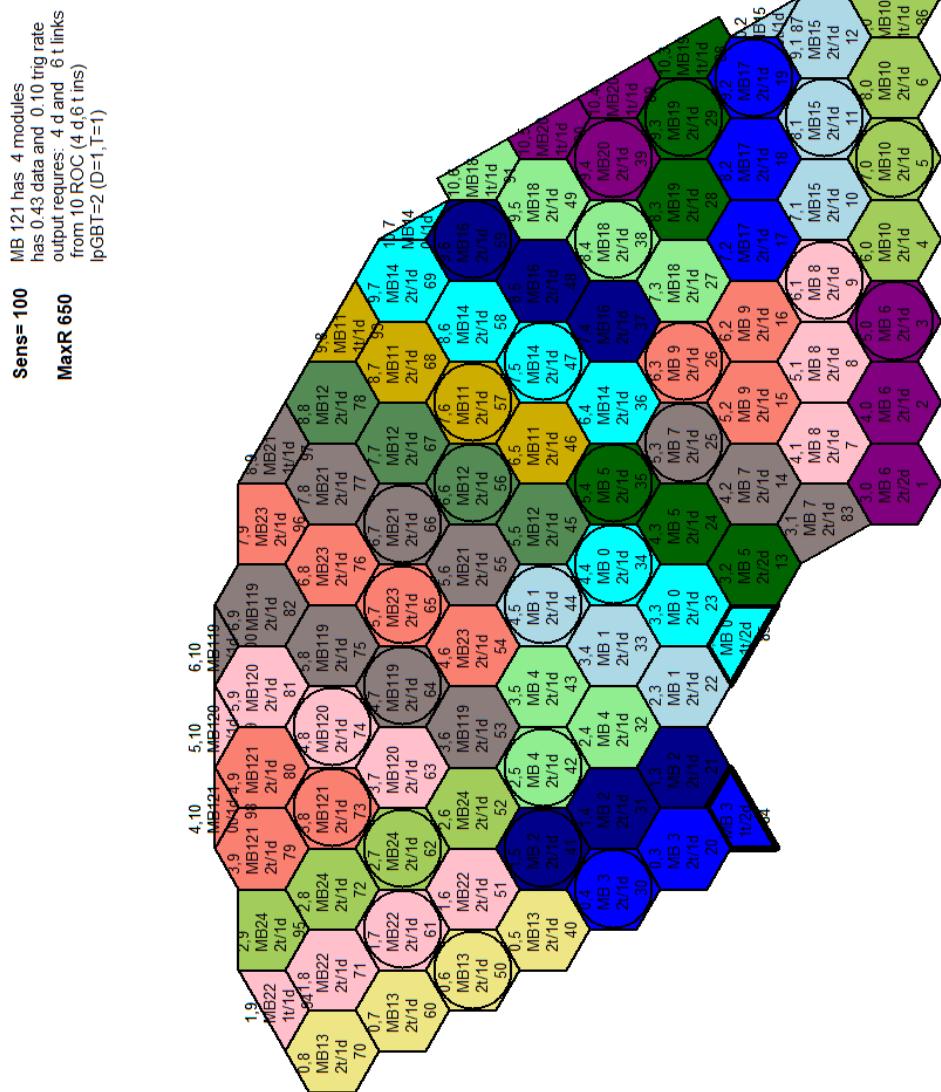


Figure 50: Tiling assignment for CE-H Cassettes 0 and 1, Layer 37

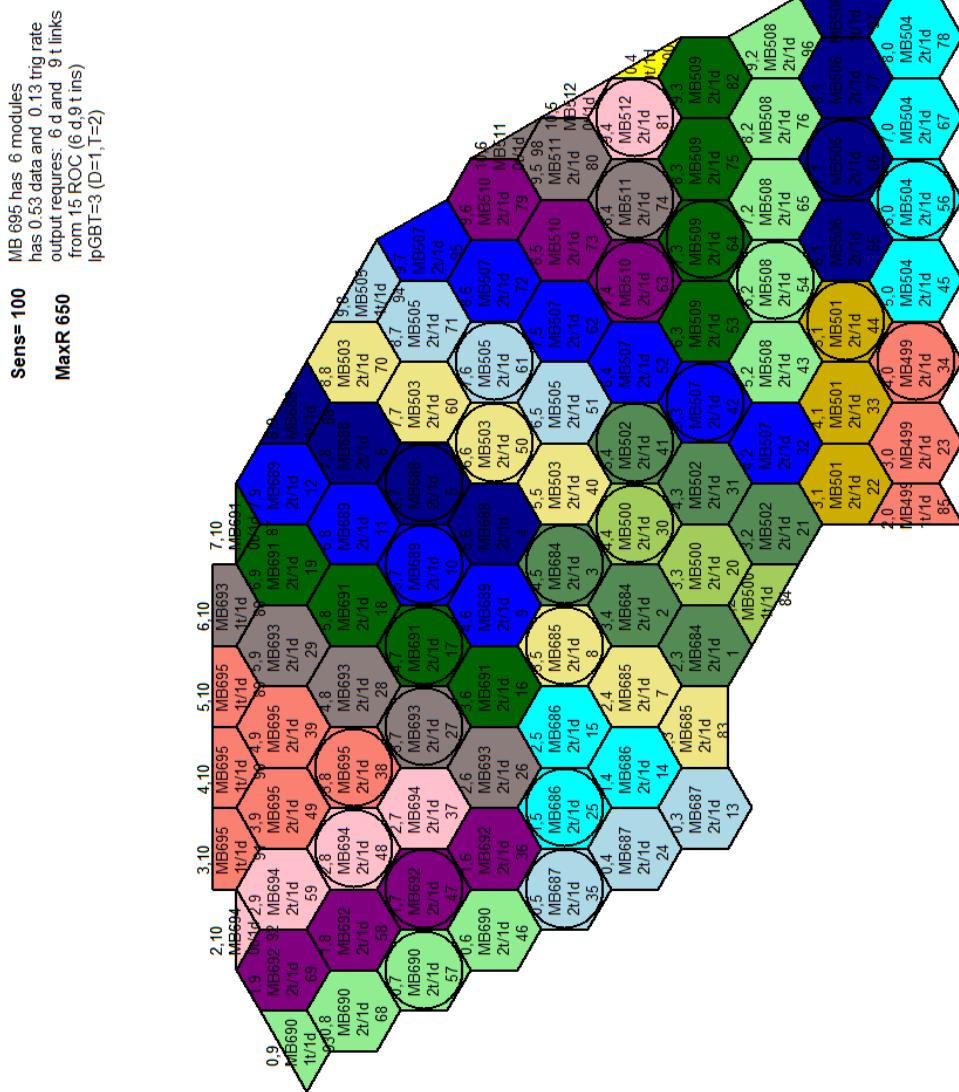


Figure 51: Tiling assignment for CE-H Cassette 0 and 1, Layer 38

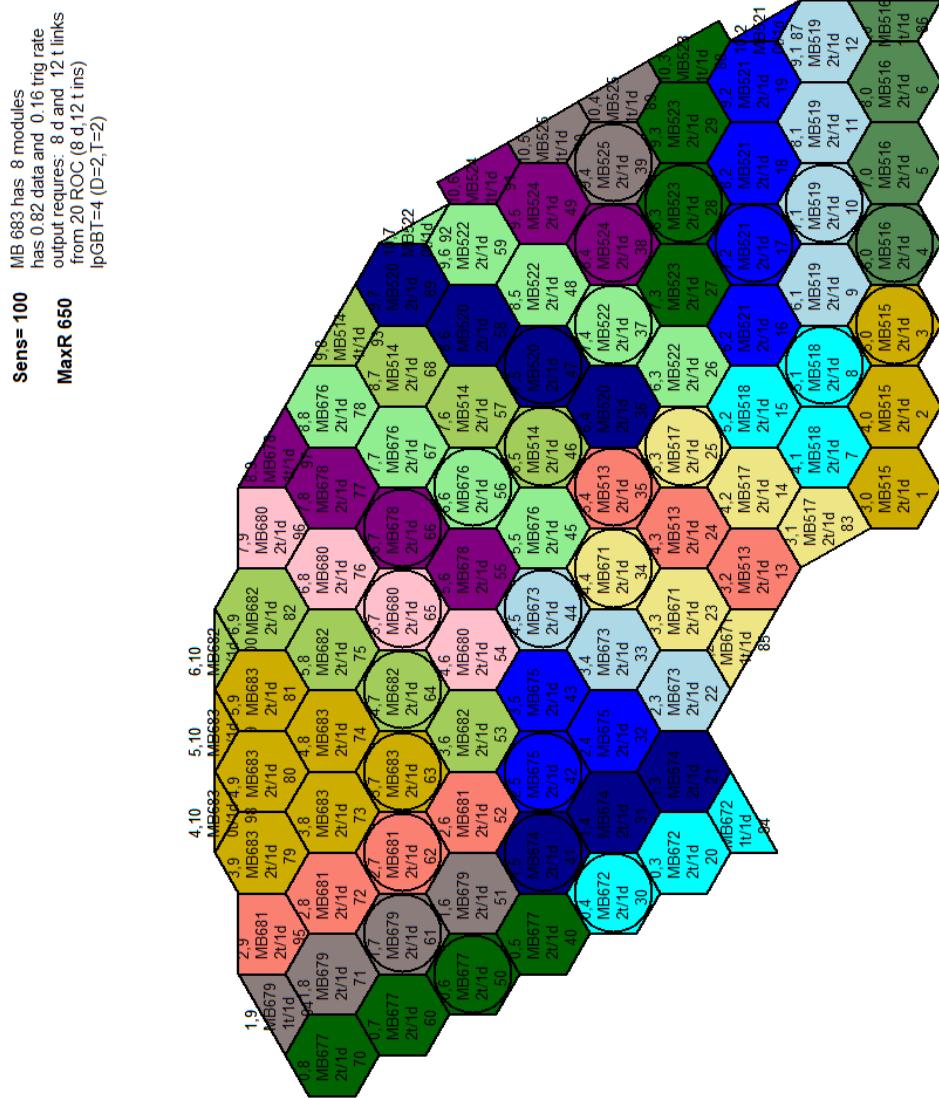
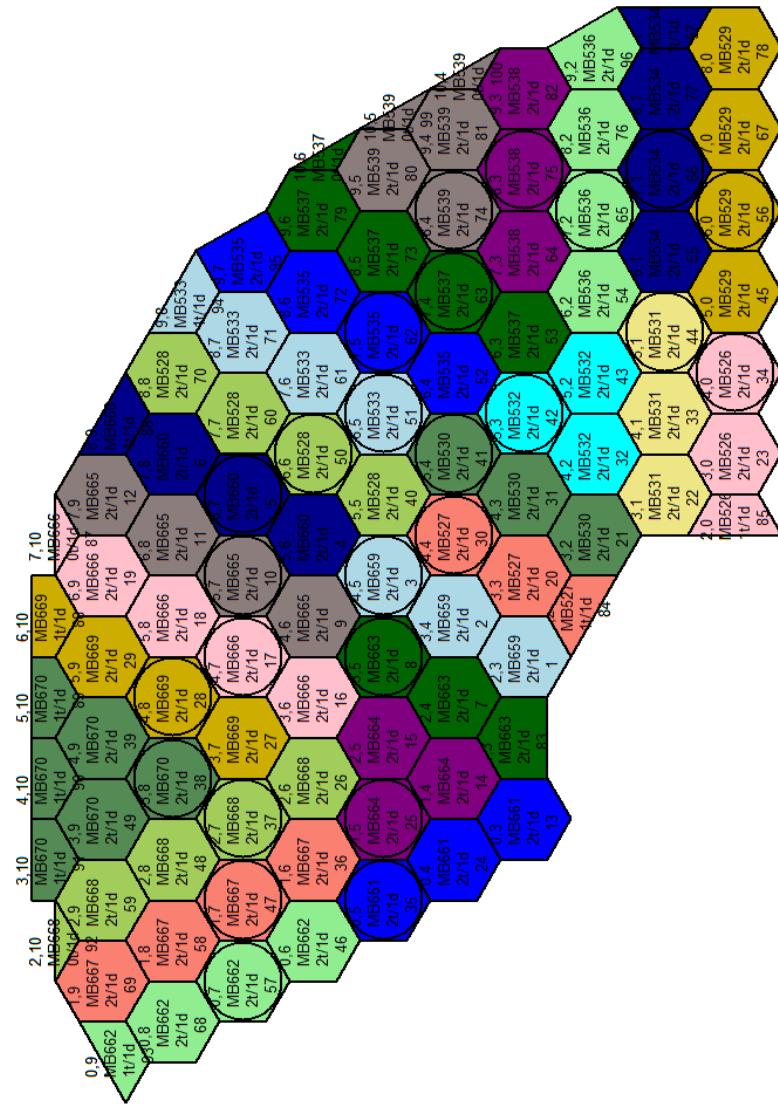


Figure 52: Tiling assignment for CE-H Cassettes 0 and 1, Layer 39

Sens= 100 MB670 has 6 modules
has 0.43 data and 0.10 trig rate
output requires: 6 d and 9 t links
from 15 ROC (6 d, 9 t ms)
lpGBT=3 (D=1, T=2)

MaxR 650



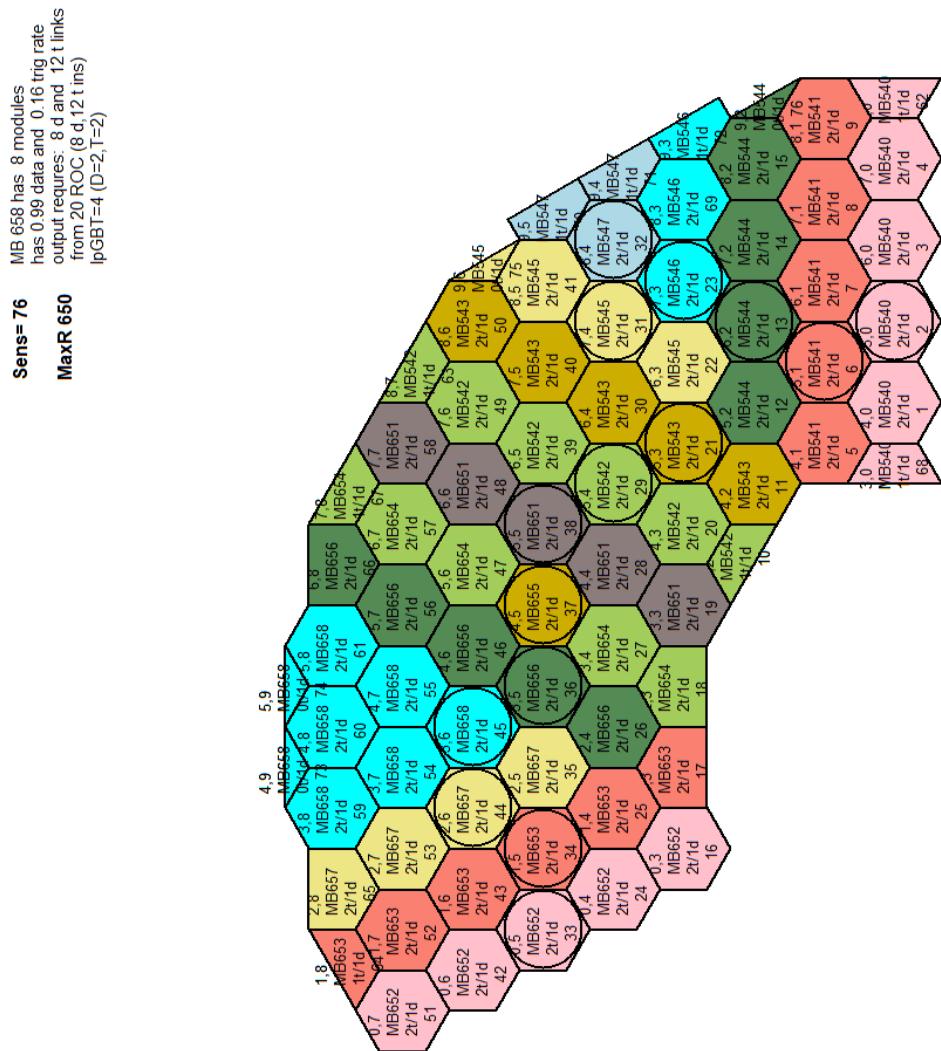


Figure 54: Tiling assignment for CE-H Cassettes 0 and 1, Layer 41

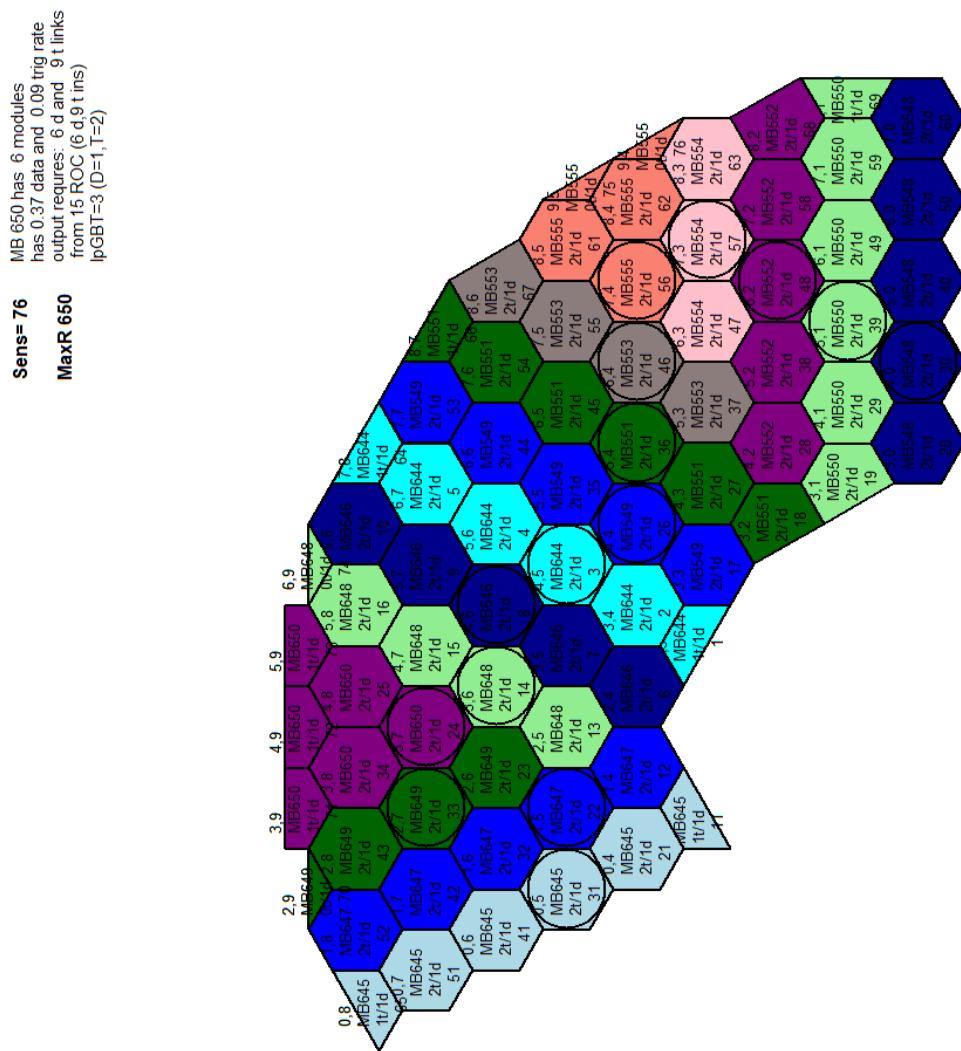
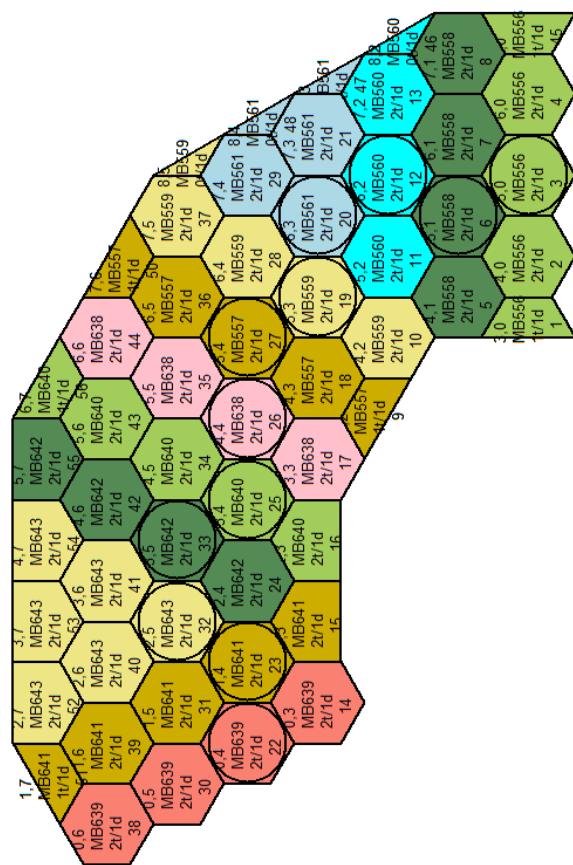


Figure 55: Tiling assignment for CE-H Cassettes 0 and 1, Layer 42

Sens= 56 MB 643 has 6 modules
has 1.02 data and 0.10 trig rate
output requires: 6 d and 12 t links
from 18 ROC (6 d,12 tins)
lpGBT=3 (D=1,T=2)

MaxR 650



Sens= 56
 MB 637 has 5 modules
 has 0.33 data and 0.04 trig rate
 output requires: 5 d and 6 t links
 from 11 ROC (5 d, 6 t ms)
 lpGBT=2 (D=1, T=1)

MaxR 650

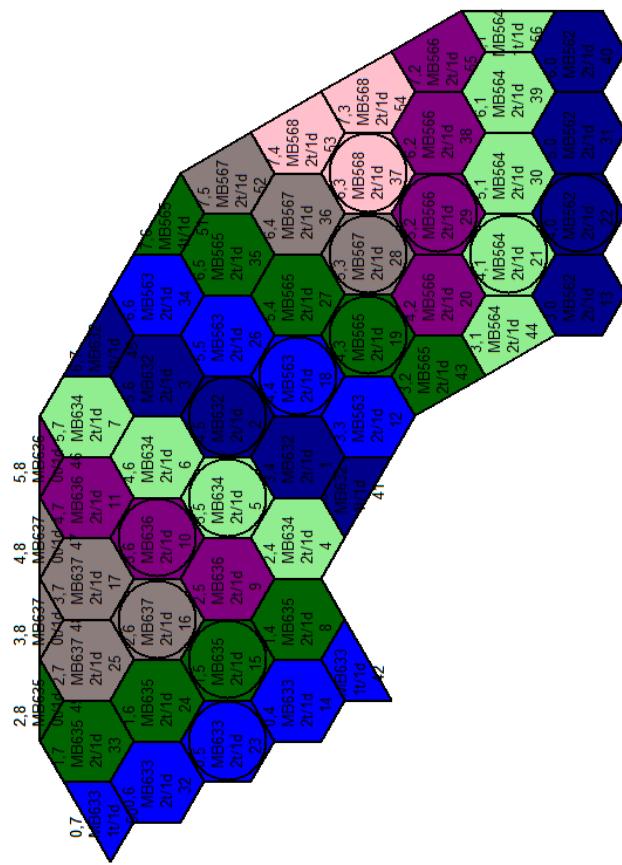


Figure 57: Tiling assignment for CE-H Cassette 0 and 1, Layer 44

Sens= 56
 MB 631 has 6 modules
 has 0.88 data and 0.07 trig rate
 output requires: 6 d and 12 t links
 from 18 ROC (6 d,12 tins)
 lpGBT=3 (D=1,T=2)

MaxR 650

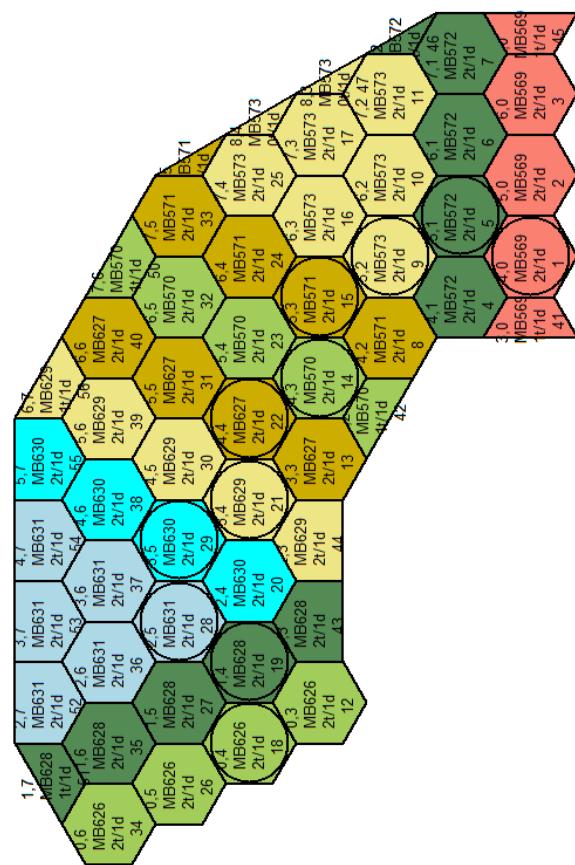
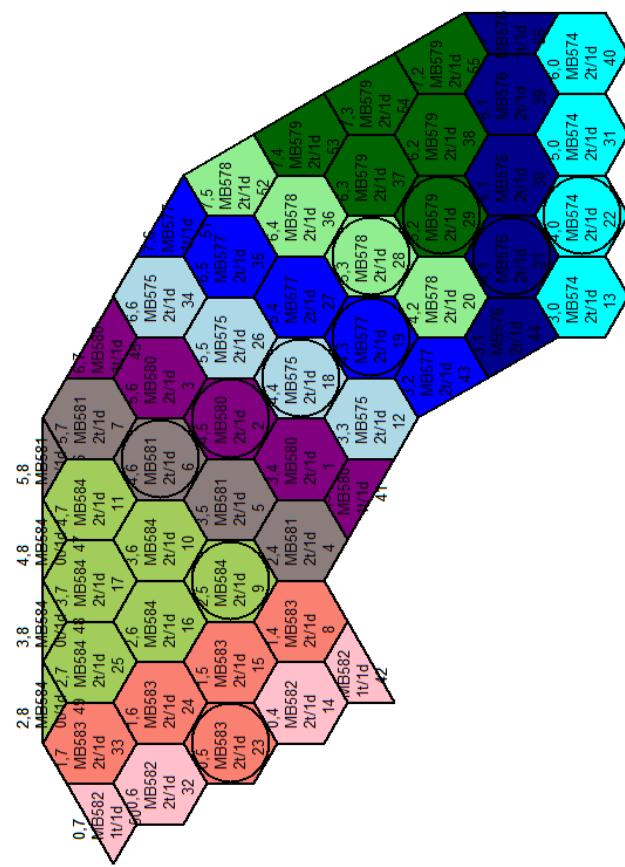


Figure 58: Tiling assignment for CE-H Cassettes 0 and 1, Layer 45

Sens= 56 MB 584 has 9 modules
has 0.96 data and 0.07 trig rate
output requires: 9 d and 12 t links
from 21 ROC (9 d,12 t ins)
lpGBT=4 (D=2, T=2)

MaxR 650



Sens= 40
 MB 625 has 6 modules
 has 1.65 data and 0.11 trig rate
 output requires: 6 d and 12 t links
 from 18 ROC (6 d,12 tins)
 lpGBT=3 (D=1,T=2)

MaxR 650

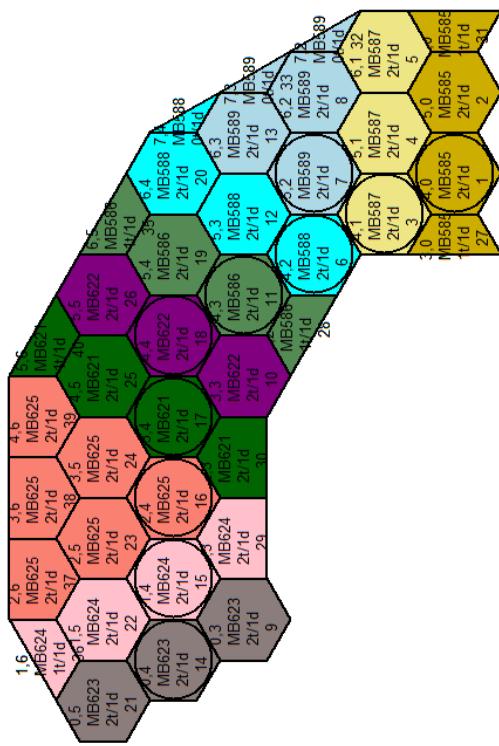


Figure 60: Tiling assignment for CE-H Cassette 0 and 1, Layer 47

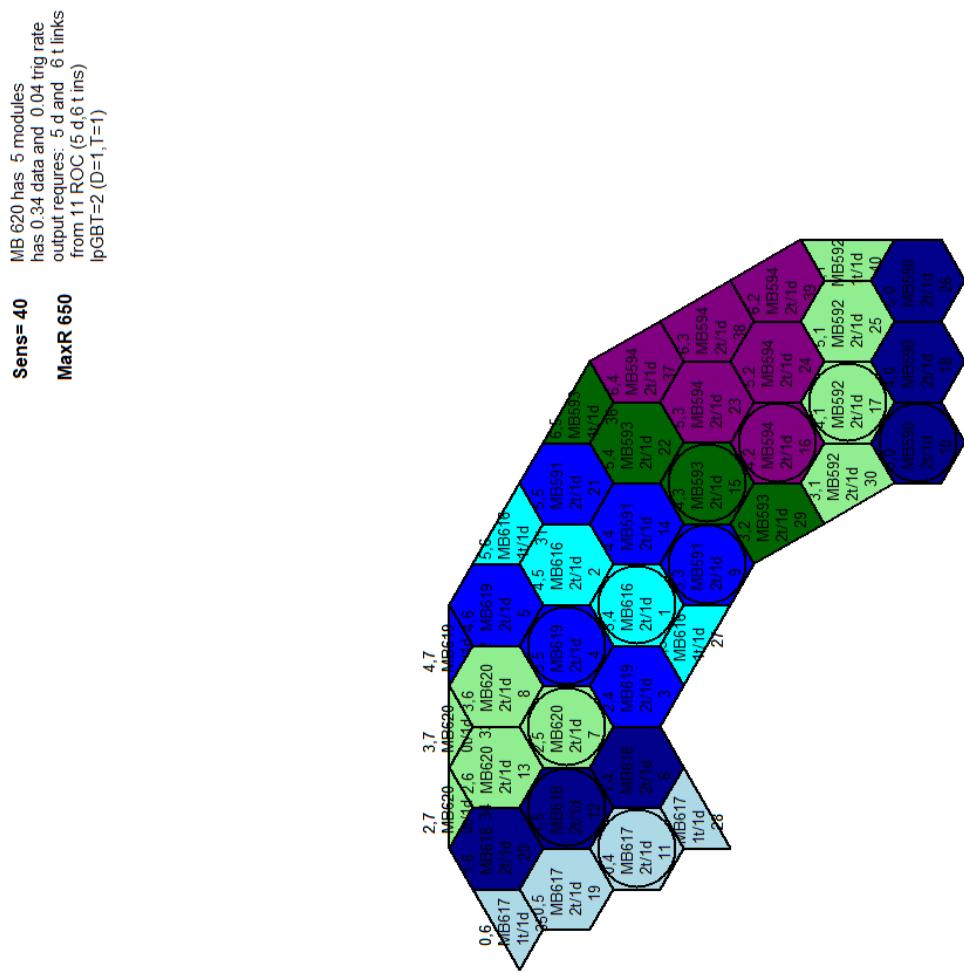


Figure 61: Tiling assignment for CE-H Cassettes 0 and 1, Layer 48

Sens= 40 MB 615 has 6 modules
has 1.18 data and 0.08 trig rate
output requires: 6 d and 12 t links
from 18 ROC (6 d,12 tins)
lpGBT=3 (D=1,T=2)

MaxR 650

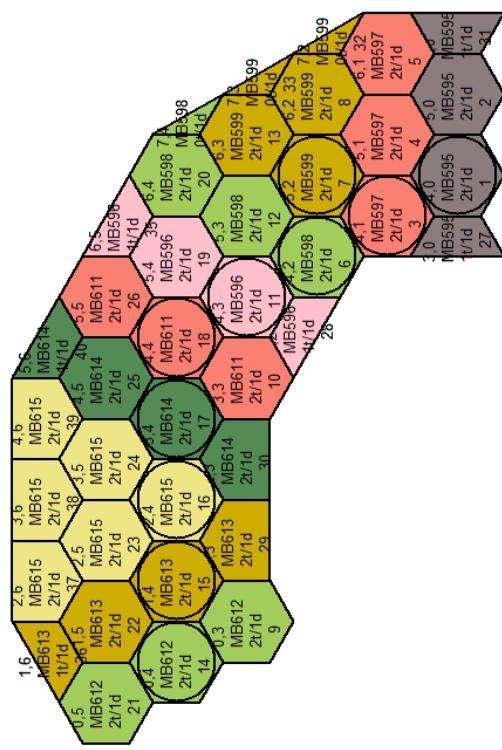


Figure 62: Tiling assignment for CE-H Cassettes 0 and 1, Layer 49

Sens= 40
 MB 10 has 3 modules
 has 0.20 data and 0.03 trig rate
 output requires: 3 d and 6 t links
 from 9 ROC (3 d, 6 t ins)
 lpGBT=2 (D=1, T=1)

MaxR 650

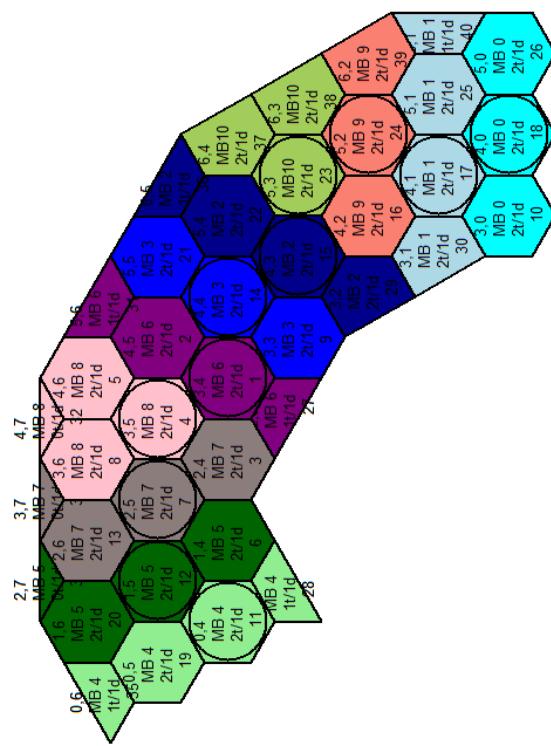


Figure 63: Tiling assignment for CE-H Cassette 0 and 1, Layer 50