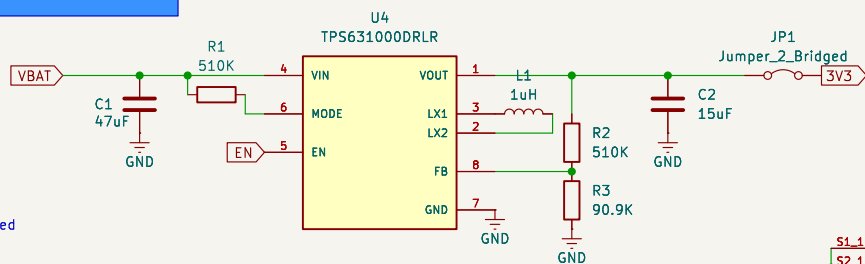


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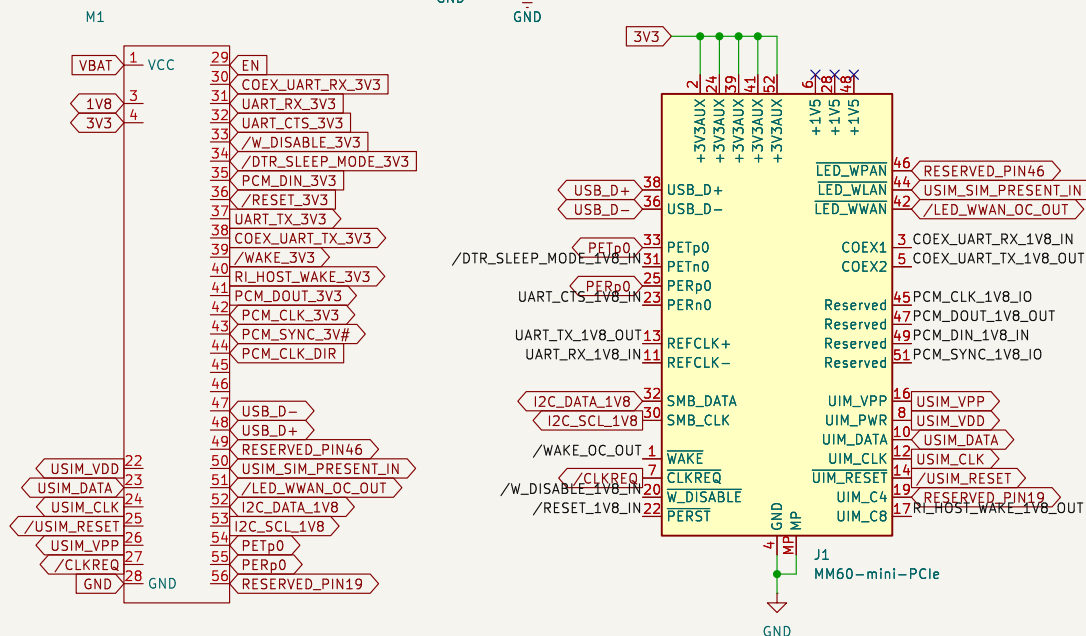
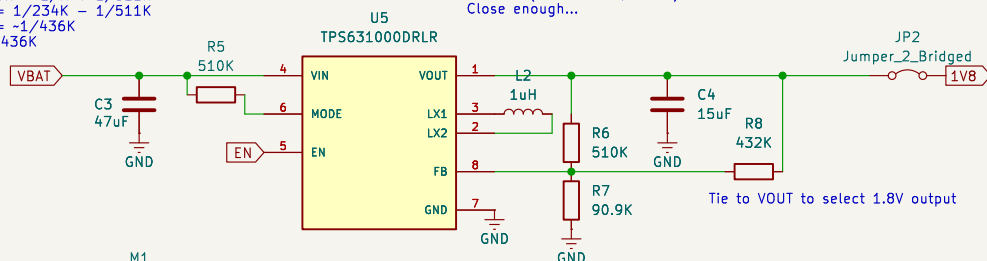


VFB = 0.5V
R2 <= 100K, 91K recommended

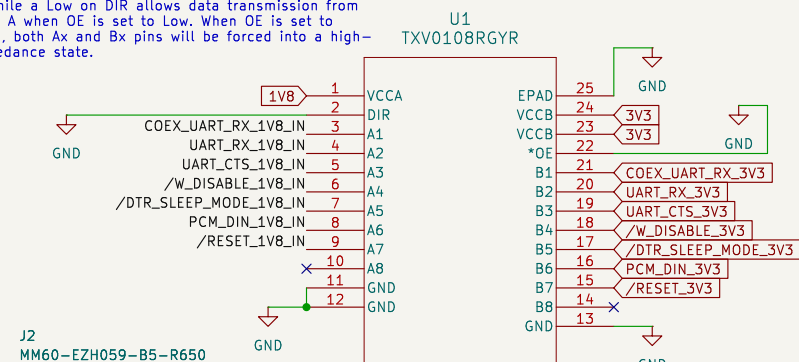
$$\begin{aligned} R1 &= R2 \times (VOUT / VFB - 1) \\ 1.8V : \quad R1 &= R2 \times (1.8 / 0.5 - 1) = R2 \times 2.6 = 234K \\ 3.3V : \quad R1 &= R2 \times (3.3 / 0.5 - 1) = R2 \times 5.6 = 511K \end{aligned}$$

So SEL1V8 should tie FB to VOUT with a resistor that in parallel to 511K yields 234K.

$$\begin{aligned} 1/R_P &= 1/R + 1/R \\ 1/260K &= 1/R + 1/511K \\ 1/R &= 1/234K - 1/511K \\ 1/R &= \sim 1/436K \\ R &= \sim 436K \end{aligned}$$

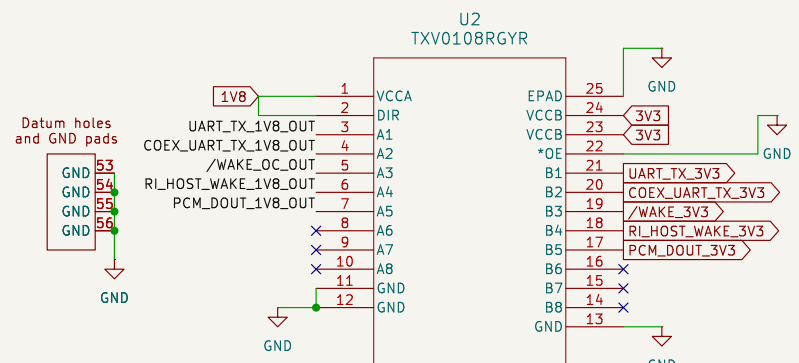
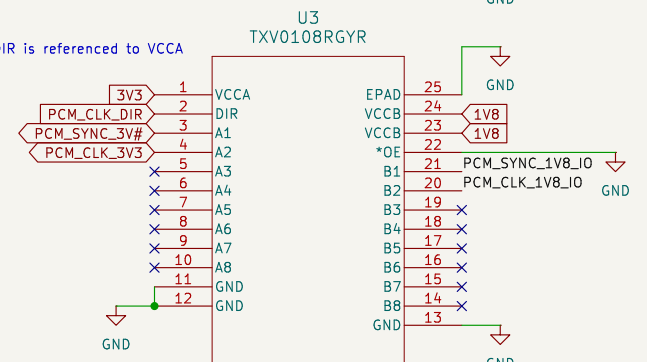


A High on DIR allows data transmission from A to B while a Low on DIR allows data transmission from B to A when OE is set to Low. When OE is set to High, both Ax and Bx pins will be forced into a high-impedance state.



J2
MM60-F7H059-B5-R650

DIR is referenced to VCCA



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