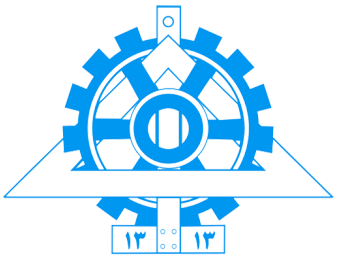

In The Name Of God

University of Tehran

Department of Engineering Science

Algorithms of Machine Learning

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Project 3

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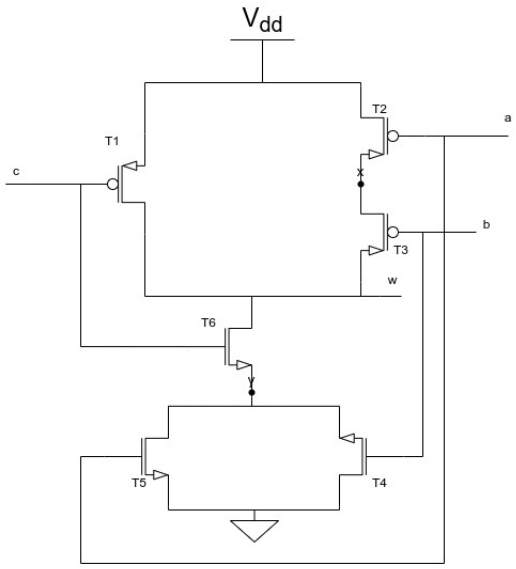
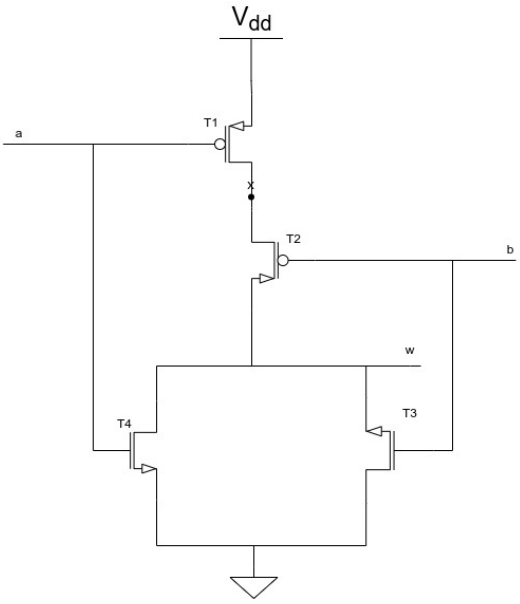
1. Well, as you can see, the codes and diagrams are corresponding.

OAI1



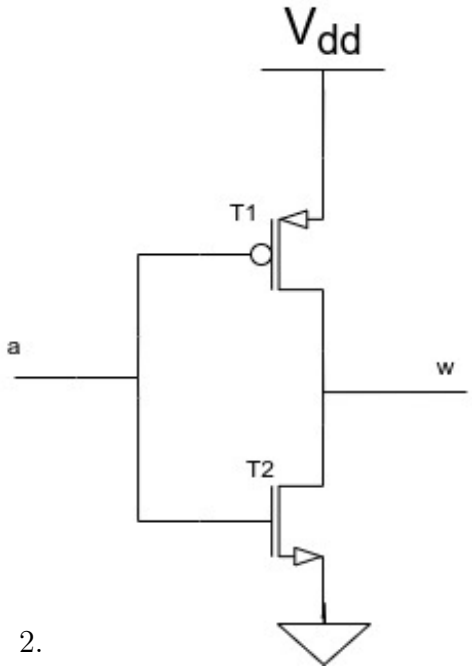

```
`timescale 1ns/1ns

module OAI1 (input a,b,c, output w);

        wire x,y;
        supply1 Vdd;
        supply0 Gnd;

        pmos #(5,6,7) T1(w, Vdd, c);
        pmos #(5,6,7) T2(x, Vdd, a);
        pmos #(5,6,7) T3(w, x, b);
        nmos #(3,4,5) T4(y, Gnd, b);
        nmos #(3,4,5) T5(y, Gnd, a);
        nmos #(3,4,5) T6(w, y, c);

endmodule
```

Nor



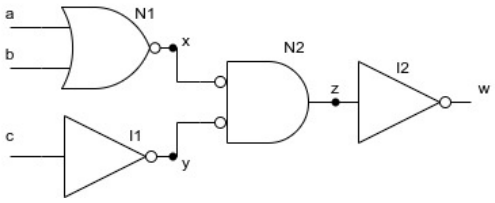

```
`timescale 1ns/1ns

module Nor (input a,b , output w);

        wire x;

        supply1 Vdd;
        supply0 Gnd;

        pmos #(5,6,7) T1(x, Vdd, a);
        pmos #(5,6,7) T2(w, x, b);
        nmos #(3,4,5) T3(w, Gnd, b);
        nmos #(3,4,5) T4(w, Gnd, a);

endmodule
```

inverter




```
`timescale 1ns/1ns

module Inv (input a, output w);

        supply1 Vdd;
        supply0 Gnd;
        pmos #(5,6,7) T1(w, Vdd, a);
        nmos #(3,4,5) T2(w, Gnd, a);
endmodule
```

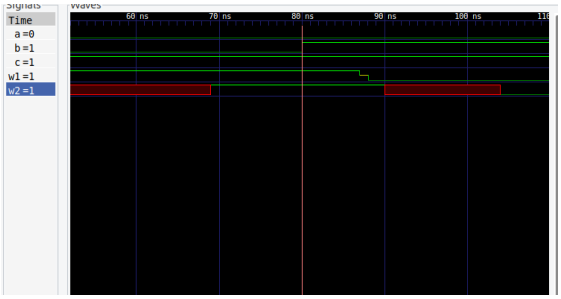
2.




```
`timescale 1ns/1ns

module OAI2 (input a,b,c, output w);

        wire x,y,z;

        Inv I1(.a(c), .w(y));

        Nor N1(.a(a), .b(b), .w(x));

        Nor N2(.a(x), .b(y), .w(z));

        Inv I2(.a(z), .w(w));


endmodule
```

3. for OAI1 I beleive the worse case delay happens when T2 and T3 transistors change(to 1) and it happens when T3 conducts(b=0) but T2 changes and c = 1 and it's 10 Ns (5+5 to1) and this in the case of OAI2 is 29 Ns ! which is a lot worse! according to the wave form but my calculation says it should be 25 (2*10 Ns for Nors and 5 Ns for invertion) for to0 case it holding the previous situation we change b to 1 for OAI1 it would be 8NS and for OAI2 it's 24(according to the

critical path)




```
`timescale 1ns/1ns

module test12;
        reg a, b, c;
        wire w1, w2;

        OAI1 sample1(.a(a), .b(b), .c(c), .w(w1));
        OAI2 sample2(.a(a), .b(b), .c(c), .w(w2));

        initial begin

                $dumpfile("OAI12TB.vcd");
                $dumpvars(0, test12);
                c = 1;
                a = 1;
                b = 0;
                #40 a = 0;

                #40 b = 1;
                #40 $finish;
        end
endmodule
```

4. mmmmm report is incomplete but it's due to the lack of time but codes are all complete sorry