ASSEMBLER

ABSTRACT

For this project I had to design an Instruction Set Architecture and implement an assembler for the same. I used the C++ programming language for the implementation of the assembler. The assembler inputs the symbolic program in the form of a .txt file and outputs the machine code representation as a string of 0's and 1's on the terminal. The instructions are fixed length instructions of length 32 bits each.

Machine Organization

The hypothetical machine for which the ISA is designed consists of:

1. A 32 bit data bus and a 16 bit address bus.
2. Fixed length instruction size of 32 bits.
3. There are 2 general purpose registers named R1 and R2 respectively. They are of 32 bits.
4. There are 6 flags namely zero flag, carry flag, overflow flag, input flag, output flag, and interrupt flag.
5. There exists mainly two more registers: Instruction Pointer and Address Register.
6. Instruction Pointer is the register that stores the address of the current executing instruction. It is of 16 bits.
7. Memory is accessible only through the address register, hence all memory addresses must go through the address register. This register is connected to the memory address bus and stores the memory addresses that we access. It is of 16 bits.
8. No direct memory operations allowed. All operations on memory operands must go through the accumulator register named here as R1. All memory reference instructions transfer their data into the R1 register.

Instruction Format

The instructions are majorly grouped into memory reference instructions, register instructions and input output instructions. There are 32 bits in each instrucon. Various groups of bits are assigned to addressing modes, opcodes and operands. The machine code format for each type of instrucon is described below.

Memory Reference Instructions:

0 3 15 32

Addressing Mode	Opcode Address

Register Reference Instructions:

0 3 15 23 32

Addressing Mode	Opcode	Register 1 Register 2

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Input – Output Instructions:

0 3 32

Addressing Mode	Opcode		

Addressing Modes:

There are 3 addressing modes in the ISA. These are

1. Immediate: The operand is part of the instrucon and is specified in the instrucon only. We append IM at the end of the instrucon to specify this addressing mode.

2. Direct: The operand is found at the address specified in the instrucon. We append D at the end of the instrucon to specify that the addressing mode is direct.

3. Indirect: The operand is found at the address found in the memory address specified in the instrucon. We append # at the end of the instrucon to specify that it is an indirect instruction.

In addition to these memory addressing modes we have 2 more addressing modes that refer to register mode and I/O mode that help the assembler in identifying the instrucon. In register reference instructions we have to append an R at the end of the instrucon to specify that instrucon is a register reference, similarly for IO instructions we append IO at the end.

Codes for addressing modes:

1. IM	0000	Immediate addressing mode
2. D	0011	Direct addressing mode
3. #	0010	Indirect addressing mode
4. IO	0111	I/O addressing mode
5. R	1111	Register mode

Instructions

INSTRUCTION	BINARY CODE	FUNCTION
1. LD	000000000001	Loading instruction from memory or from other register
2. AND	000000010000	Performs AND operation
3. ADD	000000000010	Performs ADD operaon
4. XOR	000000000100	Performs XOR operation

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5. ADC	000000001111	Performs AND operation including previous carry
6. XCHG	000000010001	Exchange the operands
7. STA	000000000101	Store content of R1 to memory
8. BUN	000000000111	Branch unconditionally
9. BSA	000000001010	Branch and save return address
10. NOT	000000100000	NOT the operand
11. IN	000000100001	Increment operand
12. DEC	000000100101	Decrement operand
13. SZ	111100000000	Skip if 0
14. SP	111100000001	Skip if > 0
15. SN	111100010000	Skip if < 0

16. CLA	111100000010	Clear R1
17. CLE	111100000100	Clear E
18. CLC	111100110000	Clear C
19. CLZ	111100110000	Clear Z
20. CLR	111100100001	Clear the register

21. HLT	111111111111	Halt computer
22. CIR	111100110001	Circulate right R1 and E
23. CIL	111101000000	Circulate le R1 and E
24. CMA	111101000011	Complement R1
25. CME	111101001000	Complement E
26. BLCFILL	111101001010	Fill from lowest bit of R1
27. BLCI	111101001100	Isolate lowest clear bit
28. BLCIC	111101010011	Isolate lowest clear bit and complement
29. BLCMSLK	111101100000	Mask from lowest clear bit
30. BLCS	111110000111	Set lowest clear bit
31. INP	11010000000100000000000000	Input operand to R1
32. OUT	11010001001100000000000000	Output operand from R1
33. SKI	11010101001000000000000000	Skip on input flag

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34. SKO	11010110001100000000000000	Skip on output flag
35. ION	11010110001100000000000000	Interrupt On
36. IOF	11010111010000000000000000	Interrupt Off

INPUT FILE:-

cao_input - Notepad

File Edit Format View Help

```
 ORG 100
 LD ADS D
 STA ADS D
 LD NBR D
 STA CTR D
 CLA
LOP, ADD PTR #
 SZ PTR
 SZ CTR
 BUN LOP
 HLT
ADS, HEX 150
PTR, HEX 0
NBR, DEC -6
CTR, HEX 0
SUM, HEX 0
 ORG 150
 DEC 75
 DEC 82
 DEC 92
 DEC 34
 DEC 22
 DEC 54
 END
```

OUTPUT :-

"C:\Users\Vertika\Desktop\Cao Project\assembler.exe"

```
0011000000000001000000001101111
0011000000000101000000001101111
0011000000000001000000001110001
0011000000000101000000001110010
1111000000100000000000000000000
0010000000000001000000001110000
1111000000000000000001110000000
1111000000000000000001110010000
0000000001110000000011010100000

Process returned 0 (0x0)   execution time : 0.033 s
Press any key to continue.
```