	row a	row b	row c	notes	
1	5V	5V	5V	max 2A per 41612 pin	5 bit GA[0:4] sets CAN addr (0-31, 0x1f=bcast, 0x1e supervisor), 0=GND, 1=float. CAN is local to crate.
2	GND	GND	GND		
3	12V	12V	12V	optional power rail	
4	CAN-		IN_TX+		
5	CAN+		IN_TX-		CMOS driver fanout (for RESET and OR_OUT) limits number of slots in one crate to around 16.
6	GA0		IN_RX+		
7	GA1		IN_RX-		
8	GA2		OUT_TX+		
9	GA3		OUT_TX-		
10	GA4		OUT_RX+		A crate controller (small card not in a slot) manages power supply and other crate functions.
11			OUT_RX-		
12	GND	GND	GND		
13	3V3	3V3	3V3	optional power rail	
14	RESET~		UP_TX+		
15	OR_INA		UP_TX-		
16	OR_INB		UP_RX+		in/out, up/down, left/right are links of a 3D torus mesh network. trina, trinb, trout are links of a tree network. All links are full-duplex LVDS.
17	OR_OUT		UP_RX-		
18	TRINB_TX+		DOWN_TX+		
19	TRINB_TX-		DOWN_TX-		
20	TRINB_RX+		DOWN_RX+		
21	TRINB_RX-		DOWN_RX-		
22	GND	GND	GND		
23	TROUT_TX+		TRINA_TX+		A wired OR network (literally wired-or open drain logic on the bus) can implement a fast barrier. Two channels of output are needed to ensure successive barriers are race-free. Result are aggregated on one output pin which toggies state after each barrier is finalized.
24	TROUT_TX-		TRINA_TX-		
25	TROUT_RX+		TRINA_RX+		
26	TROUT_RX-		TRINA_RX-		
27	LEFT_RX+		RIGHT_TX+		
28	LEFT_RX-		RIGHT_TX-		
29	LEFT_TX+		RIGHT_RX+		
30	LEFT_TX-		RIGHT_RX-		
31	GND	GND	GND		
32	5V	5V	5V		