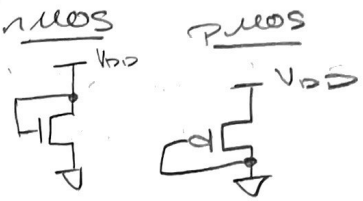
ESE 3700 HW3

2. a) nMOS current: $2.508 \cdot 10^{-5}$ A

pMOS current: $1.673 \cdot 10^{-5}$ A



b) nMOS calc:

$\mu_n = 540 \frac{cm^2}{V \cdot s}$

$C_{ox} = 35 \frac{fF}{\mu m^2}$

$V_{THn} = 300\,mV$

$V_{DS} > V_{GS} - V_{TH}$: saturation

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THn})^2$$

$$= \frac{1}{2} 540 \frac{cm^2}{V \cdot s} \cdot 35 \frac{fF}{\mu m^2} \cdot (1) (0.8V - 0.3V)^2$$

$$= \frac{1}{2} 540 \frac{cm^2}{V \cdot s} \cdot \frac{1 m^2}{10^4 cm^2} \cdot \frac{35 fF}{\mu m^2} \cdot \frac{10^{12} \mu m^2}{1 m^2} 0.25\ V^2$$

$$= 2.363 \cdot 10^{-4}\ A$$

→ calculated current is much greater than simulated

velocity saturation

not specified

$$I_D = v_{sat} C_{ox} W \left(V_{GS} - V_{th} - \frac{V_{DSAT}}{2}\right)$$

$$= 10^5 \frac{m}{s} \cdot 35 \frac{fF}{\mu m^2} \cdot \frac{10^{12} \mu m^2}{m^2} \cdot 22\,nm \cdot \left(0.8V - 0.3V - \frac{V_{DSAT}}{2}\right)$$

a) cont.

$$nMOS\ R_{DS} = \frac{0.8V}{2.508 \cdot 10^{-5} A} = 31.9\,k\Omega$$

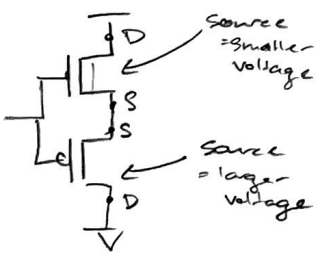
$$pMOS\ R_{DS} = \frac{0.8V}{1.673 \cdot 10^{-5} A} = 47.82\,k\Omega$$

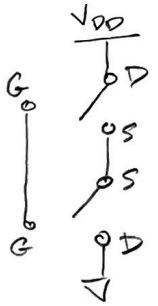
b) cont.

$$nMOS\ R_{DS} = \frac{0.8V}{2.363 \cdot 10^{-4} A} = 3.39\,k\Omega$$

6.

a)





$V_G = V_{DD}$:

nMOS: $V_{GS} = V_{DD} - 0V$

↳ closed switch

pMOS: $V_{GS} = V_{DD} - V_S = 0V$

↳ closed switch

$V_G = 0V$:

nMOS: $V_{GS} = 0V$

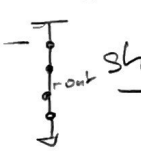
↳ open switch

pMOS: $V_{GS} = 0V > V_{THP}$ ×

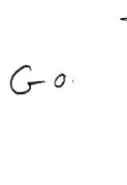
↳ open switch

Not a valid CMOS circuit because it either shorts to GND or is completely open

⇒



short!



completely open

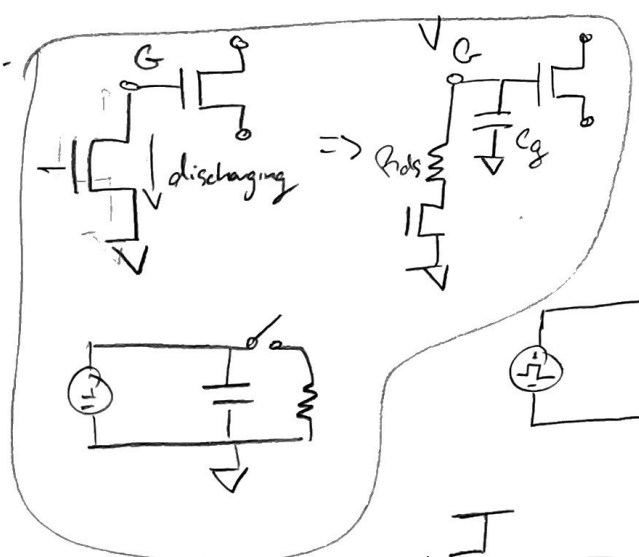
6. b) The transfer function plotted in Spice was exponential and positive → not at all what eNOS is supposed to do. It did not have clear input lows and highs and could not surpass 300 mV.

4. Subthreshold : $C_G = C_{ox}WL + 2C_o$ ← max capacitance
Linear : $C_G = C_{ox}WL + 2C_o$
Saturation : $C_G = \frac{2}{3}C_{ox}WL + 2C_o$

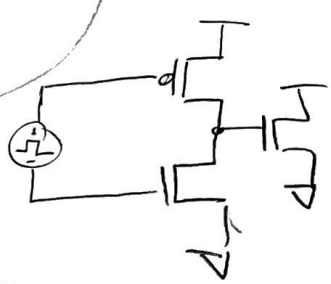
$$C_o = \frac{1}{2}C_{ox}W(L_{drawn} - L_{effective})$$
$$= \frac{1}{2}\cdot 35\frac{fF}{\mu m^2}\cdot 22nm(22nm - 17nm)$$
$$= \frac{1}{2}\cdot 35\cdot 10^{-15}\frac{F}{\mu m^2}\cdot\frac{10^{12}\mu m^2}{m^2}\cdot 22\cdot 10^{-9}m\cdot 5\cdot 10^{-9}m$$
$$= 1.925\cdot 10^{-18}F$$

$$C_G = C_{ox}W L_{eff} + 2C_o$$
$$= 35\frac{fF}{\mu m^2}\cdot 22nm\cdot 17nm + 2\cdot 1.925\ 10^{-18}F$$
$$= 1.5015\cdot 10^{-17}F$$ ← worst case gate capacitance

5.



a) $\tau = R_{ds}C_g = 3.3952\cdot 1.5015\cdot 10^{-17}F$
$= 5.08\ 10^{-14}\ s$

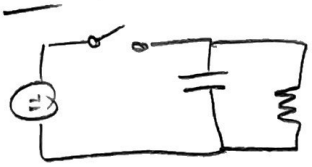


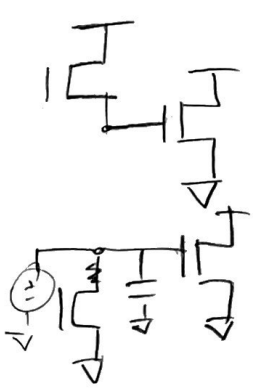
b) fall time:
$7.305\cdot 10^{-12} - 5\cdot 10^{-12}\ s$
$= 2.3\ ps$

$\tau = \frac{t_{rise}}{2.2} = 1.045\ ps$

much larger

Want:





c) This tells me that there can be huge discrepancies between my hand calculations and SPICE, and that SPICE is probably much more accurate.

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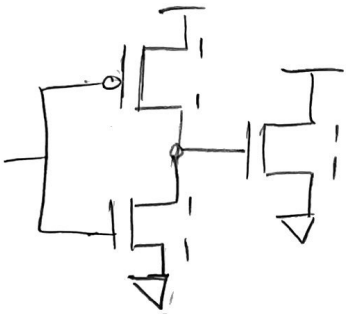
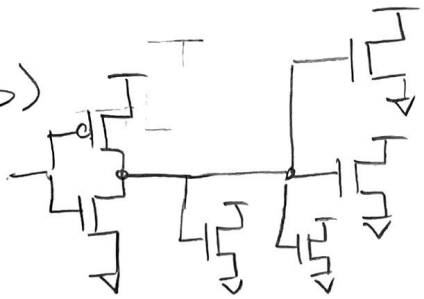
3. a)



rise time: 5.475ps - 1.9ps

$\uparrow_a = \frac{t_{rise}}{2.2} = \frac{3.575ps}{2.2} = 1.625ps$

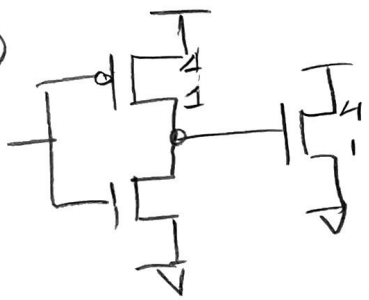
b)



rise time: 8.21ps - 2.07ps = 6.14ps

$\uparrow_b = \frac{t_{rise}}{2.2} = \frac{6.14ps}{2.2} = 2.79ps$

c)



rise time: 16.7ps - 2.36ps = 14.34ps

$\uparrow_c = \frac{t_{rise}}{2.2} = \frac{14.34ps}{2.2} = 6.52ps$

ngspice commands:

a) tran 0.1ps 20ps
plot net@11 out

b) tran 1ps 20ps
plot net@6 net@20

c) tran 0.1ps 30ps
plot net@3 out

d) $\uparrow_a$, $\uparrow_b$, $\uparrow_c$ are the time constants for their respective problems.

$\uparrow_c$ is around 4 times $\uparrow_a$, which is expected because of the width and length of the transistor being both 4 times as high, increasing the capacitance by 4x.

What surprised me was that $\uparrow_b$ was only $1.72 \times \uparrow_a$. I would expect it to be 4x as well, since all the C_g's would be in parallel, but it still seems like the output capacitance increased.