2a-nmos

```
*** SPICE deck for cell hw3_2a_nmos{sch} from library ese3700
*** Created on Wed Feb 12, 2025 08:57:45
*** Last revised on Wed Feb 12, 2025 09:34:09
*** Written on Wed Feb 12, 2025 09:36:18 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
* Model cards are described in this file:
.include C:/Users/garre/ese_3700/22nm_HP.pm

.global gnd vdd

*** TOP LEVEL CELL: hw3_2a_nmos{sch}
Mnmos@0 vdd vdd gnd gnd N L=0.022U W=0.022U
VVdd vdd gnd DC 0.8 AC 0
.END
```

2a-pmos

```
*** SPICE deck for cell hw3_2a_pmos{sch} from library ese3700
*** Created on Wed Feb 12, 2025 09:02:50
*** Last revised on Wed Feb 12, 2025 09:33:12
*** Written on Wed Feb 12, 2025 11:55:36 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
* Model cards are described in this file:
.include C:/Users/garre/ese_3700/22nm_HP.pm

.global gnd vdd

*** TOP LEVEL CELL: hw3_2a_pmos{sch}
Mpmos@0 vdd gnd gnd vdd P L=0.022U W=0.022U
VVdd vdd gnd DC 0.8 AC 0
.END
```

3a

```
*** SPICE deck for cell hw3_3a{sch} from library ese3700
*** Created on Wed Feb 12, 2025 16:18:39
*** Last revised on Wed Feb 12, 2025 16:27:52
*** Written on Wed Feb 12, 2025 16:28:05 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
* Model cards are described in this file:
.include C:/Users/garre/ese_3700/22nm_HP.pm

.global gnd vdd

*** TOP LEVEL CELL: hw3_3a{sch}
Mnmos@0 Out net@11 gnd gnd N L=0.022U W=0.022U
Mnmos@1 vdd Out gnd gnd N L=0.022U W=0.022U
Mpmos@0 vdd net@11 Out vdd P L=0.022U W=0.022U
VVPulse@0 net@11 gnd pulse (0.8V 0V 0ns 2ps 2ps 3ns 6ns) DC 0V AC 0V 0
VV_Generi@0 vdd gnd DC 0.8 AC 0
.END
```

3b

```
*** SPICE deck for cell hw3_3b{sch} from library ese3700
*** Created on Wed Feb 12, 2025 16:24:30
*** Last revised on Wed Feb 12, 2025 16:32:57
*** Written on Wed Feb 12, 2025 16:33:14 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
* Model cards are described in this file:
.include C:/Users/garre/ese_3700/22nm_HP.pm

.global gnd vdd

*** TOP LEVEL CELL: hw3_3b{sch}
Mnmos@0 net@20 net@6 gnd gnd N L=0.022U W=0.022U
Mnmos@1 vdd net@20 gnd gnd N L=0.022U W=0.022U
Mnmos@2 vdd net@20 gnd gnd N L=0.022U W=0.022U
Mnmos@3 vdd net@20 gnd gnd N L=0.022U W=0.022U
Mnmos@4 vdd net@20 gnd gnd N L=0.022U W=0.022U
Mpmos@0 vdd net@6 net@20 vdd P L=0.022U W=0.022U
VVPulse@0 net@6 gnd pulse (0.8V 0V 0ns 2ps 2ps 3ns 6ns) DC 0V AC 0V 0
VV_Generi@0 vdd gnd DC 0.8 AC 0
.END
```

3c

```
*** SPICE deck for cell hw3_3c{sch} from library ese3700
*** Created on Wed Feb 12, 2025 16:38:42
*** Last revised on Wed Feb 12, 2025 16:39:53
*** Written on Wed Feb 12, 2025 16:40:04 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
* Model cards are described in this file:
.include C:/Users/garre/ese_3700/22nm_HP.pm

.global gnd vdd

*** TOP LEVEL CELL: hw3_3c{sch}
Mnmos@0 Out net@3 gnd gnd N L=0.022U W=0.022U
Mnmos@1 vdd Out gnd gnd N L=0.088U W=0.088U
Mpmos@0 vdd net@3 Out vdd P L=0.022U W=0.022U
VVPulse@0 net@3 gnd pulse (0.8V 0V 0ns 2ps 2ps 3ns 6ns) DC 0V AC 0V 0
VV_Generi@0 vdd gnd DC 0.8 AC 0
.END
```

5b

```
*** SPICE deck for cell hw3_5b{sch} from library ese3700
*** Created on Wed Feb 12, 2025 15:38:37
*** Last revised on Wed Feb 12, 2025 15:58:21
*** Written on Wed Feb 12, 2025 15:58:28 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
* Model cards are described in this file:
.include C:/Users/garre/ese_3700/22nm_HP.pm

.global gnd vdd

*** TOP LEVEL CELL: hw3_5b{sch}
Mnmos@0 net@0 net@4 gnd gnd N L=0.022U W=0.022U
Mnmos@1 vdd net@0 gnd gnd N L=0.022U W=0.022U
Mpmos@0 vdd net@4 net@0 vdd P L=0.022U W=0.022U
VVPulse@0 net@4 gnd pulse (0 0.8V 5ps 0.1ps 1ps 250ps 500ps) DC 0V AC 0V 0
VV_Generi@0 vdd gnd DC 0.8 AC 0
.END
```

6b

```
*** SPICE deck for cell hw3_6b_test{sch} from library ese3700
*** Created on Wed Feb 12, 2025 15:06:37
*** Last revised on Wed Feb 12, 2025 15:07:37
*** Written on Wed Feb 12, 2025 15:07:56 by Electric VLSI Design System, version 9.07
*** Layout tech: mocmos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.1FF
* Model cards are described in this file:
.include C:/Users/garre/ese_3700/22nm_HP.pm

*** SUBCIRCUIT ese3700__hw3_6b FROM CELL hw3_6b{sch}
.SUBCKT ese3700__hw3_6b IN OUT
** GLOBAL gnd
** GLOBAL vdd
Mnmos@0 vdd IN OUT gnd N L=0.022U W=0.022U
Mpmos@0 OUT IN gnd vdd P L=0.022U W=0.022U
.ENDS ese3700__hw3_6b

.global gnd vdd

*** TOP LEVEL CELL: hw3_6b_test{sch}
VV_Generi@0 net@0 gnd DC 0.8 AC 0
Xhw3_6b@0 net@0 hw3_6b@0_OUT ese3700__hw3_6b
.END
```