EELE 367 - Logic Design (Activity Flow & Grading Breakdown)

Module	Section / Topic / Activity	HW Points	Lab Points	Quiz Points	Exam Points	Project Points
Course Orientation & Syllabus	Course Logistics					
Review of Classical Digital Design	EELE 261 Review Problem Set	17				
Module 8 - VHDL (part 2)	8.1 - The Process	6				
	8.2 - Conditional Programming Constructs	15				
	8.3 - Signal Attributes	6				
	8.4 - Test Benches	15				
	Lab 8(a) - 7 Segment Decoders using if/then		25			
	8.5 - Packages	15				
	Lab 8(b) - Binary Characters using case		25			
	Module 8 Quiz			20		
Module 9 - Behavioral Modeling	9.1 - Modeling Seq. Storage Devices in VHDL	6				
	Lab 9(a) - Ripple Counter & Character Displays		25			
	9.2 - Modeling FSMs in VHDL	6				
	9.3 - FSM Design Examples in VHDL	15				
	Lab 9(b) - Walking 1 FSM on Char Display		25			
	9.4 - Modeling Counters	15				
	Lab 9(c) - Counters using 1 Process		25			
	9.5 - RTL Modeling	6				
	Lab 9(d) - BCD Counter		25			
	Module 9 Quiz			20		
Exam #1	Exam #1 - Modules 8 & 9, Online				125	
Module 10 - Memory	10.1 - Memory Architecture & Terminology	6				
	10.2 - Non-Volatile Memory Technology	6				
	10.3 - Volatile Memory Technology	6				
	10.4 - Modeling Memory in VHDL	15				
	Lab 10 - Accessing Memory		50			
	Module 10 Quiz			10		
Module 11 - Programmable Logic	11.1 - Programmable Arrays	6				
	11.2 - Field Programmable Gate Arrays	6				
	Module 11 Quiz			10		
Module 12 - Arithmetic Circuitry	12.1 - Addition	15				
	12.2 - Subtraction	6				
	12.3 - Multiplication	6				
	12.4 - Division	6				
	Lab 12(a) - HEX Adder		25			
	Lab 12(b) - BCD Adder		25			
	Module 12 Quiz			20		

Exam #2	Exam #2 - Modules 10, 11, 12, Online				125	
Module 13 - Computer Systems	13.1 - Computer Hardware 13.2 - Computer Software 13.3 - 8-Bit Computer Implementation 13.4 - Architectural Considerations					
	Module 13 Quiz			20		
Final Project	8-Bit MicroComputer					200
	Total Points:	200	250	100	250	200