EELE 367 - Introduction to Logic Circuits

Lab 9(b) – Walking 1 Finite State Machine

Objective

The objective of this lab is to gain experience designing finite state machines (FSM) in VHDL using a behavioral modeling approach. You are going to design a FSM that will produce a walking 1 pattern on the character displays of the DE0-CV board. You will also gain experience using a divided down clock to trigger your FSM.

Outcomes

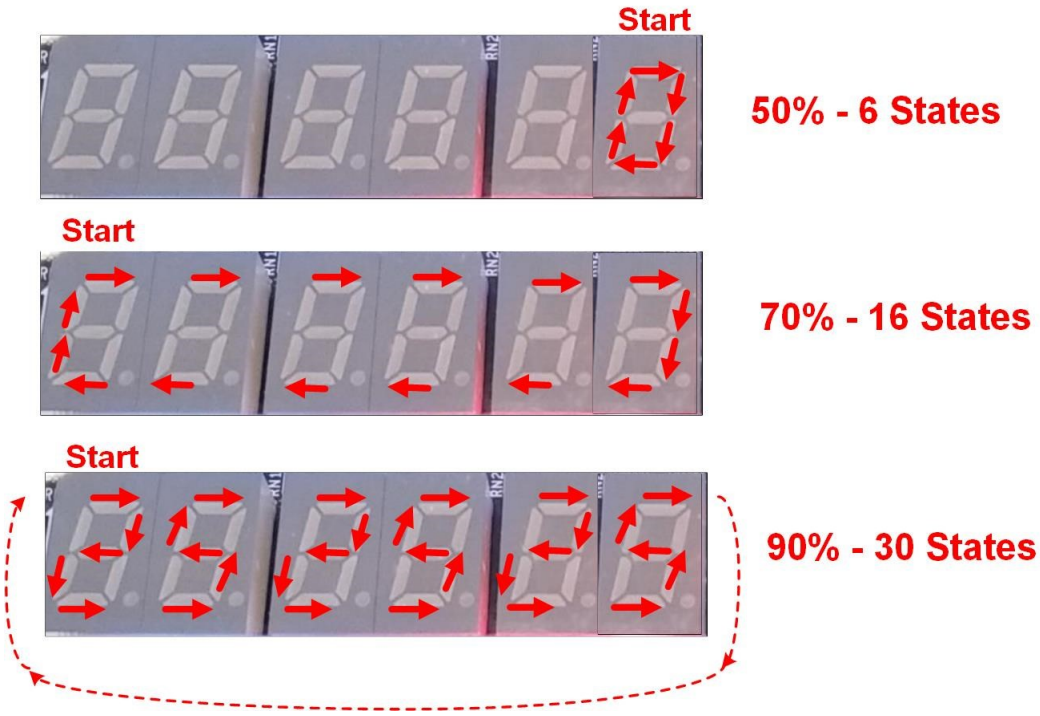
After completing this lab you should be able to:

- Create a FSM using the three process, behavioral modeling approach.
- Use a divided down clock in order to drive the FSM at a slower rate.

Deliverables

The deliverable(s) for this lab are as follows:

- Demonstrate a walking 1 FSM that displays the pattern on the segments of the character displays on the DE0-CV. A *walking 1* pattern is one that asserts one, and only one, bit at any given time. When this is displayed on LEDs, it appears that the asserted LED *walks* across the display. This lab has a varying grading scale based on the walking 1 pattern you choose to implement. Designs that include more LEDs within the pattern result in larger FSMs. You may choose to implement one of the three following options based on how many points you wish to receive.



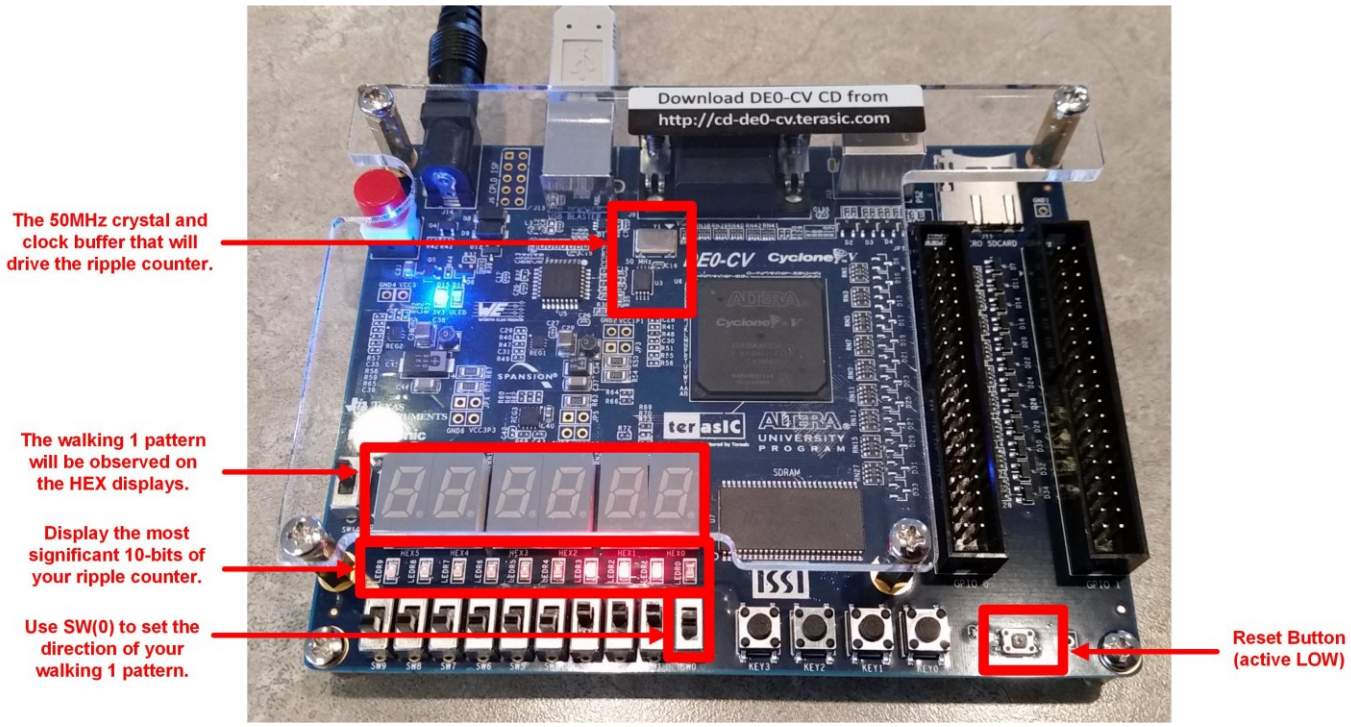
- Upload your top.vhd file to the lab DropBox (10%).

Lab Work & Demonstration

Part 1 – System Design

You are going to design a walking 1 FSM using the three process behavioral modeling approach in VHDL. Your FSM should assert (or turn on), one LED segment on the character displays at a time and create the *walking* pattern. Remember that the character displays are active LOW. You can choose the size of the FSM you wish to design based on the grade you wish to achieve. The available patterns to choose are given above. Your design must have a direction input that comes from SW(0). This input sets the direction of the walking 1 pattern. Your FSM should be able to move the walking one in both forward and reverse directions based on the SW(0) input.

In order to run the walking 1 pattern slow enough to be observed on the character displays, you will clock your FSM with one of the bits from last lab's ripple counter. You will need to choose one of the bits from the counter that has a toggle rate slow enough so that you can observe the walking 1 pattern on the DE0-CV board. You should keep the upper 10-bits of the ripple counter being displayed on the red LEDs. The following figure shows the I/O used in this lab.



A) Create new Quartus project by copying your ripple counter lab. Name it "Lab9b_Walking_1_FSM". **Don't delete your ripple counter!**

B) Create a walking 1 FSM using a three process, behavioral modeling approach. Clock your FSM using one of the outputs of your ripple counter that is slow enough so that the walking 1 pattern can be observed. You can choose how large of a FSM you wish to implement based on your desired grade. Your FSM should have a "direction" input that will reverse the flow of the pattern. This input will come from the SW(0) slider switch.

   Your ripple counter should identical as last lab. It should be clocked off of the 50MHz incoming clock and have an active LOW reset from the push button on the DE0-CV board. Display the upper 10-bits of the counter on the red LEDs.

C) Compile your design. Fix any Errors.

D) Download and test your design. Fix any Errors.

E) Demonstrate your design.

DEMO – Once checked off, upload your top.vhd file only to the lab DropBox. Let the lab instructor know what clock frequency your FSM is running at.

Lab Grading

Demo – Proper Operation of your FSM (50%, 70%, or 90%)	_____ **/ 90**
Review of your top.vhd file	_____ **/ 10** (uploaded to DropBox)
Total	_____ **/ 100**

Post Lab Survey (Just for your own knowledge. This is not graded)

1) Can you create a FSM using the three process, behavioral modeling approach in VHDL?
2) Can you use the output of a ripple counter to provide a divided down clock to your FSM?