EELE 367 – Logic Design (4cr)
Department of Electrical & Computer Engineering
Montana State University - Bozeman, MT
Spring 2016

Description: This 4-credit course introduces students to advanced digital logic design. This course is a continuation of EELE 261 and covers large scale digital system design using a hardware description language (VHDL). This course covers the VHDL language in depth and explains how to use it to describe complex combinational circuits, synchronous sequential logic circuits, and computer systems. Functional verification of VHDL designs is accomplished using a logic simulator. This course includes a weekly lab where students will get hands-on experience implementing digital systems on Field Programmable Gate Arrays.

Outcomes: At the end of this course the student should be able to:

1) Understand how to describe a digital system using a Hardware Description Language.
2) Model complex combinational logic in VHDL.
3) Model complex sequential logic in VHDL including state machines and counters.
4) Incorporate pre-existing logic cores into your VHDL design.
5) Understand the HDL design flow including synthesis and place/route and its effect on timing.
6) Perform logic simulations on your digital designs (pre and post synthesis)
7) Prototype digital systems on an FPGA.

Instructor:
Dr. Brock J. LaMeres
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Lab TA:
Krishna Chattergoon
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Time & Location:

Lecture (EELE 367-01),	MWF,	11:00am – 11:50am,	043 Gains Hall
Lecture (EELE 367-02),	W,	2:10pm – 4:00pm,	601 Cobleigh Hall
Lecture (EELE 367-03),	W,	4:10pm – 6:00pm,	601 Cobleigh Hall
Lecture (EELE 367-04),	W,	6:10pm – 8:00pm,	601 Cobleigh Hall

Textbook: "Introduction to Logic Circuits and Logic Design with VHDL", by Brock J. LaMeres
Preliminary Edition. This textbook is available in the bookstore.

Website: https://ecat.montana.edu/ This is the *Desire2Learn* (D2L) course management system. This website will be used for all materials within the course. If you have technical difficulties with the system (i.e., can't login, the system is down, etc…), contact the ITC help desk at 994-1777. **We will NOT be using the email system within *Desire2Learn*.**

Office Hours: Check instructor website for up-to-date office hours.

Requisites: Prerequisite: EELE 261

Grading:

Distribution		Letter Assignment	
Homework	- 20%	90% - 100%	= A
Laboratory	- 25%	80% - 89%	= B
Module Quizzes	- 10%	70% - 79%	= C
Exam #1	- 12.5%	60% - 69%	= D
Exam #2	- 12.5%	0% - 59%	= F
Final Project	- 20%		

Instructor reserves the right to apply a grading curve and to assign +/-'s to grades as appropriate.

Late homework assignments can be turned in up to one week after the due date to receive up to 50% credit. Assignments over one week late will not receive credit.

Labs are due by the end of the following week's lab period. Most labs can be accomplished in the allotted 2-hour lab time. Lab labs can be demonstrated up to one week after the due date to receive up to 50% credit. Labs over one week late will not receive credit.

General Outline:

1) VHDL (Part 2)
2) Behavioral Modeling of Sequential Logic
3) Memory
4) Programmable Logic
5) Arithmetic Circuits
6) Computer System Design

Hardware & Software

All of the lab exercises will be performed using the *terasIC* DE0-CV board containing the Altera Cyclone V FPGA. In the Cobleigh 601 digital lab there is one of these boards located at each computer station for you to use. If you would like to purchase your own board to work on the assignments outside of class (NOT REQUIRED), you can purchase one from http://www.terasic.com.tw/. The academic price is $99 as of January 2016.

The software used to synthesis the designs is free for download from www.altera.com. The name of the synthesizer to get is *Quartus Prime lite*. After going to the website, navigate to: Products → Design Software → Quartus → Download. You'll need to create a free account. Along with the download you will need to specify the devices that you will be targeting. Just select the Cyclone V family to minimize the size of the download. You will also want to get the *Model-Altera Edition* software as part of the download. We will be using ModelSim to perform functional simulations of your VHDL for homework and labs.

Academic Policies:

This course will follow the policies outlined in the *Conduct Guidelines and Grievance Procedures for Students" (http://www2.montana.edu/policy/student_conduct/)* and the *MSU Policy and Procedures Manual* (http://www2.montana.edu/policy/). Please consult these documents on policies regarding academic honesty, student and instructor rights, and general standards of conduct.

Collaboration: You are allowed and encouraged to collaborate on homework and lab exercises. A *collaboration* means that each member of the team contributes to the effort. It is considered cheating if a student simply provides, or receives, the solution to other team members. For homework problems in the form of multiple-choice quizzes, each student must complete the quiz in D2L. For homework problems in the form of VHDL assignments, each student must upload the requested deliverables. **You are NOT to work together on the exams**.

Plagiarism. It is considered plagiarism to simply "copy" VHDL code from the internet without citing it. The internet is a great resource for getting code examples and you are encouraged to use it. However, it is critical that if you use code from the internet, you insert a citation from the source. Citations can be inserted as comments within your VHDL. You should insert citations even if you just using the same approach that you found online.