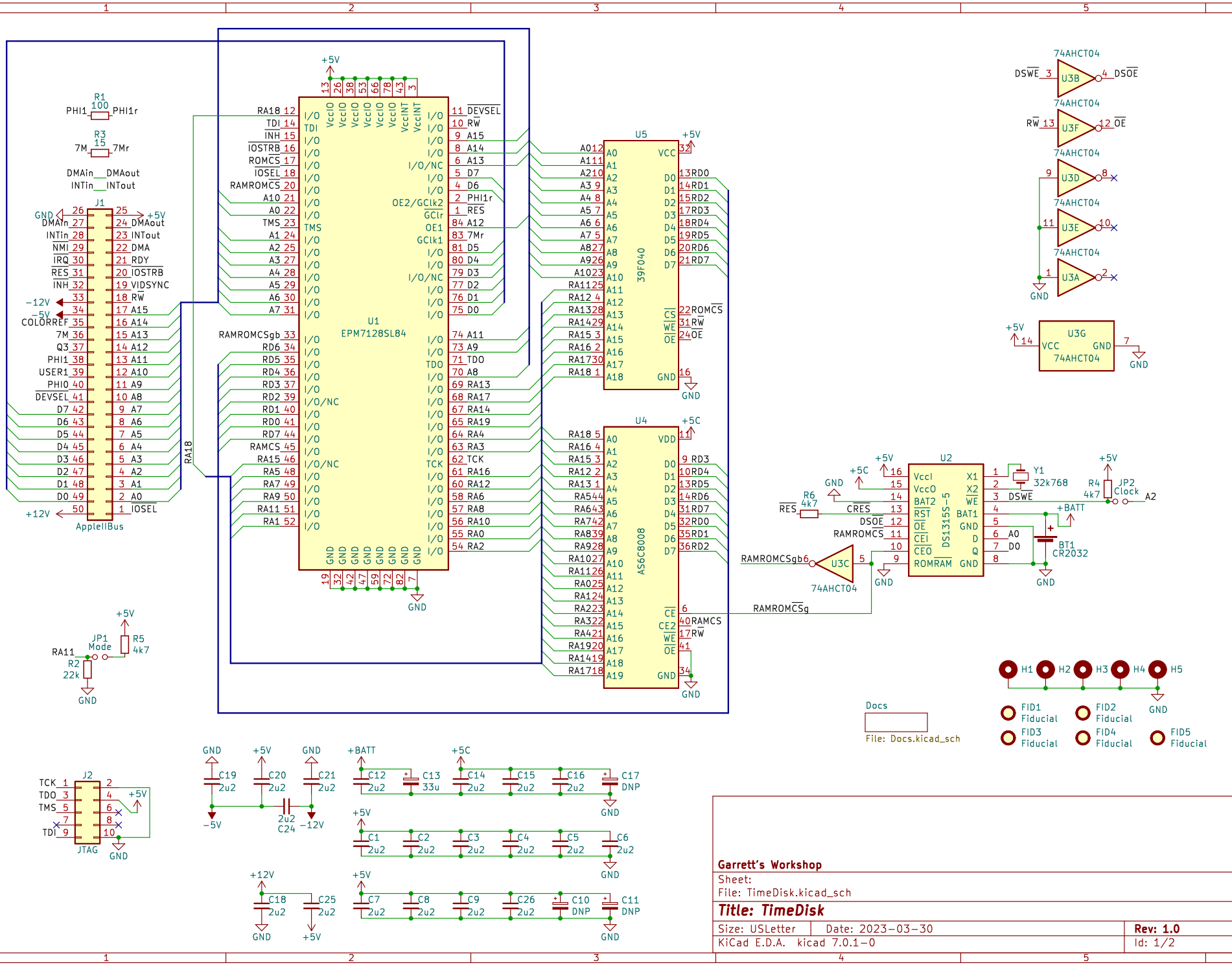
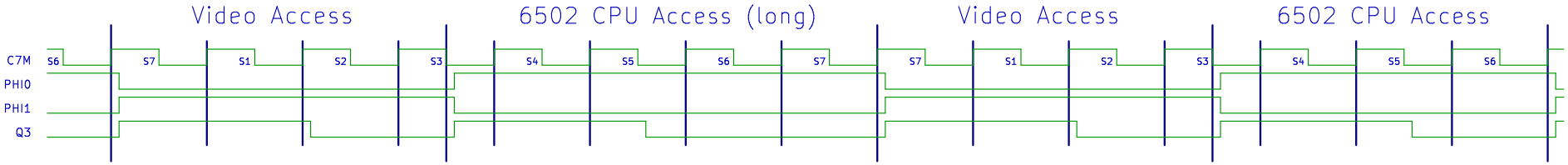

U1
EPM7128SL84
U5
39F040
U4
AS6C8008
U2
DS1315S-5
U3C
74AHCT04
U3B
U3F
U3D
U3E
U3A
U3G
J1
AppleIIBus
J2
JTAG
JP1
Mode
JP2
Clock
Y1
32k768
BT1
CR2032
H1
H2
H3
H4
H5
FID1
Fiducial
FID2
Fiducial
FID3
Fiducial
FID4
Fiducial
FID5
Fiducial
Docs
File: Docs.kicad_sch
Garrett's Workshop
Sheet:
File: TimeDisk.kicad_sch
Title: TimeDisk
Size: USLetter
Date: 2023-03-30
Rev: 1.0
KiCad E.D.A. kicad 7.0.1-0
Id: 1/2



State Synchronization

```
PHI0reg = PHI0 @ C7M
S[3:0] = (PHI0 & PHI0reg) ? 1 :
         (S==0) ? 0 : S+1 @ C7M
```

Select signals (registered)

```
BankSEL = S3 ? (A==XXXF & DEVSEL & REGEN) : BankSEL @ C7M
RAMSEL = S3 ? (A==XXX3 & DEVSEL & REGEN) : RAMSEL @ C7M
AddrHSEL = S3 ? (A==XXX2 & DEVSEL & REGEN) : AddrHSEL @ C7M
AddrMSEL = S3 ? (A==XXX1 & DEVSEL & REGEN) : AddrMSEL @ C7M
AddrLSEL = S3 ? (A==XXX0 & DEVSEL & REGEN) : AddrLSEL @ C7M

REGEN = (IOSEL & S3) ? 1 : REGEN @ C7M
IOROMEN = (A==XXFF & IOSTRB & S3) ? 0 :
          (A==XX00 & IOSEL & S3) ? 1 :
          IOROMEN @ C7M
```

ROM / SRAM Control

```
DBEN = S2 @ C7M

RAMROMCS = RAMSEL | IOSEL | (IOSTRB & IOROMEN)
RAMCS = RAMSEL
ROMCS = RAMROMCSgb & (IOSEL | (IOSTRB & IOROMEN))
```

Address Bus Routing

```
RA[19] = Addr[19]
RA[18:12] = RAMSEL ? Addr[18:12] : Bank[6:0]
RA[11] = RAMSEL ? Addr[18:12] : A[11]
RA[10:0] = Addr[11:0]
```

6502-Accessible Registers

```
Addr[19:16] = (S6 & AddrHSEL & RW) ? D[3:0] : Addr[19:16] @ C7M
Addr[15:8] = (S6 if AddrMSEL & RW) ? D[7:0] : Addr[15:8] @ C7M
Addr[7:0] = (S6 if AddrLSEL & RW) ? D[7:0] : Addr[7:0] @ C7M
if (RAMSEL & S1) Addr[19:0]++ @ C7M
Bank[7:0] = (S6 & BankSEL & RW) ? D[7:0] : Bank[7:0] @ C7M
```

Data Bus Routing

```
RD[7:0] = (DEVSEL | RW) ? 8'bZ : D[7:0]
D[7:0] = (CSEN | DEVSEL | RW) ? 8'bZ :
         AddrHSEL ? {4'hF, Addr[22:16]} :
         AddrMSEL ? Addr[15:8] :
         AddrLSEL ? Addr[7:0] :
         RD[7:0]
```

Information here may be out of date, superseded by ./cpld/TimeMachine.v

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