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Abstract

Memory is a common yet crucial element found in many integrated circuits. When implementing memory of a chip, power is one of the most important design metric to take into consideration. Power consumption has a presence in almost every part of an integrated circuits. Reducing power is necessary part of preserving its operating time. What this study aims to do is apply memory (particularly SRAM arrays) power reduction techniques and imitate, observe, and qualify their claims on the benefits of these techniques. Current techniques we plan on testing include sleeping transistors to control the virtual ground voltage, a proposed 10-T SRAM Cell, another variation of an SRAM cell along with another implementation of the wordline driver circuits, and asymmetric SRAM cells.

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