SRAM Array power reduction using multi-VDD and clamp diode

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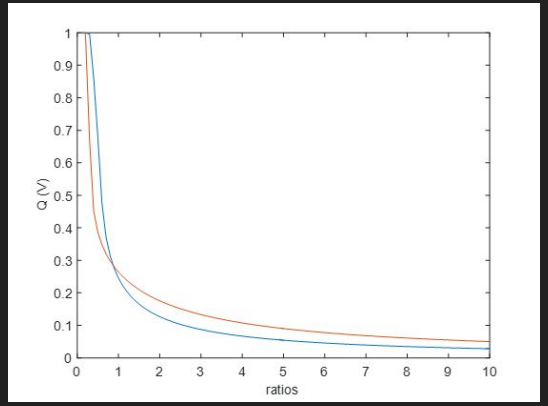
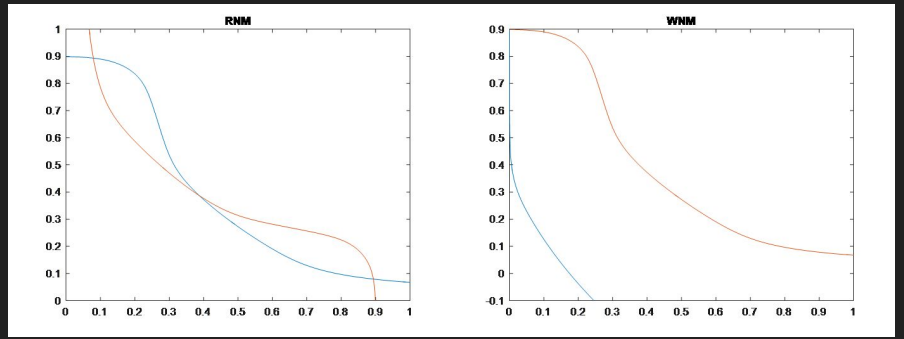
Project Goals

- Reduce SRAM power
- Use 6T cells
- Simulate array to estimate power reduction techniques
- Multi-VDD circuit is simulated
- New array architecture and with new SRAM cell tied together with new architecture

6-T Cell Setup

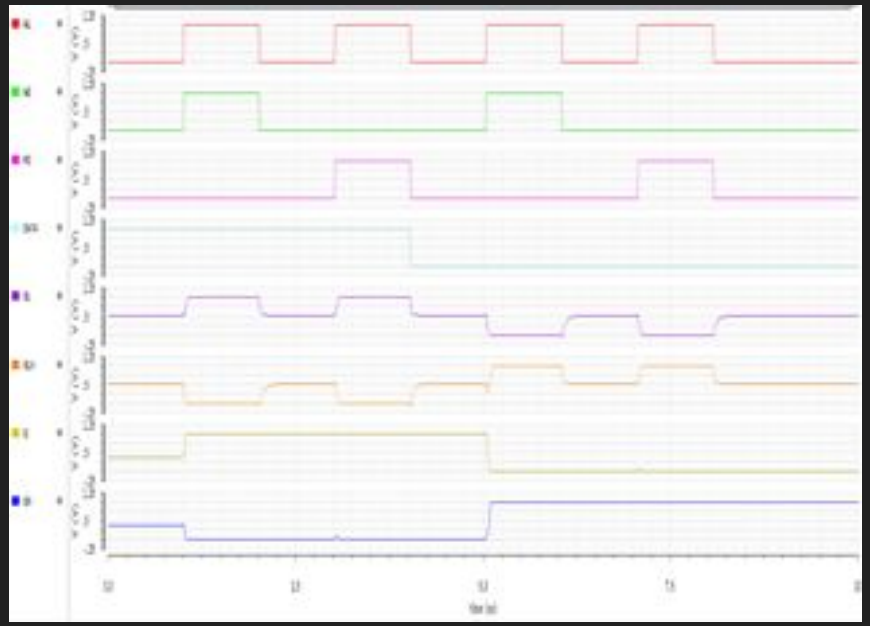
- Initial assumptions: 300 mV margin, 100 nm minimum PMOS width, approximate inverter toggle threshold to be 500 mV.
- Swept widths to find ratios that met margin
- Initial ratio was 1.6 for pull down to axis and 1.2 for axis to pull up
- RNM didn't look very satisfactory so changed ratio to 2 and 1 respectively for better looking margin





6T Cell Verifying functionality

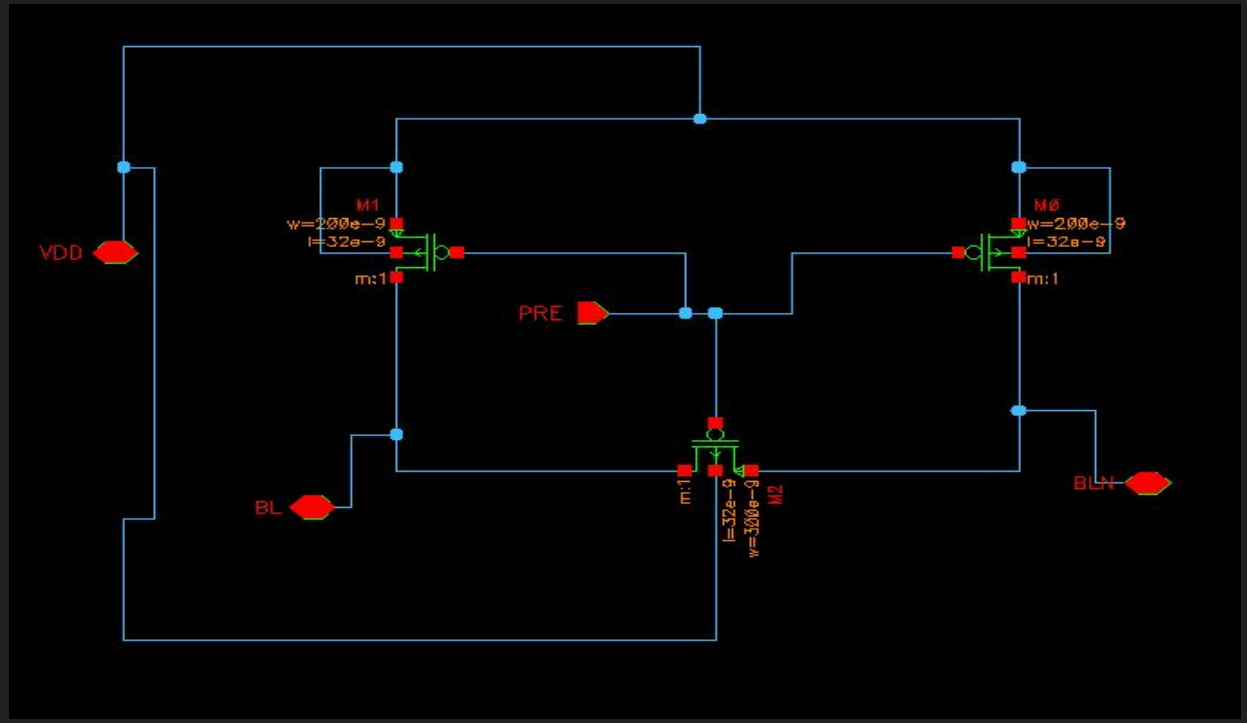
- To verify correct functionality, used simple test of two writes each of which are followed by a read
- Confirmed cell states are correct value on a read and write and bit lines are correct value on a read



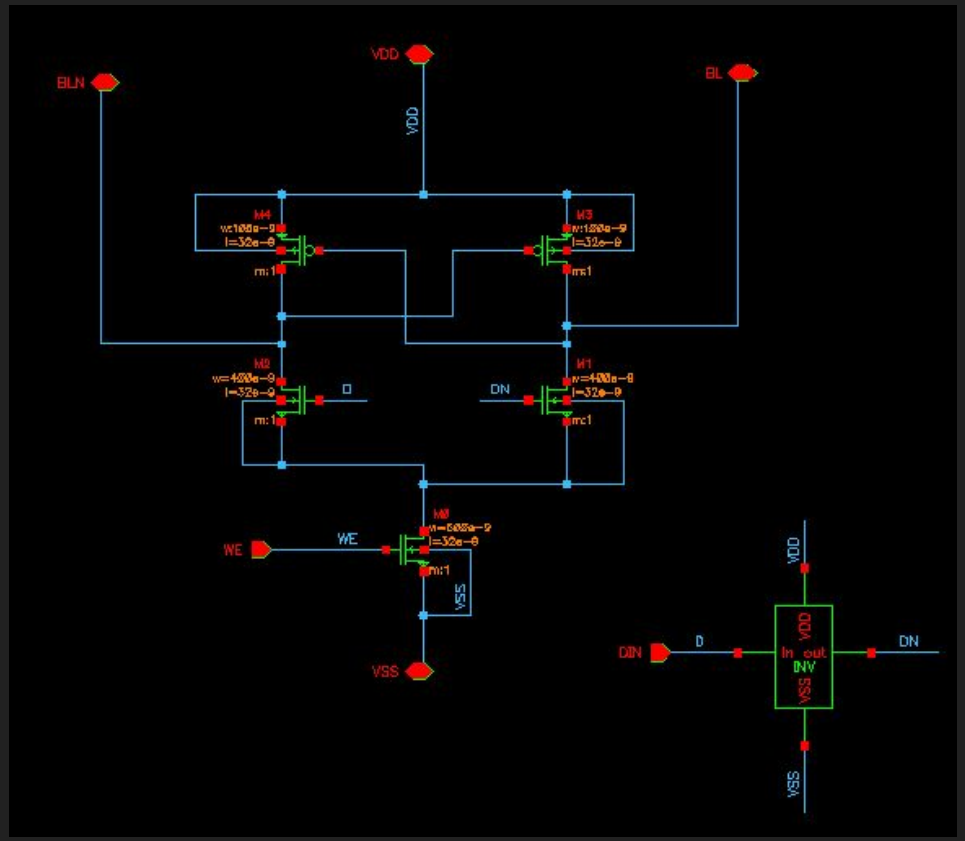
6-T Array Setup

- 32x32 SRAM Array consisted of 8x8 sub-arrays
- Peripherals
  - 5-32 Row and Column Decoder + WL Driver
  - Pre-charge Circuit (32 copies for 32 BL and BLNs)
  - Write Driver (32 copies for 32 BL and BLNs)
  - Sense Amplifier (32 copies for 32 BL and BLNs)

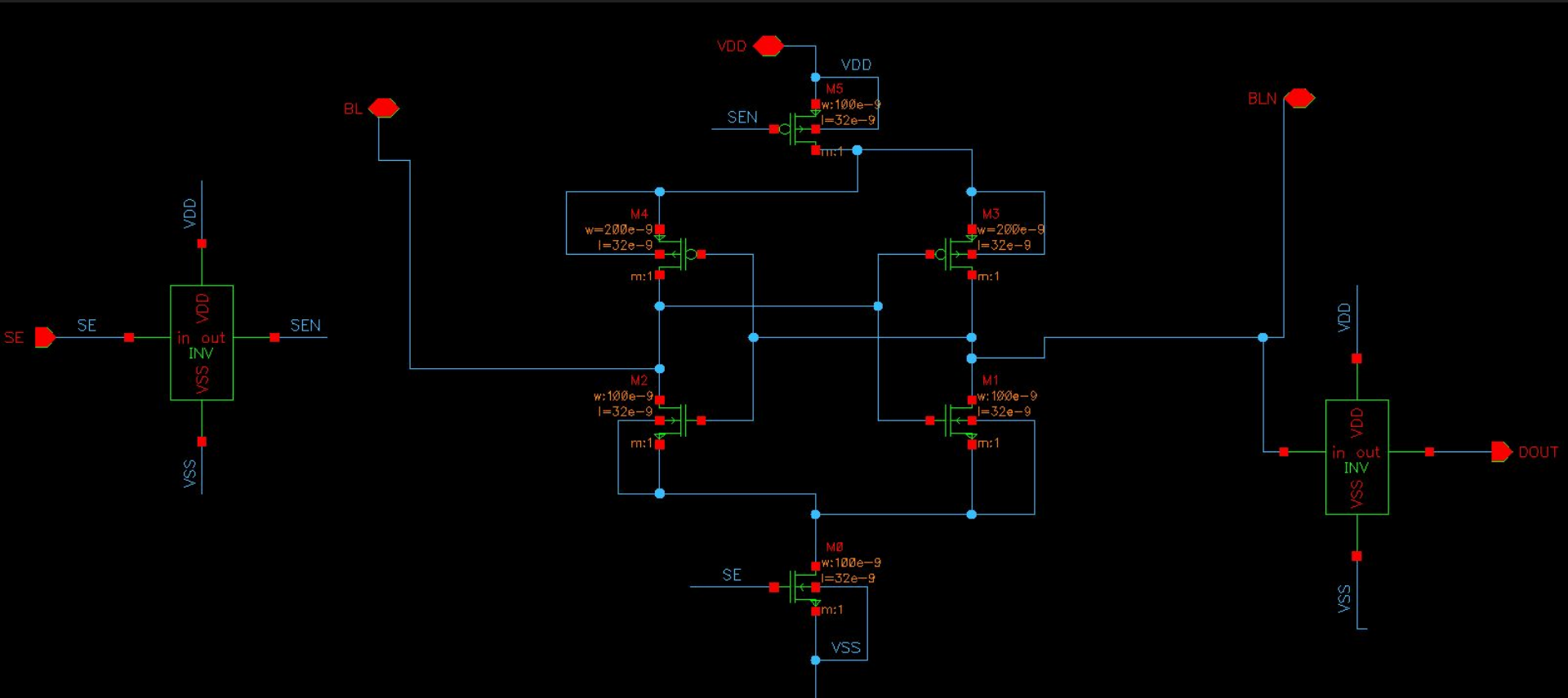
6T Array Setup - Pre-charge Circuit



6T Array Setup - Write Driver

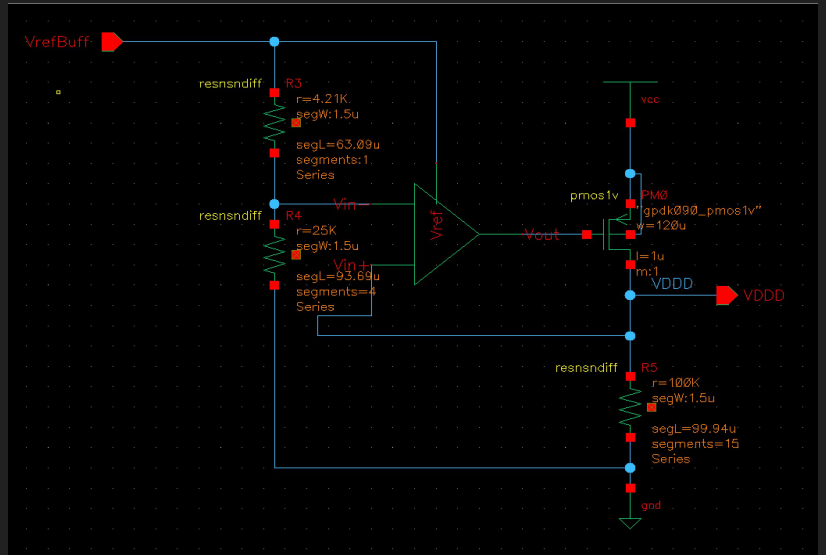


6T Array Setup - Sense Amplifier



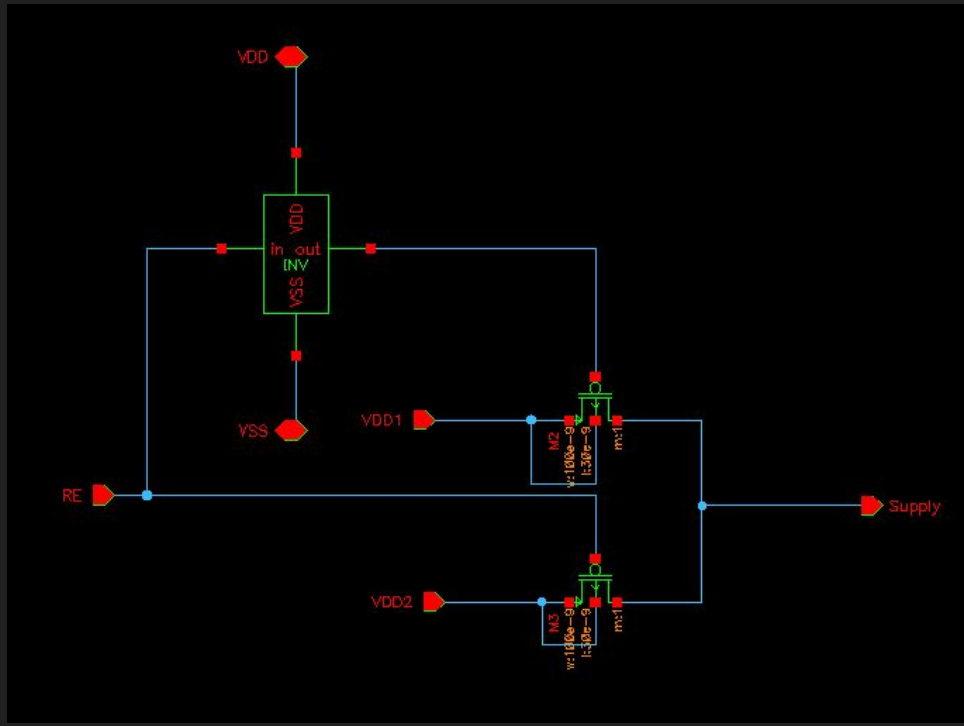
Dynamic Voltage Supply Technique

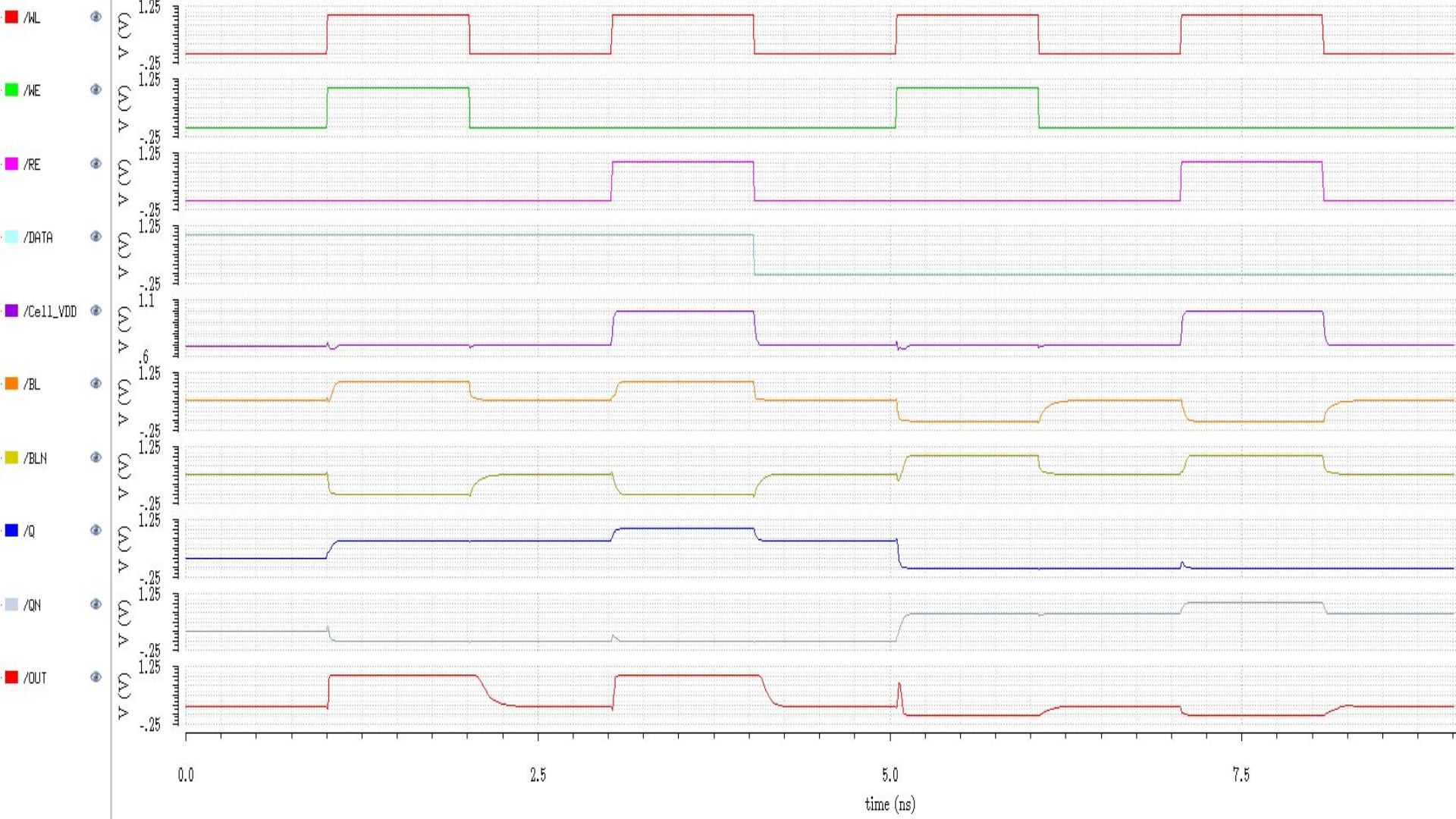
- VDD1 = 1V, VDD2 = 0.7V
  - V2/V1 = 0.7 for optimum
  - For the second supply 0.7V, we can assume entire chip already provides second supply or…
  - Build digital voltage regulator separately for SRAM array



Dynamic Voltage Supply Technique

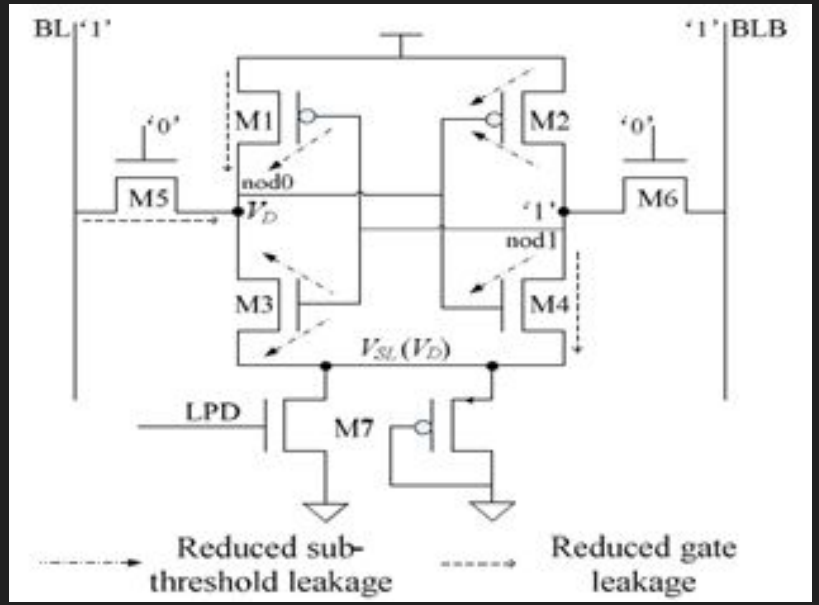
- Simple PMOS switch to choose between two VDDs sent to SRAM array cell supply
- When reading, VDD = 1V.
- When writing or inactive, VDD = 0.7 V
    - Higher supply voltage in standard 6T cell helps read operation while hurting write.




/WL
/WE
/RE
/DATA
/Cell_VDD
/BL
/BLN
/Q
/QN
/OUT
V (V)
1.25
-.25
1.1
.6
0.0
2.5
5.0
7.5
time (ns)

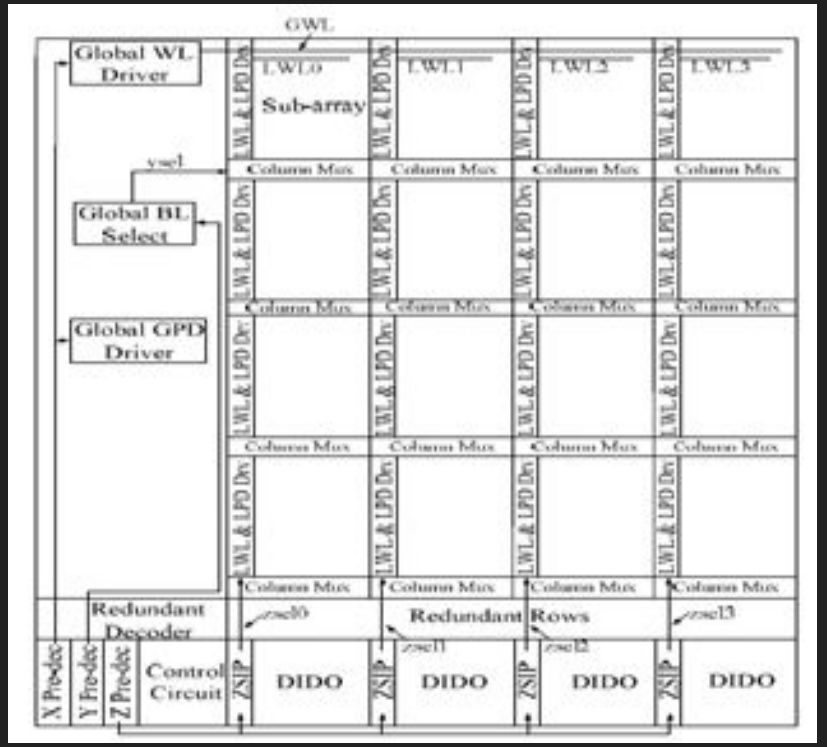
Clamp + Sleep transistor Technique

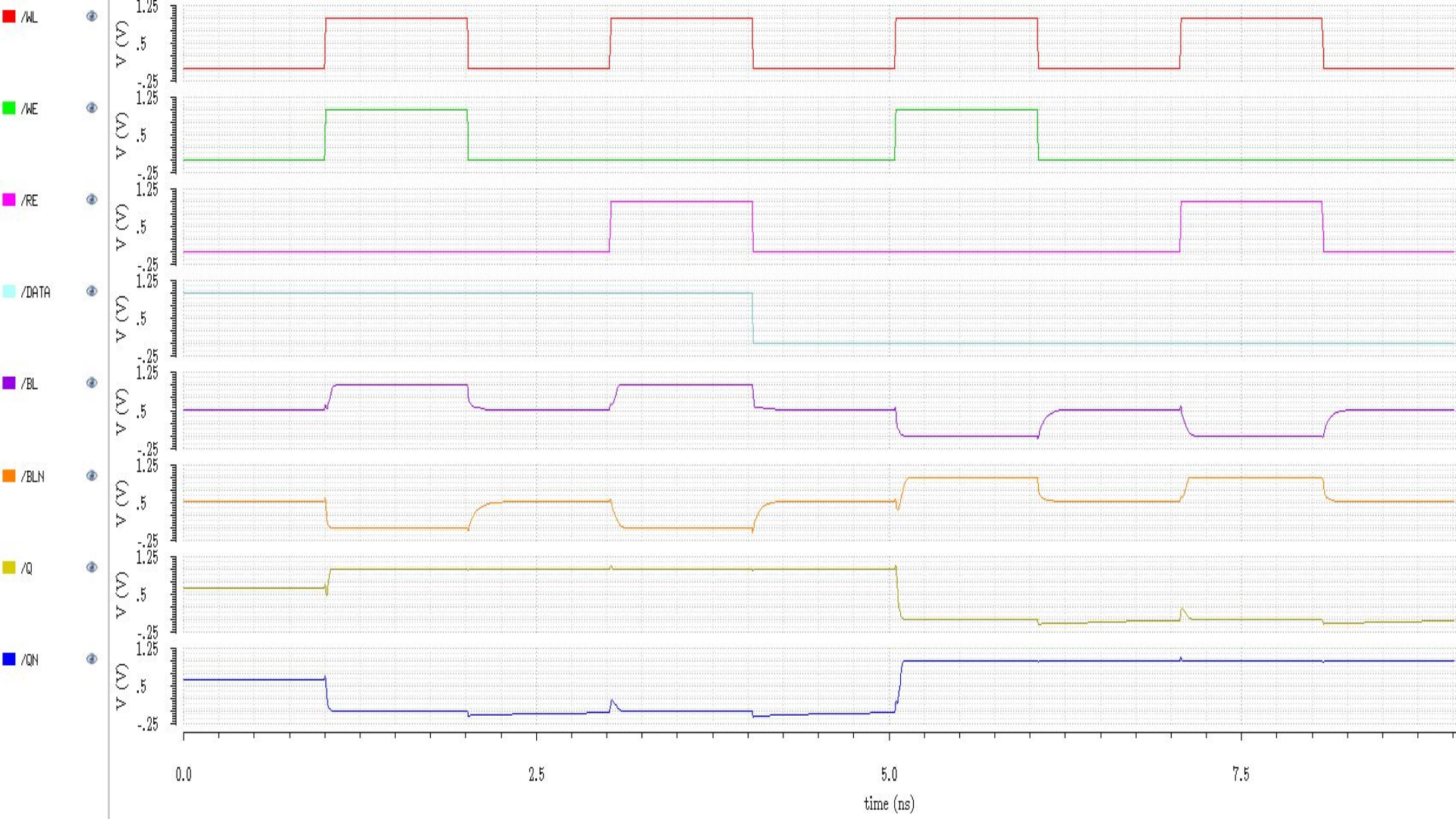
- V_SL is pulled down to ground when M7 is on.
- V_SL is a floating voltage when M7 is turned off. Diode-connected PMOS helps floating voltage to remain stable, mitigating the effects of noise that can suddenly increase V_SL to destroy value stored in cell.



Clamp + Sleep transistor Technique

- Extra Decoder is built to turn M7 on for active SRAM sub-arrays while M7 is off for inactive SRAM sub-arrays
- Less leakage power consumed for inactive SRAM sub-arrays




/WL
/WE
/RE
/DATA
/BL
/BLN
/Q
/QN
V (V)
1.25
.5
-.25
0.0
2.5
5.0
7.5
time (ns)

Results

Array power

	Read	Write	Inactive
6-T	63.2uW	620.5uW	19.5uW
Multi-VDD	36.4uW	457.7uW	7.2uW
Clamp	37.6uW	153.0uW	10.2uW
Multi-VDD and Clamp	34.3uW	86.0uW	15.8uW

Peripheral power

	Read	Write	Inactive
Pre-Charge	5.11uW	6.02uW	11.5uW
Write Driver	28.6uW	62.3uW	22.6uW
Sense-Amp	57.8uW	9.20uW	91.3uW
Decoder	12.uW	11.8uW	1.39uW
Extra Decoder	1.01uW	9.88uW	0.129uW
Dynamic Supply	0.002uW	0.007uW	0.003uW

Tradeoffs

- In general, extra peripheral overhead
- Sleep transistor/clamp diode logic
  - Turning off during active operation lowers active power
  - Turning off when inactive lowers power when cell is not being used
- Dynamic voltage source has tradeoffs between power and the overhead of the dynamic voltage source circuit along with stability
  - Dynamic voltage source circuit has to be strong enough to reliably switch between the two voltage to during relevant operations
- Clamp diode’s main tradeoff is the area overhead involved with applying the extra transistors to the cells and the decoder for the partitions

Conclusion

The techniques proposed do provide noticeably lower power. The most obvious trade off is the peripherals. In regards to the power each configuration of the technique has its own benefits such as better active power in exchange for worse inactive power. Memory access pattern and frequency is something to be taken into consideration when choosing. More thorough testing such as other access patterns can be done for more comprehensive results.

References

[1] Preeti S Bellerimatha and R. M Banakarb, "Implementation of 16X16 SRAM Memory Array using 180nm Technology", in International Journal of Current Engineering and Technology, Special Issue1 (Sept 2013)

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[4] Wu, Chen, et al. "SRAM power optimization with a
novel circuit and architectural level technique." Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on. IEEE, 2010.