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Abstract

Leakage power is one of the most scrutinized sources of power consumption because of its increasingly huge impact on the operating time of electrical devices. At a high level, many modern electronics use devices such as power management units (PMU) to manage lower level leakage reduction circuits such as sleeping transistors. At lower level, techniques such as clock gating, voltage scaling, and body biasing are employed. Due to the ongoing nature of leakage reduction, there are variations and different approaches to the same general technique. What this study aims to do is to emulate some of these techniques, and quantify and compare their effects on design metrics, especially power consumption. It will use a few simple circuit models that will tested modularly using the different techniques to compare their effects on the design metrics.

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