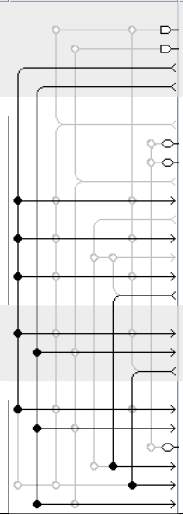

Use	Name	Description	Export	Clock	Base	End	IRQ	Tags	Opc...
☑	**clk_50**	Clock Source							
	clk_in	Clock Input	**clk**	*exported*					
	clk_in_reset	Reset Input	**reset**						
	clk	Clock Output	Double-clic	clk_50					
	clk_reset	Reset Output	Double-clic						
☑	**hps**	Arria V/Cyclone V Hard Proce...							
	h2f_user1_clock	Clock Output	Double-clic	hps_h2f_user1_clock					
	memory	Conduit	**hps_ddr3**						
	hps_io	Conduit	**hps**						
	h2f_reset	Reset Output	Double-clic						
	h2f_axi_clock	Clock Input	Double-clic	**clk_50**					
	h2f_axi_master	AXI Master	Double-clic	[h2f_axi_clock]					
	f2h_axi_clock	Clock Input	Double-clic	**clk_50**					
	f2h_axi_slave	AXI Slave	Double-clic	[f2h_axi_clock]	🔒				
	h2f_lw_axi_clock	Clock Input	Double-clic	**clk_50**					
	h2f_lw_axi_master	AXI Master	Double-clic	[h2f_lw_axi_clock]					
☑	**vga_clk_pll**	PLL Intel FPGA IP							
	refclk	Clock Input	Double-clic	**clk_50**					
	reset	Reset Input	Double-clic						
	outclk0	Clock Output	Double-clic	vga_clk_pll_outclk0					
☑	**vga_tiles**	vga_tiles							
	clock	Clock Input	Double-clic	**clk_50**					
	reset	Reset Input	Double-clic	[clock]					
	VGA	Conduit	**vga**	[vga_clock]					
	avalon	Avalon Memory Mapped Slave	Double-clic	[clock]	🔒 **0x0000_0000**	0x0000_7fff			
	vga_clock	Clock Input	Double-clic	**vga_clk_pll_outclk0**					
	vga_reset	Reset Input	Double-clic	[vga_clock]					